

# High performance PSR power switch IC

## 1. Feature

- Built-in TruePSR™ high-precision sampling technology
- Built-in 700V BVdss GaNswitch™ power switch
- Built-in high voltage fast startup control
- Highswitching frequency up to 140kHz
- The rated output power up to 40W in universal
- Precise primary side regulation accuracy is better than 2%
- Precise primary side constant current accuracy is better than 3%
- Built-in output voltage drop compensation function fixed to 3%
- Low switching loss with full valley switch mode
- Low standby consumption and high energy efficiency
- Meet the CoC V5 & DoE VI energy efficiency requirements
- No-load standby power consumption as low as 30mW or less
- Built-in CT-PSR™ active cycle tuning technology
- Low-frequency start-up characteristic control optimizes the starting performance
- Highly reliable low EMI gate drive with soft clamp
- Built-in output over-voltage, short circuit and over-load protection
- Optimized full-range audio-free operation
- ASOP8 package with Halogen-free green package to meet RoHs standard



## 2. Applications

- IT Equipment Charger
- Power Adapter
- Battery Charger
- Open-frame Power

## 3. Description

The LIC3515F is a new generation of high-performance, highly integrated current-mode PSR power switch ICs. that can easily build low-standby power consumption as low as 30mW or lower, high conversion efficiency, and low power dissipation to meet the energy efficiency standards of CoC V5 and DoE LEVEL VI in applications peak power up to 40W , High-performance PSR primary side of the CC / CV switching power supply solutions. The chip has built-in high precision constant current and constant voltage control and has an optimized valley switch technology that provides output current error of better than  $\pm 3\%$  accuracy and  $\pm 2\%$  accuracy of output voltage error over the full range.

Switching frequencies of up to 140kHz allow the use of relatively small transformer size to complete the design, while a very

small dead-time control allows the system to work in close to critical conduction mode to improve the utilization of the transformer, far superior to traditional PSR controller architecture.

With PWM / PFM / PBM mode multi-segment curve control mode of operation can further optimize the system under different load conversion efficiency, especially at light load conversion efficiency, very light load conditions will automatically lock the peak current threshold to maintain efficient conversion, segmented modulation design makes the system with high conversion efficiency while effectively avoiding audible noise, the chips built in high voltage startup function, the standby power consumption can be as low as 30mW the following.

The low-frequency start-up feature automatically operates once during each power-up and system reset to optimize startup characteristics and to reduce the impact of the switch on the high-voltage power switch. Soft-clamp gate drive control further removes high , While the active gate slope control significantly improves the level of switching interference. The new generation of cycle-rotation technology for PSR architecture makes the system extremely EMI-friendly.

The chip can also compensate for the output voltage drop through a specially designed linear output cable voltage drop compensation fixed to improve the accuracy of the output voltage under load and maintain accurate load voltage from the load. The internal fixed compensation range is 3%, for example, a 5V output system with a maximum compensation voltage of approximately 0.15V.

LIC3515F has a built-in high-voltage GaNswitch™ power switch and snubber diode, which is designed in a very simple structure and has few peripheral devices.

LIC3515F also provides a very complete protection circuit with automatic recovery, including cycle-by-cycle current limit (OCP), with high and low voltage compensation output overcurrent protection (OCP), VDD over-voltage protection and under voltage lockout (UVLO) .

Now available in halogen-free ASOP8 green package.

#### 4. Equivalent Internal Function Block Diagram

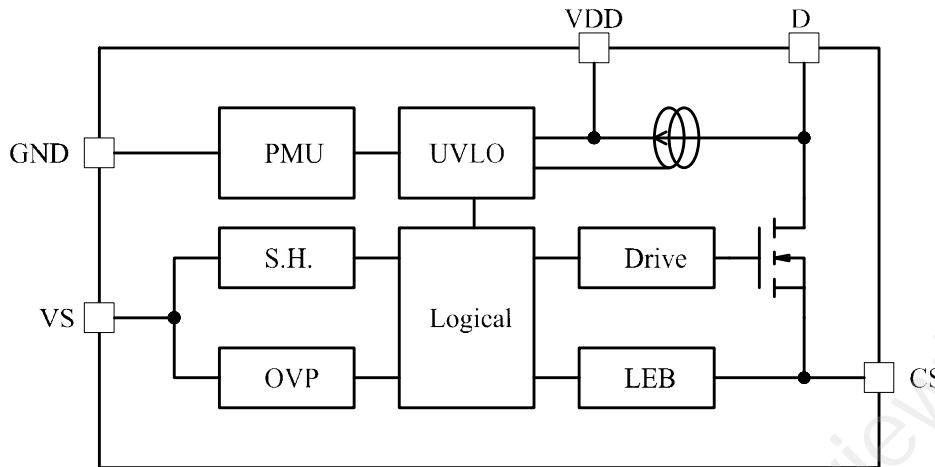


Fig1. Internal functional block diagram

#### 5. Pin Definitions

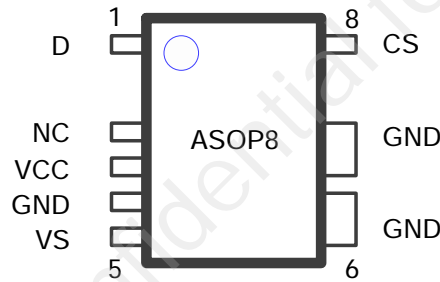


Fig2. Pin Definitions

#### 6. Pin Function Description

PIN	Symbol	Function
1	D	The high-voltage power switch drain output pin, which connects the transformer
2	NC	Empty pin, unused, and can be connected to other pin other than D in the application
3	VDD	Power supply pin, connect the starting resistor and auxiliary power supply circuit
4	GND	Ground pin , must be connected to the cooling ground ( Pin6/7 ) in the application
5	VS	Output voltage and switch signal detection pin, connected to the feedback sampling network
6,7	GND	Cooling ground pin, must be connected to the Ground ( Pin4 ) in the application
8	CS	Switch current sense signal input pin, connected to the current sense resistor

### 7. Typical Simplified Schematic

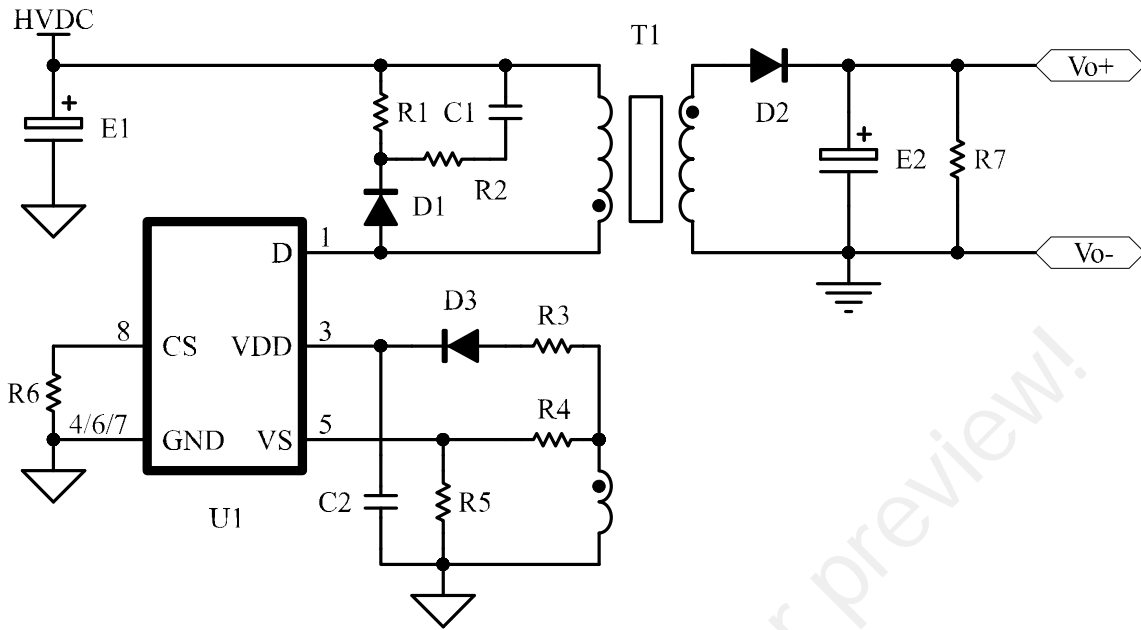


Fig3. Typical Simplified Schematic

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## 8. Absolute Maximum Ratings \*

Item	Parameter	unit
D Pin Voltage	700**	V
VDD Pin Voltage	20***	V
Other Pin Voltage	-0.3 to +7	V
D Pin Current (LIC3515F)	12****	A
Min/Max T <sub>J</sub>	-40 to 150	°C
Min/Max T <sub>stg</sub>	-55 to 150	°C
PD	1200	mW
ESD:		
HBM	2000	V
MM	200	V

Note\*: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.\*\* : with 1mA limit. \*\*\* : with 10mA limit. \*\*\*\*: For test, Pulse width is 1ms and cycle is 1S.

## 9. Recommended Operating Conditions

Symbol	Parameter	Min	Type	Max	Unit
VDD	VDD Voltage	6		15	V
FS	Switch frequency	0.40		130	KHz
I <sub>p</sub>	D Ipeak LIC3515F			4	A
TA	Operating ambient temperature	-20		85	°C

## 10. Electrical Characteristics (Ta = 25°C, VDD=10V, if not otherwise noted)

### power switch Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV <sub>DSS</sub>	Drain-Source Voltage	VDD=0V, I <sub>D</sub> =1mA	700			V
I <sub>HV</sub>	D-S leakage Current	V <sub>D</sub> =700V			10	uA
R <sub>DS(ON)</sub>	power switch RdsON	I <sub>D</sub> =1.30A, T <sub>J</sub> =25°C, LIC3515F		0.55	0.62	Ω
T <sub>R</sub>	Switch Rise Time	CL=1mH		50		nS
T <sub>F</sub>	Switch Fall Time	CL=1mH		200		nS
I <sub>D</sub>	Drain Current Pulsed	LIC3515F, T <sub>J</sub> =25°C		12		A
		LIC3515F, T <sub>J</sub> =105°C		4		A

### VDD Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>OS</sub>	VDD startup current	VDD=10V	-	1	50	uA
I <sub>Q</sub>	Operating current	VDD=10V	-	0.5	-	mA
V <sub>STOP</sub>	UVLO Threshold voltage	VDD=18V↔0V	5	5.5	6	V
V <sub>START</sub>		VDD=0V↔18V	-	14	-	V
V <sub>DDOVP</sub>	VDD Over-Voltage Off		-	18	-	V
V <sub>DD_CL</sub>	VDD soft Clamp Voltage	I <sub>VDD</sub> =10mA	-	15	-	V

### VS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CV</sub>	VS reference voltage		2.95	3.00	3.05	V
V <sub>VSOP</sub>	VS OVP threshold		-	3.50	-	V
K <sub>OCC</sub>	OCC coefficient			3		%
V <sub>OCC</sub>	OCC voltage	For 5V OUT		0.15		V

### Cycleturning™ II (C.T.II) Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF <sub>OSC</sub>	C.T. range	to Vcst	-3		+3	%
T <sub>CT</sub>	C.T. time		-	4	-	mS

CS Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{LEB}$	L.E.B Time			350		nS
$Z_{CS}$	CS Input Resistance			40		K $\Omega$
$T_{OCP}$	OCP Delay Time	VDD=10V,CS>VTH_OC		75		nS
$V_{THOCPH}$	Max. OCP Threshold			0.50		V
$V_{THOCPH}$	Min. OCP Threshold			0.20		V
$V_{THOSP}$	OSP Threshold voltage			1.5		V

OSC Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$F_{OSC}$	Switching Frequency	Burst Mode Not entered	22	-	140	kHz
$F_{OSCMIN}$	Min. Switching Frequency	Burst Mode enter	-	300	-	Hz
$\Delta F_{OSC-T}$	$F_{OSC}$ VS $T_a$	VDD = 10V, $T_a = -20^{\circ}\text{C}$ to $100^{\circ}\text{C}$	-	5	-	%
$\Delta F_{OSC-V}$	$F_{OSC}$ VS VCC	VDD = 6-15V	-	5	-	%
$T_{ONMAX}$	Max. On Time		-	20	-	us
$D_{dismax}$	Max. Discharge Duty	VS < 3V	-	50	-	%
$T_{DIS\_Min}$	Min. Discharge Time		0.5	-	1.5	us

OTP Section

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{OTP}$	OTP Threshold		-	150	-	$^{\circ}\text{C}$
$t_{OTPHYT}$	OTP Hysteresis		-	30	-	$^{\circ}\text{C}$

## Thermal Data

Symbol	Parameter	Rating	Unit
$\theta_{JA}^1$	Thermal Resistance Junction-Ambient	70	°C/W
$\theta_{JC}^2$	Thermal Resistance Junction-Case	20	°C/W

Notes: 1. All leads are soldered on a 250mm<sup>2</sup> copper foil with 2oz thick to measuring. 2. Measured on the surface of the package near pin 5/6.

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## 12. Application and Implementation

The LIC3515F is a highly integrated, constant-current, constant-voltage PSR controller IC optimized for off-line applications below. Its highly efficient BM and valley switch hybrid mode control and built-in high voltage startup function to significantly reduces standby losses, improves conversion efficiency at light loads, and easily meets international energy efficiency standards such as CoC V5 and DoE LEVEL VI energy efficiency, the system standby power as low as 30mW or lower.

### 12.1 Start-up current and start-up control

The LIC3515F is built-in high-voltage startup function, chips can operate at very low start-up current conditions, and with accurate UVLO control, so enabling fast and reliable power-up in a short period of time.

When power on, the VDD voltage is charged from 0 to 14V, the internal circuit is started and the output drive pulse is start out, the system work begins.

### 12.2 Operating Current and VDD Capacitance

LIC3515F the normal operating current as low as 2mA, the IC itself when the loss is small, a capacity of not less than 3.3uF capacitor to meet the IC power supply and drive enough energy to consider the larger power switch input capacitance and wide Of the operating temperature range, should choose a lower internal resistance (ESR) of the capacitor type to open the power switch to provide fast and large current to speed up the power switch turn-on, in a typical system design recommended 4.7uF capacitor as VDD capacitance. In order to meet the maximum operating conditions of the VDD range, the capacitor voltage should be not less than 20V better. The effect of noise can be further reduced by connecting a non-polar capacitor in parallel to the VDD pin.

### 12.3 Cycleturning™ PSR (C.T. PSR)

The LIC3515F incorporates a proprietary, second-generation CycleTurning™ technology optimized for PSR that is clocked at the set time (CT-PSR) for the duration of the work cycle, resulting in a larger switching pulse spectrum To reduce the narrowband energy density, so that any single bandwidth within the average interference intensity greatly reduced. Therefore, the system in the EMI on the cost of the cost is greatly reduced.

### 12.4 Extended BM operating characteristics

The power switch switching loss ratio will increase significantly; while the switching loss and switching frequency is proportional to the lower switching frequency can significantly reduce the power switch switching losses. LIC3515F by detecting the VS voltage and time size, the system no-load or light load will automatically adjust the switching frequency to a lower value, the internal modulation voltage is lower than the set control voltage, the more the frequency decreases, but the more The circuit automatically limits the frequency drop to a minimum of 22kHz to avoid audible noise.

When the system frequency drops to near 22KHz, if the modulation voltage is still lower than the set control voltage, the output will be disabled to ensure that the output voltage will not be too high, then the system will enter the BM mode to avoid audio noise, And as the load continues to reduce the number of pulses until the pulse into a single state, in order to

optimize the system dynamic load response performance, the system will automatically lock the lowest equivalent switching frequency of 200Hz.

## 12.5 Current detection and leading edge blanking

The LIC3515F provides cycle-by-cycle current limiting, and the switching current is sampled into the IC through the current limiting resistor. The built-in leading-edge blanking eliminates current spikes into the IC, preventing current limiter malfunctions and preventing power switches from being faulted, thus eliminating the need for a conventional external blanking circuit.

The maximum current limit threshold, the current comparator's maximum threshold voltage, is 0.50V.

At standby, system is work on minimum current limit condition, the threshold voltage, is 0.20V

## 12.6 Constant voltage control

LIC3515F by sampling the voltage waveform on the auxiliary winding, through a series of internal sampling chip, keep, analyze, deal with, produce the required various signals. Which compares the voltage signal with the internal reference voltage to generate a voltage error signal and adjusts the switch state according to the voltage error signal so as to compensate for the increase or decrease of the output load and the change of the output voltage caused by the increase or decrease of the input voltage, The typical output voltage (Vout) is:

$$V_{OUT} = \left( \frac{R_U}{R_D} + 1 \right) * V_{CV} * \frac{N_S}{N_A} - VD$$

Here, Ru for the voltage sampling pull-up resistor, Rd for the voltage sampling pull-down resistor; Vcv for the internal voltage reference, typically 3.00V; Ns and Na are the transformer secondary winding turns and auxiliary winding turns; VD is output diode VF.

Through the unique TruePSR™ waveform analysis technology, the output voltage cannot be affected by the load current size to maintain high accuracy.

When the load continues to increase to the maximum operating state of the system but the sampled voltage is still lower than the internal reference voltage, the system will enter the constant current working state.

## 12.7 Constant current control

When the system enters the constant current output state, the LIC3515F will determine the proportional relation of the switching waveform by detecting the time parameter of the VS terminal waveform and keep the demagnetizing time T<sub>DIS</sub> constant with the switching period by changing the dead time so that the output The current remains at a constant magnitude and the system's maximum demagnetization duty cycle (demagnetization time to switching period ratio) is 50%,

$$\frac{T_{DIS}}{T_{ON} + T_D + T_{DIS}} = \frac{T_{DIS}}{T} = 0.50$$

T<sub>ON</sub> is the turn-on time; T<sub>D</sub> is the dead time, the minimum is the main inductor resonant cycle of 1/4, for example 500kHz resonant period, T<sub>D</sub> is about 0.5us; T<sub>DIS</sub> for the transformer demagnetization time;

So the output constant current point Iout and the transformer turns ratio Np / Ns and the relationship between the primary

peak switch current I<sub>peak</sub>:

$$I_{OUTCC} = 0.5 * I_{PEAK} * \frac{N_P}{N_S} * 0.50$$

For a given system, if the specified flyback voltage or turn ratio, according to the size of the output current constant according to the above formula to obtain the required primary peak switch current I<sub>peak</sub> size:

$$I_{PEAK} = \frac{N_S * I_{OUTCC}}{N_P * 0.25}$$

According to the obtained primary peak switch current value, the required current limiting resistance can be calculated according to the following formula:

$$R_{CS} = \frac{V_{CSMAX}}{I_{PEAK}}$$

Here, V<sub>csmax</sub> is the chip maximum current limit threshold, typically 0.50V.

## 12.8 Frequency control

LIC3515F by adjusting the switching pulse time parameters to automatically adjust the switching current size, and the corresponding control of the output state for a specified system, each time the switching frequency of the system are automatically balanced results, the system switching frequency is the transformer And the system together, when the output current constant according to the requirements of a reasonable set of transformer turns ratio and the system's maximum peak switching current, the maximum switching frequency will be determined by the transformer inductance, the typical maximum switching frequency:

$$F_{MAX} = \frac{2 * P_{OUT}}{I_{PEAK}^2 * L_P * \eta}$$

Here, P<sub>out</sub> is the output constant current point corresponding to the maximum output power; L<sub>p</sub> is the transformer primary inductance; η is the conversion efficiency.

The maximum operating frequency of the system should be set reasonably so that it does not exceed the maximum frequency limit (typical value is 140kHz) inside the chip, taking into account the effect of system switching loss and EMI. For general applications, the maximum switching frequency can be set between 50 ~ 130kHz. The recommended value is 120kHz for most applications.

In normal operation, the chip will automatically adjust the switching frequency or switching current according to the load size and input voltage to maintain a good conversion efficiency under various conditions, while avoiding audio noise, the typical switching frequency curve is as follows The figure shows:

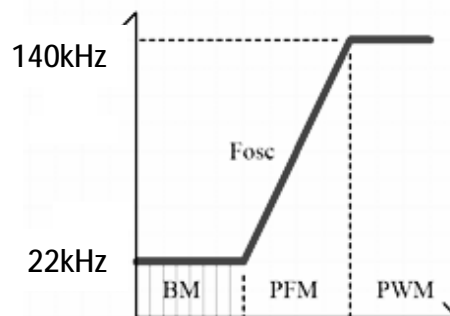


Fig4. V<sub>ea</sub> VS F<sub>osc</sub> curve

### 12.9 Valley switch control

The LIC3515F will set each turn-on action to a fixed position in the resonant period so that the current period can be automatically turned on in a reasonably designed system at the lower voltage position of each resonant waveform (best, the bottom of the resonant trough) Additional low turn-on loss characteristics can be achieved at light load conditions, further improving light-load efficiency.

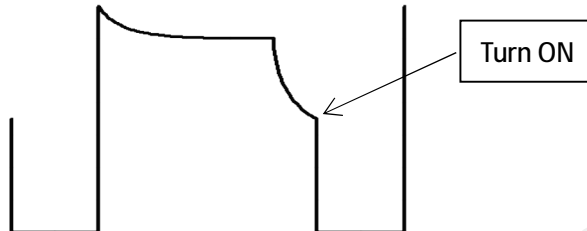


Fig5. valley switch mode

### 12.10 Soft startup characteristics

The LIC3515F will also ensure that the critical mode is active at every startup, allowing the system to start the process at a lower frequency and automatically increasing the operating frequency as the output voltage increases, so that the start-up does not occur as continuous Current-mode power supply current overshoot problem, which can effectively reduce the impact of starting current to reduce the power switch current stress.

### 12.11 Output wire voltage drop compensation

The LIC3515F features an excellent and easy-to-use output-wire voltage drop compensation technique. The compensation amplitude is set by internal fixed setting. The output current can be linearly compensated when the output current is increased, thus completely canceling the output The voltage drop generated on the wire to achieve a very precise load voltage regulator output, while the maximum compensation from the internal fixed amplitude of 3%, for example, a 5V output system with a maximum compensation voltage of approximately 0.15V.

### 12.12 Protective function

Excellent power systems require sophisticated fault protection to achieve high reliability. The LIC3515F is designed to meet a wide range of user requirements including cycle-by-cycle current limiting (OCP), output overload protection (OLP), VDD overvoltage lockout, and under-voltage lockout (UVLO).

When the VS terminal voltage more than 5V per unit of time more than triple or more than 1.5V more than triple the CS voltage will directly trigger the system into over-voltage protection and overcurrent protection state until the restart.

### 12.13 Built-in switch and heat treatment

The LIC3515F incorporates a high-switching-speed power switch with a low RdsON voltage rating of 700V 12A to maintain low switching losses at switching frequencies as high as 120kHz, yet the chip operation will still produce a certain amount of

power Heat, so the application should be carried out in the appropriate heat treatment, a simple approach is to chip in the PIN5 laying enough area of copper foil and tin treatment, as a cooling measures, a typical 36W application of copper foil area should not preferably less than 120 mm<sup>2</sup>.

PCB layout should also ensure that high-voltage connection pin and other low-voltage pins or devices to maintain a sufficient safe distance, the minimum safe distance should be at least not less than 1mm is appropriate, so as to avoid damage caused by discharge.

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### 13. Layout Guidelines

#### 13.1 Principles of high-frequency layout

When switching power supply layout should follow the principle of high-frequency layout, Where possible, the current loop should be kept to a minimum. should be advanced and then out of the dual-capacitor and appropriate to maintain a single point of connection capacitance. Three typical current loops is shown in the following figure:

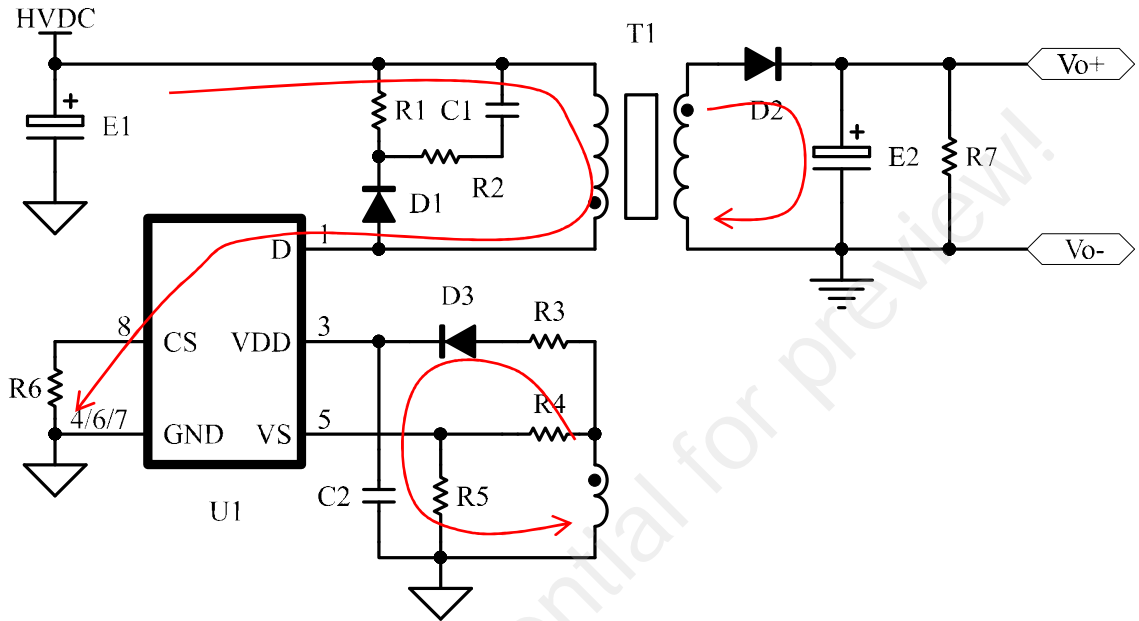


Fig6. Typical current loop diagram

#### 13.2 Typical layout reference

An example of a typical PCB layout is shown below.

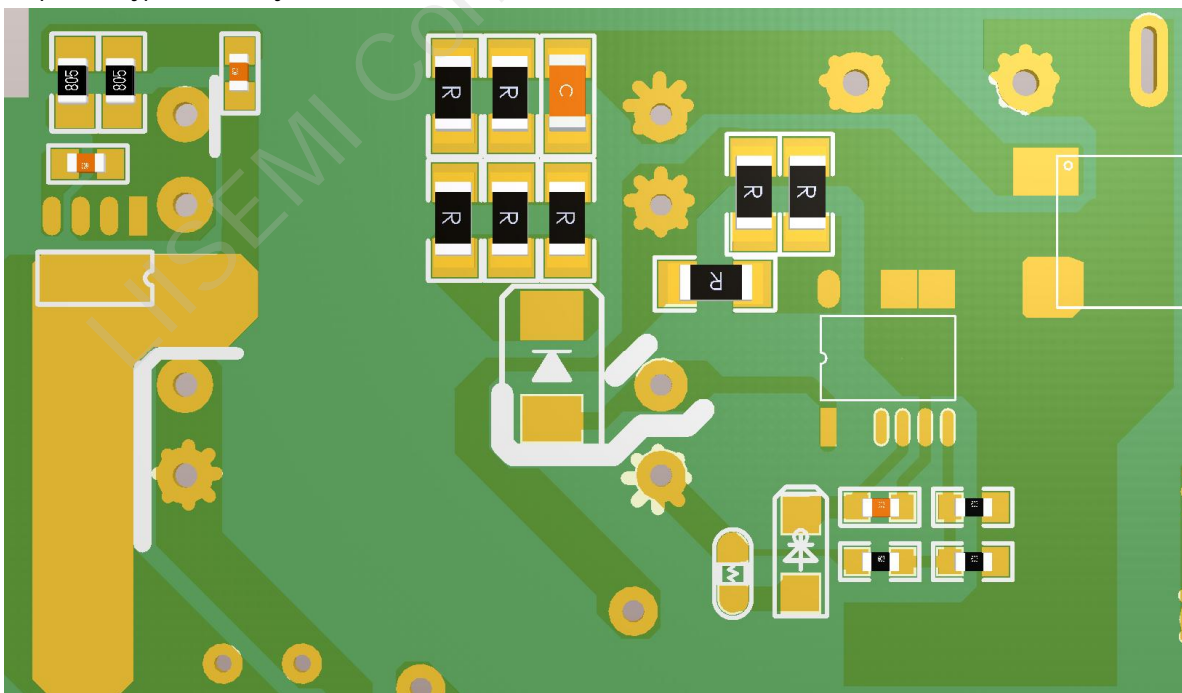


Fig7. Typical layout reference





15. Mechanical and Packaging

ASOP8

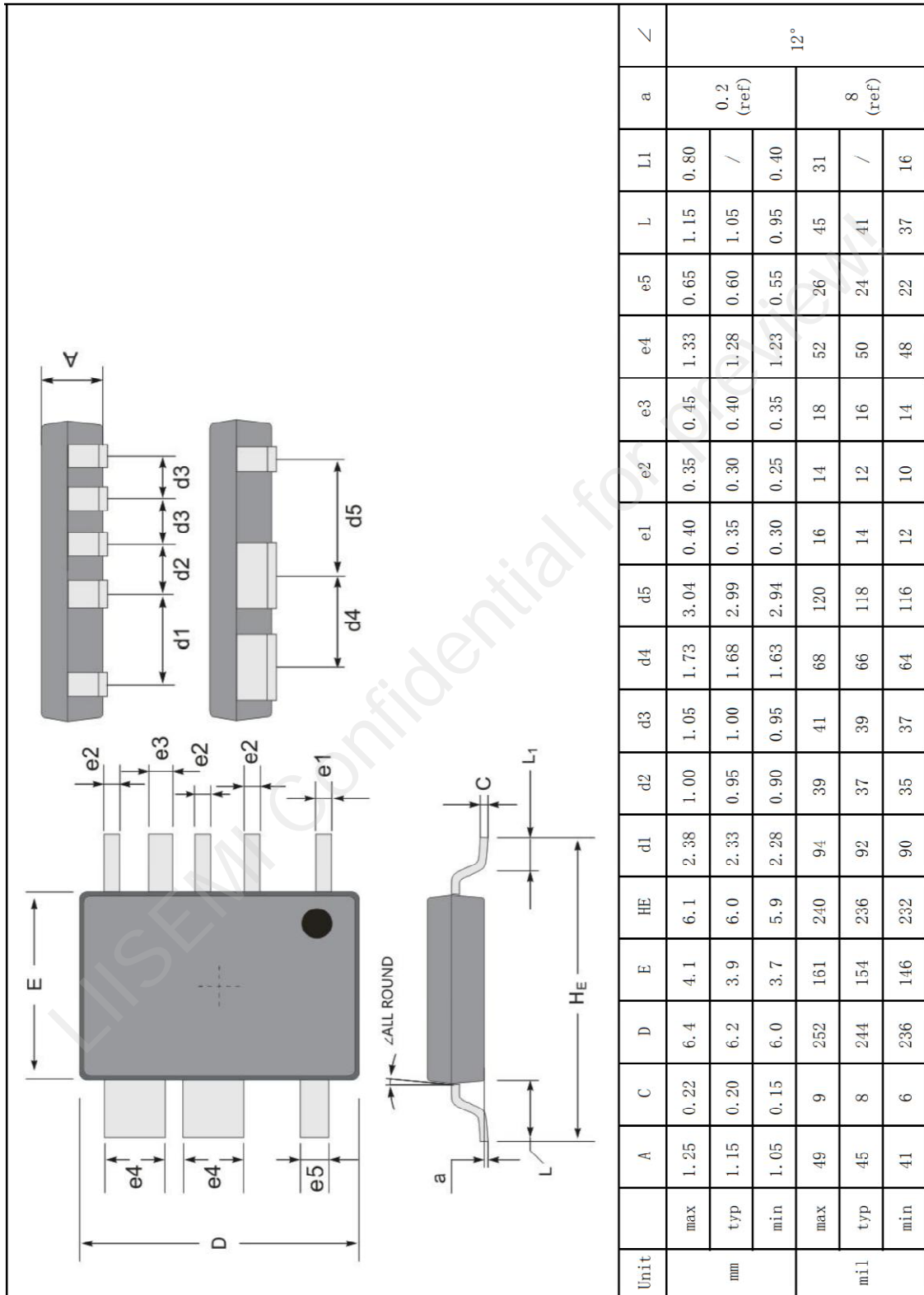
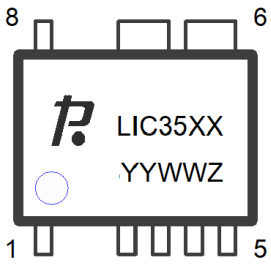


Fig9. Mechanical Dimensional Drawings


## 16. Orderable Information

Part Number	Marking	RoHs	MOS RdsON	Package	Packing
LIC3515F		Halogen Free	0.55 $\Omega$	ASOP8	100PCS/TUBE 4000PCS/Reel

Note: xx is 15F; YY is production Year; WW is production Week ; Z is other production auxiliary information.

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