

GENERAL DESCRIPTION

OB6566L is an active transition-mode (TM) power factor correction (PFC) controller for AC-DC switching mode power supply applications.

OB6566L features a demagnetization detector to ensure TM operation, a current sensing comparator with built-in leading-edge blanking, and a totem pole output ideally suited for driving a power MOSFET.

OB6566L offers great protection coverage including system over-voltage protection (OVP) to eliminate runaway output voltage due to load removal, VCC under voltage lockout (UVLO), cycle-by-cycle current limiting, Inductor short protection(ISP), and gate drive output clamping for external power MOSFET protection.

With added system open loop protection feature, OB6566L shuts down system when the feedback loop is open.

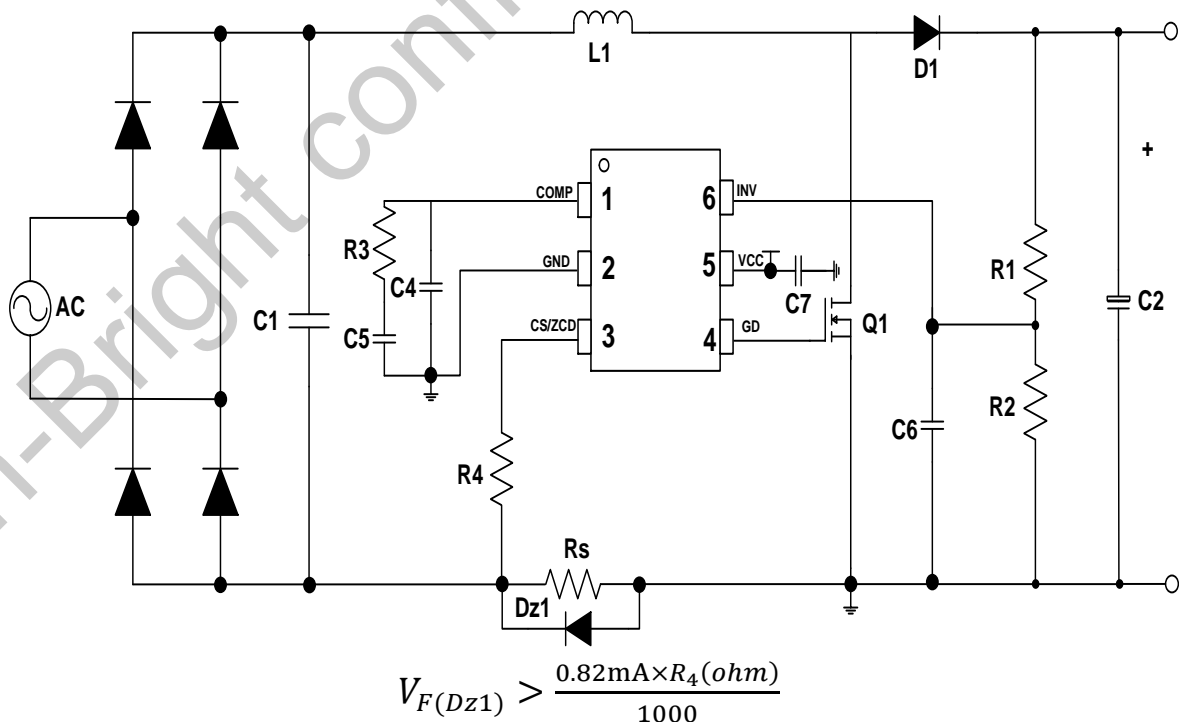
FEATURES

- Transition Mode (TM) Operation
- Works without Transformer ZCD Winding(simple inductor)
- Low Start-up Current and Operating Current
- Cycle-by-Cycle Current Limiting
- Adjustable Demagnetization detection delay
- Under Voltage Lockout with Hysteresis
- Very Precise Adjustable Output Overvoltage Protection
- Dynamic OVP & Static OVP function
- Totem Pole Output with High State Clamping
- System Open Loop Protection
- Inductor short protection
- Audio Noise Free
- 9V to 26V wide range of VCC voltage

APPLICATIONS

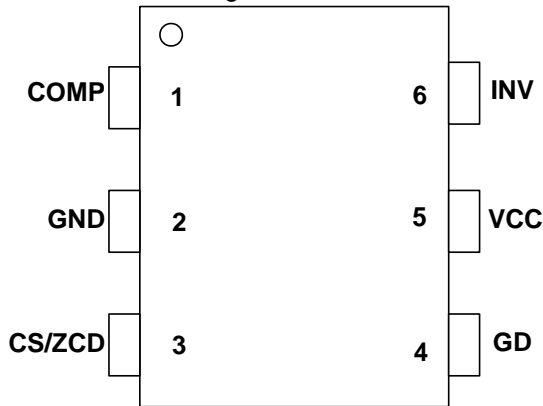
- LED lighting

TYPICAL APPLICATION



GENERAL INFORMATION

Terminal Assignment
 In SOT23-6 Package.



Ordering Information

Part Number	Description
OB6566LMP	SOT23-6, Halogen-free, T&R

Package Dissipation Rating

Package	R _{θJA} (°C/W)
SOT23-6	200

Absolute Maximum Ratings

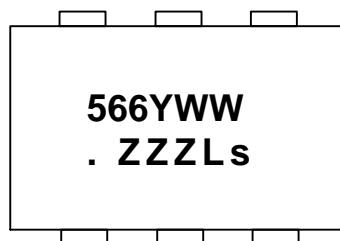
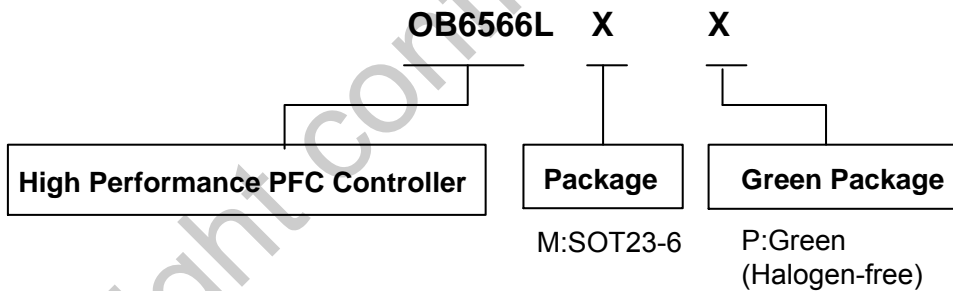
Symbol	Parameter	Value
VCC	DC Supply voltage	30 V
INV/COMP/CS	Analog inputs & outputs	-0.7 to 7V
T _j	Min/Max Operating Junction Temperature	-40 to 150 °C
T _A	Operating Ambient Temperature	-20 to 85 °C
T _{stg}	Min/Max Storage Temperature	-55 to 150 °C
Lead Temperature	(Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Range

Symbol	Parameter	Min/Max
VDD	VDD Supply Voltage	9V to 26V

Marking Information

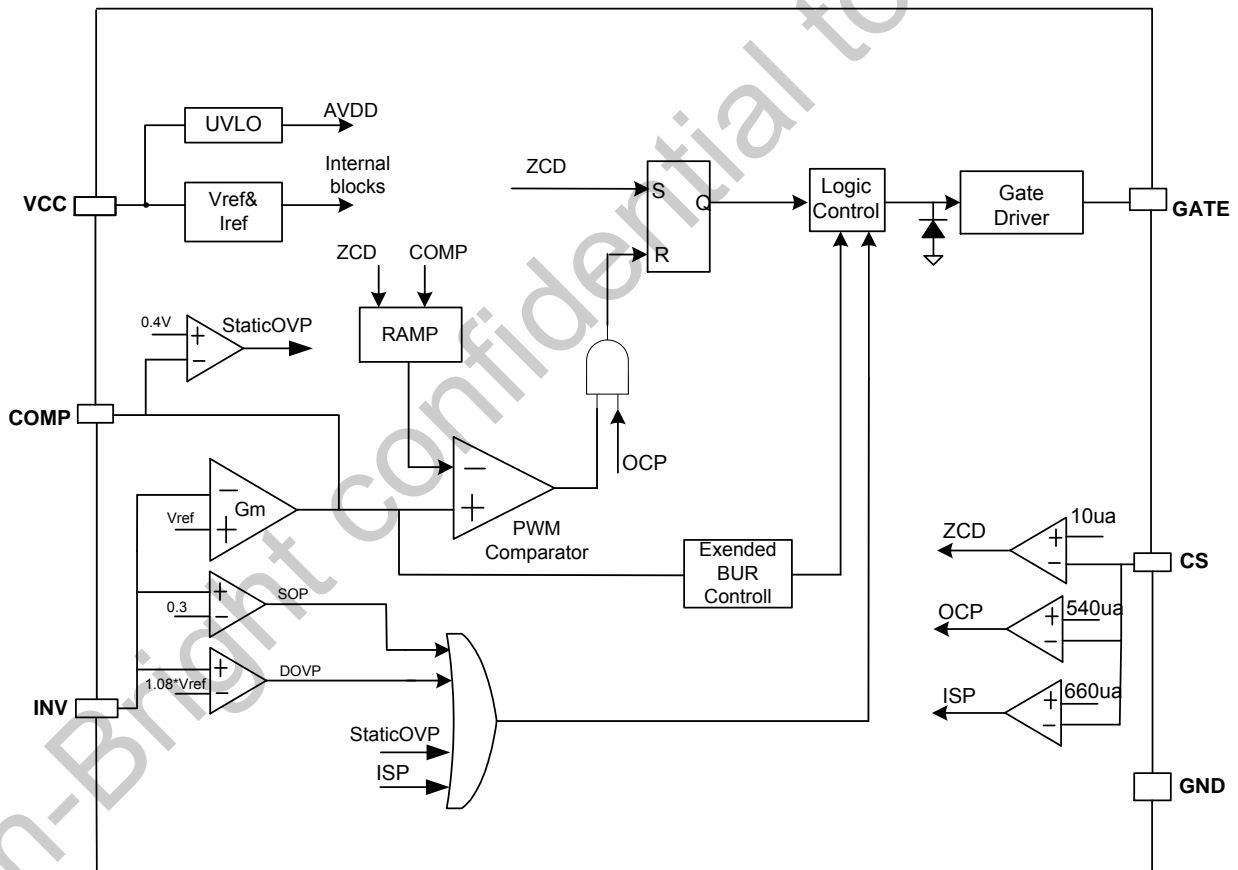


Y:Year Code
 WW:Week Code(01-52)
 L:Character Code
 s: Internal code
 ZZZ: Lot code

TERMINAL DESCRIPTIONS

Pin Num	Pin Name	I/O	Description
1	COMP	O	Output of Error Amplifier. A feedback compensation network is placed between COMP pin and GND.
2	GND	P	Ground Pin.
3	CS/ZCD	I	Current Sense Input Pin.
4	GD	O	Gate driver output. Drive Power MOSFET.
5	VCC	P	DC Supply Voltage.
6	INV	I	Inverting Input of Error Amplifier. Connect to resistor divider from system output. Connect a cap from INV to ground to set the demagnetization detection delay.

BLOCK DIAGRAM



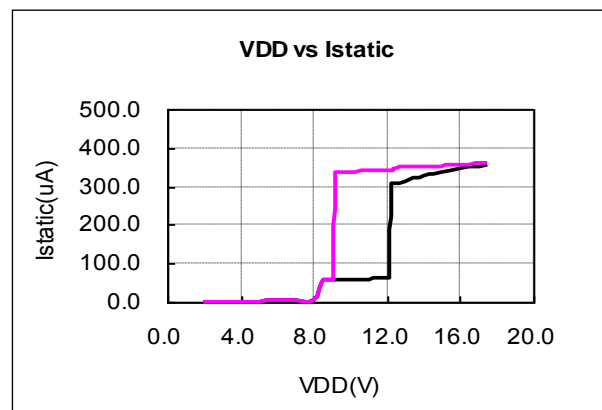
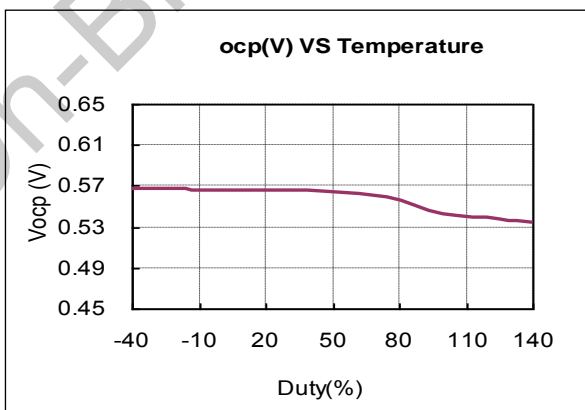
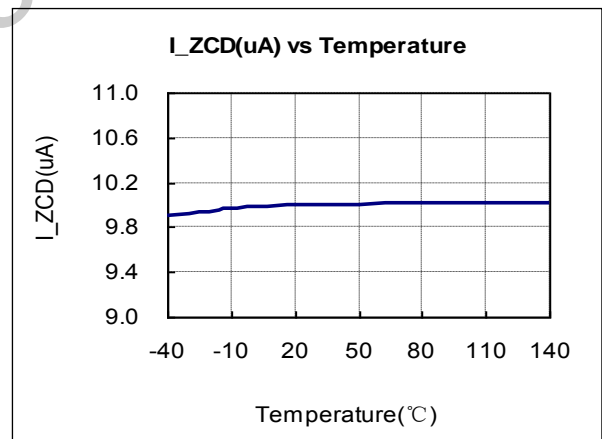
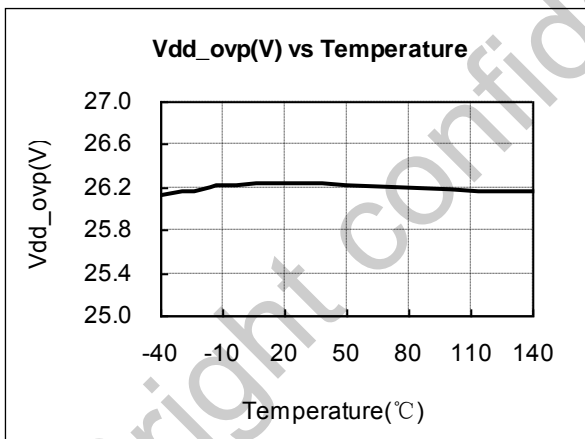
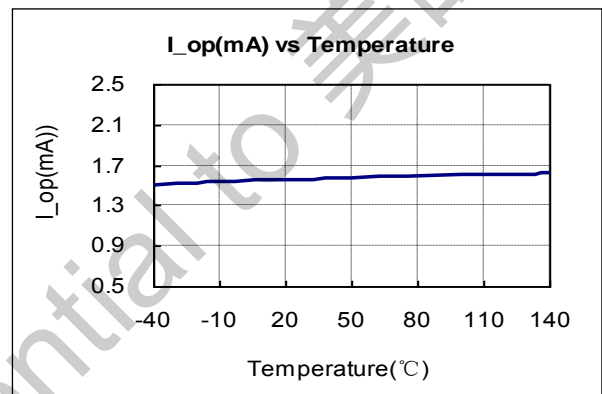
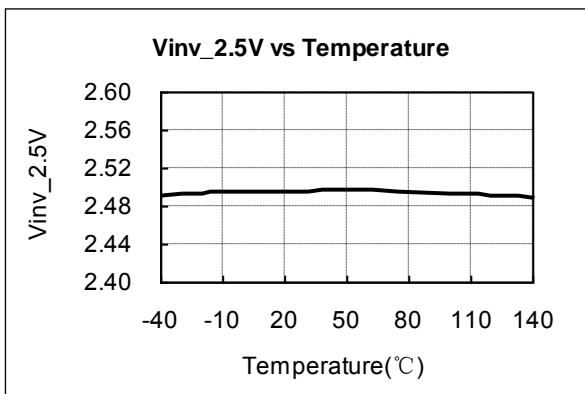
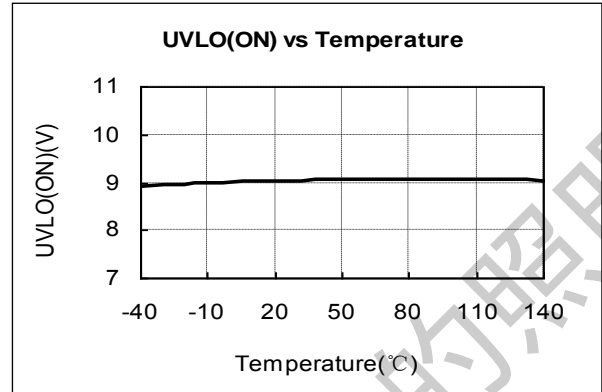
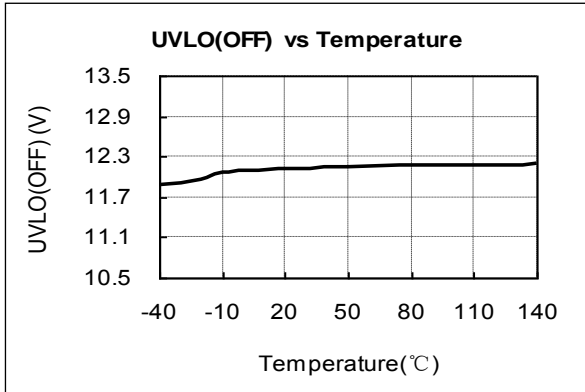
ELECTRICAL CHARACTERISTICS

 (T_A = 25°C if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
SUPPLY VOLTAGE SECTION						
V _{cc}	Operating Range	After Turn On	11		26	V
UVLO	Turn-on Threshold		11	12	13	V
	Turn-off Threshold		8	9	10	V
Hys	Hysteresis			3		V
V _z	Zener Voltage	I _{cc} =5mA	24	26	28	V
SUPPLY CURRENT SECTION						
I _{cc-start}	Start-up Current	V _{cc} =9V		50	70	uA
I _{cc}	Operating Supply Current	CL=1nf		1.6	2.6	mA
I _q	Quiescent Current	V _{pin6} ≤300mV V _{cc} =15V		0.5	1	mA
		V _{pin6} ≤300mV, V _{cc} <V _{cc} off		50	70	uA
ERROR AMPLIFIER SECTION						
V _{inv}	Voltage Feedback Input Threshold	V _{cc} =15V	2.45	2.5	2.55	V
V _{inv}	Line Regulation	12V<V _{cc} <26V		2	5	mV
I _{inv}	Input Bias Current	I _{DD} = 10 mA		-0.1	-1	uA
G _m	Transconductance	Open Loop		200		uS
I _{comp}	Source Current	V _{comp} =3.6V, V _{inv} =2.4V		-20		uA
	Sink Current	V _{comp} =3.6V, V _{inv} =2.6V		20		uA
V _{comp}	Upper Clamp Voltage			5.2		V
	Lower Clamp Voltage			0.3		V
OVER VOLTAGE PROTECTION						
V _{sovp}	Static OVP triggering voltage	V _{INV} =2.5V		0.4		V
V _{dovp}	Dynamic OVP triggering voltage	V _{comp} =3.0V	2.65	2.7	2.74	V
ZERO CURRENT DETECTOR						
I _{th_zcd}	ZCD threshold current	R ₄ =1k	7	10	13	uA
LEB	Lead edge blanking time			200		ns
OCP & ISP						
I _{th_OCP}	OCP threshold current	R ₄ =1K		540		uA
I _{th_ISP}	ISP threshold current	R ₄ =1K		660		uA
T _{d_ISP}	ISP debounce time			16		Cycle
GATE DRIVE SECTION						
V _{oL}	Low Output Voltage	V _{cc} =15V, I _o =100mA			1.5	V
V _{oH}	High Output Voltage	V _{cc} =15V, I _o =100mA	10			V

Ton_max	Max Ton time corresponding to Vcomp=4V			30		us
Tr	Rising Time	Cl=1000pF, 10~90%		80	150	ns
Tf	Falling Time	Cl=1000pF, 10~90%		30	70	ns
Voclap	Output Clamp Voltage	Vcc=25V		11	12	V
Clamped low operational frequency						
Fmin	Clamped low operational frequency under extended BUR mode			23		KHz
STARTUP TIMER						
Tstart	Re-Start Timer Period			150		us
SYSTEM OPEN LOOP PROTECTION COMPARATOR						
Vth_sop	System Open Loop Protection Comparator Threshold			300		mV

TYPICAL PERFORMANCE CHART



OPERATIONAL DESCRIPTION

OB6566L is a highly integrated power factor correction (PFC) controller IC. The transition mode control greatly reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

- **Error Amplifier**

Connected to a resistor divider from output line, the inverting input of the Error Amplifier (EA) is compared to an internal reference voltage (2.5V) to set the regulation on output voltage.

The EA output is externally connected for loop compensation. It is usually realized with a type II filter which connected between the ground and EA output. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

- **Dynamic Output Overvoltage Protection**

OB6566L offers two level OVP protection including dynamic OVP for output fast transient protection and static OVP for output steady-state protection.

When output voltage exceeds 432V which correspond to a INV voltage larger than $1.08 \cdot V_{ref}$, the GATE output is turned off and OB6566L is disabled. Only when INV voltage reach below $1.06 \cdot V_{ref}$, the operation of OB6566L is resumed.

- **Static Output Overvoltage Protection**

With the loading goes low, Ton of power MOSFET GATE decreases and eventually stays at its minimum. The system will enter Extended BUR mode in which Toff is extended to lower the burst point. Static OVP comparator is finally activated and power MOSFET Gate is off when COMP voltage is dropped below 0.4V. Normal operation is resumed when Error Amplifier goes back to its linear region after output voltage drops.

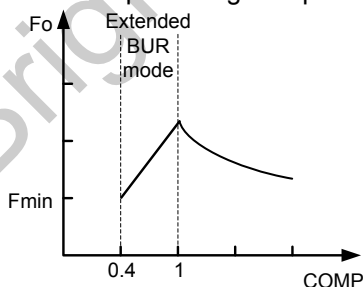


Fig1 Extended BUR mode

- **Startup Current and Start up Control**

The typical startup current of OB6566L is 50uA when the VCC voltage is lower than the UVLO threshold so that VCC could be charged up and

start up the device. A high value, low wattage startup resistor can therefore be used to minimize the power loss during the normal operation.

- **Current Sensing Comparator and Leading Edge Blanking**

Cycle-by-cycle current limiting is provided in OB6566L's peak current mode control. The switch current is detected by a sense resistor into the sense pin. The switch-on spike is blanked out via an internal leading edge blanking (LEB) circuit. Another extra function of LEB is that it limits the system minimum on time, thus the THD of system at light load will be decreased.

The RS flip-flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle.

- **Demagnetization Detection**

OB6566L can perform demagnetization detection by using current sensing mechanism. When the stored energy is fully released to the output, the absolute voltage at CS pin decrease. A new switching cycle is initiated once the CS voltage > -10mv. The turn on of power MOSFET is initiated after a delay when the inductor's current reaches zero.

- **Gate Drive Output**

The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 11V clamp at the gate output protects the MOSFET gate from high voltage stress.

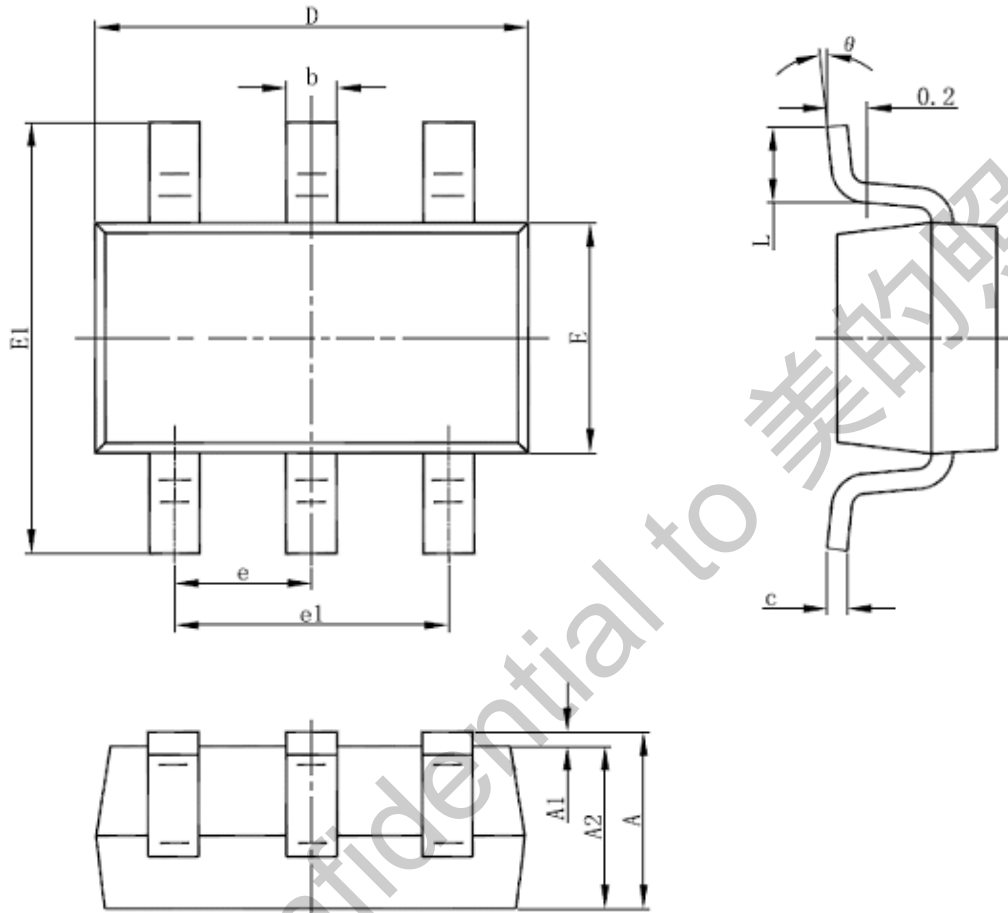
- **Protection Controls**

OB6566L ensures good reliability design through its good protection coverage. Output dynamic and static over-voltage protection (OVP), VCC under voltage lockout (UVLO), VDD over-voltage protection (VDDOVP), System open protection (SOP), cycle-by-cycle current limiting, Inductor short protection (ISP) and output gate clamp are standard features provided by OB6566L.

- **System Open Loop Protection**

A new function of system open loop protection is provided in OB6566L. The voltage at INV pin is sensed. If INV pin is below 0.3V typical, the switching will be stopped. In this way, the system output voltage cannot increase too high (only the rectified line voltage), and the pre-converter will be protected from damage.

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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