

1MHz, 3.5A Step-Up Current Mode PWM Converter



General Description

The FP6293 is a current mode boost DC-DC converter. Its PWM circuitry with built-in 0.14Ω power MOSFET make this regulator highly power efficient. The internal compensation network also minimizes as much as 6 external component counts. The non-inverting input of error amplifier connects to a 0.6V precision reference voltage and internal soft-start function can reduce the inrush current.

The FP6293 is available in the DFN-8L/SOP-8L(EP) package and provides space-saving PCB for the application fields.

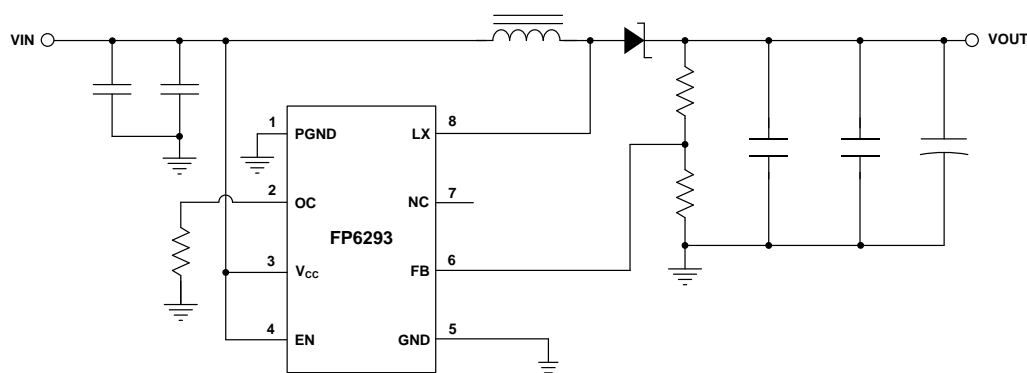
Features

- Adjustable Output up to 13V
- Internal Fixed PWM frequency: 1.0MHz
- Precision Feedback Reference Voltage: 0.6V ($\pm 2\%$)
- Internal 0.14Ω, 3.5A, 18V Power MOSFET
- Shutdown Current: 0.1μA
- Over Temperature Protection
- Over Voltage Protection
- Adjustable Over Current Protection: 0.5A ~ 3.5A
- Package: DFN-8L, SOP-8L(EP)

Applications

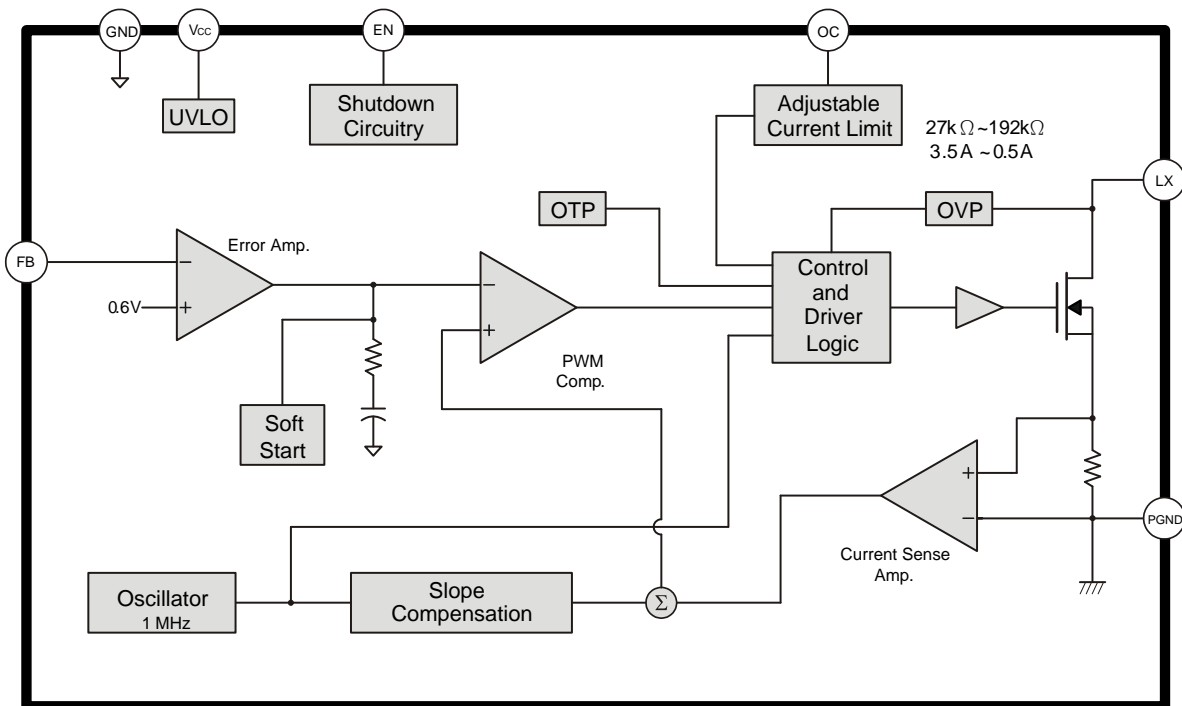
- Chargers
- LCD Displays
- Digital Cameras
- Handheld Devices
- Portable Products

Typical Application Circuit



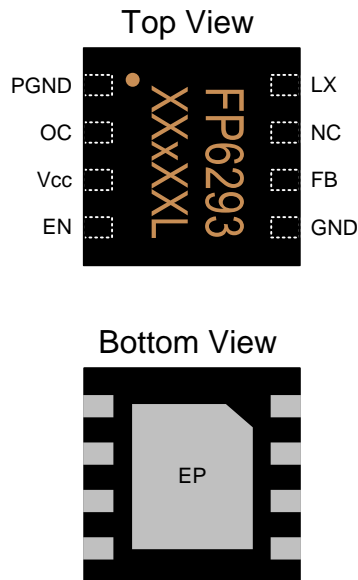
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Function Block Diagram



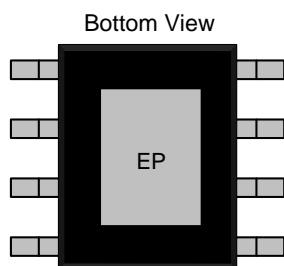
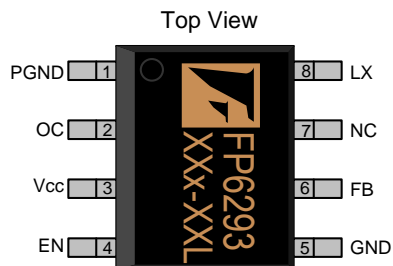
Pin Descriptions

DFN-8L



Name	No.	I / O	Description
PGND	1	P	IC Ground
OC	2	I	Adjustable Current Limit (Floating Available)
Vcc	3	P	IC Power Supply
EN	4	I	Enable Control (Active High)
GND	5	P	IC Ground
FB	6	I	Error Amplifier Inverting Input
NC	7	NA	Not Connected
LX	8	O	Power Switch Output
EP	9	P	Exposed PAD-Must connect to Ground

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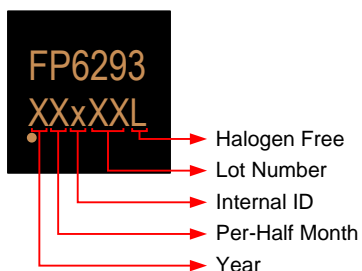
SOP-8L(EP)


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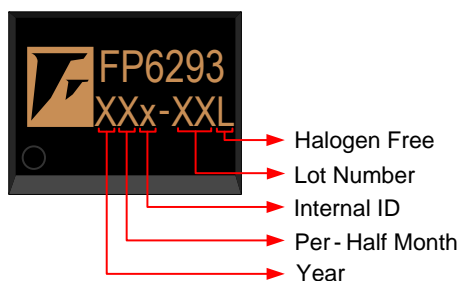
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Marking Information

DFN-8L



SOP-8L



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example → Lot : 123456 → XXx-56L

Internal ID: Internal Identification Code

Per-Half Month: Production period indicator in half month time unit

- For Example :
- A → First Half Month of January
 - B → Second Half Month of January
 - C → First Half Month of February
 - D → Second Half Month of February

Year: Production year's last digit

Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6293dR-G1	-40°C ~ 85°C	DFN-8L	2500EA	Tape & Reel
FP6293XR-G1	-40°C ~ 85°C	SOP-8L(EP)	2500EA	Tape & Reel

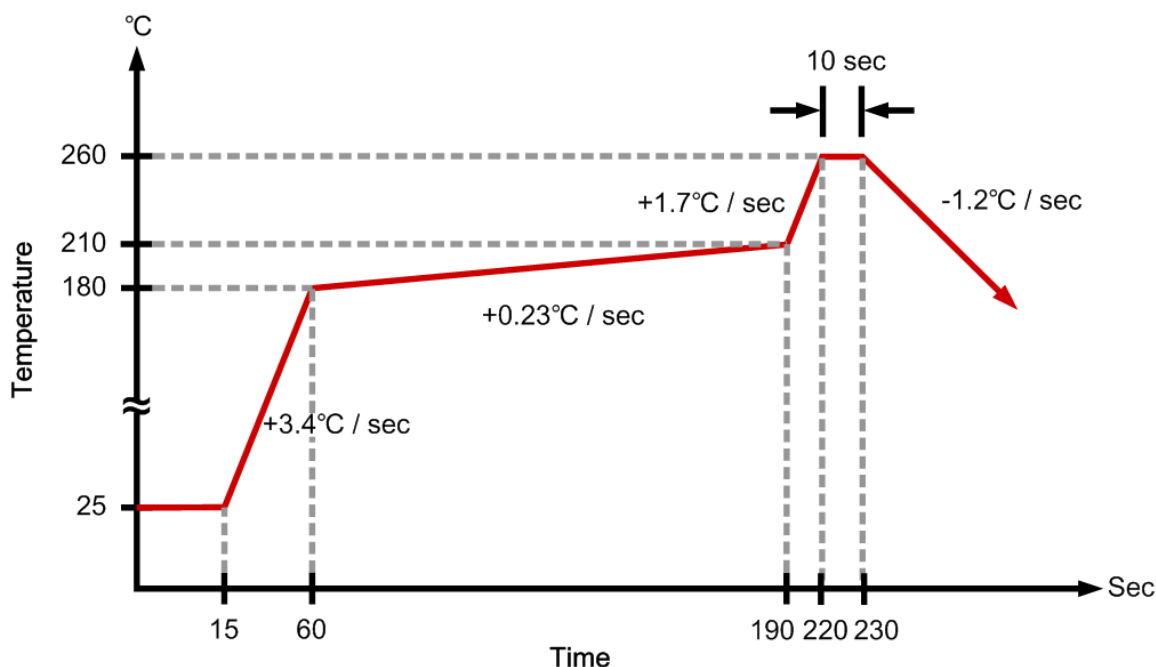
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		0		6	V
LX Voltage	V_{LX}		0		18	V
EN,FB Voltage			0		6	V
Thermal Resistance (Note1)	θ_{JA}	DFN-8L(3x3mm)			+68	°C / W
		SOP-8L(EP)			+83	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-40		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

Note1:

θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V _{IN}		2.6		5.5	V
Operating Temperature Range	T _A	Ambient Temperature	-40		+85	°C

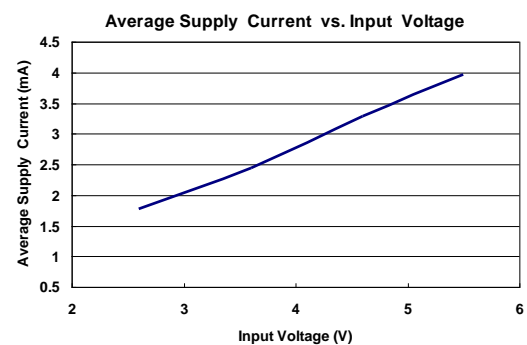
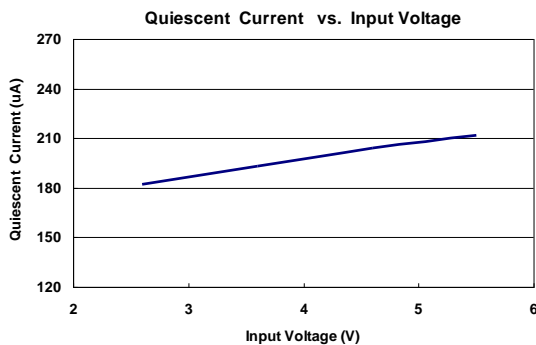
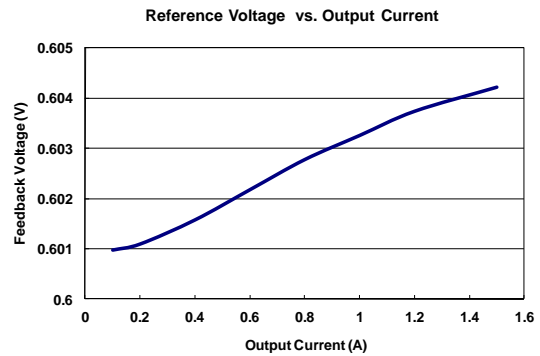
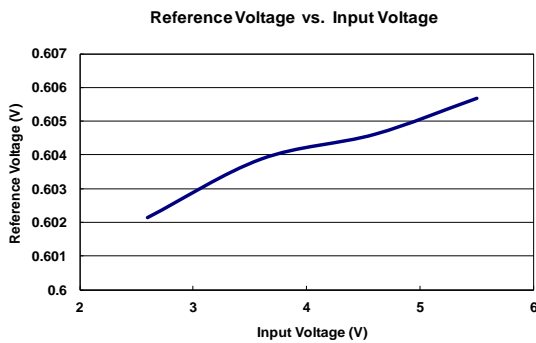
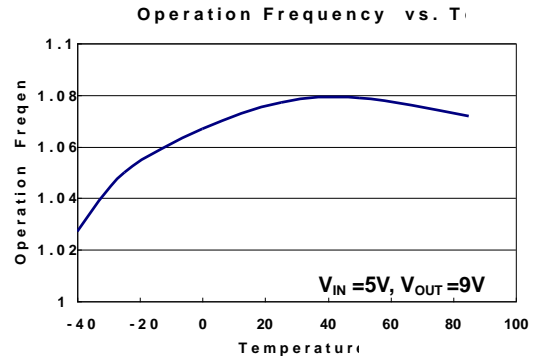
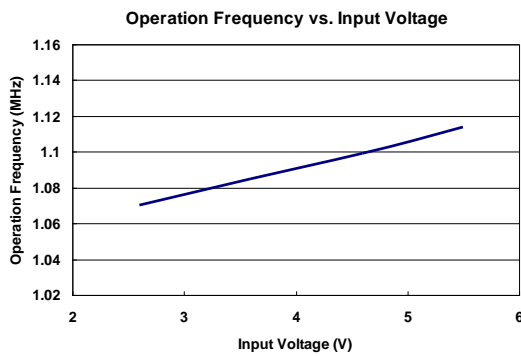
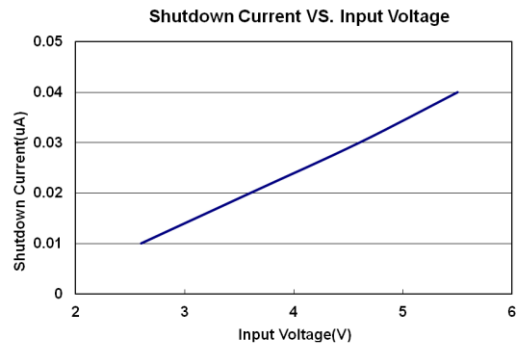
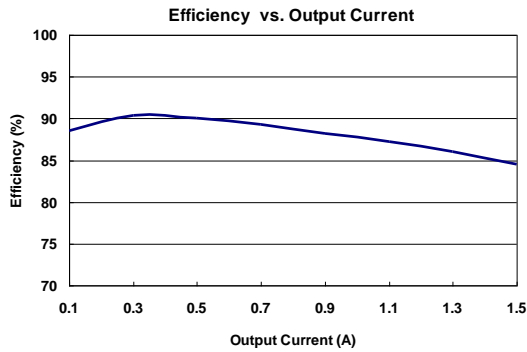
DC Electrical Characteristics (V_{CC}=3.3V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System Supply Input						
Input Supply Range	V _{CC}		2.6		5.5	V
Under Voltage Lockout	V _{UVLO}			2.2		V
UVLO Hysteresis				0.1		V
Quiescent Current	I _{CC}	V _{FB} =0.66V, No switching		0.19		mA
Average Supply Current	I _{CC}	V _{FB} =0.55V, Switching		2.84		mA
Shutdown Supply Current	I _{CC}	V _{EN} =GND		0.1		μA
Oscillator						
Operation Frequency	F _{OSC}	V _{FB} =1.0V	0.8	1.0	1.2	MHz
Frequency Change with Voltage	Δ f / Δ V	V _{CC} =2.6V to 5.5V		5		%
Maximum Duty Cycle	T _{DUTY}			90		%
Reference Voltage						
Reference Voltage	V _{REF}		0.588	0.6	0.612	V
Line Regulation		V _{CC} =2.6V ~ 5.5V		0.2		% / V
Enable Control						
Enable Voltage	V _{EN}		0.96			V
Shutdown Voltage	V _{EN}				0.6	V
MOSFET						
On Resistance of Driver	R _{DS (ON)}	I _{LX} =2A		0.14		Ω
Protection						
OCP Current	I _{OCP}			3.5		A
Adjustable OCP Current	I _{OCP}	With External Resistor : 27k~192k	0.5		3.5	A
OTP Temperature	T _{OTP}			+150		°C

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Typical Operating Characteristics

($V_{CC}=3.3V$, $V_{OUT}=5V$, $T_A= 25^{\circ}C$, unless otherwise noted)



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Function Description

Operation

The FP6293 is a current mode boost converter. The constant switching frequency is 1MHz and operates with pulse width modulation (PWM). Build-in 18V / 3.5A MOSFET provides a high output voltage. The control loop architecture is peak current mode control; therefore slope compensation circuit is added to the current signal to allow stable operation for duty cycles larger than 50%.

Soft Start Function

Soft start circuitry is integrated into FP6293 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Current Limit Program

A resistor between OC and GND pin programs peak switch current. The resistor value should be between 27k and 192k. The current limit will be set from 3.5A to 0.5A. Keep traces at this pin as short as possible. Do not put capacitance at this pin. To set the over current trip point according to the following equation:

$$I_{OCP} = \frac{96000}{R3}$$

Over Temperature Protection (OTP)

FP6293 will turn off the power MOSFET automatically when the internal junction temperature is over 150°C. The power MOSFET wake up when the junction temperature drops 30°C under the OTP threshold temperature.

Over Voltage Protection (OVP)

In some condition, the resistive divider may be unconnected, which will cause PWM signal to operate with maximum duty cycle and output voltage is boosted higher and higher. The power MOSFET will be turned off immediately, when the output voltage exceeds the OVP threshold level. The FP6293's OVP threshold is 16V.

Application Information

Inductor Selection

Inductance value is decided based on different condition. 3.3 μ H to 4.7 μ H inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency. Also, it avoid inductor saturation which will cause circuit system unstable and lower core loss at 1 MHz.

Capacitor Selection

The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

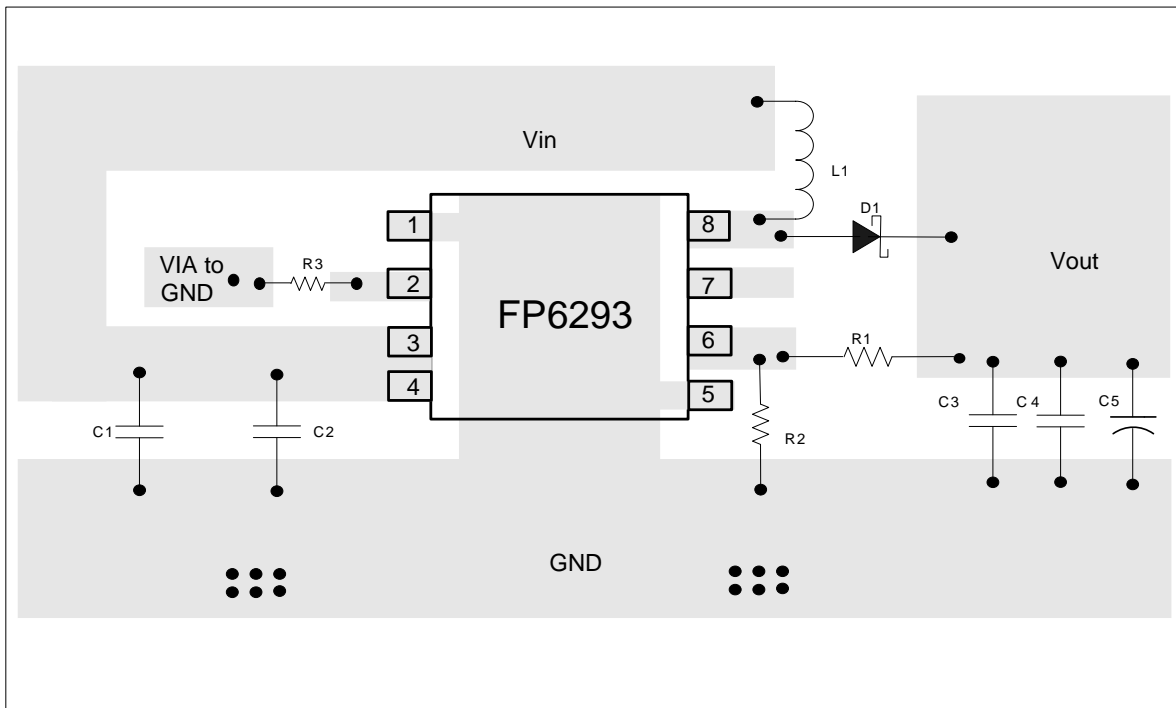
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 0.6V \left(1 + \frac{R1}{R2} \right)$$

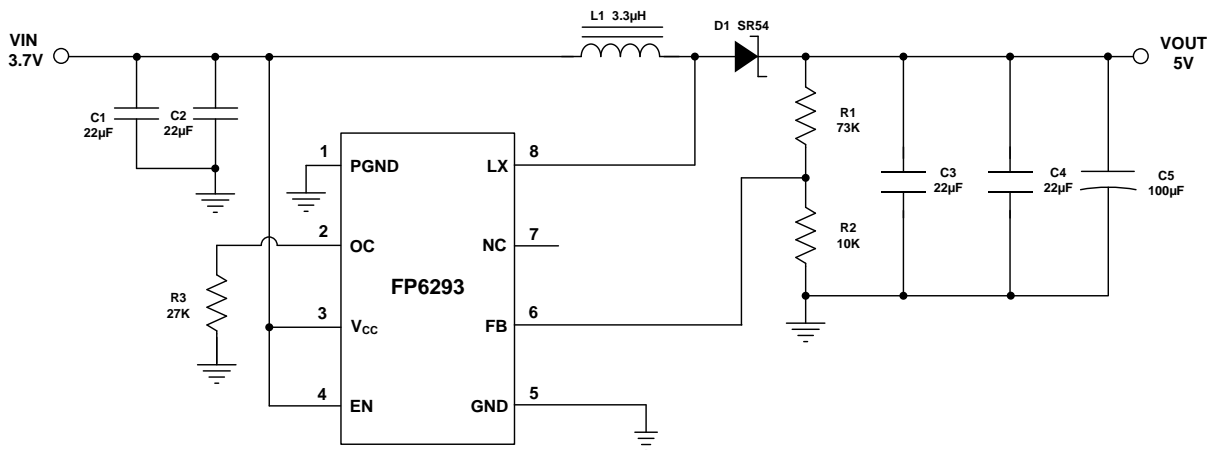
Layout Considerations

1. The power traces, consisting of the GND trace, the LX trace and the V_{CC} trace should be kept short, direct and wide.
2. LX, L and D switching node, wide and short trace to reduce EMI.
3. Place C_{IN} near V_{CC} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
4. The resistive divider R1 and R2 must be connected to FB pin directly as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, LX.
6. The GND of the IC, C_{IN} and C_{OUT} should be connected close together directly to a ground plane.



Suggested Layout

Typical Application

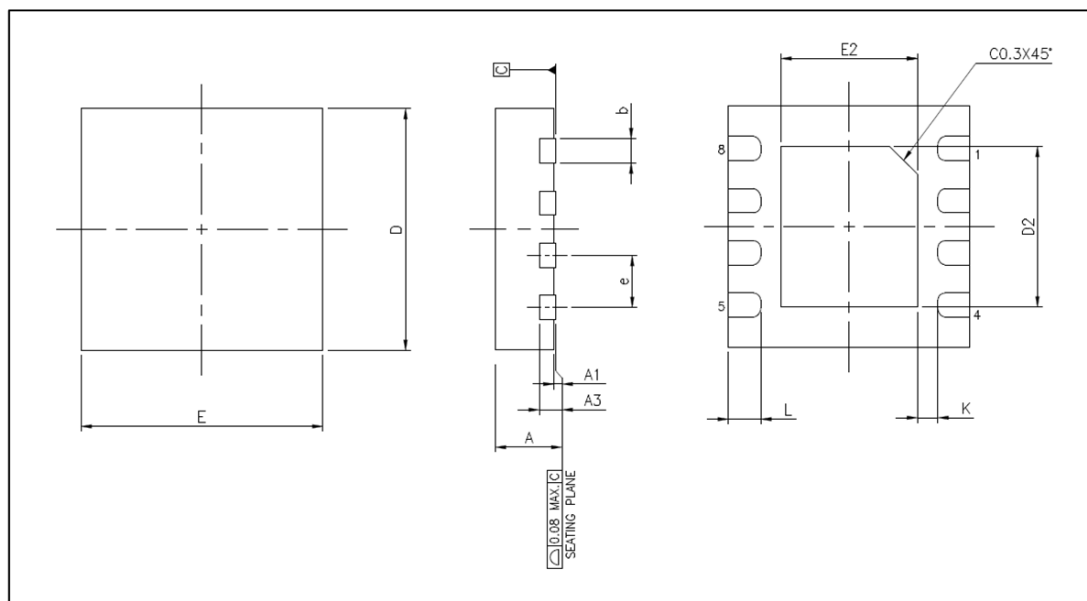


Note:

1. Don't pull the Vout back to the FP6293's Vcc pin. When the system receives the noise, it will lead to Vout ripple too high and over the absolute maximum rating of the Vcc pin.
2. EN voltage must be less than or equal to V_{CC} voltage.

Package Outline

DFN-8L



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	0.700	0.800
A1	0.000	0.050
A3	0.20REF	
b	0.25	0.35
D	3.000 BSC	
E	3.000 BSC	
e	0.650 BSC	
K	0.200	-

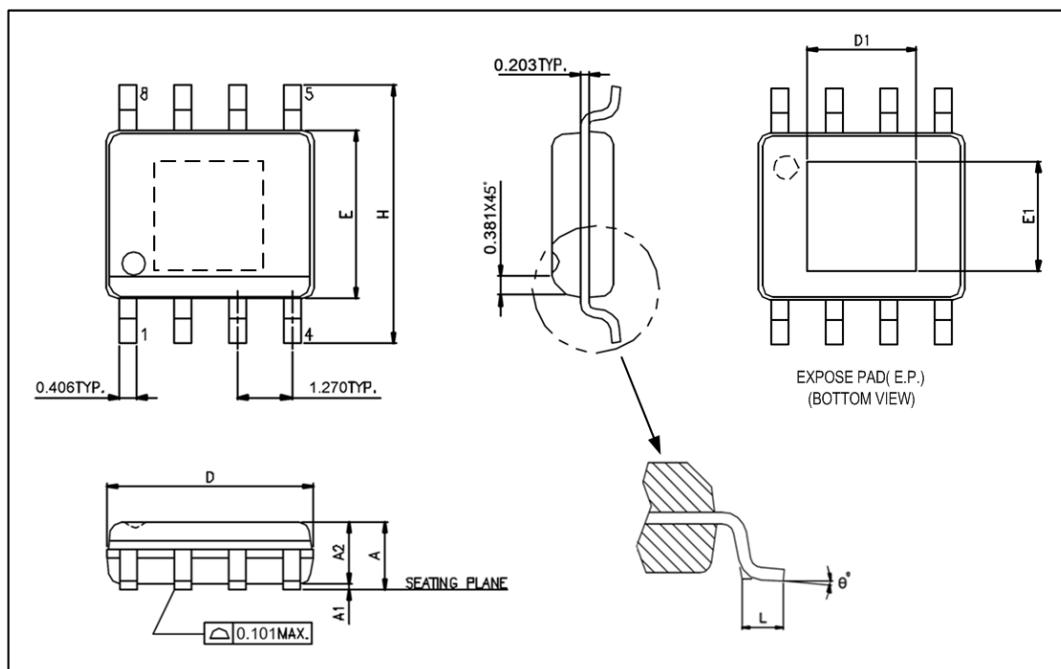
Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E2	1.600	1.800
D2	1.900	2.050
L	0.350	0.450

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-229
2. Dimension b applied to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

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SOP-8L(EP)

UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1		2.184 REF
D1		2.971 REF

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash or protrusions.

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