2SP0215F2Q0C
SCALE EV Family

Automotive Dual Channel Plug-and-Play Gate Driver
for 17 mm Modules

PRELIMINARY

Product Highlights

- Ready-to-use dual channel gate driver solution for EconoDUAL™ 17 mm IGBT power modules up to 1200 V
- Primary-side electrical interface with reinforced isolation
- +20 A / -15 A peak output gate current
- Up to 20 kHz switching frequency
- Gate power of 1.5 W per channel at maximum ambient temperature
- Digital Communication Interface
- -40 °C to +85 °C operating ambient temperature
- Operation up to 5500 m altitude
- High common-mode transient immunity

Protection, Safety and Diagnostic Features

- 5 V input logic
- DC-link Active Discharge (AD) function
- Motor Active Short Circuit (ASC) function
- Galvanically isolated analog temperature measurement for module integrated NTC elements
- Rail-to-rail stabilized secondary-side output voltage
- Integrated FluxLink™ technology providing reinforced isolation barrier between primary-side and secondary-side
- Advanced Resistive Overvoltage Control (AROC) controlled soft turn-off in response to any critical failure
- Internal communication monitoring
- Undervoltage monitoring (UVLO) for primary-side and secondary-side
- Secondary-side overvoltage monitoring (OVLO)
- Gate monitoring
- Two-stage primary-side and secondary-side die temperature monitoring
- Desaturation monitoring
- DC/DC controller over current monitoring
- Separate isolated digital failure and status outputs
- Active Miller clamp
- Conformal coating

Full Safety and Regulatory Compliance

- ASIL-B certification (pending)
- Clearance and creepage distances between primary and secondary sides meet requirements for reinforced isolation (according to IEC 60664-1, IEC 60664-3)
- SEooC product certification (pending)
- 100% production partial discharge test
- 100% production HIPOT testing at 4000 kV_{RMS} for 1 s

Applications

- E-Bus and E-Truck traction inverter
- Diesel-electric traction inverter
- Fuel cell inverter
- Agricultural and construction vehicles and equipment
- Other automotive and industrial applications
- General purpose drives

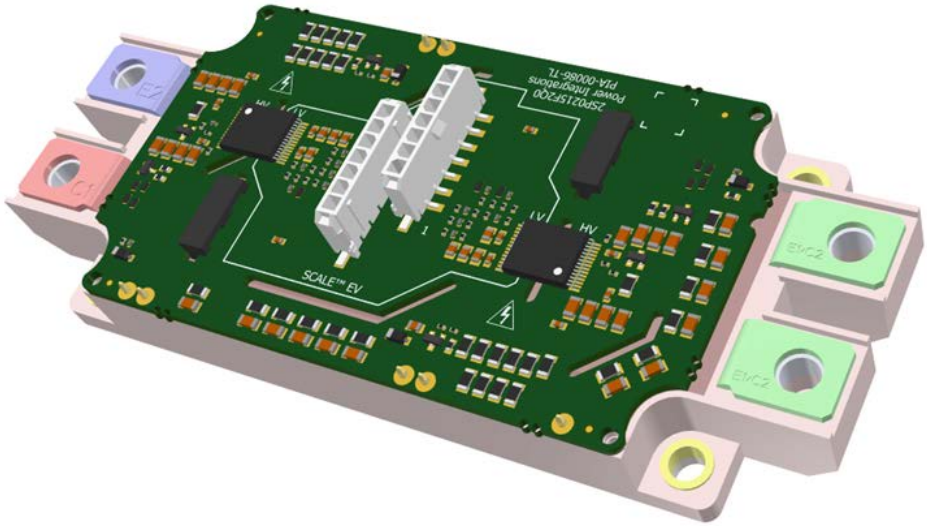

Figure 1. 2SP0215F2Q0C Mounted to Target Module.

Product Portfolio

Product	Power Module Technology	Voltage Class	Current Class	Package	Power Module Supplier
2SP0215F2Q0C-FF900R12ME7W_B11	Si-IGBT Gen7, Si-Diode	1200 V	900 A	EconoDUAL	Infineon

Table 1. 2SP0215F2Q0C Portfolio.

Assembly Drawing and Interface Description

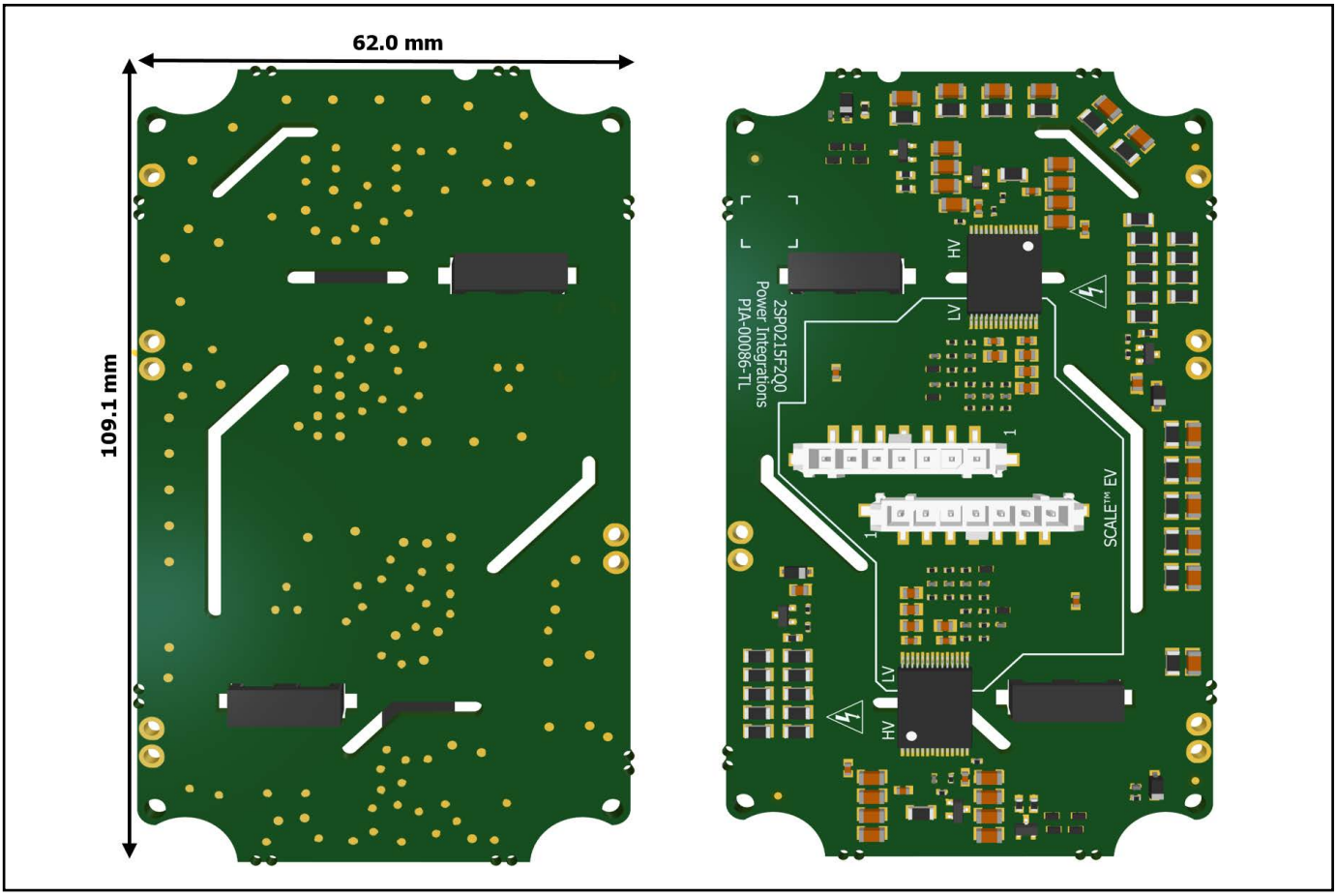

Figure 2. Assembly Drawing.

Connector X400

Connection to external system controller from top domain (Molex Micro-Fit 3.0 connector).

VCC2 (Pin 1)
Primary-side 5 V supply voltage.

ASC_AD2 (Pin 2)
ASC_AD Mode selector.

ASC_AD_EN2 (Pin 3)
ASC_AD Mode enable selector.

SO2 (Pin 4)
Status output.

IN2 (Pin 5)
Primary-side PWM signal.

B_OUT2 (Pin 6)
Digital serial output interface.

GND (Pin 7)
Primary-side GND supply connection for the primary side electronics.

Connector X300

Connection to external system controller from bottom domain (Molex Micro-Fit 3.0 connector).

VCC1 (Pin 1)
Primary-side 5 V supply voltage.

ASC_AD1 (Pin 2)
ASC_AD Mode selector.

ASC_AD_EN1 (Pin 3)
ASC_AD Mode enable selector.

SO1 (Pin 4)
Status output.

IN1 (Pin 5)
Primary-side PWM signal.

B_OUT1 (Pin 6)
Digital serial output interface.

GND (Pin 7)
Primary-side GND supply connection for the primary-side electronics.

Functional Description

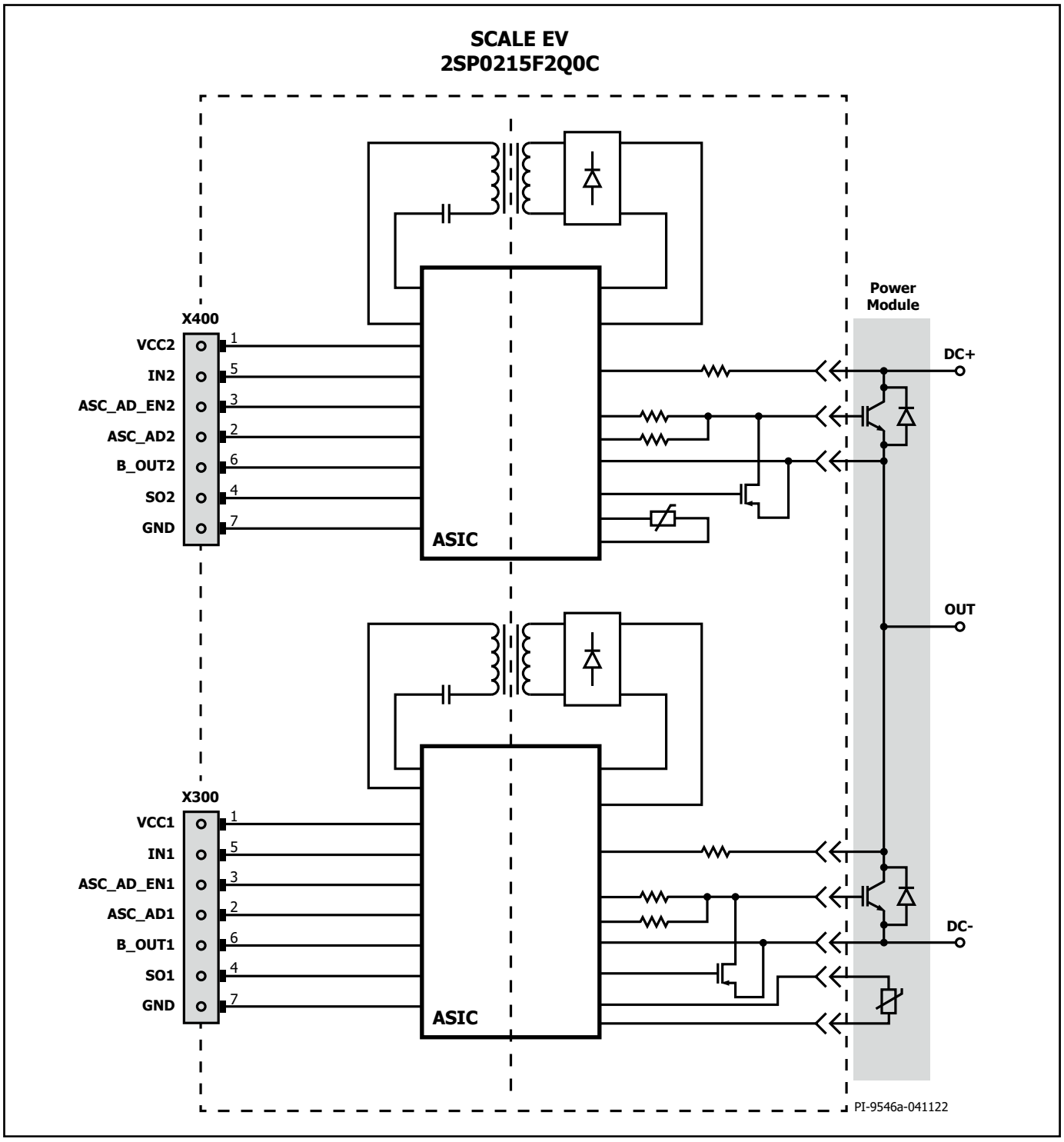

Figure 3. Functional Block Diagram.

Description

The 2SP0215F2Q0C is a dual channel gate driver for EconoDUAL 17 mm modules driving IGBT switches. The Plug-and-Play gate driver board is designed for applications requiring automotive qualification like e-BUS, e-Truck, Battery Electrical Vehicles, Hybrid Electrical Vehicles or fuel cell inverters operating up to 1000 V battery voltage. The gate driver provides automotive related protection functionalities and diagnostics. A galvanic isolated IGBT module integrated NTC read-out provides IGBT module temperature information.

As a plug-and-play gate driver, the 2SP0215F2Q0C characteristics match the requirements of specific power modules. The command signals are transferred from the primary-side (IN1 and IN2) to the secondary-side via the FluxLink isolation technology. Secondary-side supplies provide a positive gate voltage and drives the power semiconductor gate during the turn-on process and while turned on. Similar, the secondary-side supplies provide a negative gate voltage and discharges the gate during the turn-off process and clamps the gate while turned off. In addition, the AMC (Active Miller Clamp) clamps the gate to the negative supply voltage to prevent parasitic turn-on of the power semiconductor. Short-circuit protection as well as dynamic overvoltage limiting (AROC – Advanced Resistive Overvoltage Control) are also provided. In case of a short-circuit during a turn-on event, the 2SP0215F2Q0C initiates turn-off in order to protect the semiconductor device from damage due to the short-circuit. During turn-off events, the 2SP0215F2Q0C senses turn-off V_{CE} overvoltages and limits them by using AROC to restrict the voltage to a safe value below maximum blocking voltage of the semiconductor device.

PWM Signals

The input logic (IN1 low-side switch and IN2 high-side switch) is designed to work directly with controllers using 5 V CMOS logic. The recommended pull-down resistors (R_{IN}) that suppress EMI at the gate driver inputs are included in the design. Gate driver commands are transferred from IN1 and IN2 to GH (turn-on) and GL (turn-off) with propagation delays $t_{P(LH)}$ and $t_{P(HL)}$ respectively.

PWM Interlocking

Input PWM signals IN1 and IN2 are interlocked with each other. This feature prevents a synchronous turn-on of channel 1 and channel 2 at the same time. An IGBT bridge short-circuit is not possible under standard operating conditions. If an interlock event occurs, i.e. IN1 and IN2 both exceed the threshold voltages $V_{IN+(H)}$ and $V_{IN-(H)}$, B_OUT[28] will be set to Logic Low and the gate driver output stage will be turned off.

Protection Dead-Time

A minimum protection dead-time avoids synchronous or overlapping switching of the power switches. The 2SP0215F2Q0C provides the minimum dead-time necessary to protect from bridge short-circuits. In case the dead-time between IN1 and IN2 is smaller than t_{DT}, the gate driver will insert a minimum dead-time of t_{DT} and set B_OUT[28] to Logic Low. The system dead-time is generated in the external system controller.

Note: Synchronous or overlapping switching of top and bottom switches within a half-bridge leg may damage or destroy the power switch(es) and in conjunction with a secondary failure, the attached gate driver itself. Half-bridge currents are difficult to measure and can present a reliability issue over time. The 2SP0215F2Q0C protects the system from false overlapping switching events. 2SP0215F2Q0C may not protect against continuously asserted incorrect system dead-times.

Power Supply

Two individual supply voltages (VCC2-GND and VCC1-GND) for top channel and bottom channel respectively are necessary to operate the 2SP0215F2Q0C. The supply voltage must be within specification limits to avoid malfunctions. The current consumption of the gate driver depends on the switching frequency.

Note: The gate driver does not provide reverse voltage protection.

Note: The cable connecting to X400 and X300 should be made as short as possible. Routing the cable such that it touches or crosses high voltage potentials is not permitted.

Safe Power-Up and Power-Down

During the power-up and power-down events, IN1 and IN2 pins must stay at logic low. Any supply voltage related to V_{CCx} or GND should be stabilized with ceramic capacitors. Once the supply voltages reach their nominal values, the driver will begin to function after a time delay t_{START}.

Integrated DC/DC Controller

The 2SP0215F2Q0C operates with an integrated DC/DC controller and power stage MOSFETs for each channel. The DC/DC controller provides, through the transformers, the secondary-side isolated supply voltages for the gate driver.

The isolation requirements e.g. clearances and creepage distances of the 2SP0215F2Q0C fulfill safety standards for applications with an IGBT blocking voltage up to V_{CES}.

The 2SP0215F2Q0C monitors the temperature of its internal die that are related to the DC/DC converter output stage on the primary-side for each channel. In addition the currents for each DC/DC converter are monitored and controlled.

Table 2 shows an overview of the different sensor signals and associated response of the DC/DC controllers during the start-up phase and once the system is stabilized after start-up. An "X" indicates that the particular threshold level of the sensor signal has been reached. In column "B_OUT" the bits are listed. These are set to Logic Low when a fault/warning is present.

Die Temperature Threshold $OT1_{DCDC}$	Die Temperature Threshold $OT2_{DCDC}$	Over-Current I_{DCDC1} and/or I_{DCDC2}	B_OUTx	DC/DC Controller Operation During Start-up Phase	DC/DC Controller Operation During Stabilized Phase
–	–	–	–	Normal Operation	Normal Operation
X	–	–	B_OUT[23]	Normal Operation	Normal Operation
–	X	–	B_OUT[23] B_OUT[24]	Turned-Off	Turned-Off
–	–	X	B_OUT[25]	Turned-Off	Normal Operation
X	–	X	B_OUT[23] B_OUT[25]	Turned-Off	Normal Operation
–	X	X	B_OUT[23] B_OUT[24] B_OUT[25]	Turned-Off	Turned-Off

Table 2. DC/DC Controller States at Different Conditions for Each Channel.

Integrated Gate Voltage Stabilization
During switching events, the gate voltage is affected by the Miller capacitance of the driven power semiconductor. During short-circuit conditions this effect increases the gate voltage, thereby, increasing the short-circuit current and related energy. To keep the gate voltage stable, an integrated regulator monitors the supply voltage between positive gate voltage and negative gate voltage and generates a stabilized voltage between positive gate voltage and emitter potential. This voltage is set to a default value of 15 V.

SOx and B_OUTx
The gate driver uses two logic output pins SOx and B_OUTx per channel for failure and status monitoring. SO is a fast responding 1-bit output pin using an open drain topology. Pull-up resistors of 1.5 kΩ to VCC are present on these pins.

B_OUT is a digital bit stream output (Figure 4). Multiple different status conditions can be determined by using SOx and B_OUTx together. Details are shown in Table 3.

Note:The definition of Logic Low or High condition of B_OUTx bits is described in Figure 4.

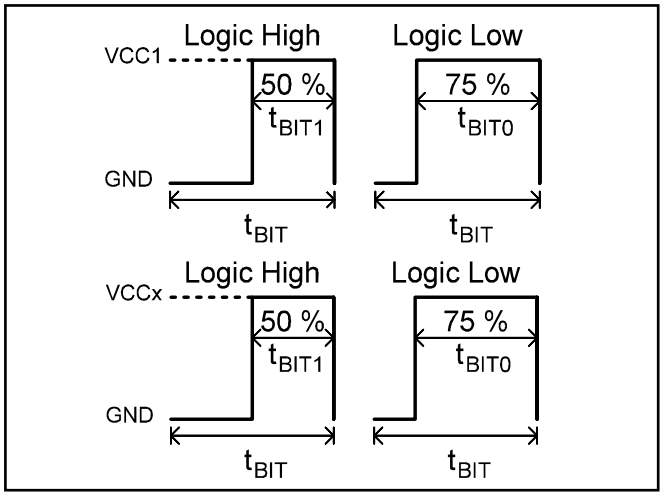

Figure 4. Definition of Logic Low and Logic High Levels at B_OUTx.

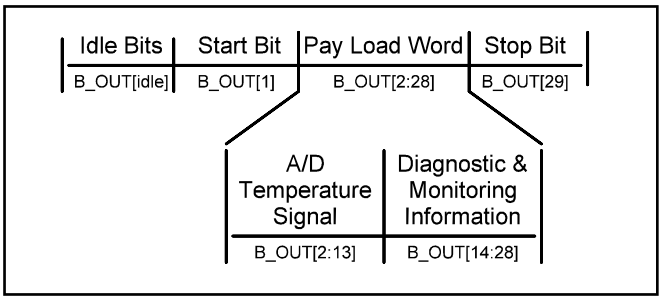

Figure 5. B_OUT Bit Assignment.

The information of the digital bit stream of B_OUTx consists of a Start Bit Logic High, 27 Pay load bits and 1 Stop Bit. Prior to the Start Bit, a series of Logic Low bits (B_OUTx[idle]) are sent. The number of bits is not fixed. It is defined by the asynchronous frame time t_{B_OUT} minus the time required for the transmission of the Start Bit, Pay load bits and the Stop Bit.

Collector Connection Top Channel and Bottom Channel
To determine the status of the power semiconductor, the voltage of the collector pin is monitored.

The collector pin connection supports two different functions:
- VCE short-circuit monitoring
- Overvoltage limiting during turn off (AROC)

VCE Short-Circuit Protection
When the gate driver is in a turn-on transition or in the on-state, the short-circuit detection algorithm is activated after a gate driver internally response time tSENSE(BL) has elapsed. A drop of VSENSE ≥ 0.41 V (typ.) between the collector and VEE is interpreted as a short-circuit.

A short-circuit failure turns-off the appropriate 2SP0215F2Q0 gate driver channel. SOx is set to GND potential and B_OUTx[20] set to logic low to signal this condition.

Overvoltage Limitation (AROC)
If the driver is in a turn-off transition or in off-state, the overvoltage limit algorithm is activated, the driver will regulate the gate current to limit the IGBT turn-off di/dt and therefore the voltage on the collector with respect to emitter during turn-off.

Short-Pulse Operation

If command signals applied to IN1 and IN2 are shorter than the minimum specified by $t_{GE(MIN)}$, then 2SP0215F2Q0 gate output signals will be extended to $t_{GE(MIN)}$. The duration of pulses that are longer than $t_{GE(MIN)}$ will not be changed.

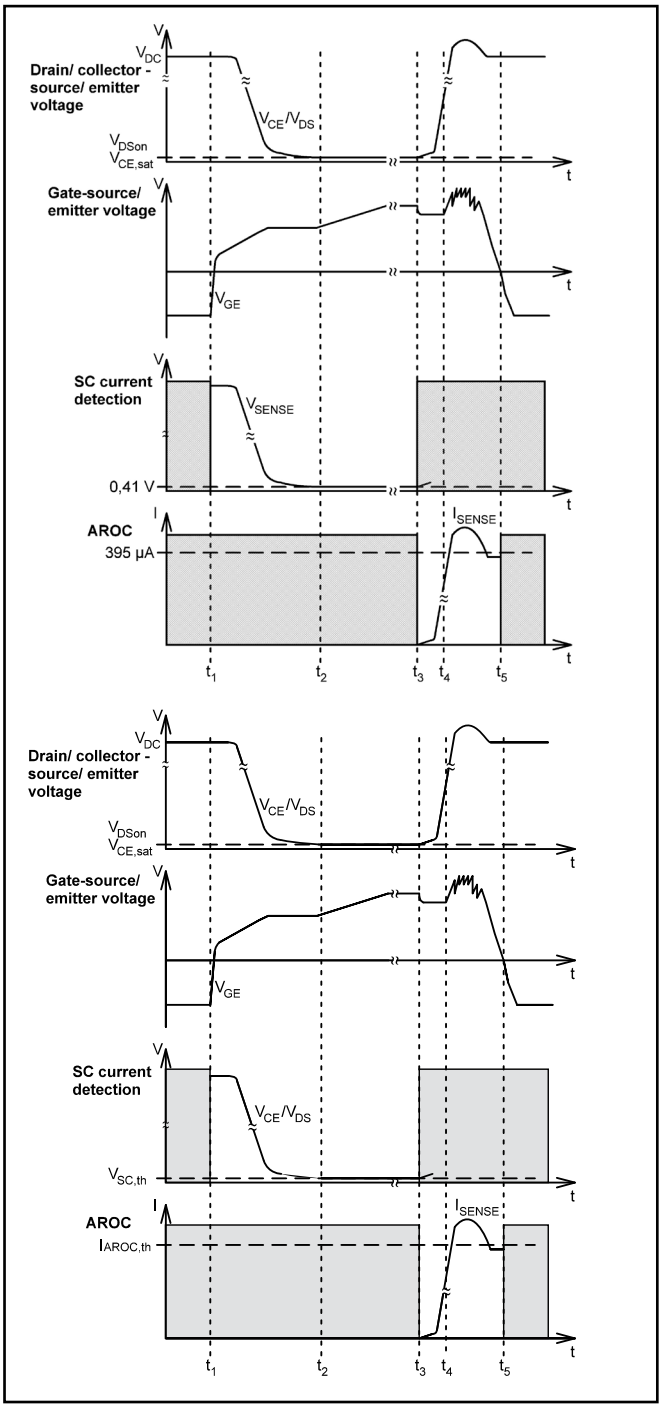

Figure 6. Short-Circuit Monitoring and AROC Timing.

Integrated Active Miller Clamp

The integrated Active Miller clamp is necessary to protect power semiconductors with a low gate-emitter threshold voltage. To avoid parasitic turn-on in half-bridge topologies during switching events, the Active Miller Clamp provides a low impedance connection between the gate of the power semiconductor and the negative supply voltage. A potential that would be induced on the gate due to the switching dv/dt acting with the Miller capacitance is prevented by the low impedance to the negative gate voltage. This prevents the low high-frequency impedance of the Miller capacitance from charging the gate capacitance of the power semiconductor and driving the gate potential above the threshold voltage.

NTC Temperature B_OUT

Besides the gate driver functionality, the 2SP0215F2Q0C provides a galvanically isolated return channel. The return channel provides the value of the low-side power semiconductor module integrated NTC resistor.

The temperature sensor is connected to the 2SP0215F2Q0C. The analog temperature information is applied to an ADC (Analog Digital Converter) before the signal is transferred to B_OUT1 on the primary-side (low-voltage side) via the FluxLink communication path. The thermistor is therefore galvanically isolated from the low-voltage of the primary-side.

At B_OUT1 the temperature induced resistance of the thermistor can be inferred. Equation 1 describes the translation with B_OUT1[2] being the MSB and B_OUT1[13] the LSB.

$$R_{TEMP} = 32 \times \frac{V_{TEMP}}{I_{TEMP} \times B\_OUT1[2:13]} \quad \text{Eq. 1}$$

Example:
B_OUT1[2:13] = 0110111000102 = 176210
VTEMP = 0.3 V (typ.)
ITEMP = 20 µA (typ.)

$$R_{TEMP} = 32 \times \frac{0.3\ V}{20\ \mu A \times 1762} = 272\ \Omega$$

This allows the actual temperature of the thermistor, to be inferred from information provided by the device data sheet. The board NTC value is provided in the high-side data stream.

SO	B_OUTx[x]	Fault/Warning
GND	VCCx	VVCCx Undervoltage Fault
VCCx	[14] = Low	Gate Undervoltage Warning
VCCx	[15] = Low	Gate Overvoltage Warning
VCCx	[16] = Low	Gate Monitoring Warning
VCCx	[17] = Low	Over-Temperature Warning $OT2_{GD}$
VCCx	[18] = Low	Over-Temperature Warning $OT1_{GD}$
VCCx	[19] = Low	Secondary-Side FluxLink-out-of-Service Warning (10 µs communication fault duration)
GND	[19] = Low	Secondary-Side FluxLink-out-of-Service Warning (≥ 20 µs communication fault duration)
GND	[20] = Low	DESAT Detection Fault
VCCx	[21] = Low or High	Parity Bit, set in a way that the amount of logic high bits from secondary-side to primary-side is even
VCCx	[22] = Low	Primary-Side FluxLink-out-of-Service Warning (10 µs communication fault duration)
GND	[22] = Low	Primary-Side FluxLink-out-of-Service Warning (≥ 20 µs communication fault duration)
VCCx	[23] = Low	Over-Temperature Warning $OT1_{DCDC}$
VCCx	[24] = Low	Over-Temperature Warning $OT2_{DCDC}$
GND	[25] = Low	Over-Temperature Warning $OT1_{DCDC}$
VCCx	[25] = Low	Over-Temperature Warning $OT2_{DCDC}$
VCCx	[27] = High	Dead-Time Insertion Warning
VCCx	[28] = High	Interlock Warning

Table 3. Combined Fault and Status Feedback of SO and B_OUT.

Under and Overvoltage Monitoring and Warning
The supply voltages are closely monitored. In case of an under (UVLO) or overvoltage condition (OVLO) a failure signal or a warning signal is generated by the 2SP0215F2Q0C. The gate driver distinguishes between VCC and the two channels.

- Low-voltage side VCC undervoltage = Failure, related gate driver channel turns-off. SOx set to GND.
- Gate undervoltage warning = Related channel warning only at B_OUTx[14] (Logic Low).
- Gate overvoltage warning = Related channel warning only at B_OUTx[15] (Logic Low).

Gate Monitoring Failure Diagnostic
The 2SP0215F2Q0C monitors the gate output on the secondary-side of each driver channel, comparing the expected level with the commanded input via IN1 / IN2 on the primary-side.

If 5 V is applied at INx, the gate output will turn-on the gate of the power semiconductor. The output voltage of the gate is measured across the series connected gate resistors $R_{G(ON)}$ and $R_{G(OFF)}$ after the time $t_{GM(ON)}$ has elapsed. The voltage level must be larger than the internal measurement value $V_{GM(ON)}$. If not, a gate monitoring warning will be generated and signaled as a Logic Low signal at B_OUTx[16].

Similarly, if 0 V is applied at IN1 or IN2, the gate output will turn-off the gate of the power semiconductor. The output voltage of the gate is measured after the internal time $t_{GM(OFF)}$ has elapsed. The voltage level must be smaller than the internal reference voltage $V_{GM(OFF)}$, or a gate monitoring warning will be generated and signaled as a Logic Low signal at B_OUTx[16].

The gate monitoring function is able to detect:
1. An open or high impedance gate resistor.
2. Gate driver communication failure.
3. Gate-emitter shorts of the driven power semiconductor.

Note: The digital bit stream might have a lower frequency (typ. 1 kHz) than the applied command signals at IN1 or IN2. Nevertheless, all switching events will be monitored and any faulty signal reported with a delay of up to $f_S \times f_{SW}$. A fault condition is latched and reported at the next bit stream transmission).

Gate Driver Output Stage Over-Temperature Sensing
The gate driver 2SP0215F2Q0C monitors the internal temperature for each channel on the primary-side (low-voltage side) and secondary-side (high-voltage side). On the primary-side the temperature described is that of the DC/DC converter output and on the secondary-side the temperature of the gate driver output stage is monitored.

If the temperature on the secondary-side reaches the $OT1_{GD}$ threshold level a warning is issued (B_OUTx[18] is set to Logic Low). If the temperature further increases to $OT2_{GD}$, a second warning is issued by setting B_OUTx[17] to Logic Low.

Note:The gate driver will not stop its operation. Therefore, to prevent any thermal damage to the gate driver, the external microcontroller should initiate proper action to keep gate driver operating conditions within recommended levels.

FluxLink Communication Monitoring Failure Diagnostic
The 2SP02015F2Q0C constantly monitors the status of the internal communication channel (FluxLink) between the primary-side and secondary-side for both the top channel and the bottom channel.

If the communication from the primary-side to the secondary-side is compromised for 10 µs (typical), the gate driver sets B_OUTx[22] to logic low. If the interruption remains for longer than 20 µs (typical), then the output SOx will be set to GND and the gate driver will turn-off the gate driver output stage of the related channel.

B_OUTx[21] contains a parity bit. The parity bit is set to create an even number of logic high bits in the communication from the secondary-side to the primary-side.

Note: If a communication failure occurs in one the two gate driver channels only the effected channel turns off.

Motor Active Short-Circuit Mode (ASC)

To get energy out of a turning electric motor and to avoid overvoltages in the system generated by the BEMF of the electric motor the 2SP0215F2Q0C provides an Active Short Circuit (ASC) mode. This mode allows the system to keep the gate driver output stage in a defined state either permanently turned-on or permanently turned-off, regardless of any applied signal at the inputs IN1 and IN2. This feature makes it possible to short the phases of the electrical machine together and de-energize it by creating a negative torque. The 2SP0215F2Q0C supports top side (Channel 2) or bottom side (Channel 1) ASC, and is activated from the primary-side of the gate driver by the microcontroller.

The ASC mode is activated by applying 5 V to pin ASC_AD_ENx. The status of the gate driver output is determined by the signal applied at pin ASC_ADx. The gate output is turned-on as long as 5 V is applied. Similarly, the output if turned-off as long as 0 V is applied.

ASC_AD_ENx	ASC_ADx	Mode
0 V	0 V	Normal Mode
5 V	0 V	ASC Mode Gate Output turned-off
5 V	5 V	ASC Mode Gate Output turned-on

Table 4. Active Short-Circuit Mode.

DC-Link Active Discharge Mode (AD)

To avoid the need for additional components to discharge the DC-link, the 2SP0215F2Q0C provides an Active Discharge (AD) mode. The role of the AD mode is to discharge the DC-link voltage through the power semiconductors of one or more half-bridges. The power modules are operated for a short period of time in a "quasi half-bridge short-circuit" condition. To limit the stress for the power semiconductors, the gate voltage is automatically reduced by the gate driver to limit the effective short-circuit current. This is possible as the short-circuit current is a direct function of the applied gate voltage.

The AD mode is initiated by applying 5 V at pin ASC_AD_ENx while keeping ASC_AD_ENx at 0 V.

ASC_AD_ENx	ASC_ADx	Mode
0 V	0 V	Normal Mode
0 V	5 V	AD Mode

Table 5. Active Discharge Scheme.

To discharge a DC-link the scheme of Figure 8 should be followed. In Figure 7 an example implementation of the Active Discharge function is shown. In this example, the scheme position (Figure 8) is #6, i.e. the microcontroller has initiated the active process of discharging the DC-link. It is not necessary (but possible) to operate both gate driver channels in one half-bridge in AD mode. To reduce complexity, it is sufficient to keep one power semiconductor channel in the on-state, while operating the opposite channel in AD mode. In the example, the top switch is kept turned-on, while the bottom switch is controlled by a switching signal from the external microcontroller.

Note 1: During the AD mode, the driven power semiconductors may trigger desaturation detection in the gate driver, which leads to a turn-off of the gate driver output stage. This event can be ignored, as the applied external command pulses will turn-on the power semiconductor for the next cycle. Also, the gate driver will not report such desaturation events during the AD mode to the controller, i.e. the fault is masked at SOx.

In the event that the implementation shown in Figure 7 is used and the top switch turns-off due to an desaturation monitoring event, it is necessary to apply AD scheme (IN2 of the top and IN1 of bottom switch are operated in parallel) to both top and bottom channels.

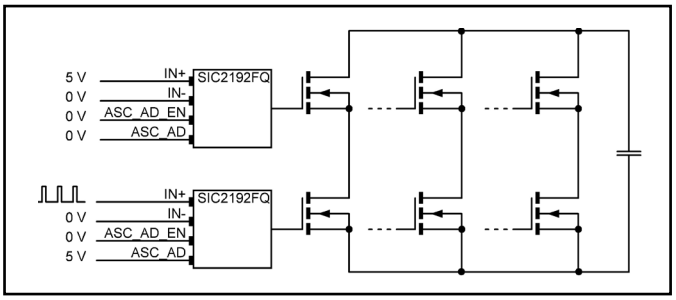

Figure 7. Active Discharge Implementation.

Note: It is possible to apply the AD mode to more than one half-bridge 2SP0215F2Q0C gate driver. This may be beneficial when the power semiconductors are comparatively small and the DC-link capacitance is high. Using more than one half-bridge will spread the dissipation across more devices.

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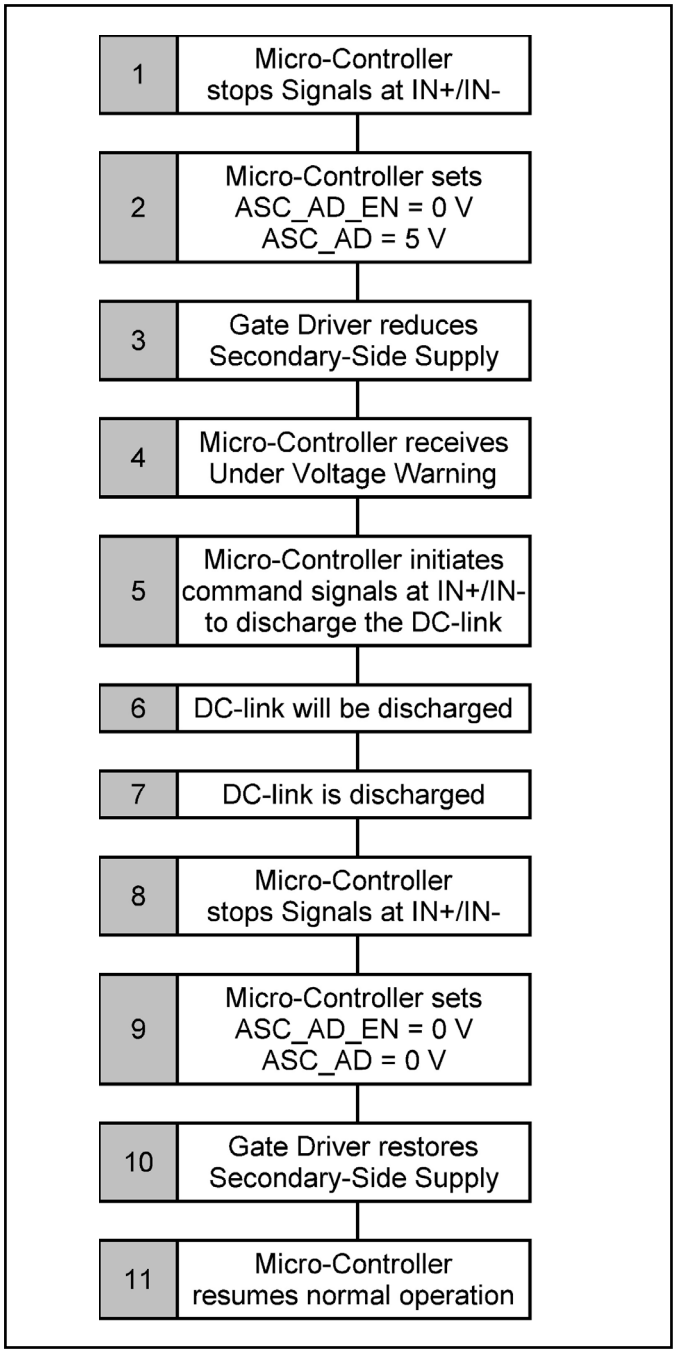


Figure 8. Active Discharge Scheme.

Conformal Coating

The electronic components of the gate driver are protected by a layer of an acrylic conformal coating with a typical thickness of 50 µm. The material is ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on the top side of the PCB. This coating increases product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer should be avoided as this water will diffuse through the layer over time. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause a rise in potentially harmful leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

Functional Safety

The 2SP0215F2Q0C is designed according to the ISO 26262 safety lifecycle at the ASIL-B level.

The 2SP0215F2Q0C is a half-bridge architecture using two Power Integrations' gate driver ASICs. One driving the top side switch and the other driving the bottom side switch. The 2SP0215F2Q0C Plug&Play gate driver receives commands from a microcontroller.

2SP0215F2Q0C is designed with various warning and fault monitoring functions:

- Warnings are defined such that the 2SP0215F2Q0C will report an event to the system (through the bit stream output B_OUTx), but will not activate the SOx failure output.
- Faults are defined such that the 2SP0215F2Q0C will report an event to the system (with the SOx output and the bit stream output) and switch to the safe state (defined as the Off-state).

The warnings and faults can be further be sub-divided into self-diagnostics and support-to-system diagnostics. The system diagnostics are designed to enhance the system's diagnostic features and support the system designer in his mission to reach the required level of functional safety.

Primary-Side Self-Monitoring Diagnostic Warnings

Warning	Description
Primary-side FluxLink-out-of-service fault	Triggered on a time-out if no valid message is detected for 10 µs.
DC/DC over-temperature level 1	Activated if temperature of DC/DC converter rises over $OT1_{DCDC}$.
DC/DC over-temperature level 2	Activated if temperature of DC/DC converter rises over $OT2_{DCDC}$. The DC/DC converter also turns off as long as the condition persists.

Table 6. Primary-Side Self-Monitoring Diagnostic Warnings.

Primary-Side Self-Monitoring Fault Diagnostic

Fault	Description
Primary-side FluxLink-out-of-service fault per channel 1 and 2	Triggered on a time-out if no valid message is detected after 20 µs. Sends SOx command and a turn-off command to the secondary-side gate driver output stage.
Undervoltage per channel 1 and 2	The SOx output is activated and a turn-off command is sent to the secondary-side (high-voltage side) of 2SP0215F2Q0C. For as long as the condition persists B_OUTx is disabled and the 2SP0215F2Q0C does not accept any further commands.

Table 7. Primary-Side Self-Monitoring Fault Diagnostic.

Primary-Side Support to System Safety Diagnostic Warnings

Warning	Description
DC/DC over current per channel 1 and 2	Detects that DC/DC converter circuit external to the 2SP0215F2Q0C is sinking too much current. Activated if current load of DC/DC converter rises over internal threshold $I_{DCDC1,th}$ and/or $I_{DCDC2,th}$.
Violation of IN1/IN2 interlock	Detects the condition that both IN1 and IN2 are high at the same time.
Violation of IN1/IN2 dead-time	Detects if the dead-time between switching either channel is below a minimum threshold.

Table 8. Primary-Side Support to System Safety Diagnostic Warnings.

Secondary-Side Self-Monitoring Diagnostic Warnings

Warning	Description
Secondary FluxLink-out-of-service fault per channel 1 and 2	Triggered on a timeout if no valid message is detected for 10 µs.
Gate monitoring per channel 1 and 2	Reads back Gate status and compares to command received on secondary-side. If the value is not correct then it latches a warning which will be sent to the primary. Although the warning update is f_{SW} times slower than the 2SP0215F2Q0C switching frequency f_{SW}, any error is latched and transmitted on the next frame.
Gate driver output stage temperature level 1 per channel 1 and 2	Activated if temperature of gate driver output stage rises over $OT1_{GD}$.
Gate driver output stage temperature level 2 per channel 1 and 2	Activated if temperature of gate driver output stage rises over $OT2_{GD}$.
CRC parity bit per channel 1 and 2	An even parity bit is added to digital bit stream from secondary- to primary-side. It is added to B_OUTx.

Table 9. Secondary-Side Self-Monitoring Diagnostic Warnings.

Secondary-Side Self-Monitoring Fault Diagnostic

Fault	Description
Secondary-side Flux -Link out of service fault per channel 1 and 2	Triggered on a timeout if no valid message is detected after 20 µs. Sends SO command to primary-side and a turn-off command to gate driver output stage.

Table 10. Secondary-Side Self-Monitoring Fault Diagnostic.

Secondary-Side Support to System Safety Diagnostic Warnings

Warning	Description
Undervoltage warning per channel 1 and 2	Activated if secondary-side supply voltage goes below internal threshold UVW_{VISO}.
Overvoltage per channel 1 and 2	Activated if secondary-side supply voltage goes above internal threshold OVW_{VISO}.

Table 11. Secondary-Side Support to System Safety Diagnostic Warnings.

Secondary-Side Support to System Fault Diagnostic

Fault	Description
Desaturation short circuit monitoring per channel 1 and 2	Detects if the driven power module goes into desaturation during turn-on. This is a half-bridge relevant diagnostic and detects if the power switch of the other half of the bridge is turned on or in short-circuit.

Table 12. Secondary-Side Support to System Fault Diagnostic.

Maximum Ratings

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Units
Absolute Maximum Ratings[1]					
Primary-Side Supply Voltage	V_{CCx}	VCC applied to GND	-0.5	6	V
Primary-Side SupplyCurrent	I_{VCCx}	Average supply current at full load		340	mA
Logic Input Voltage (Command Signal)[2]	V_{INx}	INx to GND	-0.5	V_{VCC} + 0.5	V
Logic Input Voltage ASC_AD_ENx and ACS_ADx	V_{ASCx}	ASC_ADx /ASC_AD_ENx to GND	-0.5	V_{VCC} + 0.5	V
Logic Output Voltage SOx (Status Signal)	V_{SOx}	SOx to GND	-0.5	V_{VCC} + 0.5	V
Logic Output Current SOx (Status Signal)	I_{SOx}	V_{VCCx} = 4.75 V, R_{SOx} = 1.5 kΩ V_{VCCx} = 5.25 V, R_{SOx} = 1.5 kΩ	3.2	3.5	mA
Logic Output Current B_OUTx (Bitstream Signal)	V_{B_OUTx}	B_OUTx to GND	-0.5	V_{VCC} + 0.5	V
Logic output Current B_OUTx (Bitstream Signal)	I_{B_OUTx}	V_{VCCx} = 4.75 V, R_{B_OUTx} = 1.5 kΩ V_{VCCx} = 5.25 V, R_{B_OUTx} = 1.5 kΩ	3.2	3.5	mA
Gate Output Power Per Channel	P_{gx}	T_A = 85 °C		1.5	W
Switching Frequency	f_{SW}	T_A = 85 °C		20	kHz
Test Voltage Primary-Side to secondary-side	$V_{IMP(PS)}$			4000	V_{PK}
Test Voltage Secondary-Side to Secondary-Side	$V_{IMP(SS)}$			2500	V_{PK}
Operating Voltage Primary-Side to Secondary-Side	V_{OP}	Transient only		1200	V_{PK}
Operating Voltage Primary-Side to Secondary-Side DC-link voltage	$V_{DC\text{-}Link}$	Permanently applied		1000	VDC
		Switching operation		950	VDC
Common-Mode Transient Immunity	|dv/dt|			50	kV/µs
Storage Temperature[3]	T_{st}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Surface Temperature[4]	T			125	°C
Relative Humidity	H_R	No condensation		85	%
Altitude of Operation[5]	A_{OP}			5500	m

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. INx signals must statically be within the given limits.
3. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85 °C.
4. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
5. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Recommended Operating Conditions

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Recommended Operation Conditions						
Primary-Side Supply Voltage	V_{VCCx}	VCC – GND	4.75	5	5.25	V
Secondary-Side Total Gate Voltage	V_{GATEX}	VISO – VEE		15.0		V
VEE Voltage	V_{VEEx}	VEE - COM		2.5		V
Logic Low Input Voltage (command signals)	$V_{INx(L)}$ $V_{INx(L)}$ $V_{ASC\_AD\_ENx(L)}$ $V_{ASC\_ADx(L)}$	Referenced to GND			0.5	V
Logic High Input Voltage (command signals)	$V_{INx(H)}$ $V_{INx(H)}$ $V_{ASC\_AD\_ENx(H)}$ $V_{ASC\_ADx(H)}$	Referenced to GND	3.3			V
Logic Output Current SOx (fault signal)	I_{SOx}	V_{VCCx} = 5 V, R_{SOx} = 1.5 kΩ		3.3		mA
Logic Output B-OUT Current (bit stream)	I_{B_OUTx}	V_{VCCx} = 5 V, R_{B_OUTx} = 1.5 kΩ		3.3		mA
Switching Frequency	f_{SW}				20	kHz
Operating Ambient Temperature	T_A		-40		85	°C

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics						
Logic Low Input Threshold Voltage (command signals)	$V_{INx(HL)}$	V_{VCCx} = 5 V, T_A = 25 °C, f_{SW} = 20 kHz	0.8	1	1.3	V
	$V_{INx(HL)}$					
	$V_{ASC\_AD\_ENx(HL)}$	V_{VCCx} = 5 V, T_A = 25 °C	0.8	1	1.3	V
	$V_{ASC\_ADx(HL)}$					
Logic High Input Threshold Voltage (command signals)	$V_{INx+(LH)}$	V_{VCCx} = 5 V, T_A = 25 °C, f_{SW} = 20 kHz	2.3	2.7	3.1	V
	$V_{INx-(LH)}$					
	$V_{ASC\_AD\_ENx(LH)}$	V_{VCCx} = 5 V, T_A = 25 °C	2.3	2.7	3.1	V
	$V_{ASC\_ADx(LH)}$					
Input Bias Current	I_{INx}	V_{VCCx} = 5 V, R_{INx+} = 0.75 kΩ		6.6		mA
	$I_{ASC\_AD\_ENx}$	V_{VCCx} = 5 V, $R_{ASC\_AD\_ENx}$ = 1.5 kΩ		3.3		
	I_{ASC_ADx}	V_{VCCx} = 5 V, R_{ASC_ADx} = 1.5 kΩ		3.3		
Supply Current (Primary-Side)	I_{VCCx}	V_{VCCx} = 5 V, V_{INx} = 0 V, V_{IN-} = 0 V		60		mA
		V_{VCCx} = 5 V, V_{INx} = 0/5 V, V_{INx} = 5/0 V, f_{SW} = 10 kHz		340		
Supply Current (Secondary-Side)	I_{VISOx}	V_{TOTx} = 25 V, V_{INx}+ = 0 V, V_{INx-} = 0 V	6.67	6.70	6.98	mA
		V_{TOTx} = 25 V, V_{INx+} = 0/5 V, V_{INx-} = 5/0 V, f_{SW} = 20 kHz	7.81	8.26	8.94	
Undervoltage Power Supply Monitoring Threshold (Primary-Side)	$UVLO_{VCCx}$	Resume Operation	4.30	4.35	4.45	V
		Suspend Operation	3.85	4.12	4.20	
Undervoltage Power Supply Monitoring Blanking Time (Primary-Side)	$UVLO_{VCCx(BL)}$		4.30	4.35	4.45	ns
Undervoltage Power Supply Monitoring Threshold (Secondary-Side)	UVW_{VISOx}	Clear Warning	12.3	12.85	13.5	V
		Set Warning	11.6	12.3	13	
		Hysteresis	0.35			
Undervoltage Power Supply Monitoring Blanking Time (Secondary-Side)	$UVW_{VISOx(BL)}$			TBD		ns

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
Overvoltage Power Supply Monitoring Threshold (Secondary-Side)	OVW_{VISOx}	Clear Warning	17.3	18.5	19.8	V
		Set Warning	18	19.1	20.4	
		Hysteresis	0.3	0.6	0.84	
VEE Source (Emitter) Capability	$I_{VEEx(SO)}$	V_{TOTx} = 25 V, V_{VEEx} = 7.5 V	335	855	1470	µA
VEE Sink Capability	$I_{VEEx(SI)}$	V_{TOTx} = 25 V, V_{VEEx} = 10 V	300	730	1240	µA
Power-On Start-Up Time	t_{START}				10	ms
Minimum Turn-On and -Off Pulses	$t_{GE(MIN)}$		10		1000	ns
Turn-On Propagation Delay	$t_{P(LH)}$	V_{VCCx} = 5 V, V_{TOTx} = 25 V, T_J = 25 °C, 50% V_{INx} to 10% V_{GH}, C_{GXX-GH} = 10 nF, No-Load at GH and GL		270		ns
		$V_{VCC}x$ = 5 V, V_{TOTx} = 25 V, T_J = 125 °C, 50% V_{INx} to 10% V_{GH}, C_{GXX-GH} = 10 nF, No-Load at GH and GL		tbd		
Turn-Off Propagation Delay	$t_{P(HL)}$	V_{VCCx} = 5 V, V_{TOT} = 25 V, T_J = 25 °C, 50% V_{INx} to 10% V_{GH}, C_{GXX-GH} = 10 nF, No-Load at GH and GL		317		ns
		V_{VCCx} = 5 V, V_{TOTx} = 25 V, T_J = 125 °C, 50% V_{INx} to 10% V_{GH}, C_{GXX-GH} = 10 nF, No-Load at GH and GL		tbd		
Gate Monitoring Turn-On Threshold	$V_{GM(ON)}$	$V_{GM(ON)} = V_{VISO} - V_{GL}$, V_{IN1} = 5 V, V_{IN2} = 0 V	2.8	3.1	3.4	V
Gate Monitoring Turn-Off Threshold	$V_{GM(OFF)}$	$V_{GM(OFF)} = V_{GH} - V_{COM}$, V_{IN1} = 0 V, V_{IN2} = 0 V	2.3	2.7	3.4	V
Gate Monitoring Turn-On Delay	$t_{GM(ON)}$	V_{TOT} = 25 V, V_{IN1} = 0 V to 5 V 9 (step), V_{IN1} = 0 V, No-Load attach to GH and GL	4.8	5.5	6.2	µs
Gate Monitoring Turn-Off Delay	$t_{GM(OFF)}$	V_{TOT} = 25 V, V_{IN1} = 5 V to 0 V (step), V_{IN2} = 0 V, No-Load attach to GH and GL	4.8	5.5	6.2	µs
Gate Driver Output Stage Over-Temperature	$OT1_{GD}$	Setting Bit B_OUTx[18]	135	150	165	°C
	$OT2_{GD}$	Setting Bit B_OUTx[17]	160	175	190	
Half-Bridge Dead-Time	t_{DT}		465	660	870	ns

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
DC/DC Controller Over Current Threshold	$I_{DCDC1(TH)}$	Setting Bit B_OUTx[25]	0.75	1	1.3	A
	$I_{DCDC2(TH)}$	Setting Bit B_OUTx[25]	0.75	1	1.3	
DC/DC Controller Over-Temperature	$OT1_{DCDC}$	Setting Bit B_OUTx[23]	135	150	165	°C
	$OT2_{DCDC}$	Setting Bit B_OUTx[24], Shutdown of DC/DC Controller Operation	160	175	190	
Internal TEMP Reference Voltage	V_{TEMP}	Referenced to COM	0.29	0.3	0.33	V
Internal TEMP Reference Current	I_{TEMP}		18.5	20	21	µA
TEMP Sampling Time			4.75	4.81	5.1	ms
SOx Output Voltage Logic Low	$V_{SO(0)}$	V_{VCCx} ≥ 3.9 V, I_{SOx} = 3.4 mA, Referenced to GND	80	144	278	mV
SOx Fault Signalization Duration Time	t_{SO}	Duration of SO signal at low level during fault event, (50% falling edge to 50% rising edge)	6.8	10	13.4	µs
SO Fault Signalization Delay Time	$t_{SO(dl)}$		145	195	85	ns

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
EB_OUTx Characteristics Channel 1 and 2							
Bit Length	t_{BIT}			2.25	2.35	2.49	µs
Bit Pulse Width	t_{BIT0}	Percentage of B_OUTx bit length t_{BITn}		72.40	73.19	74.00	%
	t_{BIT1}			46.40	47.44	47.60	
Bit Frame Transmission Rate	$t_{B(OUT)}$			588	615	631	ms
Internal TEMP Reference Current	$B_{OUTx[idle]}$	Always Logic Low, Note 1		28			Bit
	$B_{\_OUTx[1:29}$	B_OUTx[2:13]	Start Bit, Logic High		1		
		B_OUTx[2:13]	Digitized TEMP Signal, B_OUTx[2] = MSB, B_OUTx[13] = LSB		12		
		B_OUTx[14]	V_{VISO} Undervoltage Warning, Active Low		1		
		B_OUTx[15]	V_{VISO} Overvoltage Warning, Active Low		1		
		B_OUTx[16]	Gate Monitoring Warning, Active Low		1		
		B_OUTx[17]	Over-Temperature Warning $OT2_{GD}$, Active Low		1		
		B_OUTx[18]	Over-Temperature Warning $OT1_{GD}$, Active Low		1		
		B_OUTx[19]	Secondary-Side FluxLink-out-of-Service Warning, Active Low		1		
		B_OUTx[20]	DESAT Detection Fault, Active Low, Note 2		1		
		B_OUTx[21]	Parity Bit of Secondary- to Primary-Side Communication		1		
		B_OUTx[22]	Primary-Side FluxLink-out-of-Service Warning, Active Low		1		
		B_OUTx[23]	Over Temperature Warning OT1DCDC, Active Low		1		
		B_OUTx[24]	Over Temperature Warning $OT2_{DCDC}$, Active Low		1		
		B_OUTx[25]	Primary-Side DC/DC Controller Over Current Warning, Active Low		1		
		B_OUTx[26]	Not used, always Logic Low		1		
		B_OUTx[27]	Dead-Time Insertion Warning, Active High		1		
		B_OUTx[28]	Interlock Warning, Active High		1		
		B_OUTx[29]	Stop Bit, Logic High		1		
B_OUTx Output Voltage Logic Low	$V_{B(OUT)(0)}$	V_{CCx} ≥ 3.9 V, I_{B_OUTx} = 1 mA, Referenced to GND1		23	41	80	mV

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Package Insulation Characteristics						
Distance Through the Insulation	DTI	Primary- to Secondary-Side (ASIC)	0.4			mm
Creepage Distance	CPG_{P-S}	Primary-side to secondary-side	11			mm
	CPG_{S-S}	Secondary-side to secondary-side	4.6			
Clearance Distance	CLR_{P-S}	Primary-side to secondary-side	4.9			mm
	CLR_{S-S}	Secondary-side to secondary-side	3.0			mm
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, 25 °C ≤ T_J ≤ $T_{A(MAX)}$	100			MΩ
	$R_{IO(S)}$	V_{IO} = 500 V at T_S[3] = 125 °C	100			
Isolation Capacitance, Input to Output	C_{IO}	V_{CIO} = 2 V, f_{CIO} = 1 MHz, T_A = 25 °C (Per channel)	10			pF
Maximum Repetitive Peak Isolation Voltage	V_{IORM}				1200	V
Impulse Voltage	$V_{IMP(PS)}$				4	kV_{PK}
Input to Output Partial Discharge Test Voltage	V_{PD}	IEC 60664-3:2016 Section 5.8.5 $V_{IN(A)} = 1.2 \times V_{IOT(M)}$, $V_{PD(M)} = 1.875 \times V_{IORM}$, t = 1 s, Q_{PD} < 5 pC	2.25			kV_{PK}

[3] T_S is the safety temperature of the gate driver PCB above which the insulation resistance between the primary-side and secondary-side starts to deteriorate with a certain factor depending on the temperature change.

NOTES
1. The actual amount depends on the actual frame duration and may vary due to asynchronous transmission.
2. Always send twice in 2 successive B_OUTx frame.

Mounting Instruction and PressFIT

The gate driver is mounted on top of the target power module via a press fit connection or soldering connection to the gate, emitter, collector and NTC terminals.

To maintain the electrical isolation distances, the screw head on the main terminals, including any washer, must not extend outside the available metallic terminal mounting area.

Cables
The cable from gate driver connector X300/X400 to the system level controller is not part of the 2SP0215F2Q0 gate driver and has to be provided by the designer of the system. It is recommended that this be routed to ensure minimum parasitic coupling between the controller to the gate driver. In particular, Parasitic coupling to any potential on the secondary-side of the gate driver (i.e. high-voltage side) and the AC and/or DC bus bar must be avoided. Otherwise, increased common-mode currents may circulate, which may cause interferences with command, measurement and/or status feedback signals. Furthermore, use of twisted-pair cables is recommended.

Connector
The Molex Micro-Fit 3.0 vertical SMD 7 Pin connector on the board comes with 3.0 mm pitch and SMD solder tabs on the sides for better mechanical stability. It has tin coated connector pins and is glow-wire capable. This complies with the international standard IEC 60335-1 5th edition.

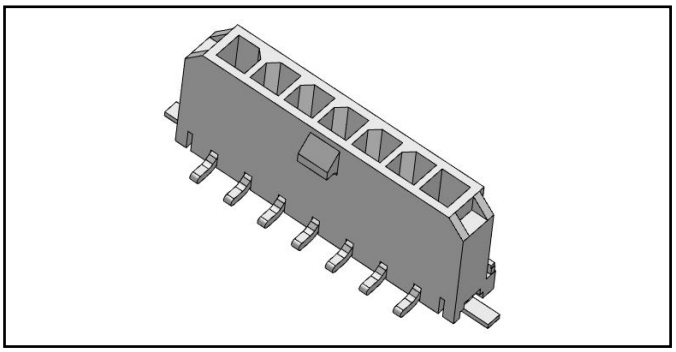


Figure 9. Molex Micro-Fit 3.0 Vertical 7 Pin Connector.

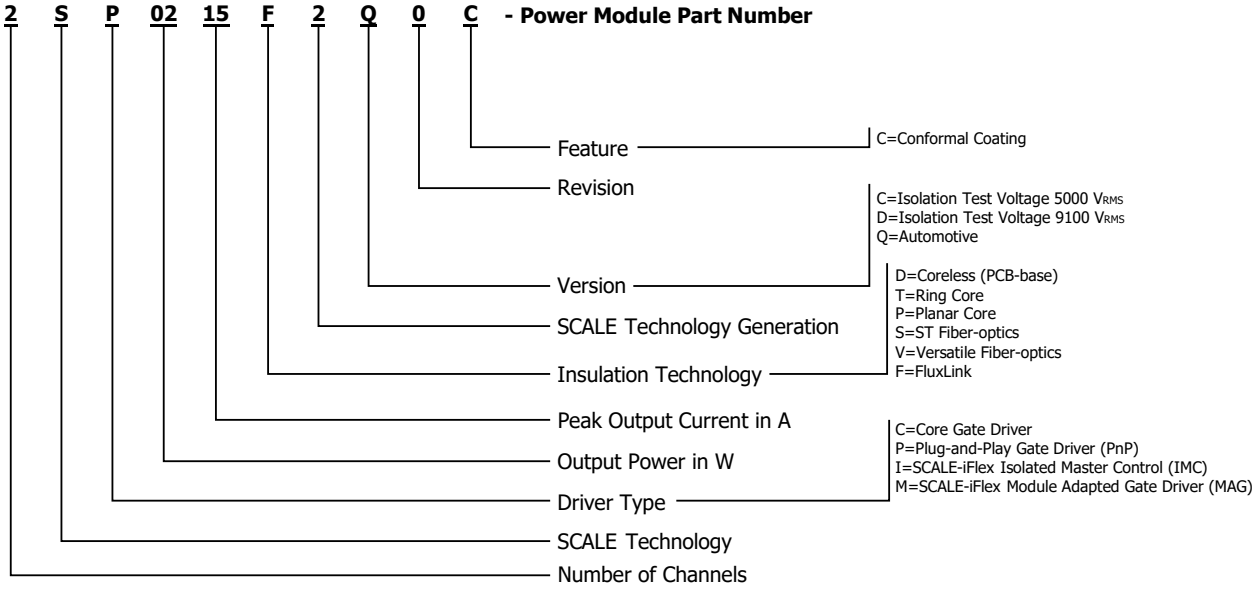
Transportation and Storage Conditions
For transportation and storage, conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement
We hereby confirm that the product supplied does not contain any restricted substances according Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values permitted by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Part Ordering Information Table

Part Ordering Information



Revision	Notes	Date
C	Code B.	05/22

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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