

100V Input, Ultra-Low I_Q , Synchronous Buck Converter

1 DESCRIPTION

The TS16E13 operates over a wide input voltage range from 4.5V to 100V. With integrated the main MOSFET and a synchronous MOSFET, the TS16E13 delivers up to 1A output current. With the 3A current limit, TS16E13 can deliver 3A peak current for some special applications.

The TS16E13 adopts a constant on-time (COT) control architecture to achieve excellent transient response.

With patented standby circuits, the device can achieve ultra-low I_Q , and exit the standby mode fast.

2 APPLICATIONS

- GPS tracker
- Automotive and Industry Systems
- Motor Drives, Telecom

3 FEATURES

- Wide Input Voltage 4.5V-100V
- 3A Current limit
- Low $R_{DS(ON)}$ for Internal MOSFETS 500m Ω /240m Ω
- <200 μ A Supply Current under $I_{LOAD}=100\mu$ A
- TS16E13 Adjustable F_{SW} up to 1MHz
- Internal 3ms Soft-start
- Smart power saving and ultra-Fast Transient Response
- Precision $\pm 1\%$ Feedback Reference
- Open-Drain Power Good Indicator
- OC, OT Protection with Hiccup Mode
- No Loop Compensation Components
- ESOP8 Package with Thermal PAD

4 TYPICAL APPLICATION

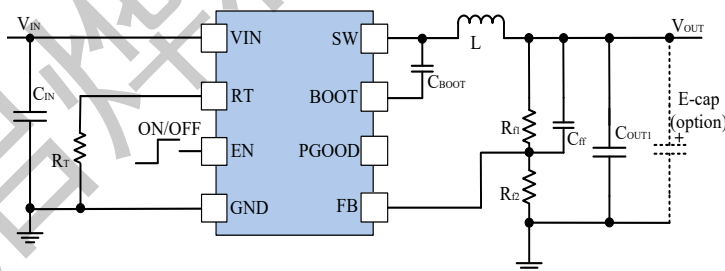


Figure 1. Typical Application Diagram

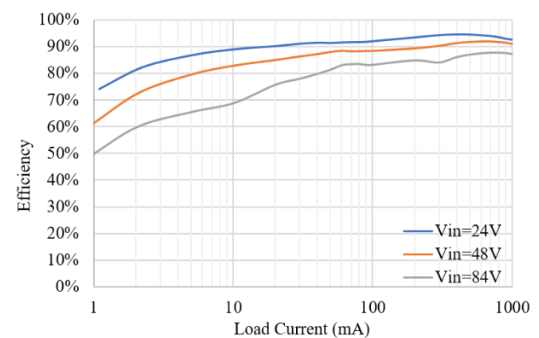
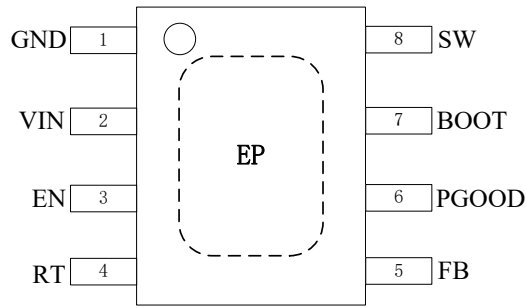


Figure 2. Efficiency at 12Vout

5 PACKAGE REFERENCE AND PIN FUNCTION



ESOP8(top view)

Order No.	Description
TS16E13GAD	ESOP-8, tape, 4k/reel

Pin #	Name	Description
1	GND	Ground pin.
2	VIN	Input pin. Decouple this pin to GND with a low ESR ceramic capacitor.
3	EN	Enable control pin. The device has accurate 1.24V rising threshold and a programable falling threshold. This pin also can be used for programming the VIN turn on voltage with the resistor divider.
4	RT	On-time programming pin. A resistor between this pin and GND sets the buck switch on-time. $F_{SW}(kHz) = \frac{2.56 \times V_{out}(V)}{R_T(M\Omega)}$
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 1.2 \times (1 + R_{f1}/R_{f2})$
6	PGOOD	Power good indicator pin. This pin is an open-drain output pin. Connect to a source voltage through an pull-up resistor.
7	BOOT	Boot-strap pin. Decouple this pin to SW pin with a 10nF ceramic capacitor.
8	SW	Inductor pin. Connect to the switch node of the power inductor.
EP	Thermal PAD	Exposed pad of the package. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

6 ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VIN, EN, SW to GND	-0.3V to 110V
SW to GND (20ns pulse)	-3V to 110V
BS to GND	SW+6.6V
RT to GND	-0.3V to 6.6V
FB to GND	-0.3V to 6.6V
PGOOD to GND	-0.3V to 30V
Power Dissipation, P _D @T _A =25°C, ESOP8	3.3W
Package Thermal Resistance	
θ _{JA} (Junction to ambient)	30°C/W
θ _{JC} (Junction to case)	10°C/W
Operating Junction Temperature, T _J	-40°C to 160°C
Storage Temperature, T _{stg}	-65°C to 160°C
Soldering Temperature(10 second), T _{slid}	260°C

Notes:

- (1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENDED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 RECOMMENDED OPERATING CONDITIONS

VIN Voltage	4.5V to 100V
EN Voltage	-0.3V to 100V
SW Voltage	-0.3V to 100V
Ambient Temperature	-40°C to 85°C

8 ESD RATINGS

		Value	Units
Electrostatic discharge V _{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, SW, BOOT, EN, RT, FB, PGOOD ⁽¹⁾ .	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, SW, BOOT, EN, RT, FB, PGOOD ⁽²⁾ .	±500	V

Notes:

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

9 ELECTRICAL CHARACTERISTICS

$V_{IN}=48V$, $V_{OUT}=5V$, $L=22\mu H$, $C_{OUT}=22\mu F$, $T_A=25^\circ C$, unless otherwise specified

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Input Voltage					
V_{IN}	Input Voltage	4.5		100	V
Supply Current					
$I_{SHUTDOWN}$	Shutdown Current	$V_{EN}=0V$	7.7		μA
$I_{STANDBY}$	Standby Current	$V_{EN}=V_{IN}$, $I_{OUT}=0A$,	155		μA
Feedback					
V_{REF}	Feedback reference voltage		1.2		V
EN/UVLO					
V_{ENH}	EN rising threshold	$V_{IN}=48V$, $I_{OUT}=0.1A$	1.24		V
I_{EN} Hysteresis	Hysteresis Input Current	$V_{IN}=48V$, $I_{OUT}=0.1A$	-2		μA
PGOOD					
V_{PGH}	FB rising threshold for PGOOD low to high	V_{FB} rising	1.187		V
V_{PGL}	FB falling threshold for PGOOD high to low	V_{FB} falling	1.138		V
Frequency					
F_{SW}	Programmable Switching Frequency Range	$F(kHz) = \frac{2.56 \times V_{OUT}(V)}{R_T(M\Omega)}$	100	1000	kHz
Timing					
t_{ON-MIN}	Minimum on-time		50		ns
$t_{OFF-MIN}$	Minimum off-time		270		ns
Power Switches					
$R_{DS(on)-HS}$	High-side MOSFET $R_{DS(on)}$		0.5		Ω
$R_{DS(on)-LS}$	Low-side MOSFET $R_{DS(on)}$		0.24		Ω
Current Limit					
$I_{PEAK-HS}$	High-side MOSFET Peak Current limit		4		A
$I_{VALLEY-LS}$	Low-side MOSFET Valley Current limit		2		A
Soft Start					
t_{SS}	Soft-start time		3		ms
Thermal Shutdown					
T_{SD}	Thermal Shutdown Threshold	T_J rising	160		$^\circ C$
T_{HYS}	Thermal Shutdown Hysteresis		25		$^\circ C$

10 BLOCK DIAGRAM

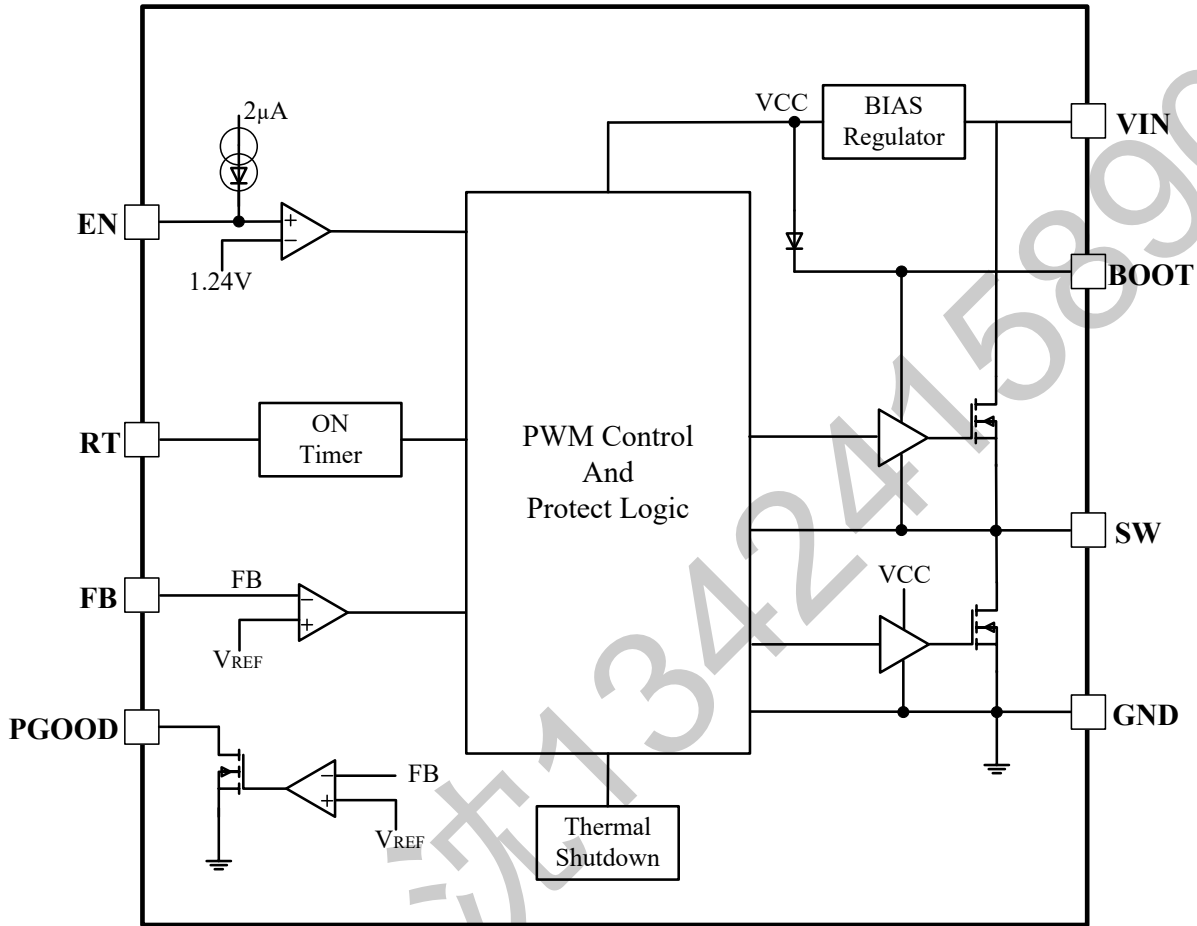
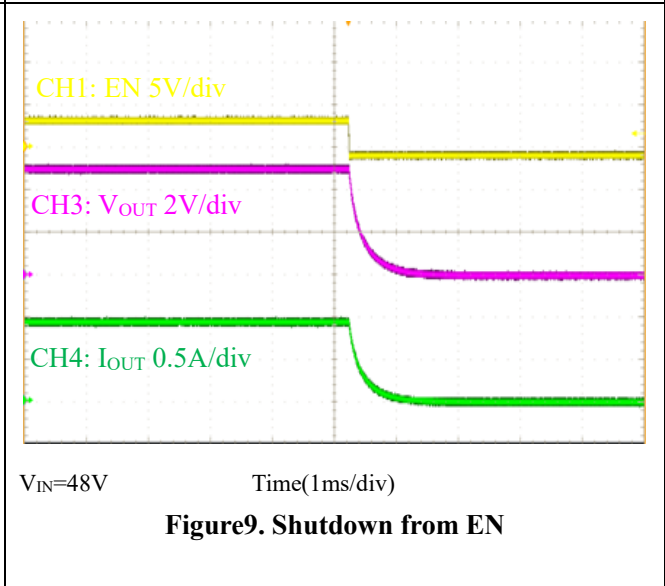
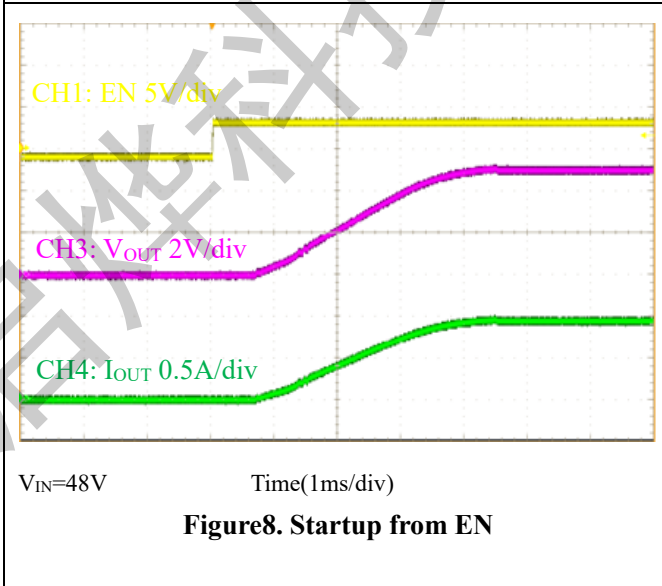
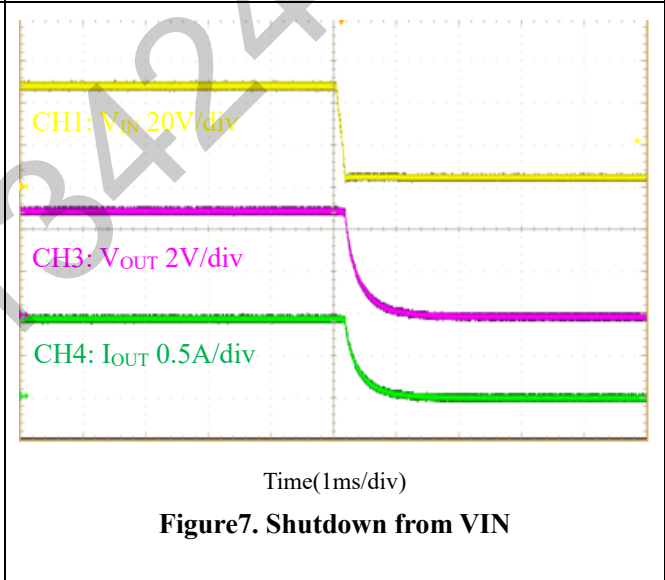
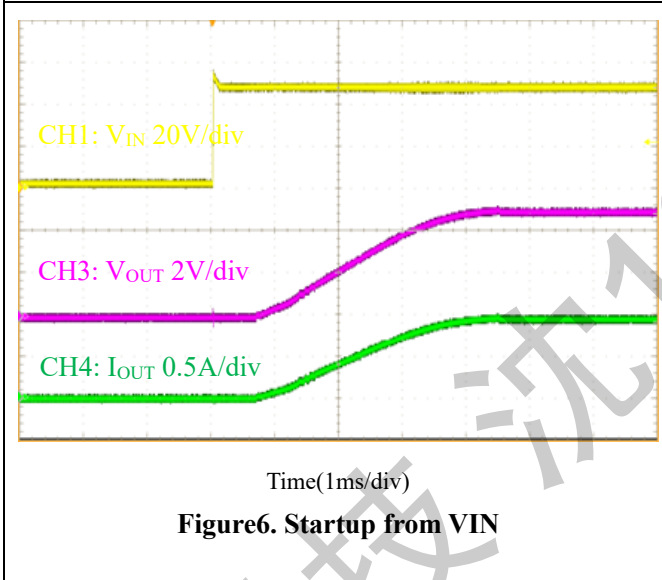
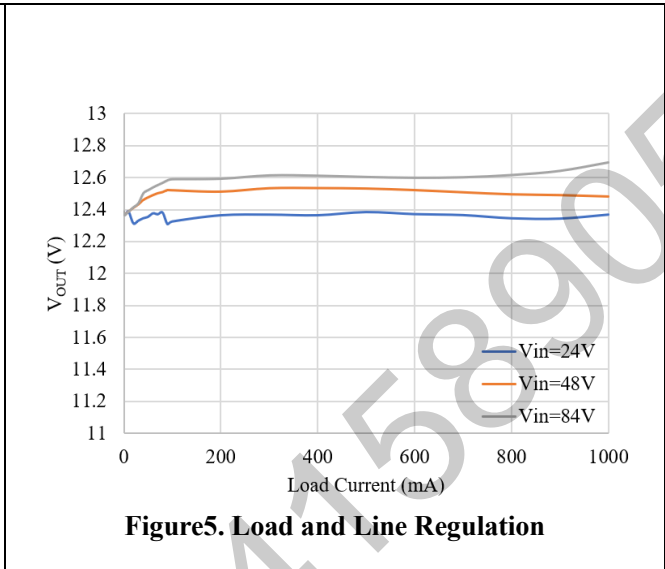
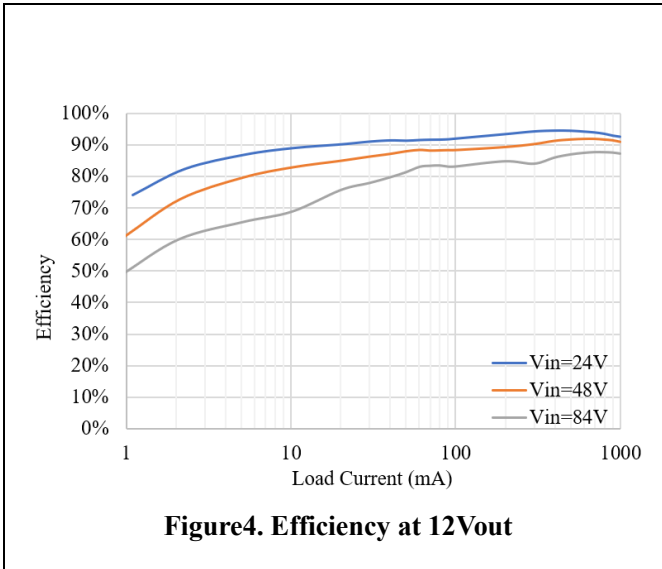
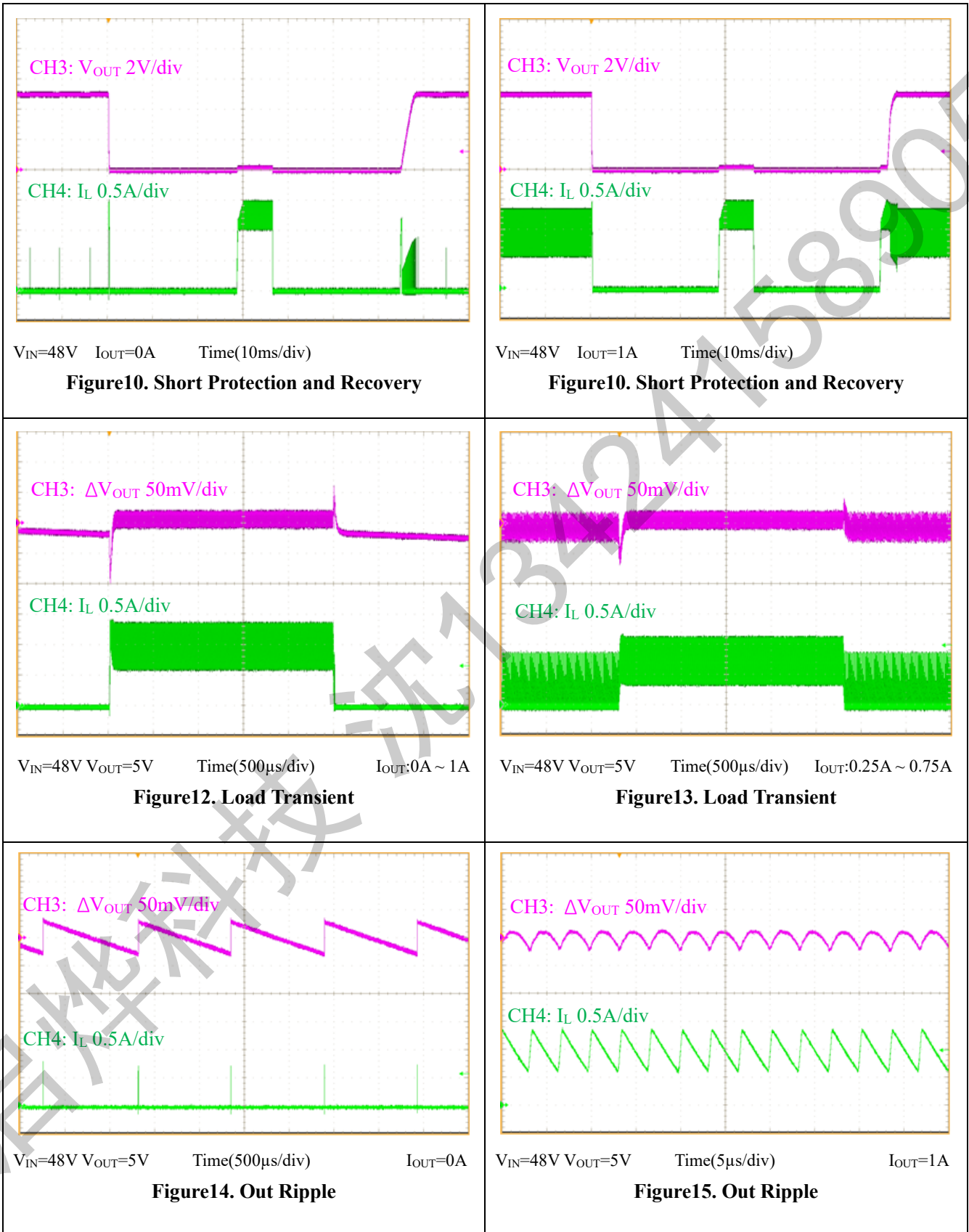


Figure3. Block Diagram

11 TYPICAL CHARACTERISTICS





12 APPLICATIONS

12.1 Operation Overview

The TS16E13 is a ultra-low I_Q synchronous buck converter. With very low $R_{DS(ON)}$ MOSFETs, the TS16E13 can achieve very high efficiency. This converter operates over a wide input voltage range from 4.5V to 100V delivering up to 1A DC load current or 3A peak current. As adopting constant on-time (COT) mode, TS16E13 can achieve fast transient responses for high voltage step down applications. Control loop compensation is not required for this regulator, reducing design time and external component count. And the pin arrangement is designed for a simple layout requiring only a few external components.

Because of high integration in the TS16E13, the application circuit is very simple. Only the on-timer resistor R_T , the feedback resistors (R_{f1} and R_{f2}), the BOOT capacitor C_{BOOT} , the feedforward capacitor C_{ff} , the input capacitor C_{IN} , the output capacitor C_{OUT} and the output inductor L need to be selected for the targeted applications.

12.2 Switching Frequency (R_T)

The switch frequency of TS16E13 is set by the on-time resistor R_T . As shown below, in 5V_{OUT} application a 43k Ω resistor sets the switching frequency at 300kHz.

$$F_{SW}(kHz) = \frac{2.56 \times V_{OUT}(V)}{R_T(M\Omega)}$$

Note that the final switching frequency is not only affected by component tolerant but also t_{ON-MIN} and $t_{OFF-MIN}$.

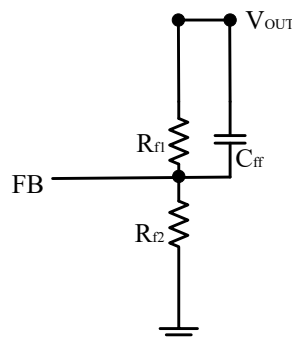
12.3 Output Voltage Program

Choose R_{f1} and R_{f2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{f1} and R_{f2} using below equation:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R_{f1}}{R_{f2}}\right)$$

R_{f1} in the range of 100k Ω to 500k Ω is recommended for most applications. Larger feedback resistors consumes less DC current, which is important if light-load efficiency is critical. But too large resistors is not recommended as the feedback path would become more susceptible.

The feedforward capacitor C_{ff} is strongly recommended, which can improve the system stability and transient responses.



12.4 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X5R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 1 μ F low ESR ceramic capacitor is recommended.

12.5 Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current $I_{OUT(max)}$ for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT(max)} + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the $I_L(\text{peak})$. An inductor whose saturation current is above the current limit setting of the TS16E13 will be best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

12.5 Output Capacitor (C_{OUT})

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only take the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X5R or better grade ceramic capacitor larger than 22 μ F is recommended. For high peak current applications, an E-cap larger than 100uF is recommended too.

12.6 Enable Operation

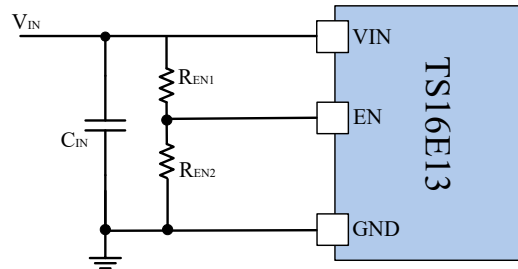
Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \times V_{ENH}$$

V_{ENH} is EN rising threshold voltage, typical is 1.24V.

The UVLO hysteresis is accomplished with an internal $2\mu\text{A}$ current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(V) = R_{EN1} \times 2\mu\text{A}$$



12.7 Boot-strap capacitor

This capacitor provides the energy for high-side gate driver. A high quality 10nF ceramic capacitor connected between the BS pin and the SW pin is recommended. Also a RC series net can be used for slow down the turn-on speed of high side MOSFET.

12.8 Power Good (PGOOD)

TS16E13 provides a PGOOD flag pin to indicate whether the output voltage is within the regulation level. PGOOD is an open-drain output that requires a pullup resistor to a DC source. The typical range of pullup resistance is about 10k Ω . When the FB voltage exceeds 96% of the reference, the internal switch will be turned off and PGOOD can be pulled high by the pullup resistor. If the FB voltage falls below 92% of the reference, the switch will be turned on and PGOOD is pulled low to indicate the output voltage is out of regulation.

13 LAYOUT

13.1 Layout Guideline

To achieve high performance of the TS16E13, the following layout tips must be followed.

- (1) At least one low-ESR ceramic bypass capacitor C_{IN} must be used. Place the C_{IN} as close as possible to the TS16E13 VIN and GND pins.
- (2) Minimize the loop area formed by C_{IN} connections to VIN and GND pins.
- (3) Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.
- (4) Maximize the PCB area connecting to the GND pin and thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.
- (5) Place the feedback resistors, R_{f1} and R_{f2} , close to the FB pin. Route the feedback V_{OUT} sense path away from noisy nodes such as the SW net.
- (6) The RT pin is sensitive to noise. The on-time set resistor R_T must be close to the device.

13.2 Layout Example

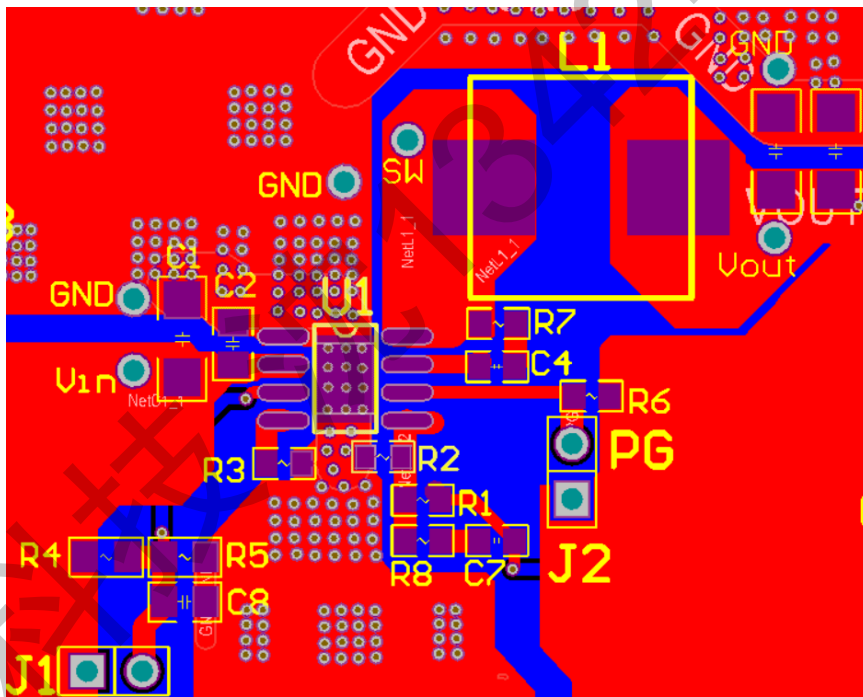
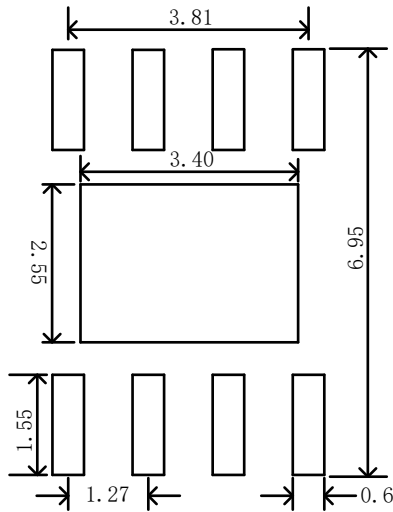
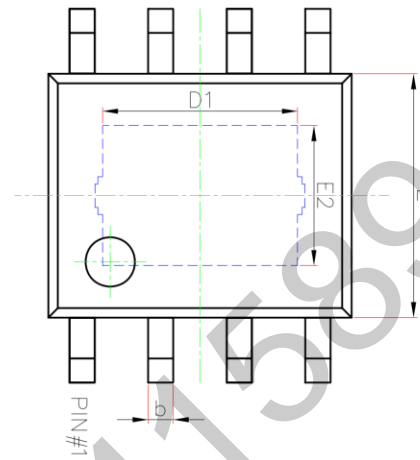
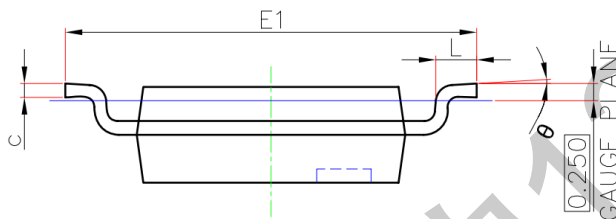
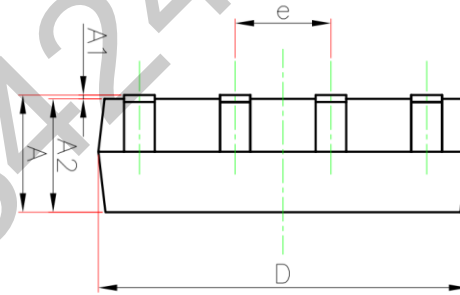
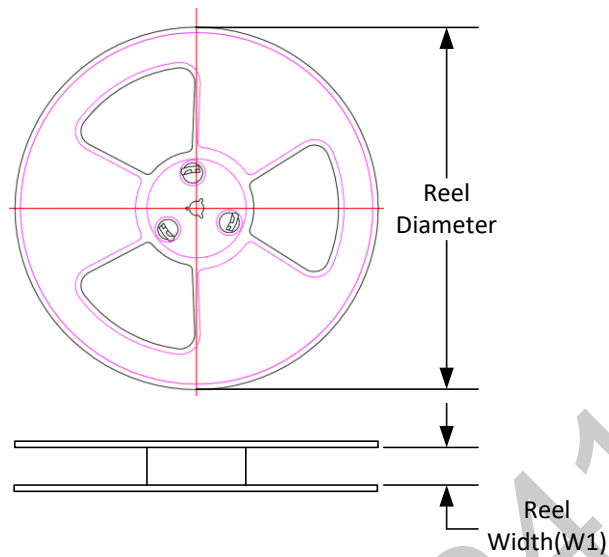
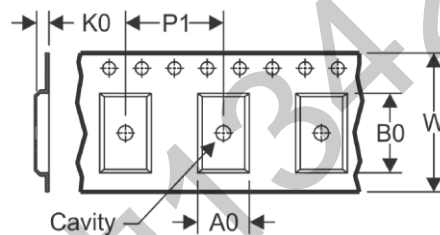


Figure16. Layout Example

14 PACKAGE SIZE

Figure17. Recommended Land Pattern (mm)

Figure 18. TS16E13 Top View

Figure19. TS16E13 Side View

Figure20. TS16E13 Side View

SYMBOL	Millimeter	
	MIN	NOM
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

15 REEL AND TAPE INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	Quantities	Reel Diameter (mm)	Reel Width W1(mm)
TS16E13	ESOP8	8	4000	332	12.5
A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	
4.0	3.3	1.1	8.0	12.0	

16 TAPE AND REEL BOX DIMENSIONS

