



TP90H180PS

900V Cascode GaN FET in TO-220 (source tab)

Description

The TP90H180PS 900V, 165mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

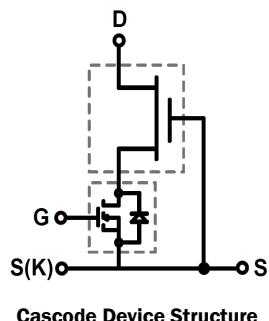
Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

- [AN-0003](#): Printed Circuit Board Layout and Probing
- [AN-0002](#): Characteristics of GaN Power Switches

Key Specifications	
V _{DS} (V) min	900
R _{DS(on)} (mΩ) max*	198
Q _{rr} (nC) typ	50
Q _g (nC) typ	10.3

* Includes dynamic R_(on)



Features

- GSD pin layout improves high speed design
- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Q_{rr} of 50nC—no free-wheeling diode required
- JEDEC-qualified GaN technology
- RoHS compliant

Benefits

- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

Ordering Information

Part Number	Package (RoHS compliant)
TP90H180PS	3 Lead TO-220



TP90H180PS

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Limit Value	Unit
$I_{D25^\circ\text{C}}$	Continuous drain current @ $T_c=25^\circ\text{C}$	15	A
$I_{D100^\circ\text{C}}$	Continuous drain current @ $T_c=100^\circ\text{C}$	9.5	A
I_{DM}	Pulsed drain current (pulse width: 10μs)	59	A
V_{DSS}	Drain to source voltage	900	V
V_{TDS}	Transient drain to source voltage ^a	1000	V
V_{GSS}	Gate to source voltage	± 18	V
$P_{D25^\circ\text{C}}$	Maximum power dissipation	78	W
T_c	Operating temperature	Case	-55 to +150
T_j		Junction	-55 to +150
T_s	Storage temperature	-55 to +150	°C
T_{csold}	Soldering peak temperature ^b	260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta jc}$	Junction-to-case	1.6	°C/W
$R_{\theta ja}$	Junction-to-ambient	62	°C/W

Notes:

- a. In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$
- b. For 10 sec., 1.6mm from the case

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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Maximum drain-source voltage	900	—	—	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	$V_{DS}=V_{GS}, I_D=0.5\text{mA}$
$R_{DS(on)}$	Drain-source on-resistance ($T_J=25^\circ\text{C}$)	—	165	198	$\text{m}\Omega$	$V_{GS}=8V, I_D=10\text{A}, T_J=25^\circ\text{C}$
	Drain-source on-resistance ($T_J=150^\circ\text{C}$)	—	340	—	$\text{m}\Omega$	$V_{GS}=8V, I_D=10\text{A}, T_J=150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current ($T_J=25^\circ\text{C}$)	—	2.5	30	μA	$V_{DS}=900V, V_{GS}=0V, T_J=25^\circ\text{C}$
	Drain-to-source leakage current ($T_J=150^\circ\text{C}$)	—	12	—	μA	$V_{DS}=900V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	Drain-to-source forward leakage current	—	—	100	nA	$V_{GS}=18V$
	Drain-to-source reverse leakage current	—	—	-100	nA	$V_{GS}=-18V$
Dynamic						
C_{ISS}	Input capacitance	—	730	—	pF	$V_{GS}=0V, V_{DS}=600V, f=1\text{MHz}$
C_{OSS}	Output capacitance	—	44	—		
C_{RSS}	Reverse transfer capacitance	—	5	—	pF	$V_{GS}=0V, V_{DS}=0V \text{ to } 600V$
$C_{O(er)}$	Output capacitance, energy related ^a	—	58	—		
$C_{O(tr)}$	Output capacitance, time related ^b	—	96	—	nC	$V_{DS}=400V, V_{GS}=0V \text{ to } 8V, I_D=8.8A$
Q_g	Total gate charge	—	10.3	—		
Q_{gs}	Gate-source charge	—	2.1	—		
Q_{gd}	Gate-drain charge	—	2.2	—		
$t_{d(on)}$	Turn-on delay	—	28.4	—	ns	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=12A, R_G=15\Omega \text{ (driver internal series resistance), } Z_{FB}=180\text{ohm @100MHz}$
t_r	Rise time	—	4.5	—		
$T_{d(off)}$	Turn-off delay	—	37.2	—		
t_f	Fall time	—	8	—		
Reverse Operation						
I_s	Reverse current	—	—	9.5	A	$V_{GS}=0V, T_C=100^\circ\text{C}$
V_{SD}	Reverse voltage	—	2.3	—	V	$V_{GS}=0V, I_s=9.5A, T_J=25^\circ\text{C}$
V_{SD}	Reverse voltage	—	1.6	—	V	$V_{GS}=0V, I_s=5A, T_J=25^\circ\text{C}$
t_{rr}	Reverse recovery time	—	29	—	ns	$I_s=13A, V_{DD}=400V, di/dt=1000A/\text{ms}, T_J=25^\circ\text{C}$
Q_{rr}	Reverse recovery charge	—	50	—	nC	

Notes:

- a. Equivalent capacitance to give same stored energy from 0V to 600V
- b. Equivalent capacitance to give same charging time from 0V to 600V

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Typical Characteristics (25 °C unless otherwise stated)

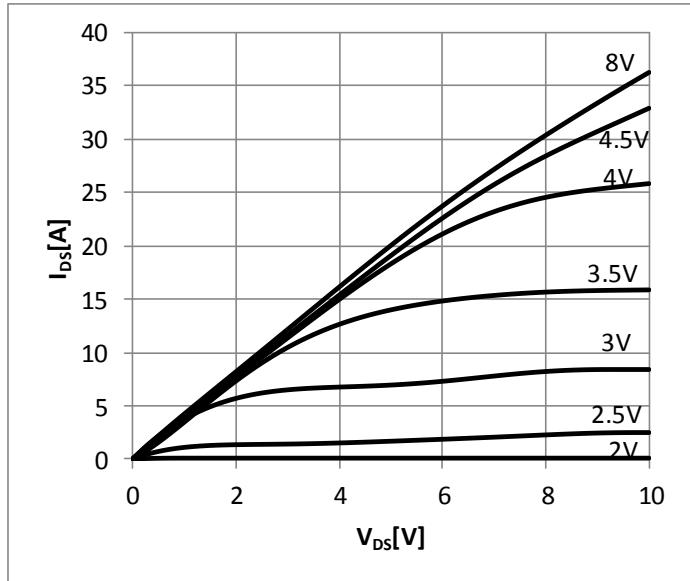
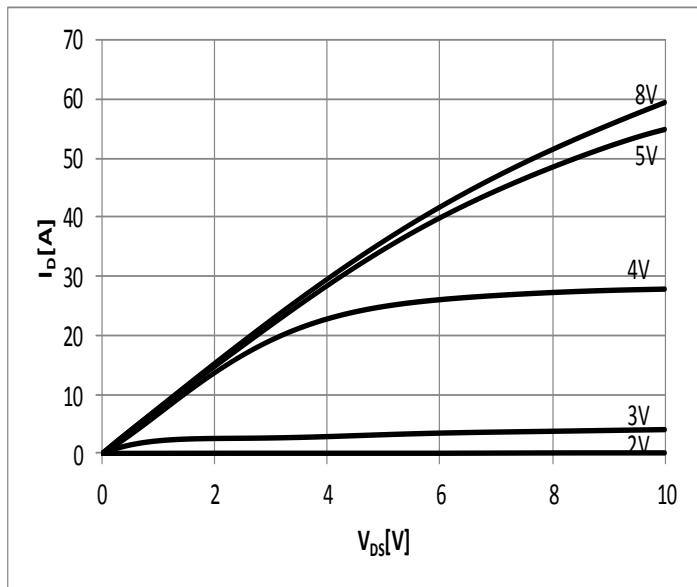


Figure 1. Typical Output Characteristics $T_J=25\text{ }^\circ\text{C}$

Parameter: V_{GS}

Figure 2. Typical Output Characteristics $T_J=150\text{ }^\circ\text{C}$

Parameter: V_{GS}

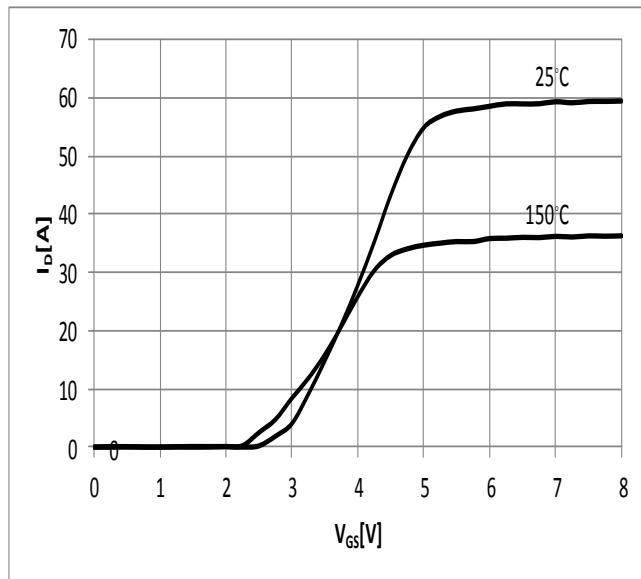


Figure 3. Typical Transfer Characteristics

$V_{DS}=10\text{V}$, Parameter: T_J

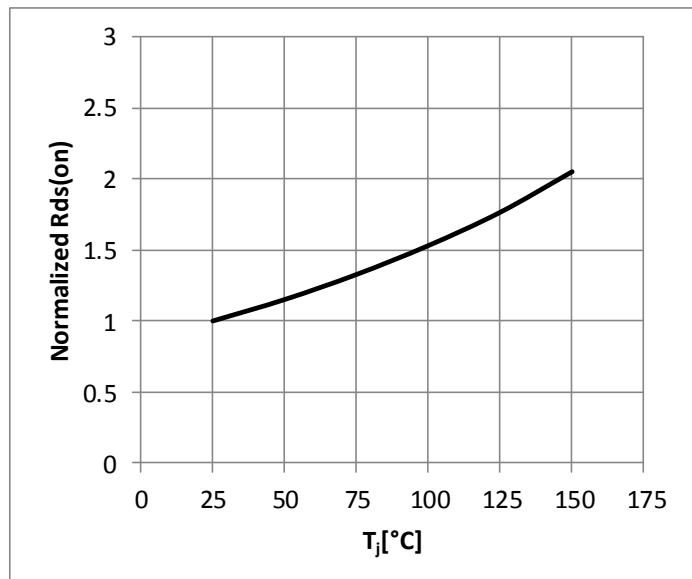


Figure 4. Normalized On-Resistance

$I_D=11\text{A}$, $V_{GS}=8\text{V}$

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Typical Characteristics (25 °C unless otherwise stated)

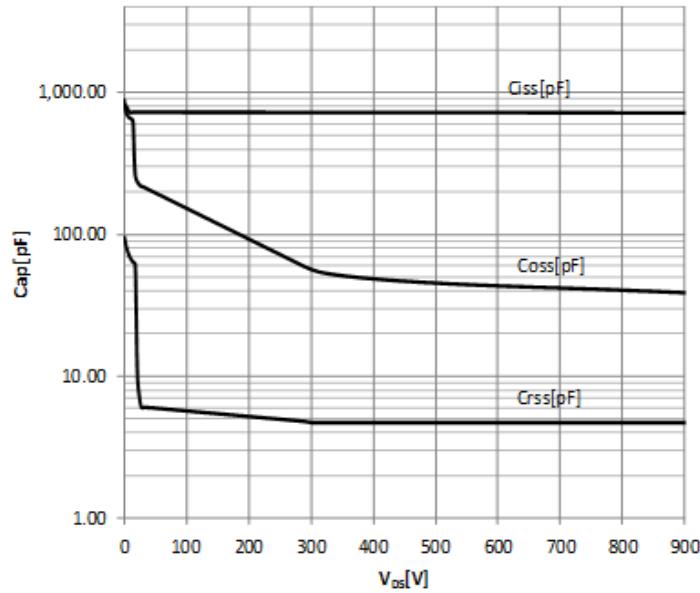


Figure 5. Typical Capacitance

$V_{GS}=0V$, $f=1MHz$

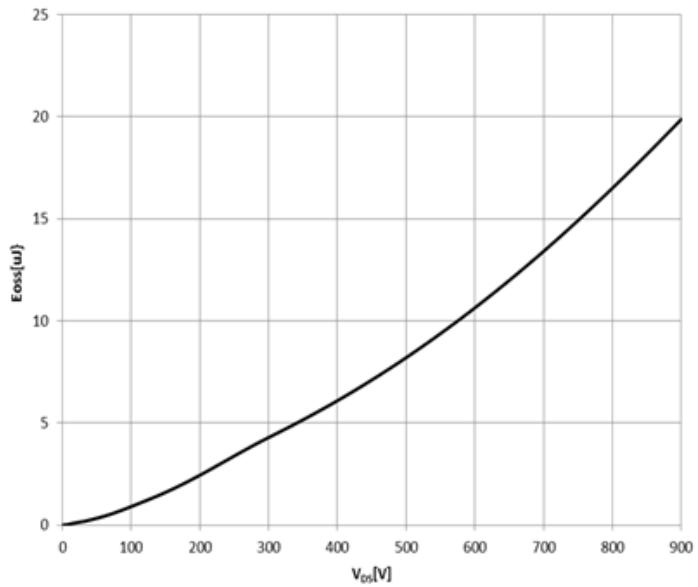


Figure 6. Typical C_{oss} Stored Energy

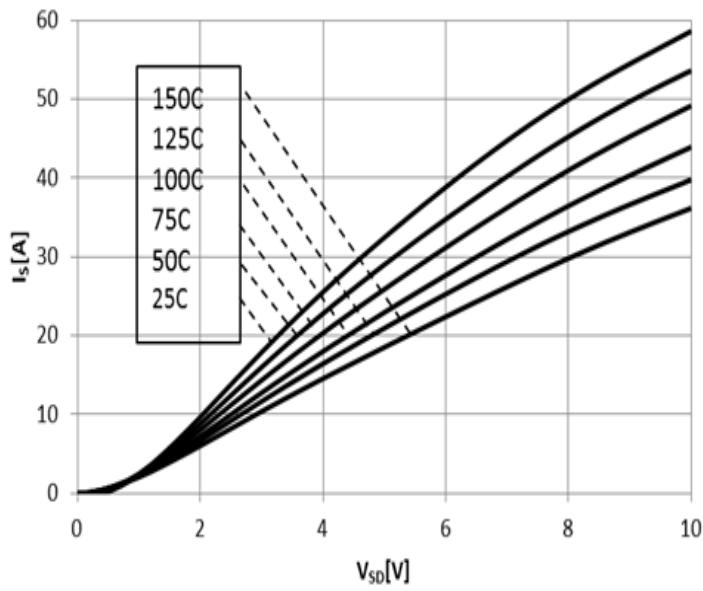


Figure 7. Forward Characteristics of Rev. Diode

$I_S=f(V_{SD})$, Parameter T_J

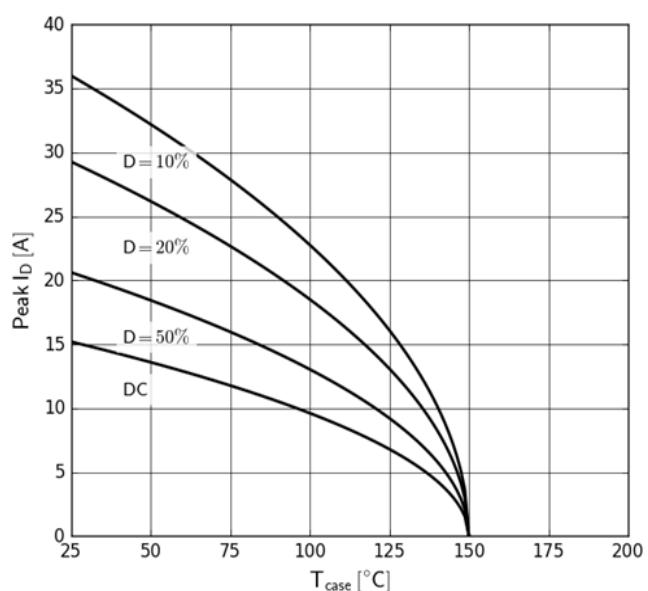


Figure 8. Current Derating

Pulse Width = 100μs

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Typical Characteristics (25 °C unless otherwise stated)

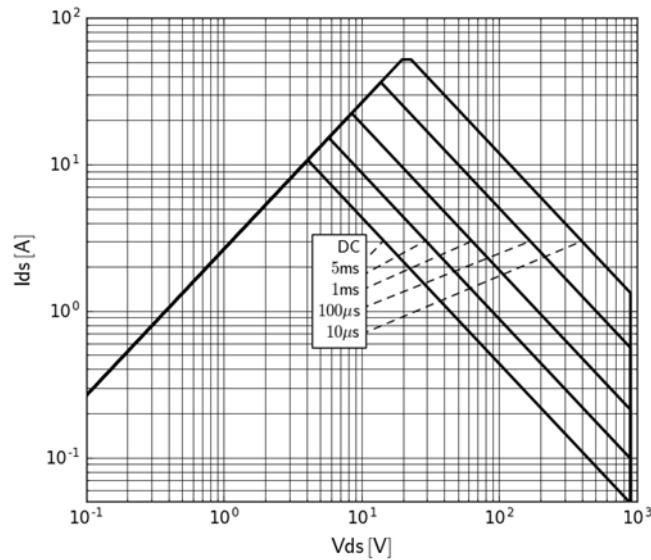


Figure 9. Safe Operating Area $T_c=25\text{ }^\circ\text{C}$

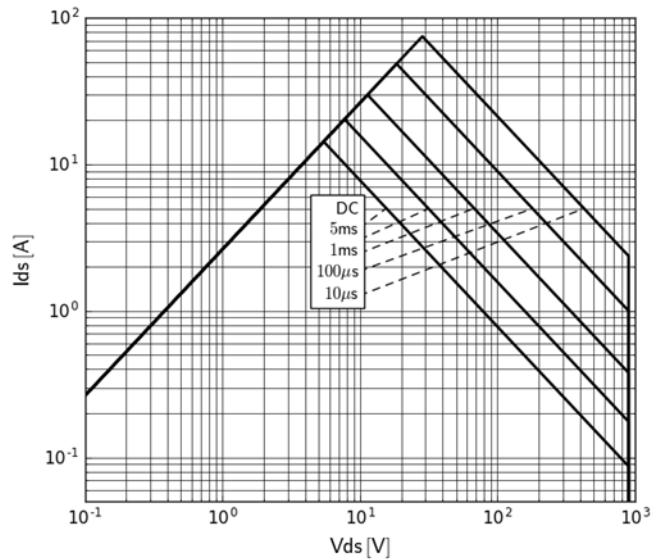


Figure 10. Safe Operating Area $T_c=80\text{ }^\circ\text{C}$

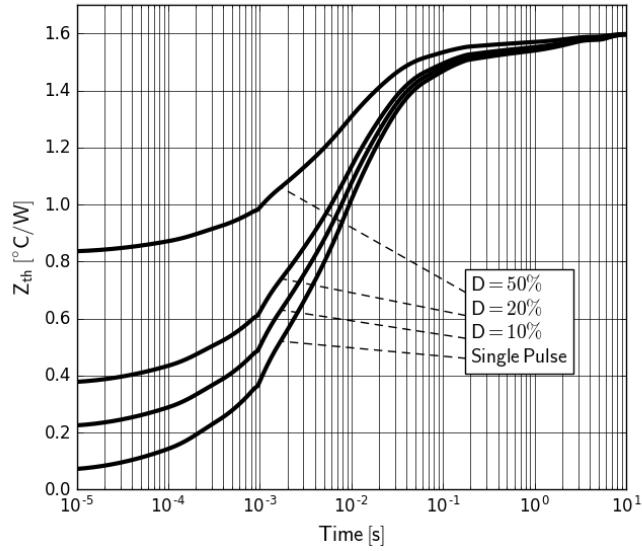


Figure 11. Transient Thermal Resistance

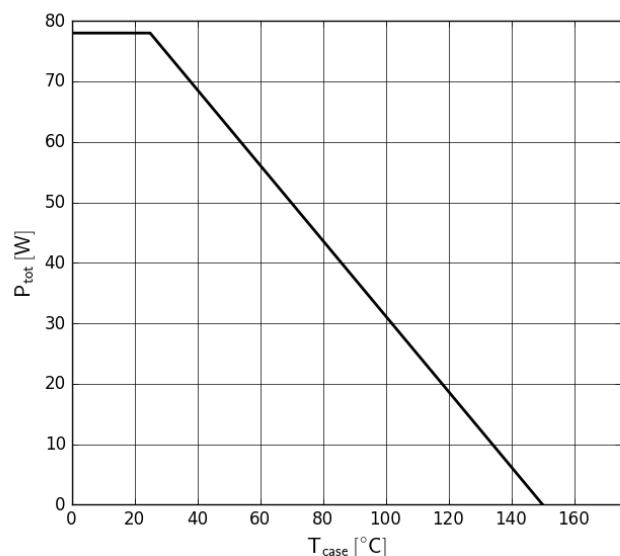
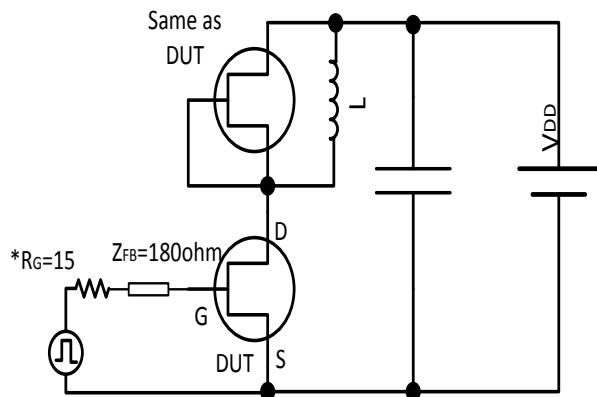


Figure 12. Power Dissipation

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Test Circuits and Waveforms



*Driver Internal Series Resistance

Figure 13. Switching Time Test Circuit

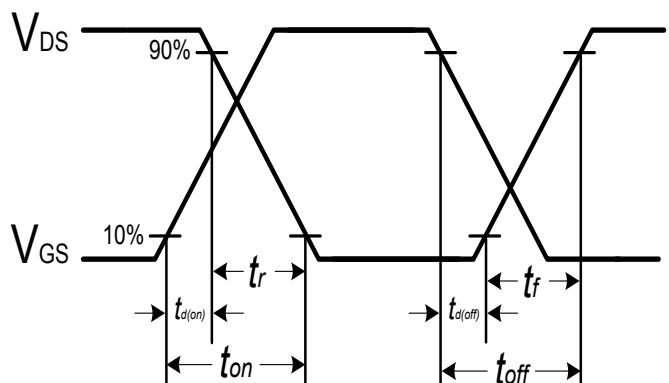


Figure 14. Switching Time Waveform

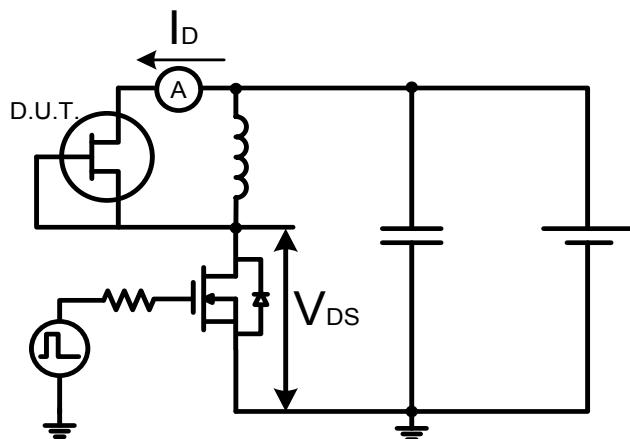


Figure 17. Test Circuit for Diode Characteristics

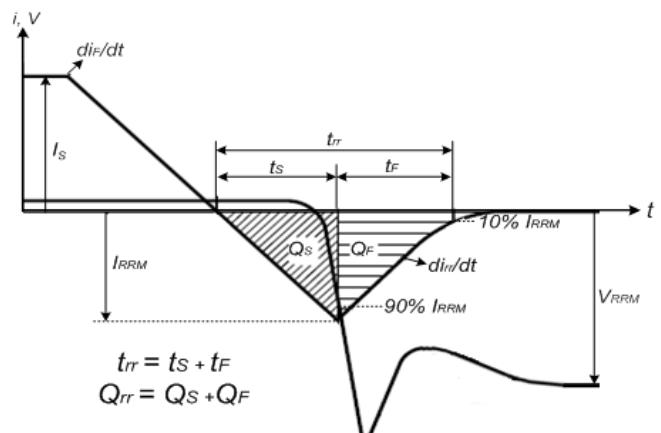
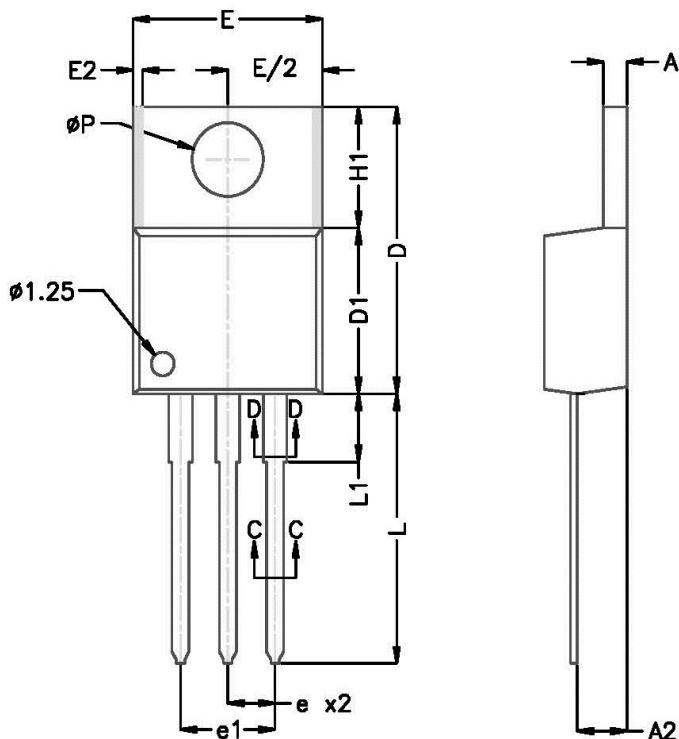


Figure 18. Diode Recovery Waveform

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MECHANICAL

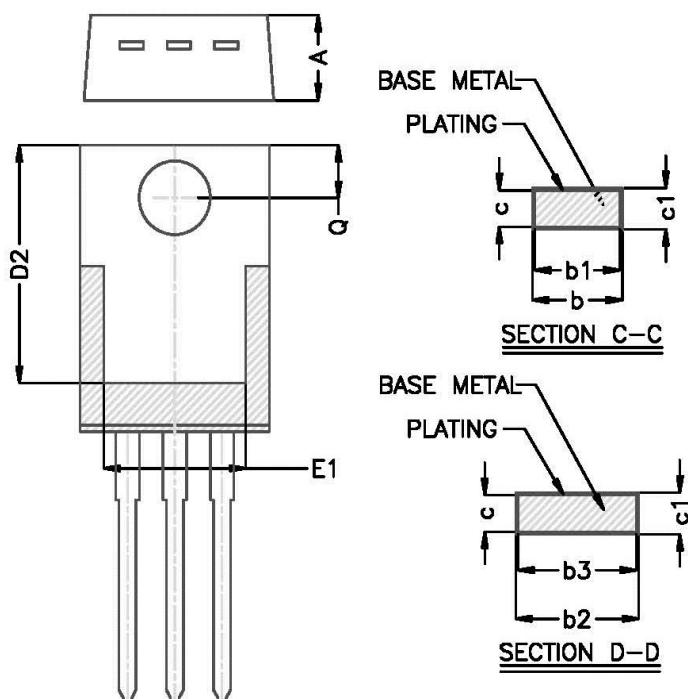
TO-220 Package



SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	—	2.92	0.080	—	0.115
b	0.38	—	1.01	0.015	—	0.040
b1	0.38	—	0.97	0.015	—	0.038
b2	1.14	—	1.78	0.045	—	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.38	—	0.61	0.014	—	0.024
c1	0.38	0.38	0.56	0.014	0.015	0.022
D	14.22	—	16.51	0.560	—	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	—	12.88	0.460	—	0.507
E	9.85	10.19	10.87	0.380	0.401	0.420
E1	6.86	—	8.89	0.270	—	0.350
E2	—	—	0.76	—	—	0.030
e	2.54	BSC	—	0.100	BSC	—
e1	5.08	BSC	—	0.200	BSC	—
H1	5.84	6.30	6.88	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	—	—	6.35	—	—	0.250
ØP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	—	3.42	0.100	—	0.135

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO-220AB.



TO-220 Package

Pin 1: Gate, Pin 2: Source, Pin 3: Drain, Tab: Source

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN-0003 : Printed Circuit Board Layout and Probing	

Application Notes

- [AN-0002](#): Characteristics of Transphorm GaN Power Switches
- [AN-0003](#): Printed Circuit Board Layout and Probing for GaN Power Switches
- [AN-0004](#): Designing Hard-switched Bridges with GaN
- [AN-0008](#): Drain Voltage and Avalanche Ratings for GaN FETs