transphorm

TP65H050BS (Preliminary)

650V Cascode GaN FET in TO-263 (source tab)

Description

The TP65H035BS 650V, 35mΩ gallium nitride (GaN) FET is an enhancement mode normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

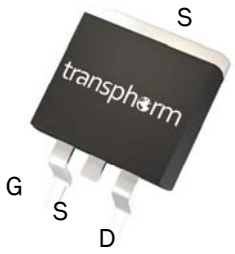
Related Literature

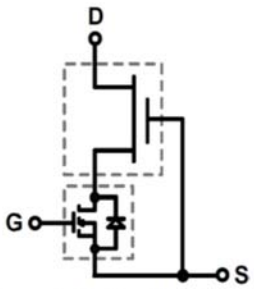
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Ordering Information

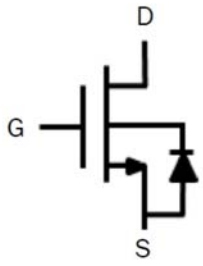
Part Number	Package	Package Configuration
TP65H050BS	TO-263	Common Source

TP65H050BS
TO-263
(top view)





Cascode Device Structure



Cascode Schematic Symbol

Features

- JEDEC-qualified GaN Technology
- Includes dynamic on resistance
- Robust design, defined by
  - Lifetime intrinsic testing
  - Wide gate safety margin
- Lower Qrr over silicon
- Reduced crossover loss
- Compatible with commonly-used gate drivers
- RoHS compliant and Halogen-free

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
- Increased power density
- Reduced system size and weight
- Overall lower system cost

Applications

- Renewable energy
- Industrial
- Telecom and datacom
- Servo motors

Key Specifications	
V_{DS} (V) min	650
V_{TDS} (V) max	800
$R_{DS(on)}$ (mΩ) max*	60
Q_{rr}** (nC)	125
Qg (nC) typ	16

* Dynamic $R_{(on)}$

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Absolute Maximum Ratings (T_j=25 °C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25 °C [a]		34	A
$I_{D100°C}$	Continuous drain current @T_C=100 °C [a]		22	A
I_{DM}	Pulsed drain current [b]		150	A
di/dt_{RDC}	Reverse diode di/dt, continuous [c]		1600	A/us
I_{RDC1}	Reverse diode switching current, continuous (dc) [d]		24	A
I_{RDC2}	Reverse diode switching current, continuous (ac) [d]		28	A
di/dt_{RDT}	Reverse diode di/dt, transient [e]		3000	A/us
I_{RDT}	Reverse diode switching current, transient		36	A
V_{DSS}	Drain to source voltage		650	V
V_{TDS}	Transient drain to source voltage [f]		800	V
V_{GSS}	Gate to source voltage		±20	V
$P_{D25°C}$	Maximum power dissipation		119	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [g]		260	°C

All recommended current levels (I_{DM}) are based on adequate heat sinking ensuring T_j < 150C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.05	°C/W
$R_{\Theta JA}$	Junction-to-ambient	TBD	°C/W

Notes:
a. For high current operation, see application note AN0009
b. Pulse width: 10μs
c. Continuous switching operation
d. Definitions: dc refers to dc to dc converter topologies and ac refers to inverters and PFC topologies
e. ≤ 300 pulses in 1 second
f. In off-state, spike duty cycle D<0.01, spike duration <1μs
g. For 10 sec., 1.6mm from the case

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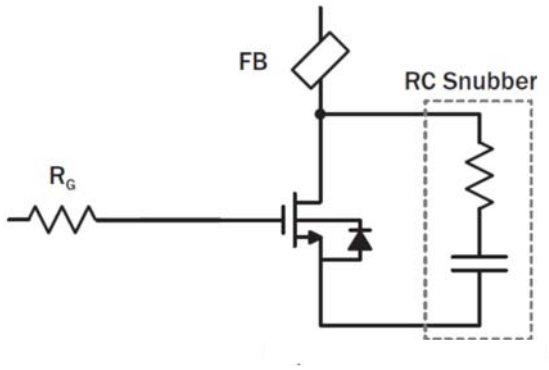
Circuit Configuration [a]



Sustained oscillation can occur in switching applications using high speed GaN devices, but must be prevented for safe operation. By inserting a ferrite bead and/or an RC snubber with the recommended values below, Transphorm GaN FETs can operate in a hard-switching bridge up to their full-rated current even with a less-than-ideal PCB layout. See application note AN0009: Recommended External Circuitry for more information.

Ferrite Beads and Recommended RC Snubbers

Devices	Drain Ferrite Bead	RC Snubber Network
TP65H050BS	TBD	15 Ω / 33—47 pF

Notes:

a. Recommended gate drive: (10V to 13V, 0V), R_G = 22Ω using either a 0.5 A or 4.0 A silicon labs driver.

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Electrical Parameter (T_j=25°C unless otherwise stated)

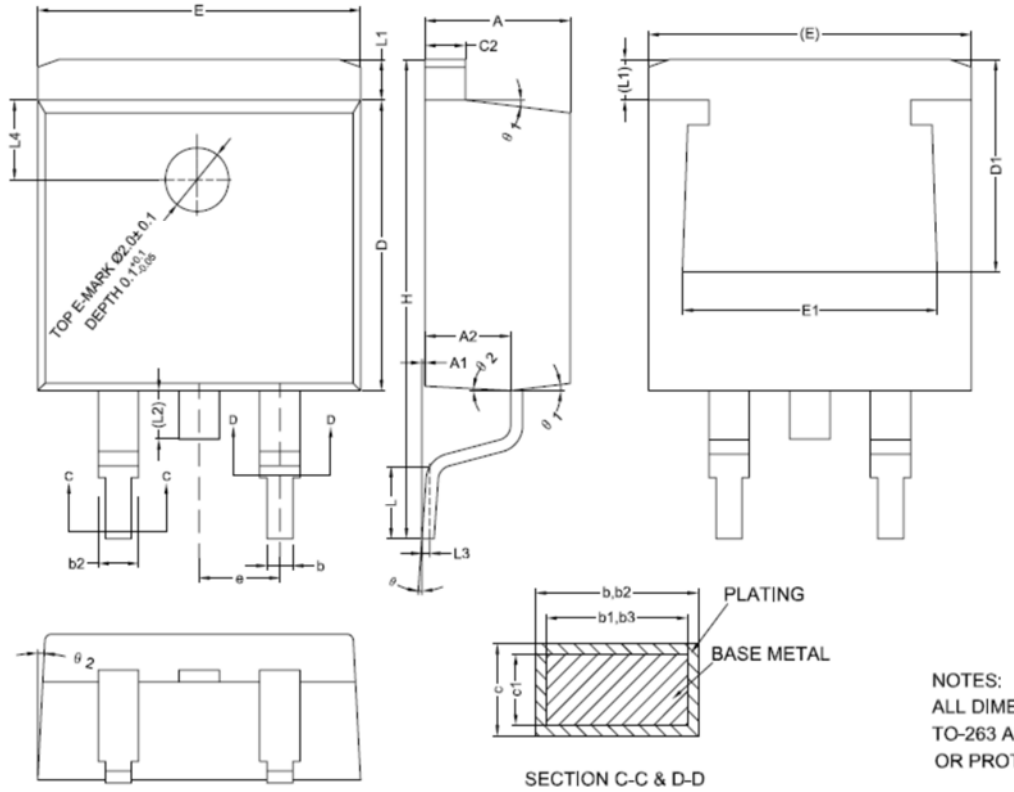
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS-MAX}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0 V
$V_{GS(th)}$	Gate threshold voltage [d]	3.4	3.9	4.4	V	V_{DS}=V_{GS}, I_D=0.7 mA
$R_{DS(on)}$	Drain-source on-resistance [a]	—	50	60	mΩ	V_{GS}=10 V, I_D=24 A, T_J=25°C
		—	105	—		V_{GS}=10 V, I_D=24 A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	4	40	μA	V_{DS}=650 V, V_{GS}=0 V, T_J=25°C
		—	15	—		V_{DS}=650 V, V_{GS}=0 V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20 V
		—	—	-100		V_{GS}=-20 V
C_{ISS}	Input capacitance	—	960	—	pF	V_{GS}=0 V, V_{DS}=400 V, *f*=1MHz
C_{OSS}	Output capacitance	—	130	—		
C_{RSS}	Reverse transfer capacitance	—	TBD	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	TBD	—	pF	V_{GS}=0 V, V_{DS}=0 V to 400 V
$C_{O(tr)}$	Output capacitance, time related [c]	—	290	—		
Q_g	Total gate charge	—	24	36	nC	V_{DS}=400 V, V_{GS}=10 V, I_D=24 A
Q_{gs}	Gate-source charge	—	TBD	—		
Q_{gd}	Gate-drain charge	—	TBD	—		
Q_{oss}	Output charge	—	TBD	—	nC	V_{GS}=0 V, V_{DS}=0 V to 400 V
$t_{d(on)}$	Turn-on delay	—	TBD	—	ns	V_{DS}=400 V, V_{GS}=10 V, I_D=24 A
t_r	Rise time	—	TBD	—		
$T_{d(off)}$	Turn-off delay	—	TBD	—		
t_f	Fall time	—	TBD	—		
Reverse Device Characteristics						
I_s	Reverse current	—	—	22	A	V_{GS}=0 V, T_C=100C, ≤50% Duty Cycle
V_{SD}	Reverse voltage [a]	—	2.2	2.6	V	V_{GS}=0 V,I_s=24 A, T_j=25C
		—	1.6	1.9	V	V_{GS}=0 V,I_s=12 A, T_j=25C
t_{rr}	Reverse recovery time	—	30	—	ns	I_s=24 A, V_{DD}=400 V, di/dt=1000A/us, T_j=25C
Q_{rr}	Reverse recovery charger	—	125	—	nC	

Notes:
a. Dynamic value
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

Mechanical

3 Lead TO-263 (BS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source



SECTION C-C & D-D

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.40	4.57	4.70
A1	0	0.10	0.25
A2	2.59	2.69	2.79
b	0.77	-	0.90
b1	0.76	0.81	0.86
b2	1.23	-	1.36
b3	1.22	1.27	1.32
c	0.34	-	0.47
c1	0.33	0.38	0.43
c2	1.22	-	1.32
D	9.05	9.15	9.25
D1	6.60	-	-
E	10.06	10.16	10.26
E1	7.80	-	8.20
e		2.54BSC	
H	14.70	15.10	15.50
L	2.00	2.30	2.60
L1	1.17	1.27	1.40
L2	-	-	1.75
L3		0.25BSC	
L4		2.00REF	
θ	0°	-	8°
θ1	5°	7°	9°
θ2	1°	3°	5°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-263 AB DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs
- AN0010: GaN FETs in Parallel Using Drain Ferrite Beads and RC Snubbers for High-power Applications

Evaluation Boards

- TBD

Revision History

Version	Date	Change(s)
0	08/01/2017	Gen III Preliminary Specification