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transphorm

TPH3202P Series

600V Cascode GaN FET TO-220 Series

Description

The TPH3202P Series 600V, 290mΩ gallium nitride (GaN) FETs are normally-off devices. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

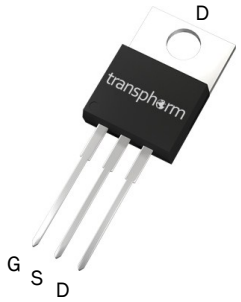
Related Literature

- AN0003: Printed Circuit Board Layout and Probing
- AN0002: Characteristics of GaN Power Switches

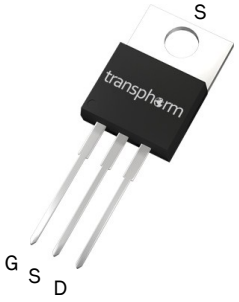
Product Series and Ordering Information

Part Number	Package	Package Configuration
TPH3202PD	3 Lead TO-220	Common Drain
TPH3202PS	3 Lead TO-220	Common Source

TPH3202PD
TO-220
(top view)



TPH3202PS
TO-220
(top view)



Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 29nC—no free-wheeling diode required
- GSD pin layout improves high speed design
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

Benefits

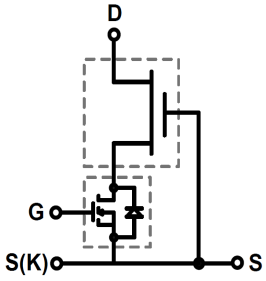
- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

- Renewable energy
- Industrial
- Automotive
- Telecom and datacom
- Servo motors

Key Specifications	
V_{DS} (V) min	600
V_{TDS} (V) max	750
$R_{DS(on)}$ (mΩ) max*	350
Q_{rr} (nC) typ	29
Qg (nC) typ	6.2

* Includes dynamic $R_{(on)}$



Cascode Device Structure

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Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25°C		9	A
$I_{D100°C}$	Continuous drain current @T_C=100°C		6	A
I_{DM}	Pulsed drain current (pulse width: 100µs)		35	A
V_{DSS}	Drain to source voltage		600	V
V_{TDS}	Transient drain to source voltage [a]		750	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25°C}$	Maximum power dissipation		65	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +175	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [b]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	2.3	°C/W
$R_{\Theta JA}$	Junction-to-ambient	62	°C/W

Notes:
a. In off-state, spike duty cycle D<0.1, spike duration <1µs
b. For 10 sec., 1.6mm from the case

Electrical Characteristics (T_C=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Static						
$V_{DSS-MAX}$	Maximum drain-source voltage	600	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2	2.5	V	V_{DS}=V_{GS}, I_D=250μA
$R_{DS(on)}$	Drain-source on-resistance (T_J=25°C)	—	290	350	mΩ	V_{GS}=8V, I_D=5.5A, T_J=25°C
	Drain-source on-resistance (T_J=175°C)	—	670	—		V_{GS}=8V, I_D=5.5A, T_J=175°C
I_{DSS}	Drain-to-source leakage current (T_J=25°C)	—	2.5	90	μA	V_{DS}=600V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current (T_J=150°C)	—	8	—		V_{DS}=600V, V_{GS}=0V, T_J=150°C
I_{GSS}	Drain-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Drain-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
Dynamic						
C_{ISS}	Input capacitance	—	760	—	pF	V_{GS}=0V, V_{DS}=480V, *f*=1MHz
C_{OSS}	Output capacitance	—	26	—		
C_{RSS}	Reverse transfer capacitance	—	3.5	—		
$C_{O(er)}$	Output capacitance, energy related [a]	—	36	—	pF	V_{GS}=0V, V_{DS}=0V to 480V
$C_{O(tr)}$	Output capacitance, time related [a]	—	57	—		
Q_g	Total gate charge [b]	—	6.2	9.3	nC	V_{DS}=100V [a], V_{GS}=0V to 4.5V, I_D=5.5A
Q_{gs}	Gate-source charge	—	2.1	—		
Q_{gd}	Gate-drain charge	—	2.2	—		
$t_{d(on)}$	Turn-on delay	—	6.2	—	ns	V_{DS}=400V, V_{GS}=0V to 10V, I_D=5.5A, R_G=2Ω
t_r	Rise time	—	4.5	—		
$T_{d(off)}$	Turn-off delay	—	9.7	—		
t_f	Fall time	—	5	—		
Reverse Operation						
I_S	Reverse current	—	—	8.9	A	V_{GS}=0V, T_C=100°C
V_{SD}	Reverse voltage	—	2.11	—	V	V_{GS}=0V, I_S=5.5A, T_J=25°C
		—	3.1	—		V_{GS}=0V, I_S=5.5A, T_J=175°C
		—	1.48	—		V_{GS}=0V, I_S=3A, T_J=25°C
t_{rr}	Reverse recovery time	—	11.5	—	ns	I_S=5.5A, V_{DD}=480V, di/dt=1500A/μs, T_J=25°C
Q_{rr}	Reverse recovery charge	—	29	—	nC	

Notes:
a. Fixed while V_{DS} is rising from 0 to 80% V_{DSS}
b. Q_g does not change for V_{DS} > 100V

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Typical Characteristics (25°C unless otherwise stated)

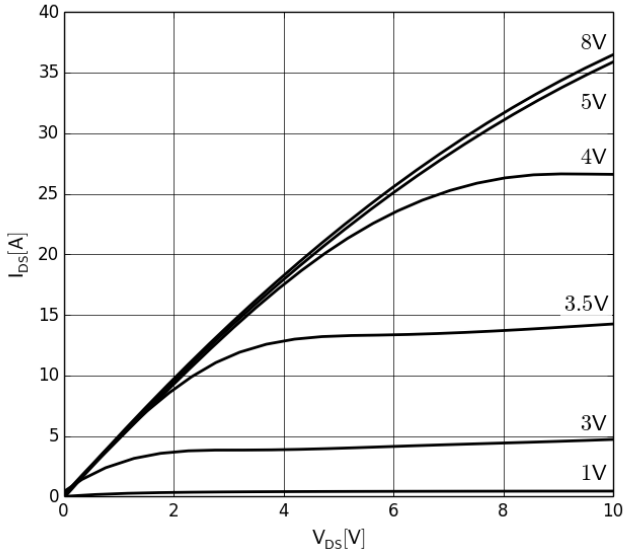


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

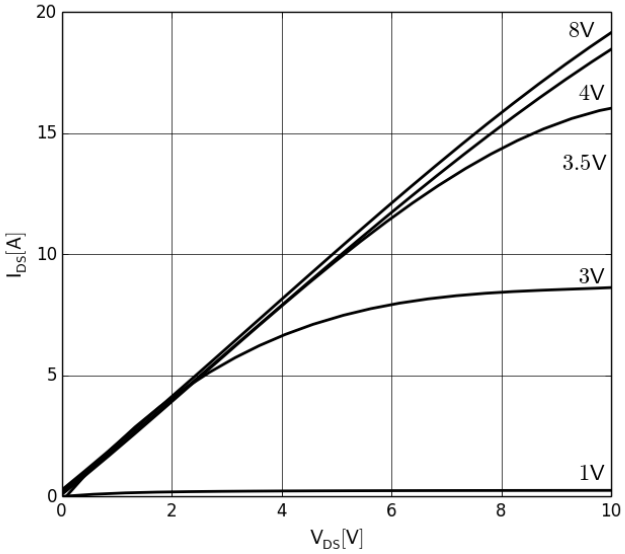


Figure 2. Typical Output Characteristics T_J=175°C
Parameter: V_{GS}

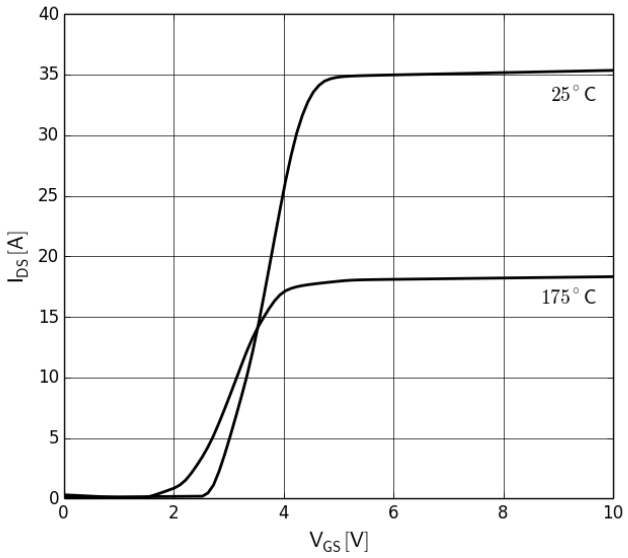


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

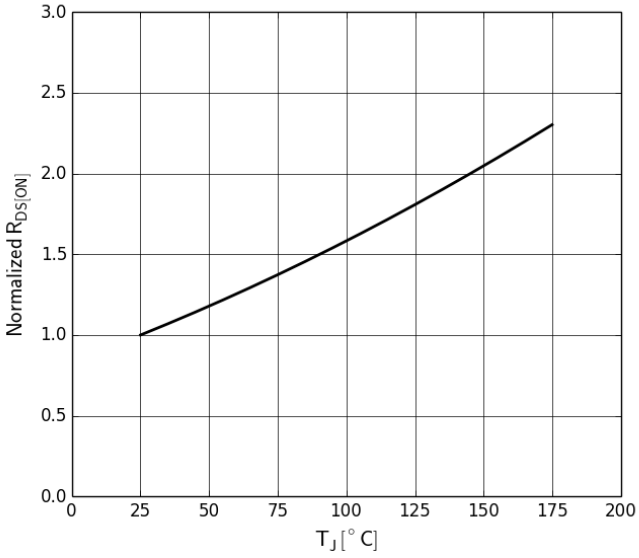


Figure 4. Normalized On-Resistance
I_D=6A, V_{GS}=8V

Typical Characteristics (25 °C unless otherwise stated)

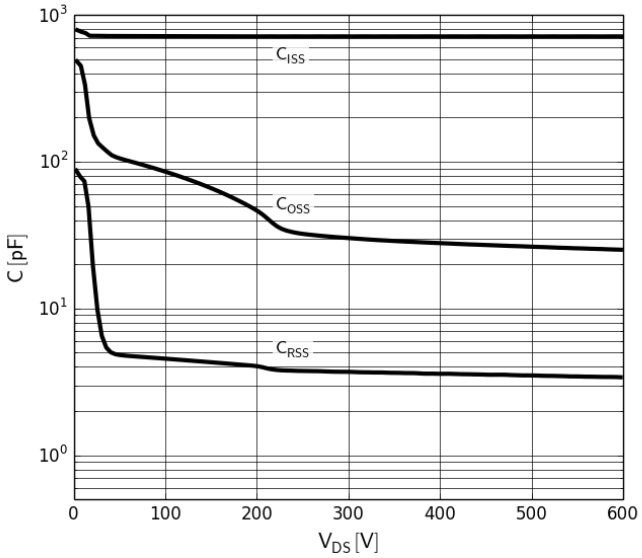


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

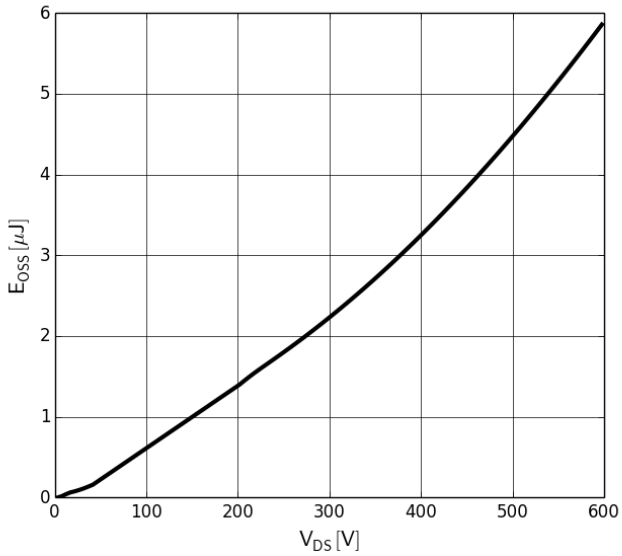


Figure 6. Typical C_{OSS} Stored Energy

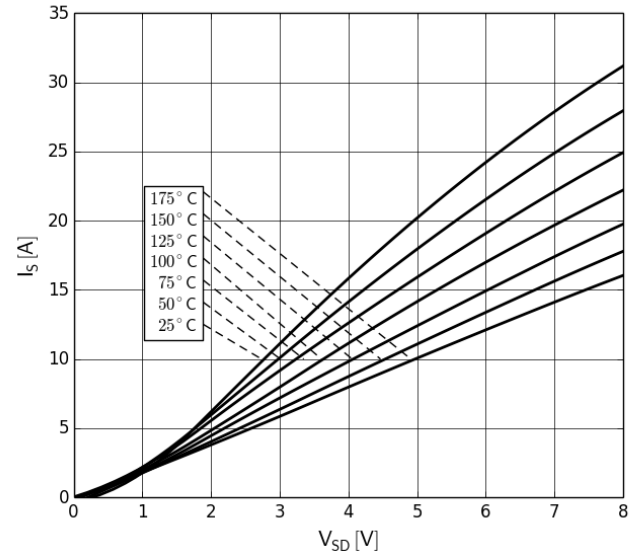


Figure 7. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$, parameter: T_J

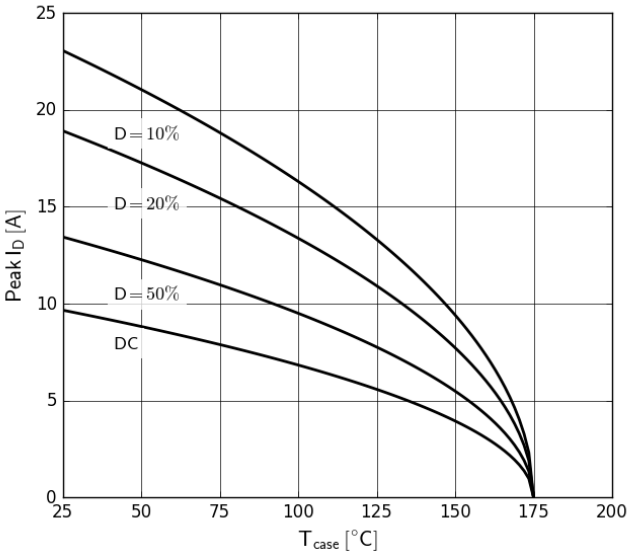


Figure 8. Current Derating
Pulse width ≤ 100µs

Typical Characteristics (25 °C unless otherwise stated)

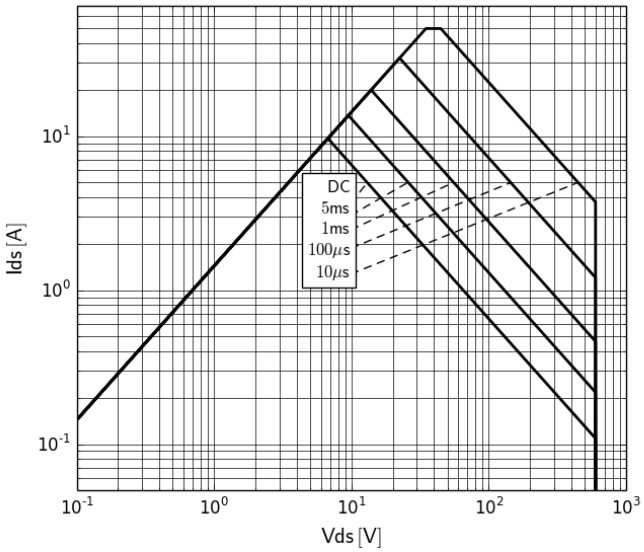


Figure 9. Safe Operating Area T_C=25 °C

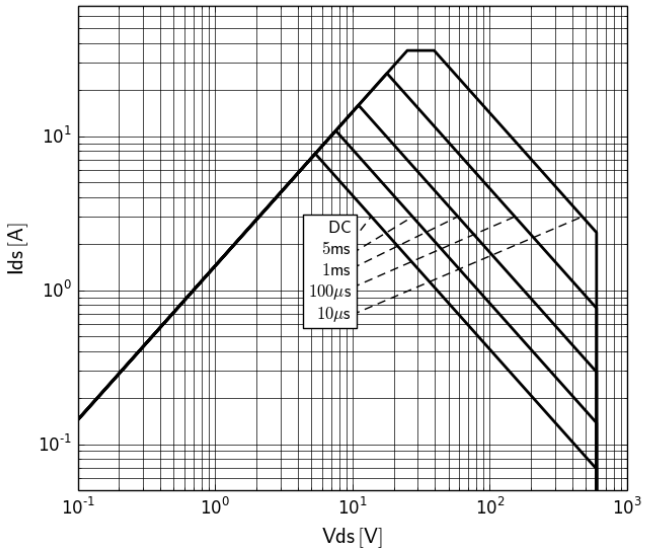


Figure 10. Safe Operating Area T_C=80 °C

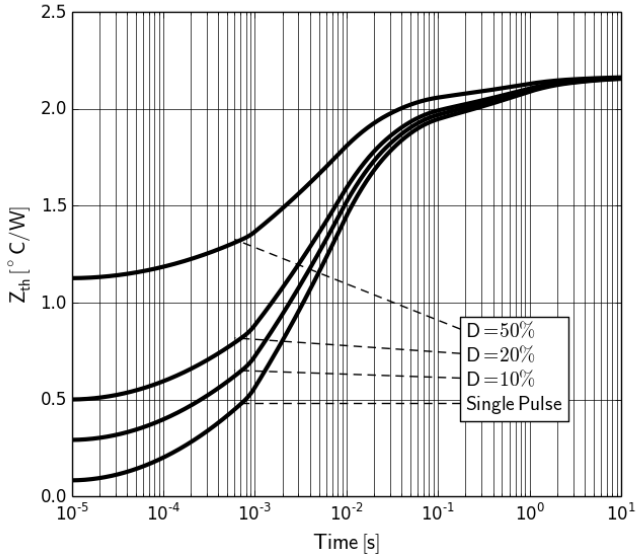


Figure 11. Transient Thermal Resistance

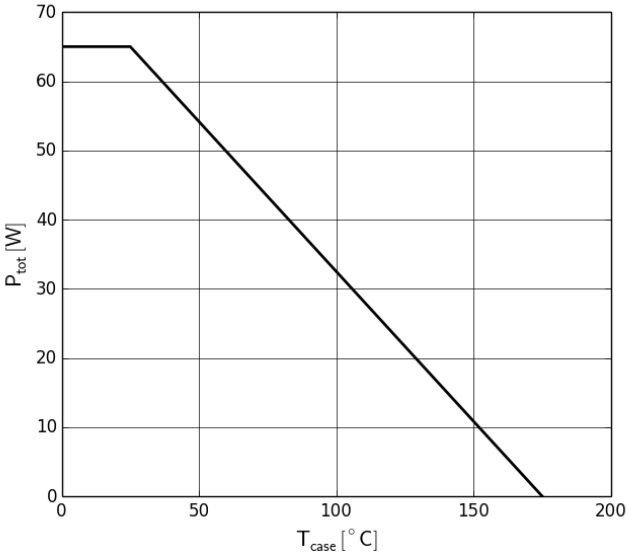


Figure 12. Power Dissipation

Test Circuits and Waveforms

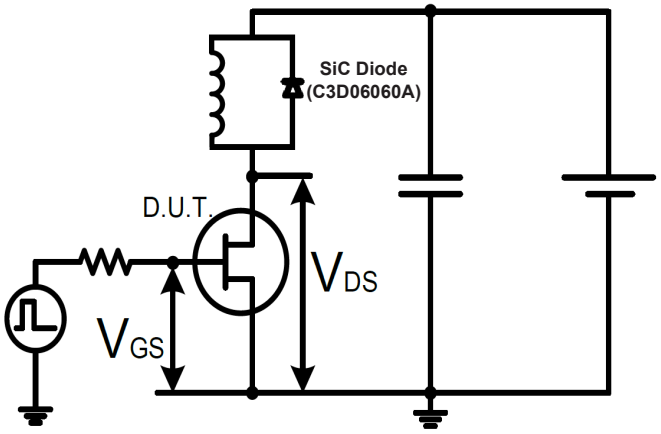


Figure 13. Switching Time Test Circuit

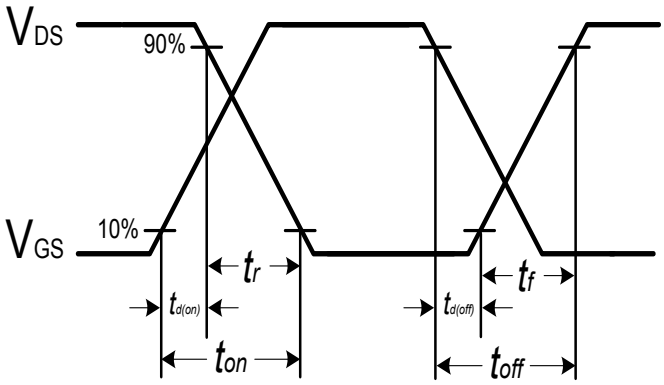


Figure 14. Switching Time Waveform

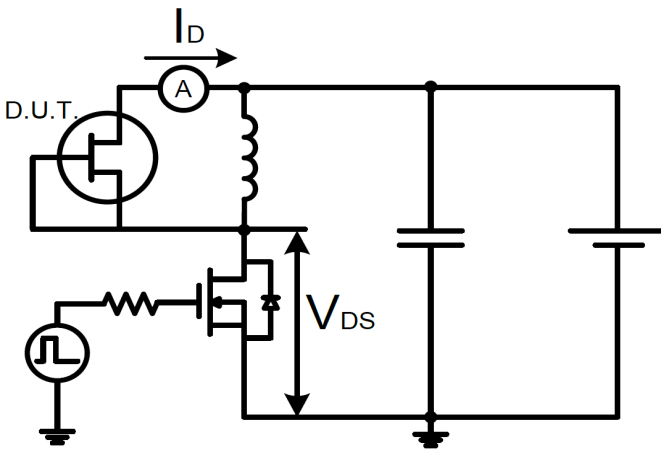


Figure 15. Test Circuit for Reverse Diode Characteristics

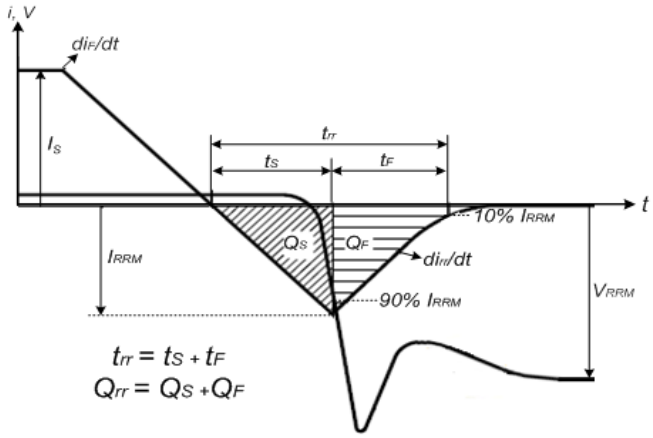
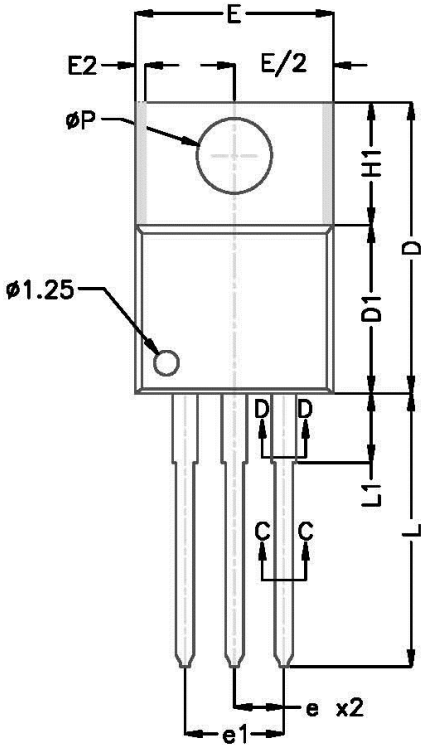


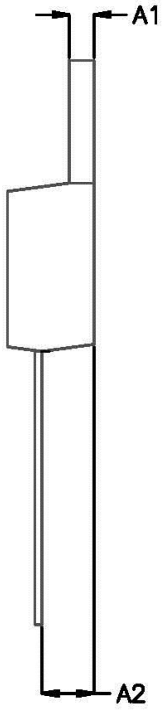
Figure 16. Diode Recovery Waveform

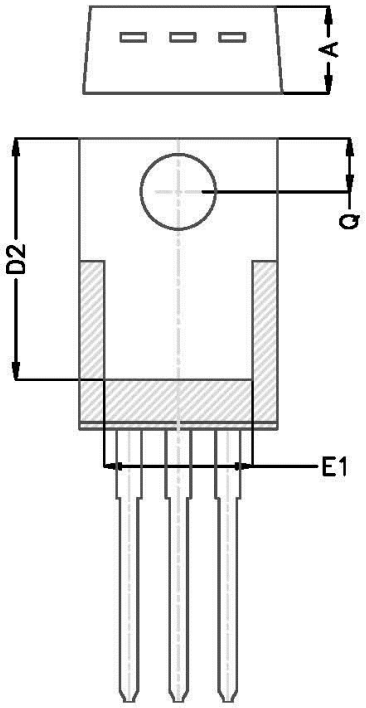
Mechanical

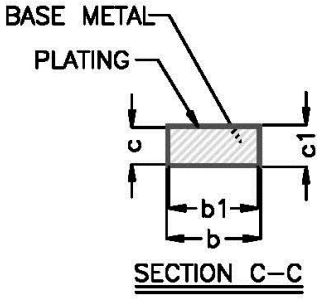
3 Lead TO-220 (PD) Package

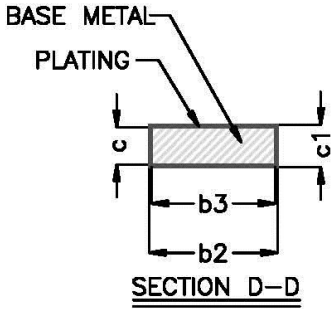
Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Drain











SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	–	2.92	0.080	–	0.115
b	0.38	–	1.01	0.015	–	0.040
b1	0.38	–	0.97	0.015	–	0.038
b2	1.14	–	1.78	0.045	–	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.36	–	0.61	0.014	–	0.024
c1	0.36	0.38	0.56	0.014	0.015	0.022
D	14.22	–	16.51	0.560	–	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	–	12.88	0.460	–	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	–	8.89	0.270	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.86	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	–	–	6.35	–	–	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	–	3.42	0.100	–	0.135

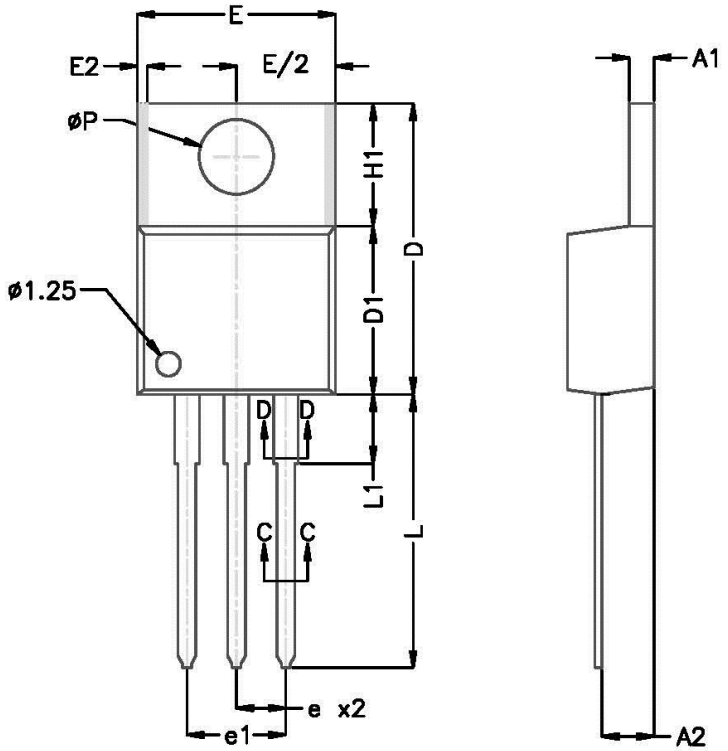
NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO-220AB.

Mechanical

3 Lead TO-220 (PS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source



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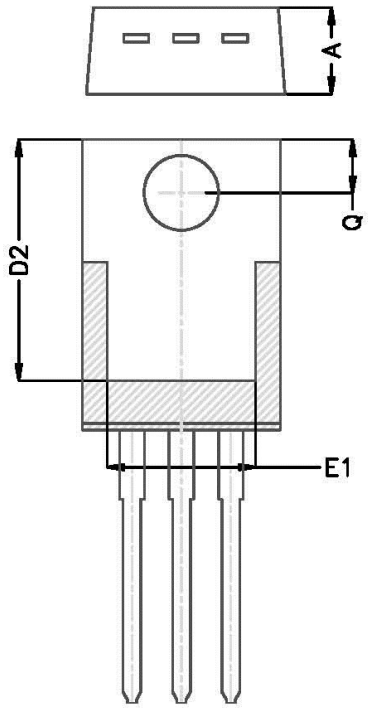
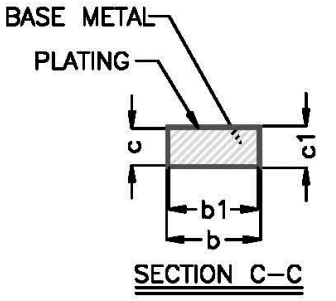
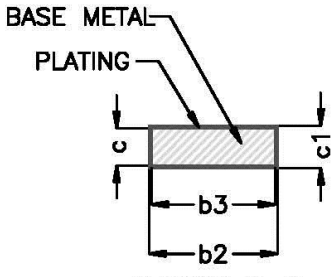
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	–	2.92	0.080	–	0.115
b	0.38	–	1.01	0.015	–	0.040
b1	0.38	–	0.97	0.015	–	0.038
b2	1.14	–	1.78	0.045	–	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.36	–	0.61	0.014	–	0.024
c1	0.36	0.38	0.56	0.014	0.015	0.022
D	14.22	–	16.51	0.560	–	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	–	12.88	0.460	–	0.507
E	9.65	10.19	10.67	0.380	0.401	0.420
E1	6.86	–	8.89	0.270	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.86	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	–	–	6.35	–	–	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	–	3.42	0.100	–	0.135





SECTION C–C



SECTION D–D

NOTES:

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2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO-220AB.

Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs

Evaluation Boards

- TDPS251E0D2-KIT: 250W LLC evaluation platform
- TDPS250E2D2-KIT: 250W all-in-one power supply evaluation platform

Revision History

Version	Date	Change(s)
0	11/14/2016	Release P series datasheet