Application Note:

TDPS500E2C1Totem Pole PFC Evaluation Board

1. Introduction

The Evaluation Board for a bridgeless totem-pole Power-Factor-Correction (PFC) circuit, using Transphorm GaN power HEMTs, is described in this paper. In this board, by using a diode-free GaN power HEMT bridge with low reverse-recovery charge, very-high-efficiency single-phase AC-DC conversion is realized. In this circuit, the performance and efficiency improvement, achieved by use of the GaN HEMTs in the fast-switching leg of the circuit, is further enhanced by use of low resistance MOSFETs in the slow-switching leg. The evaluation board is shown in Fig. 1.

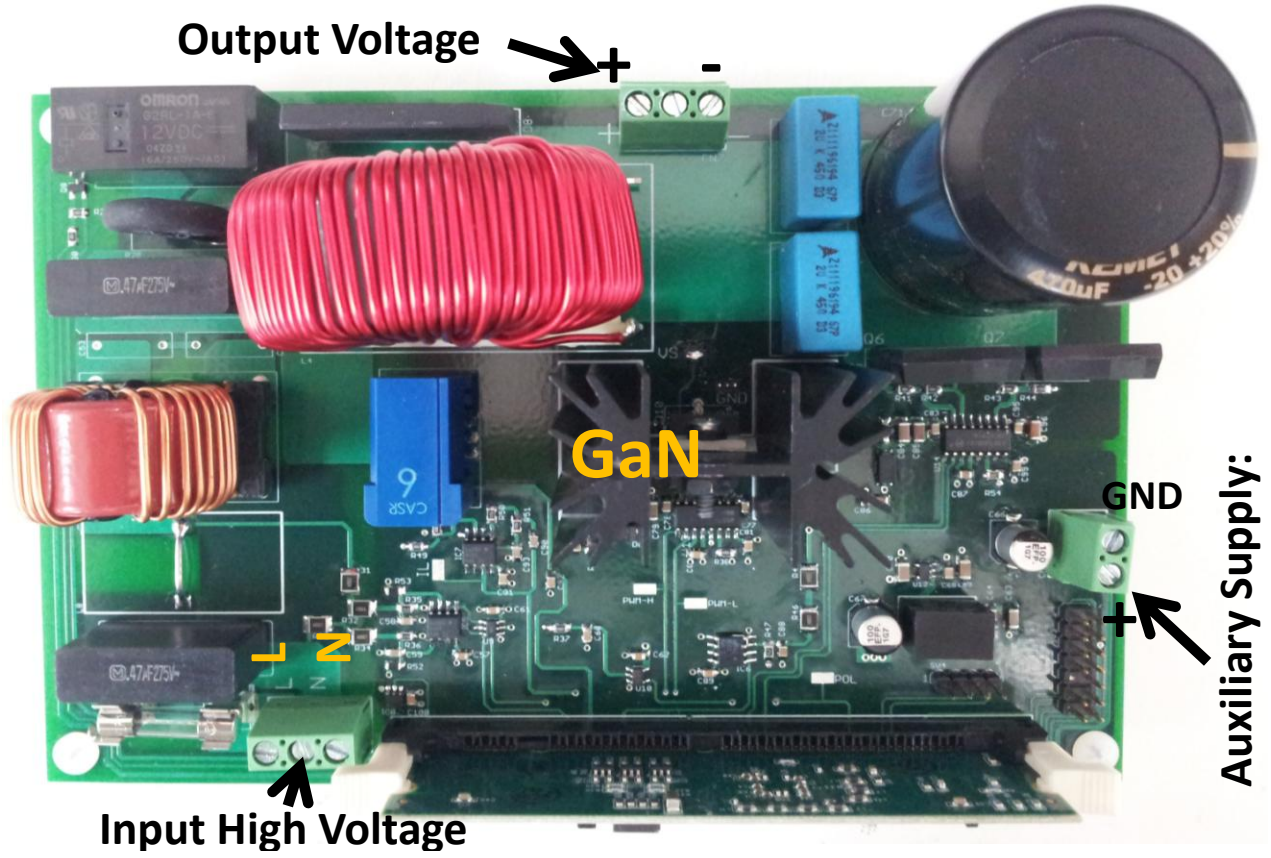


Fig.1 Totem pole PFC Evaluation Board

2. **TDPS500E2C1 Input/output Specifications**:

- Input voltage:between100 Vac to 250 Vac;
- Input current: 4.5 A (rms) (500 W at 115 Vac, 1000 W at 230 Vac);
- Output: 390 Vdc ± 5 V;
- PWM Frequency: 50 kHz;
- Auxiliary Supply (12 Vdc for bias voltage).

3. Circuit Description for Totem pole bridgeless PFC based on GaN HEMT

The totem-pole bridgeless topology is shown in Fig. 2. As shown in Fig. 2(a), two GaN HEMT and two diodes are used for the line rectification, while in Fig. 2(b),the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs to eliminate diode drop and improve the efficiency. The topology in Fig. 2(b) looks the same as any single-phase converter; however, it is controlled as the original totem-pole bridgeless PFC shown in Fig. 2(a); therefore, it is labeled the totem-pole bridgeless PFC with MOSFET for line rectification. Further information and discussion on the performance and the characteristics of bridgeless PFC circuit is provided in [1].

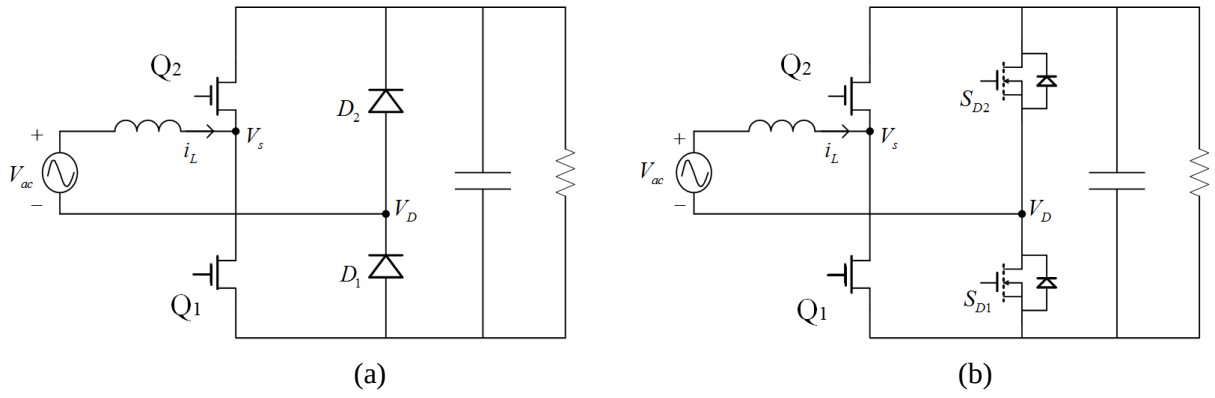


Fig.2 Totem-pole bridgeless PFC boost converter based on GaN HEMT (a) Diode for line rectification (b) MOSFET for line rectification

The large reverse recovery charge (Qrr) of existing silicon MOSFETs makes CCM operation of a silicon totem-pole bridgeless PFC impractical, and reduces the total efficiency. The industry's 1st qualified 600-V GaN HEMTs made on low-cost Si substrates has been announced by Transphorm Inc. These 1st-generation GaN power devices show a low on-resistance of 0.15 ohm typical and are capable of reverse conduction during dead time with a low Qrr of 54 nC, 20 times lower than state-of-the-art Si counterpart as seen in Fig.3. These features can remarkably expand operation space of a hard-switched bridge.

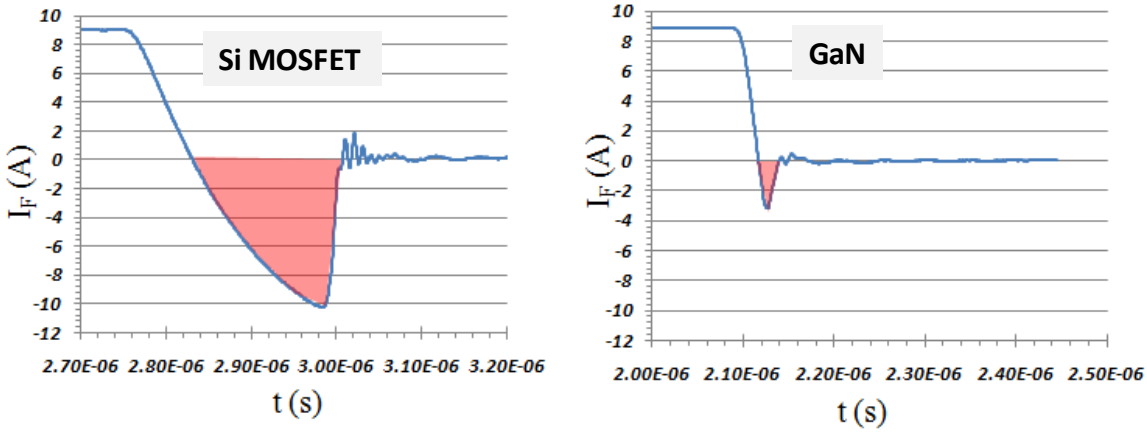


Fig.3 Reverse recovery charge test result for a Si MOSFET and a GaN HEMT with similar on resistance, showing a 20x reduction of Qrr for GaN.

Table 1 gives a comparison of CoolMOS and GaN HEMT. The low Qrr will help reducing excessive spikes during start-up process in a LLC dc-dc converter.

Table 1: Comparison of GaN HEMT with equivalent CoolMOS IPP60R190C6

Parameter	TPH3006PD/TPH3006PS	IPP60R190C6
ID	17A (continuous)	20.2A (for D=0.75)
Ron	150mΩ	170mΩ
Qg	6.2nC	63nC
Eoss(400V)	5.1uJ	5.2uJ
Qrr	54nC	6.9uC

A GaN HEMT totem pole PFC in CCM mode focusing on minimizing conduction losses was designed with a simplified schematic shown in Fig.4(a). It consists of a pair of fast GaN HEMT switches (Q_1& Q_2) operating at a high pulse-width-modulation (PWM) frequency and a pair of slow but very-low resistance MOSFETs (S_1 & S_2) operating at a much slower line frequency (60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S_1 & S_2 is that of a synchronized rectifier as illustrated in Fig.4(b) and Fig.4(c). During positive ac cycle, S_1 is on and S_2 off, forcing the ac neutral line tied to the negative terminal of the dc output. The opposite applies for the negative cycle.

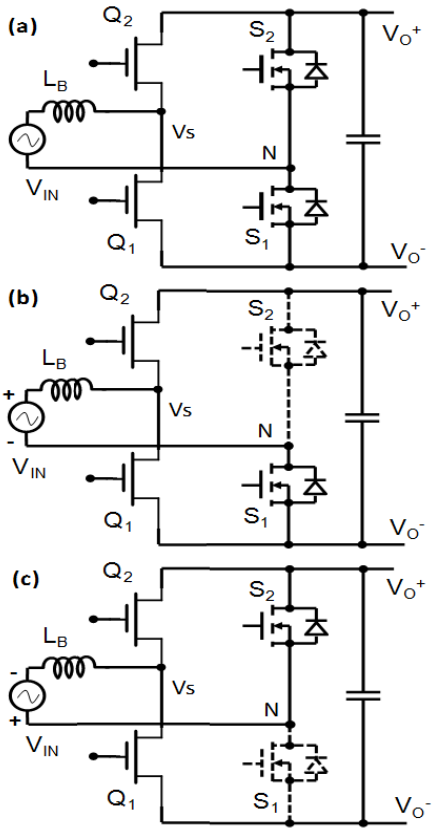


Fig. 4.GaN totem pole PFC (a) simplified schematics and illustration during (b) positive ac cycle and (c) negative ac cycle.

In either ac polarity, the two GaN HEMTs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (L_B) and another transistor as a slave switch to release energy to the dc output. The roles of the two GaN devices interchange when the polarity of the ac input changes; therefore, each transistor must be able to perform both master and slave functions. To avoid shoot through, a dead time is built in between two switching events during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor has to function as a flyback diode for the inductor current to flow during dead time. The diode current however, has to quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem pole PFC which previously led to abnormal spikes, instability and associated high switching losses due to the high Qrr of the body diode in modern high-voltage Si MOSFETs. The low Qrr of the GaN switches allow designers to overcome this barrier. As seen in Fig. 5, inductive tests at 400-V bus using either low-side or high-side GaN transistor as a master switch show healthy voltage waveforms up to inductor current exceeding 12 A. With a design goal of 1 kW output power in CCM mode at 230V ac input the required inductor current is 6 A. This test conforms a successful totem-pole power block with 2x current overhead.

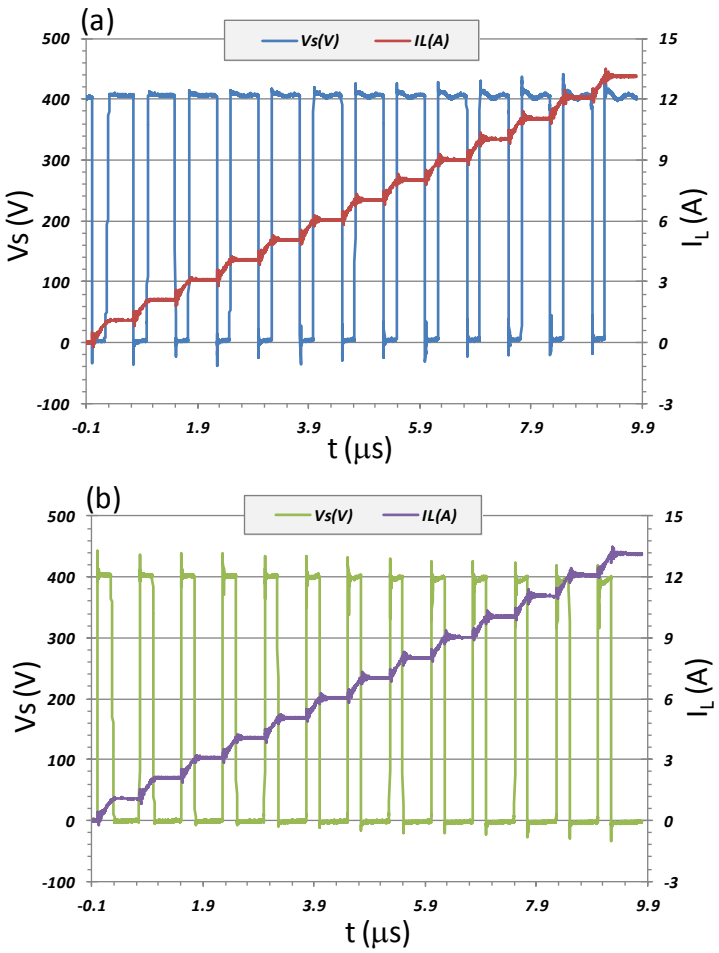


Fig.5Hard-switched waveforms of a pair of GaN HEMT switches when setting a) low side as master device and b) high side as master

One inherent issue in totem-pole bridgeless PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half line to negative half line at the zero-crossing, the duty ratio of switch Q_1 changes abruptly from almost 100% to 0%, and the duty ratio of switch Q_2 changes from 0% to 100%. Due to the slow reverse-recovery of diodes (or body diode of MOSFET), the voltage V_D cannot jump from ground to V_{DC} instantly, a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio. Since the TDPS500E2C1totem-pole bridgeless PFC is designed to run in CCM, the larger inductance actually alleviates the current

spike issue at zero-crossing. A soft-start time for a few switching cycles is enough to handle this problem.

The circuit schematic and bill of materials for totem-pole bridgeless PFC evaluation board are shown in Fig. 6 and Table.2 respectively.

For this evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN HEMT half-bridge is built with TPH3006PS devices by Transphorm, Inc. The slow Si switches are IPA60R099C6600V super junction MOSFETs with 0.1 ohm on-resistance. The inductor is made of a MPP core with inductance of 1.3 mH and a dc resistance 88 mΩ, designed to operate at 50 kHz. Drain-tab and source-tab GaN HEMT packages are used, one on the top and another on the bottom side for the least electrical lengths between these fast switches, hence minimizing power loop inductances. A simple 0.5-A rated high/low side driver IC with 0/10 V as on/off states directly drives each GaN HEMT. 150 MHz DSP controller - TMS320F28335 handles the control algorithm. The voltage and current loop control is similar to conventional boost PFC converter. The feedback signals are dc output voltage (V_O), ac input potentials (V_{ACP} and V_{ACN}) and inductor current (I_L). The input voltage polarity and RMS value are determined from V_{ACP} and V_{ACN}. The outer voltage loop output multiplied by $|V_{AC}|$ gives sinusoidal current reference. The current loop gives the proper duty-ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q_1 & Q_2. A soft-start sequence with a duty ratio ramps is employed for a short-period at each ac zero-crossing for better stability.

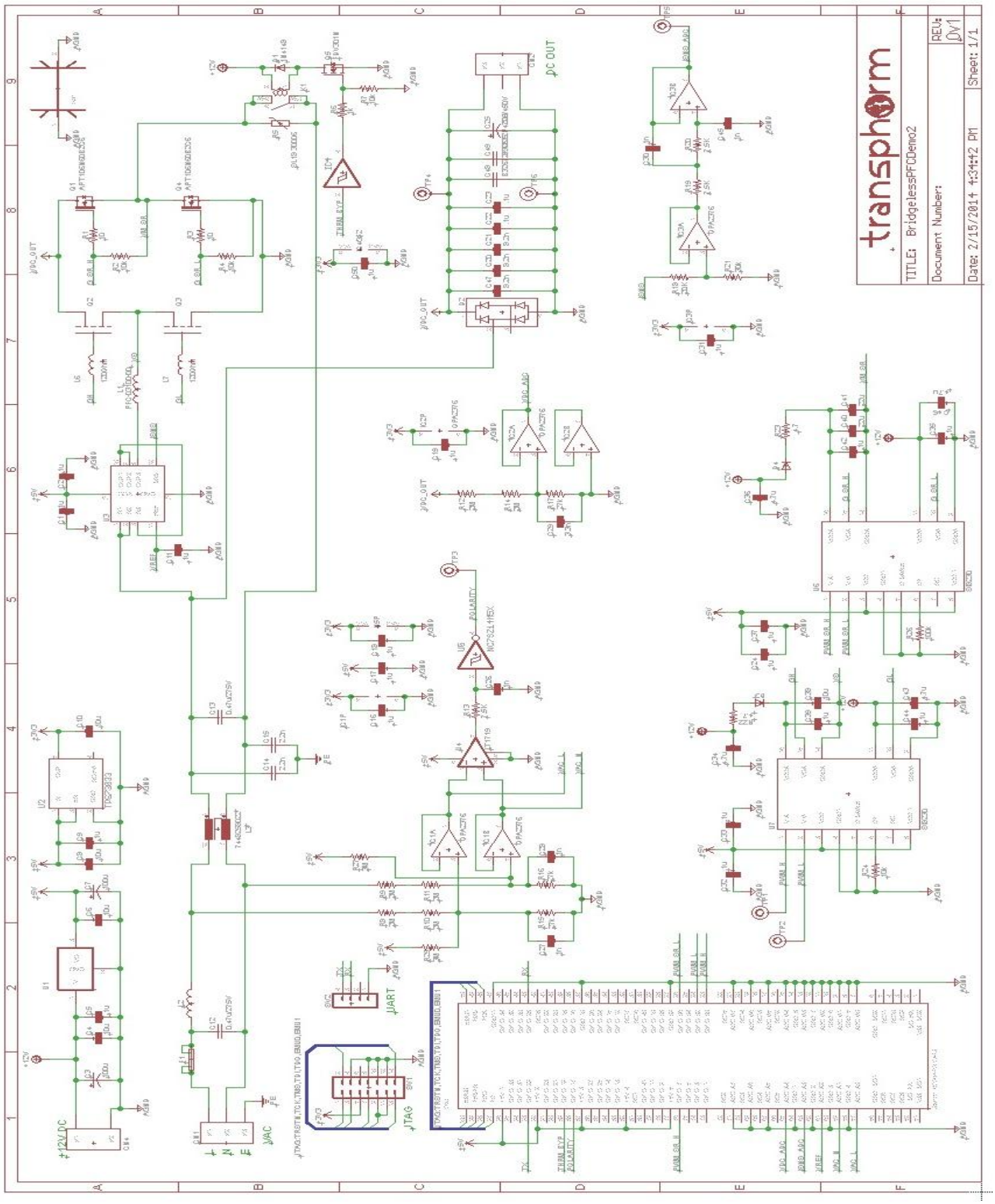


Fig.6. Totem Pole PFC Evaluation Board Schematics

Table.2. Bill of Materials

Qty	Value	Device	Parts	Manf	Manf P/N
1	**DNI**	529802B02500G	HS1	Avid	529802B02500G
1		74AUC1G17DBV	IC4	Texas Instruments	SN74AUC1G17DBVR
1		CASR6-NP_2	U3	LEM USA	CASR 6-NP
2		DIODE-DO-214AC	D3, D4	Micro Commercial	ES1J-LTP
1		FCI-20020316-2P	CN4	FCI	20020316-H021B01LF
2		FCI_20020316-3P	CN1, CN2	FCI	20020316-H031B01LF
1		G2RL-1A-E	K1	Omron	G2RL-1A-E DC12
1		GBJ2506	D2	Micro Commercial	GBJ2506-BP
1	**DNI**	L_BLPFC1	L2		
1		MA04-1	SV2	3M	961104-6404-AR
1		MA07-2	SV1	FCI	67996-114HLF
1		SHK20L	F1	Little Fuse	52000001009
6	**DNI**	TESTPOINT-KEYSTONE5015	TP1, TP2, TP3, TP4, TP5, TP6	KEYSTONE	5015
2	**DNI**	TPH_TO220VERT_TRI	Q2, Q3	Transphorm	TPH3006PS
1		V7805-500	U1	CUI	7805-500
2	.1u	C-EUC0603	C35, C44	Kemet	C0603C104J3RACTU
16	.1u	C-EUC0805	C2, C5, C9, C11, C16, C17, C18, C19, C24, C31, C32, C33, C37, C39, C42, C50	AVX	08053C104KAT2A
2	.1u	C-EUC1812	C22, C23	Kemet	C1812V104KDRACTU
2	0.47u/275V	ECQ-U2A474ML	C12, C13	Panasonic	ECQ-U2A474ML
2	10	R-US_R0805	R1, R3	Panasonic	ERJ-6GEYJ100V
1	100k	R-US_R0805	R26	Panasonic	RJ-6ENF1003V
2	100u	PANASONICFPV	C3, C7	Panasonic	EEE-FPE101XAP
4	10k	R-US_R0805	R2, R4, R7, R24	Panasonic	ERJ-6ENF1002V

5	10u	C-EUC1206	C4, C6, C8, C10, C38	AVX	12063D106KAT2A
2	120Ohm	L-SMD0603	L6, L7	TDK	MMZ1608Q121B
1	1N4148	DIODE-SOD123	D1	Vishay	1N4148W-E3-18
1	1k	R-US_R0805	R6	Panasonic	ERJ-6ENF1001V
5	1n	C-EUC0805	C26, C27, C28, C30, C45	Yageo	CC0805KRX7R9BB102
1	1u	C-EUC0805	C1	Yageo	CC0805ZRY5V8BB105
2	2.2n	PHE850YCAP	C14, C15	Kemet	PHE850EA4220MA01 R17
1	20K	R-US_R0805	R18	Panasonic	ERJ-6ENF2002V
2	22u	C-EUC1206	C40, C41	AVX	12103D226KAT2A
3	27k	R-US_R0805	R15, R16, R17	Panasonic	ERJ-6ENF2702V
6	2M	R-US_R1210	R8, R9, R10, R11, R12, R14	Rohm	KTR25JZPF2004
1	3.3n	C-EUC0805	C29	Kemet	C0805C332K5RACTU
1	30k	R-US_R0805	R21	Panasonic	ERJ-6ENF3002V
2	3M	R-US_R0805	R25, R27	Panasonic	ERJ-6GEYJ305V
2	4.7	R-US_R1206	R22, R23	Panasonic	ERJ-8RQF4R7V
4	4.7u	C-EUC1206	C34, C36, C43, C46	Kemet	C0805C475K4PACTU
1	**DNI**	ALC10A471DF450 _ 470u/450V	C25	Kemet	ALC10A471DF450
3	7.5K	R-US_R0805	R13, R19, R20	Panasonic	ERJ-6ENF7501V
1	**DNI**	WURTHER_7448258022	L3	Wurth	7448258022
3	8.2n	C-EUC1206	C20, C21, C47	TDK	C3216C0G2J822J160 AA
2	APT106N 60B2C6	STH60N10W	Q1, Q4	MicroSemi	APT106N60B2C6
2	B32672P 4225	B32672P4225	C48, C49	Epcos	B32672P4225K
1	**DNI**	DIM100_TICONTROLCARD	CN3		
1	FDV301 N	BSS138-7-F	Q5	Fairchild	FDV301N
1	LT1719	LT1719	U4	Linear Technology	LT1719CS6#TRMPBF
1	NC7SZ14 M5X	NC7SZ14M5X	U5	Fairchild	NC7SZ14M5X
3	OPA2376	AD826R	IC1, IC2, IC3	Texas Instruments	OPA2376AIDR
1	**DNI**	PFC-03100-00	L1	Precision	PFC-03200-00

1	SI8230	SI8230	U7	Silicon Labs	SI8230BB-B-IS1
1	SI8233	SI8233	U6	Silicon Labs	SI8233BB-C-IS1
1	SL18 30006	SL18_30006	R5	Ametherm	SL18 30006
1	TPS73033	TPS73033	U2	Texas Instruments	TPS73033DBVR

While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the TransphormGaN HEMT will switch at dV/dt of 100V/ns or higher to enable the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown below, in Fig. 7-9, the recommended layout keeps a minimum gate drive loop; it also keeps the traces between the switching nodes very short, with the shortest practical return trace to power bus and ground. As the power ground plane provides a large cross sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the HEMT to avoid any possible ground loop.

Note that the Transphorm GaN HEMTs in TO220 package has pin out configured as G-S-D, instead of traditional MOSFET's G-D-S arrangement. The configuration is designed with thorough consideration to minimize the Gate-Source driving loop to reduce parasitic inductance, as well as to separate the driving loop (Gate-Source) and power loop (Drain-Source) to minimize noise. For further information, different layers of TDPS500E2C1design are shown in Fig. 8-10.

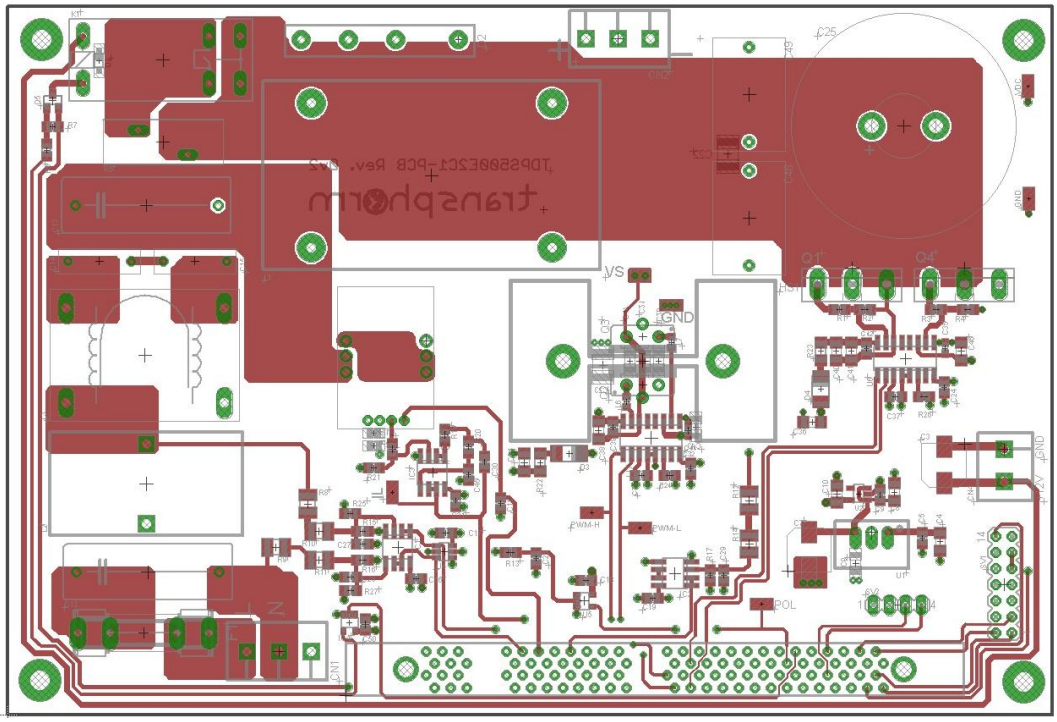


Fig. 7. Totem Pole PFC Evaluation Board Layout, Top Layer

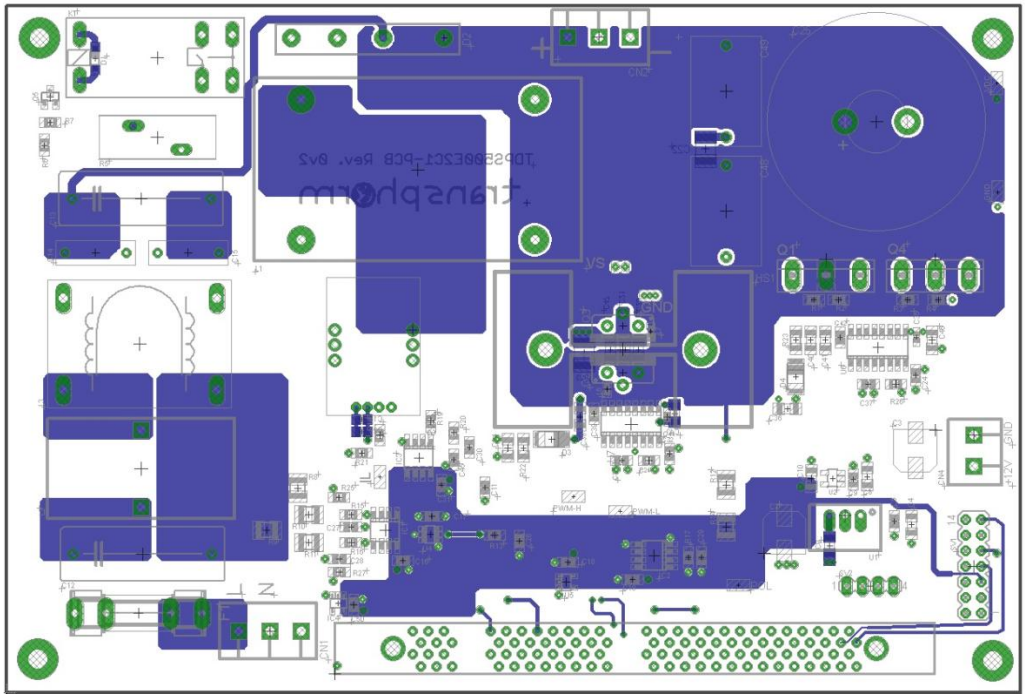


Fig. 8. Totem Pole PFC Evaluation Board Layout, Bottom Layer

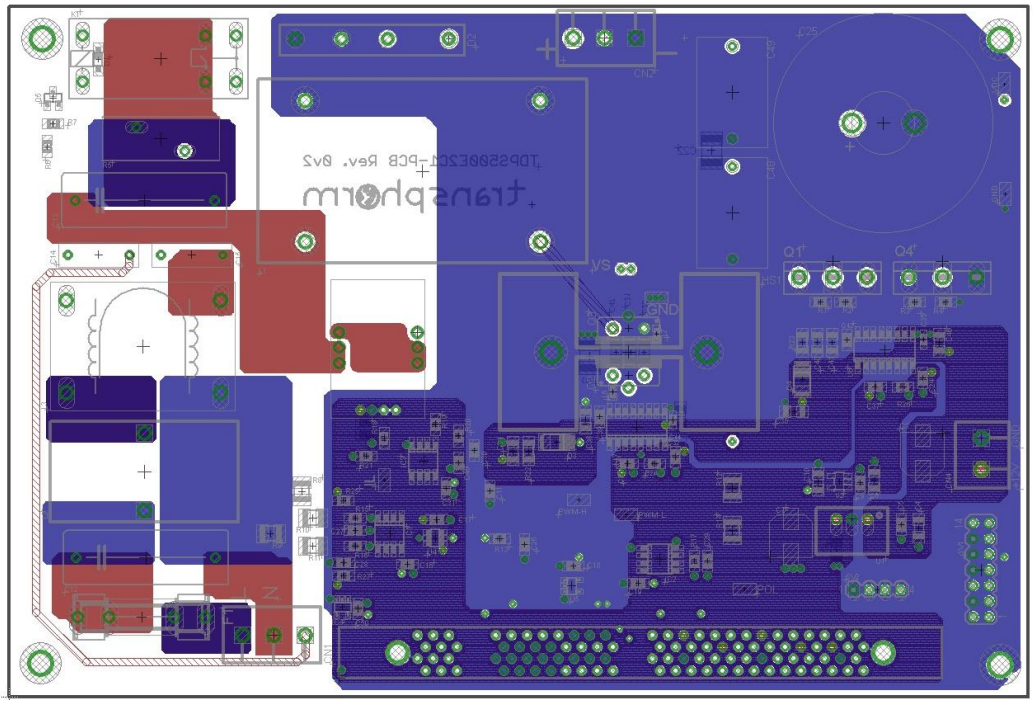


Fig. 9. Totem Pole PFC Evaluation Board Layout, Middle Layers

Startup sequence:

See the warning and procedure at page 18:

1) Connect a load; the load should be resistive.

The requirement for the resistive load:

- At 115 Vac input: ≥ 50 W and ≤ 500 W
- At 230 Vac input: ≥ 100 W and ≤ 1000 W

2) Connect the 12 Vdc auxiliary supply (a lab bench level power supply);
3) With power off, Connect the high-voltage AC power input to the corresponding marking on the PCB;

4) Place a cooling fan facing the GaN HEMTs heat sink (provide a minimum of 30 CFM air flow);
5) Enable 12 Vdc bias by turn on the bench supply;
6) Turn on the cooling fan;
7) Turn on the AC power input (100 Vac to 250 Vac).

Turn off sequences:

1) Switch off the high-voltage AC power input;
2) Power off dc bias;
3) Turn off the fan.

Fig.10shows the converter start-up, CH3 shows the DC bus voltage rapidly rising with simple rectification at the beginning and then ramping up to 400V under control, while the inductor current is kept under 1A during the start-up process. Fig.11and Fig.12show experimental waveforms under 1KW full load. In Figure 11(a), voltage V_D is either 0 V or 400 V according to the input phase. Figure 11(b) shows the PFC functionality in an isolated oscilloscope. The power factor is 0.9998 according to power analyzer reading.

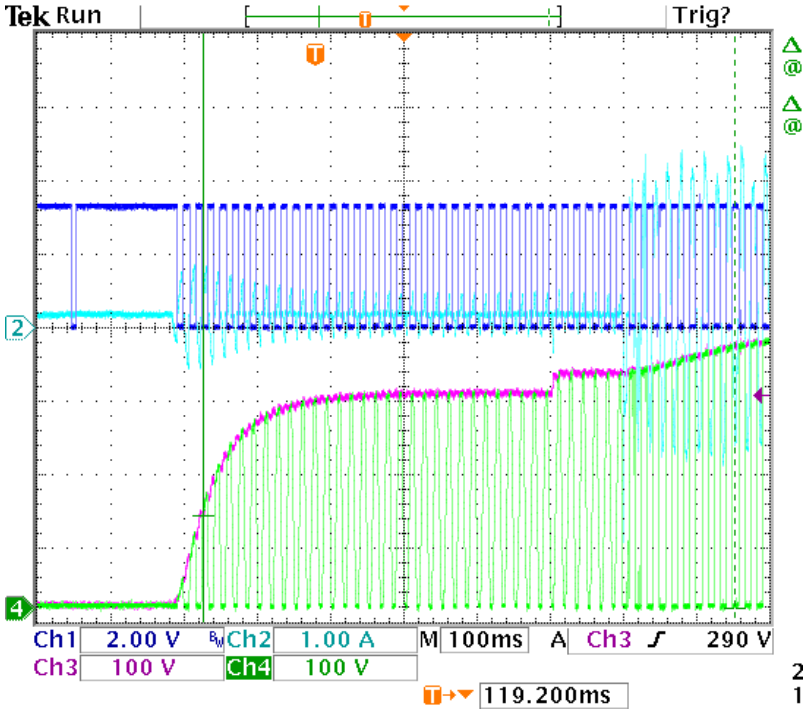
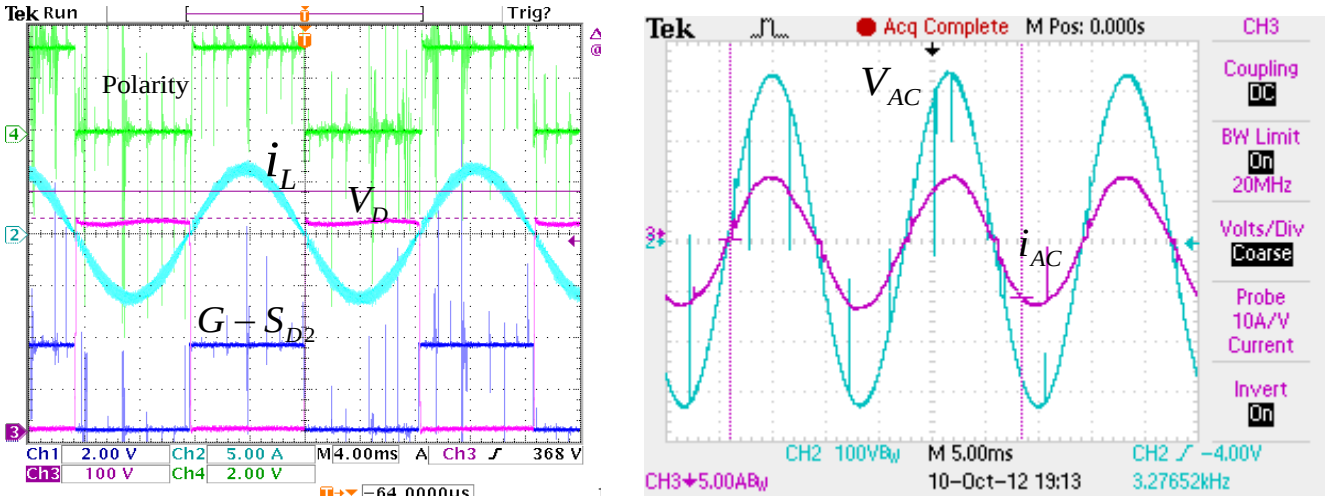


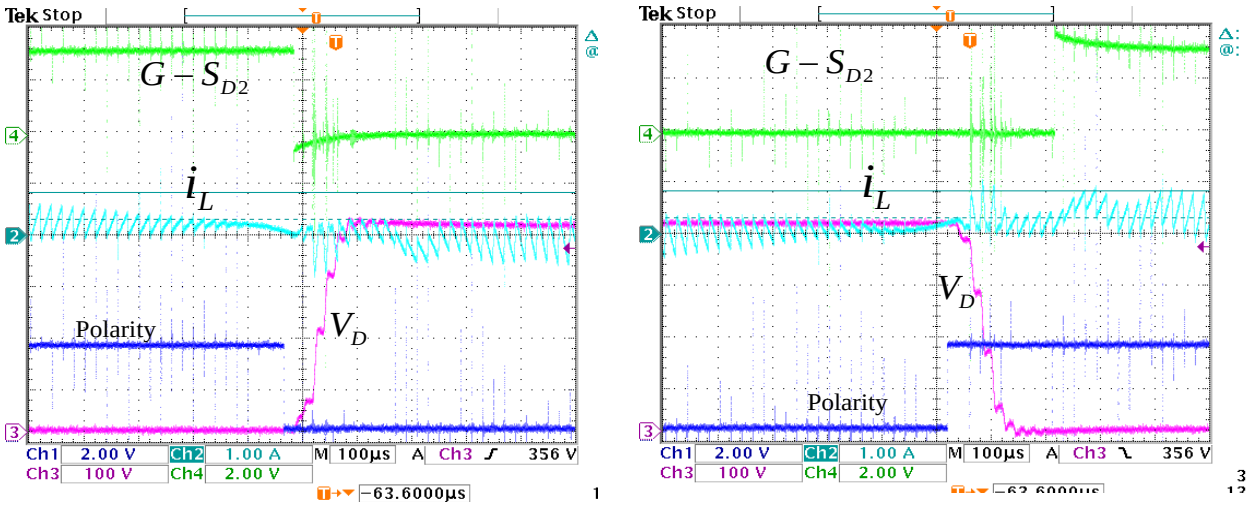
Fig.10 Start-up of the totem-pole bridgeless PFC prototypes (CH1: AC Polarity, CH2: inductor current, CH3: Vo, CH4: Vd)



(a) (b)

Fig.11 Waveform of the active switch version of the totem-pole bridgeless PFC at full load 1KW; (a) CH1: PWM Gate signal for S_{D2}; CH2: I_L waveform (5A/division); CH3: $V_D$waveform(100V/division); CH4: AC input polarity signal(b) CH2: Input AC voltage(100V/division); CH3: input AC current (5A/division)

Fig.12 shows the transitions between two half cycles. In Fig.12(a), the AC line enters the negative half. Soft-start gradually increases voltage V_D from 0V to 400 V. While in Fig. 12(b), V_D decreases from 400 V to 0 V.



(a) (b)

Fig. 12 Zero-crossing transitional waveform (a) from positive to negative half cycle (b) from negative to positive half cycleCH1: AC input polarity; CH2: I_L waveform; CH3: V_D waveform; CH4: PWM gate for S_{D2}

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at 115 Vac or 230 Vac input and 400 Vdc output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this Totem Pole PFC board are shown in Fig. 13 and Fig. 14. The extremely high efficiency of >99% at 230Vac input, and >98% at 115V ac input is the highest among PFC designs with similar PWM frequency; this high efficiency will enable customers to reach peak system efficiency to meet and exceed Titanium standards.

Table 3. The power and efficiency result for Totem Pole PFC board at115Vac input

Pin (W)	Pout (W)	Ploss (W)	Eff (%)
74.83	72.67	2.16	97.107
113.92	111.36	2.56	97.755
173.81	170.47	3.34	98.078
219.02	214.86	4.16	98.101
290.9	285.07	5.83	98.012
405.6	396.23	9.37	97.683
512.2	498	14.2	97.23

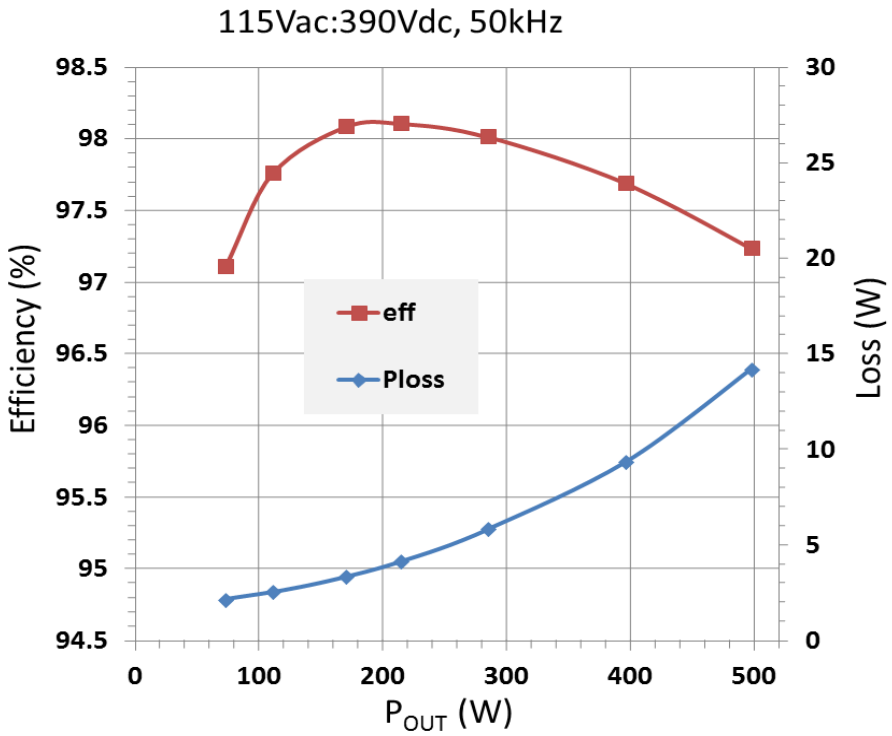


Fig. 13. The efficiency result for Totem Pole PFC board at 115 Vac input

Table 4. The power and efficiency result for Totem Pole PFC board at 230Vac input

Pin (W)	Pout (W)	Ploss (W)	Eff (%)
113.21	111.38	1.83	98.38
172.54	170.34	2.2	98.728
276.37	273.56	2.81	98.982
388.36	384.67	3.69	99.05
447.92	443.7	4.22	99.048
563.7	558.2	5.5	99.015
676.2	669.1	7.1	98.951
842	831.8	10.2	98.792
1000.1	986.5	13.6	98.645

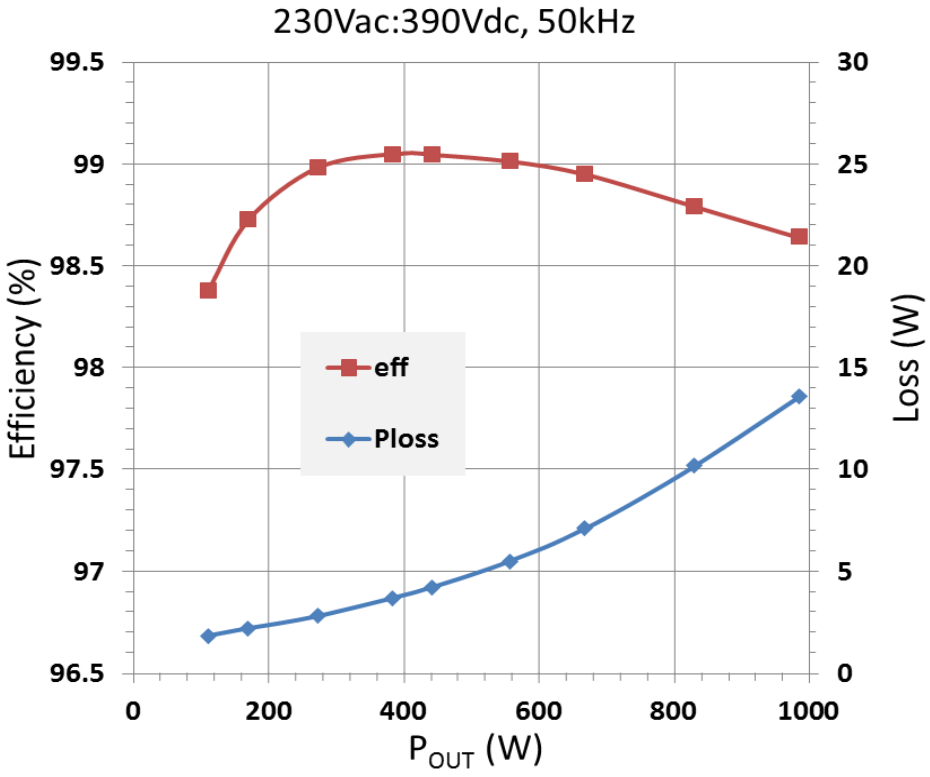


Fig. 14. The efficiency result for Totem Pole PFC board at 230 Vac input

⚠Warning:

This demo board is intended to demonstrate GaN HEMT technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. An isolated AC source should be used as input; an isolated lab bench grade power supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.

2. Use a resistor load only. The Totem-pole PFC kit also has a minimum load requirement. It DOES NOT work at no load.

3. The demo board is not intended to handle large load steps. DO NOT apply a large step in the load when it is running.

(Load Step must <450 W, which is from 10% load to 100% load of 500 W. The demo board can run up to 1 KW at high line, but the DC bus cap (470 uF) is not big enough to handle more than 450 W step load at high line. Unload more than 450 W at high line could trigger over-voltage protection in the DSP program.)

4. The demo board is intended to run for short time. Do NOT run it for a very long time (more than 8 hours).

5. DO NOT manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.

6. The auxiliary Vcc supply must be 12 V. The demo board will not work under, for example 10 V or 15V Vcc.

7. DO NOT touch any part of the demo board when it is running.

8. Use the TEST MODE control card to verify the functionality of a newly received demo board before applying high AC voltage directly. This will uncover any defects which may have occurred in shipping or any test-setup errors. Refer to "TEST MODE PROCEDURE" in this application note.

9. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.

10. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.

TEST MODE PROCEDURE:

1. Install the test mode control card.

2. Turn on the 12 V bias power supply. Take a look the control card to make sure it is in test mode one. The test mode control card is F28027 DSP, which is a smaller package. All three LED should be ON and not blinking. (In normal operation mode the control card has a blinking LED, and it is the F28335 DSP with a bigger package)

3. Connect the isolated AC source; set the protection current limit to 1A. Connect a load resistor of about 200 Ohms.

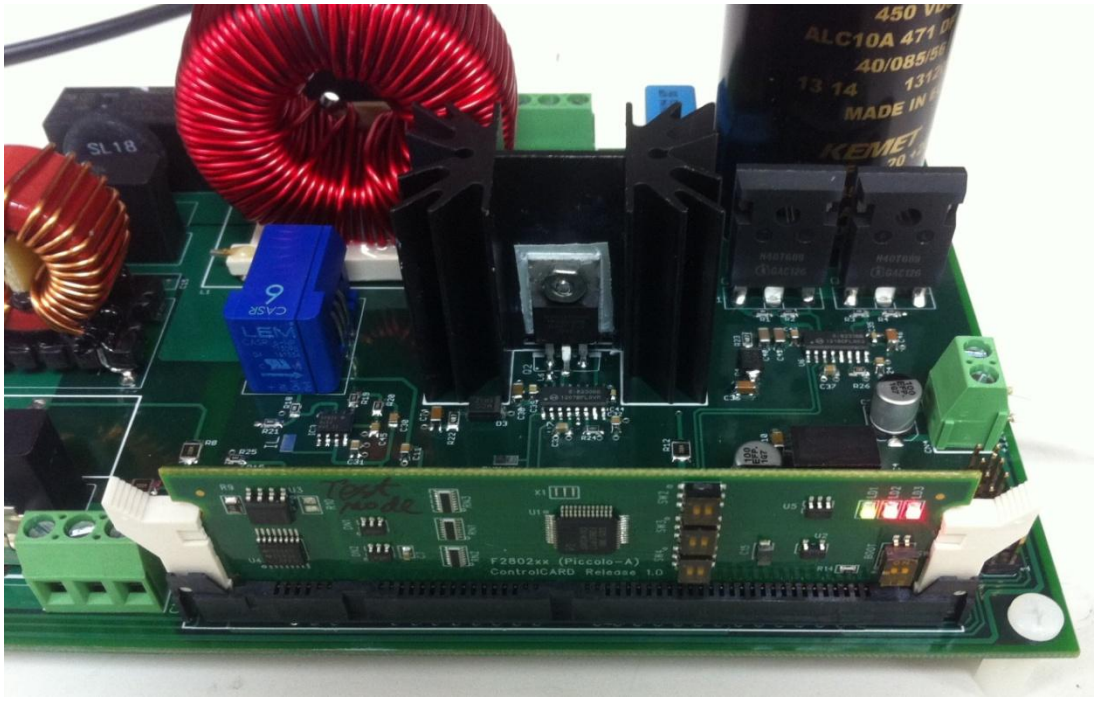
(Please notice that 200 Ohm load for 390 V DC bus of normal operation is around 800 W load, but it is very small load here because the DC bus for this test is no more than 60 V. Any load between 400 Ohm to 160 Ohm is fine for this test, that is 400 W to 1000 W load for 390 V DC bus of normal operation. Please DO NOT use light load such as 50 W/100 W for 390 V DC bus for this test at low voltage.)

4. Connect Probes: Probe the Vg of the LS sync-rec MOSFET; the line frequency switching node of the sync-rec MOSFET; and the input current.

5. Slowly turn-on the AC source from 0 V. The demo board first works as a diode-bridge rectifier. The DSP will close the loop when input reaches around 22 Vac.

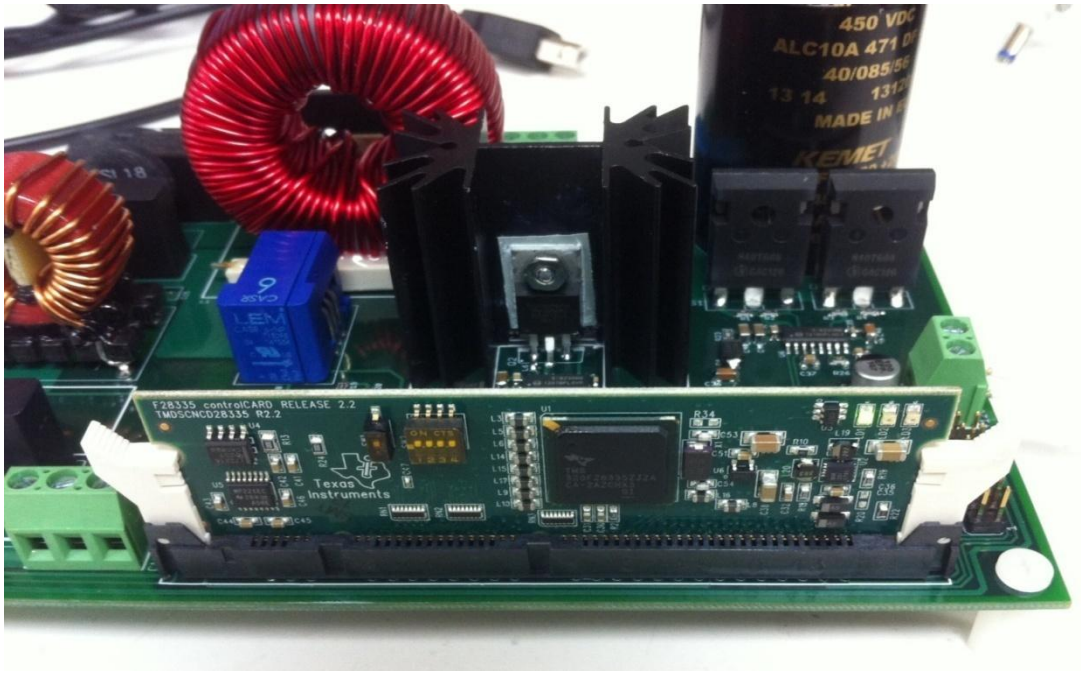
6. Further increase the AC source up to 35 Vac, the sync-rec MOSFET will be also turned on in this case.

Test mode control cards:



Picture for F28027 Control card on Totem pole for Test at Low Voltage (0-35 Vac) only.

All 3 LED are ON.



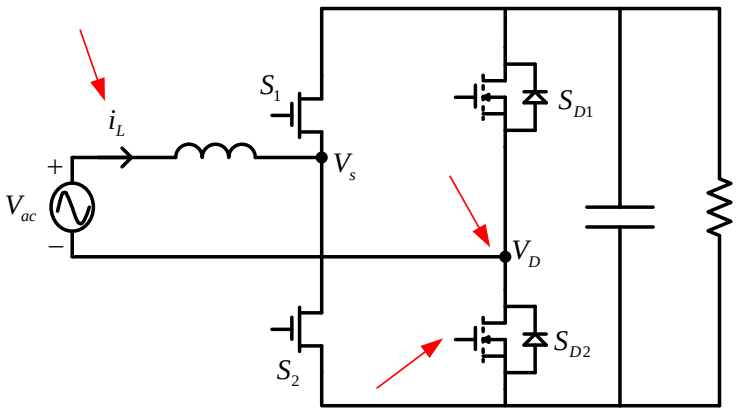
Picture of Totem Pole with the F28335 control card for Normal operation.

First Green LED is always ON indicating DSP Power;

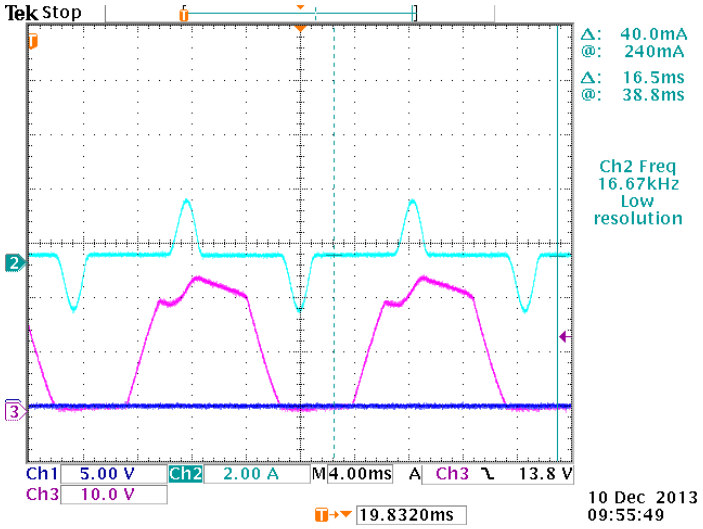
The second LED is blinking indicating that the DSP is running;

The Third LED will light when the DSP program stops due to fault protection (over voltage or current).

Probing Points:

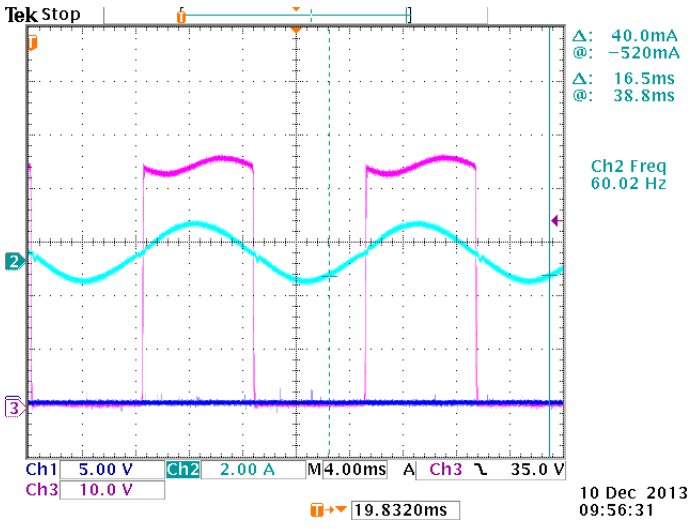


Waveform as a diode bridge in between 0 Vac to 22 Vac:



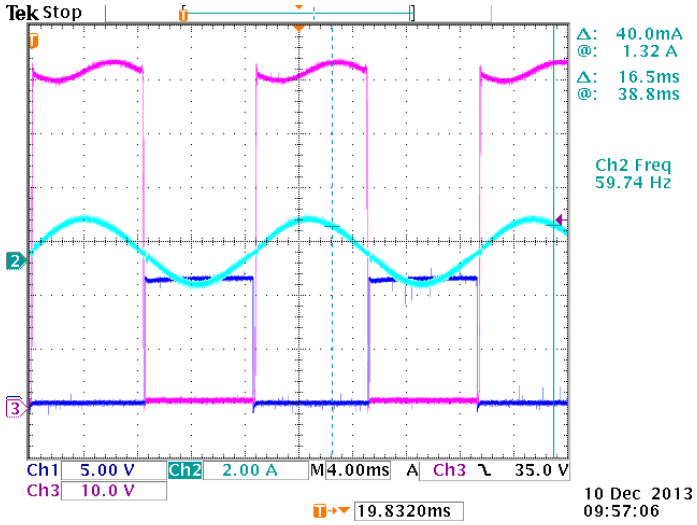
(Ch2: Iin; Ch3: Vd; Ch4: Vg)

Waveform as a closed loop PFC without MOSFET sync-rec (between 22 Vac to 32 Vac):



(Ch2: Iin; Ch3: Vd; Ch4: Vg)

Waveform as closed loop PFC with MOSFET sync-rec (more than 32 Vac):



(Ch2: Iin; Ch3: Vd; Ch4: Vg)

If the demo board works as described here, removed the control card for test and use the F28335 control card for normal operation. The control card for test mode should only be used to test the setup or functionality of the demo board at low voltage as specified here.

If you did not see a proper waveform as in the pictures, or the AC source is in over-current mode. Please do not use the demo kit. Contact a representative of Transphorm for additional support.

REFERENCE:

[1]. Liang Zhou, Yi-Feng Wu and Umesh Mishra, "True Bridgeless Totem-pole PFC based on GaN HEMTs", PCIM Europe 2013, 14-16 May, 2013, pp.1017-1022.

[2]. L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp. 1381-1390, May 2008.