ZCC5145

High Efficiency Low Iq, 0.6A, 45V 1.2MHz Step-Down Converter

1 DESCRIPTION

The ZCC5145 is a monolithic, step-down, switch- mode converter with a built-in power MOSFET. It achieves a 0.6A peak-output current over a wide input supply range with excellent load and line regulation. Current-mode operation provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The ZCC5145 requires a minimal number of readily-available external components. The ZCC5145 is available in a TSOT23-6 package.

2 FEATURES

- 0.6A Peak Output Current
- 0.6Ω Internal Power MOSFET
- Capable to Start Up with Big Output Capacitor
- Stable with Low-ESR Ceramic Output Capacitors
- Up to 94% Efficiency
- Fixed 1.2MHz Frequency
- Cycle-by-Cycle Over-Current Protection
- Wide 4.2V-to-45V Operating Input Range
- Output Adjustable from 4.5V to 0.94xV_{IN}
- Available in a SOT23-6 Package

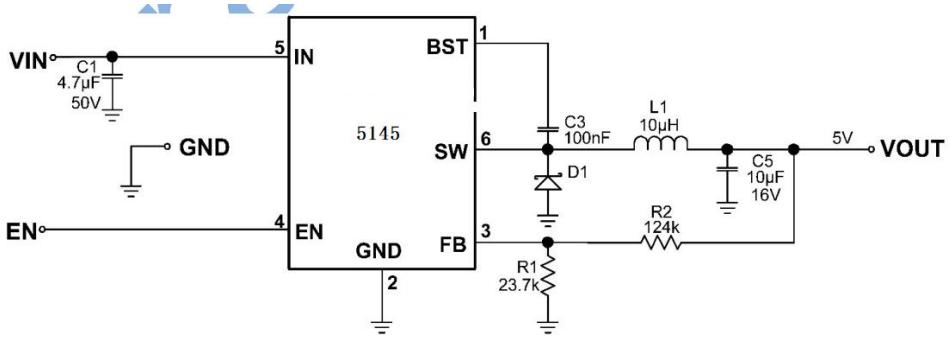
Part Number	Package
ZCC5145	SOT23-6

3 APPLICATIONS

- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators

All ZCC-Chinaparts are lead-free and adhere to the RoHS directive.

4 TYPICAL APPLICATION



5 PIN description

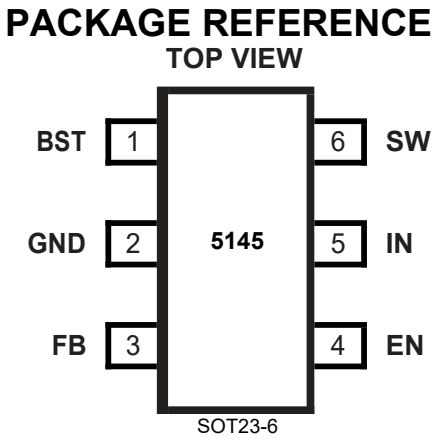


Figure 1 Packge Pinout

PIN Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BST	I	Bootstrap cap. Connect C_{BOOT} capacitor between BST and SW. Connect a 22nF effective capacitor between SW and BST pins to form a floating supply across the power switch driver.
2	GND	GND	System ground pin.
3	FB	I	Voltage feedback input. The control loop will regulation this pin to 0.8V, Set feedback voltage divider ratio with $V_{OUT} = V_{FB}(1 + (R1 / R2))$.
4	EN	I	Buck enable. Pull to GND to disable the device and pull high to enable the device.
5	VIN	PWR	Power input voltage pin,4.5-V to 42-V normal operating range.
6	SW	O	Buck switch output, connect 10uH inductor.

6 Specifications

6.1 Absolute Maximum RatingsII

See (1)

		MIN	MAX	UNIT
Voltage range at terminals	IN, SW, EN	-0.3	60	V
Voltage range at terminals	BST	-0.3	SW+6	V
Voltage range at terminals	FB	-0.3	6	V
Operating junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) ESD stress voltage(1)	±2000	V
		Charged device model (CDM) ESD stress voltage	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VIN	Input voltage range	4.2		45	V
VOUT	Buck converter output voltage range	1.8		0.9* VIN	V
L	Effective inductance range	2.2	10		μH
C_{IN}	Input effective capacitance range	2.2	4.7		μF
C_{OUT}	Output effective capacitance range	4.7	10	100	μF
T_J	Operating junction temperature	-40		125	°C

THERMAL METRIC		ZCC5145 TSOT23-6	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)(2)	220	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	110	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				45	V
V_{UVLO}	Under voltage lockout threshold	V_{SYSIN} rising		4.2		V
		V_{SYSIN} falling		3.5		V
V_{IN_HYS}	VIN UVLO hysteresis			0.7		V
V_{OUT}	Vset=5V	V_{IN}=12V	4.85	5	5.15	V
F_{SW}	Buck switch frequency	V_{IN}=12V, EN = 1	1	1.2	1.4	MHz
F_{SW_FB}	Buck switch fold back frequency	V_{IN}=12V, EN = 1, FB=0.1V		300		KHz
R_{hs}	High side FET on resistor	V_{SYSIN}=12V		600		mΩ
I_{LIM}	Switch current limit	V_{OUT} ≥ 3V, boost operation	0.9	1.2	1.4	A
Iq	Operation current with no switch	EN= 1, FB = 2V		150		uA
D_{MAX}	Maximum duty cycle		87	94		%
I_{SW}	SW leakage current	V_{SYSIN}=12V, V_{OUTD} = 3.3V			<1	uA
V_{FB}	FBU feedback voltage		784	800	816	mV
I_{FBU}	FBU leakage current				50	nA
V_{ENH}	EN Threshold, Rising	V_{IN} ≤ 1.5V		1.4		V
V_{ENL}	EN Threshold, Rising	V_{IN} > 1.5V		1		V
I_{EN}	EN input current	V_{EN} = 45V		1		uA
I_{EN_LKG}	EN input current	V_{EN} = 5V		1		uA
t_{ON}(min) (1)	Minimum ON-time			50		ns
Tsd	Overtemperature protection			150		°C
Tsd_hyst	Overtemperature hysteresis			30		°C

(1) Minimum ON-time specified by design and simulation.

7 Typical Characteristics

V_{IN}=12V, V_{out}=5V,L=10uH,T_A=25℃ unless otherwise noted.

Figure 1. Efficiency vs Load Current

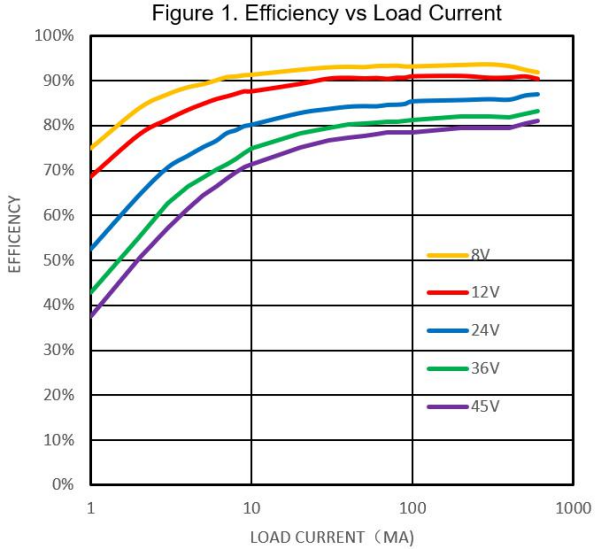


Figure 2. Temperature during operation

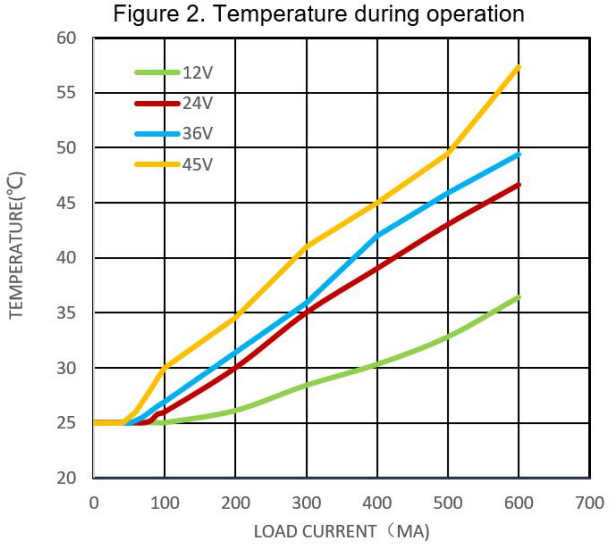


Figure 3. Line Regulation

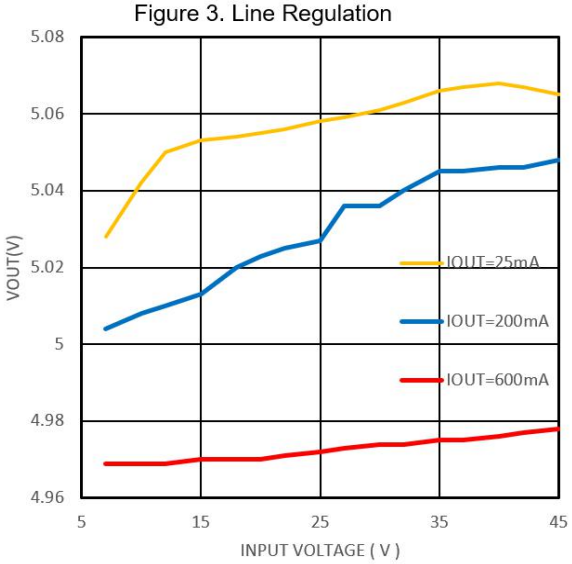
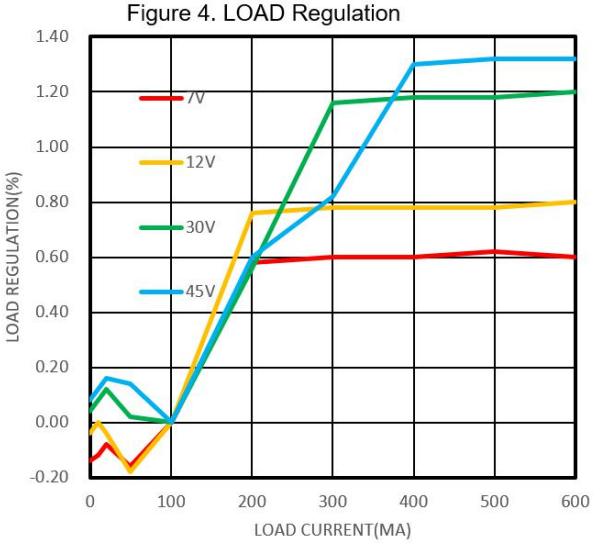


Figure 4. LOAD Regulation



TYPICAL PERFORMANCE CHARACTERISTICS

VIN=12V VOUT=5V, L=10μH, TA=25°C, unless otherwise noted.

Figure 5. Steady State(LOAD=50mA)

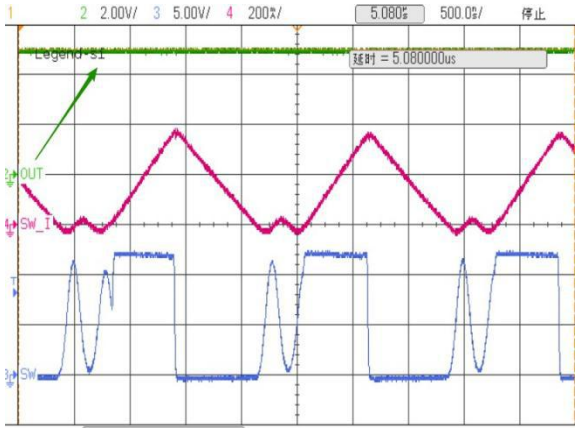


Figure 6. Steady State(LOAD=600mA)

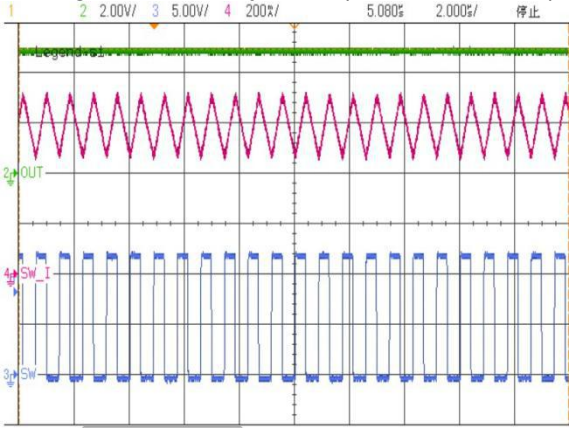


Figure 7. Power ON(LOAD=600mA)

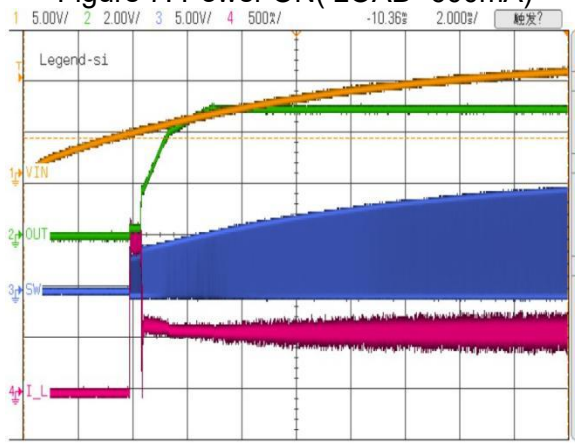


Figure 8. Power OFF(LOAD=600mA)

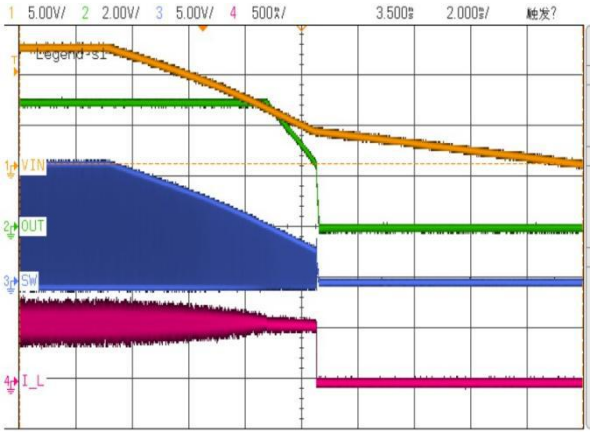


Figure 9. EN ON (LOAD=600mA)

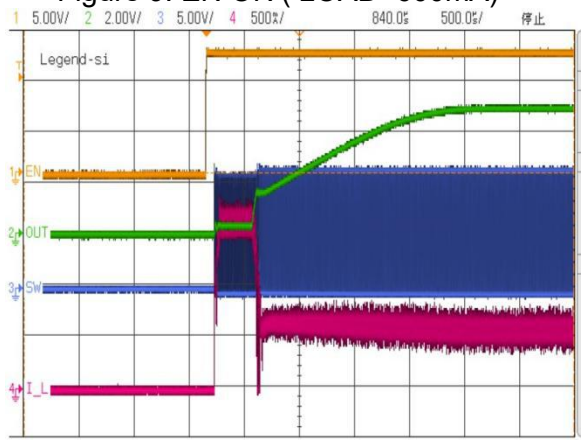
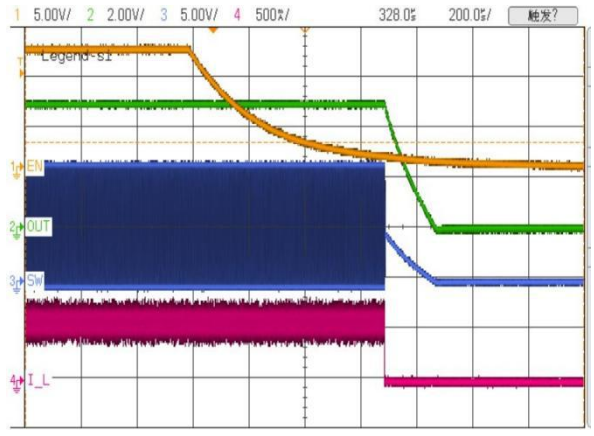


Figure 10. EN OFF (LOAD=600mA)



TYPICAL PERFORMANCE CHARACTERISTICS

VIN=12V VOUT=5V, L=10μH, TA=25°C, unless otherwise noted.

Figure 11. LOAD Transient
LOAD=300mA<->600mA@3A/us

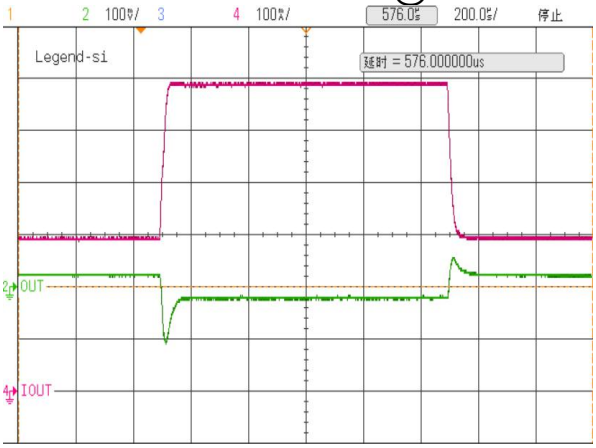


Figure 12. Short Circuit Entry
(LOAD=600mA)

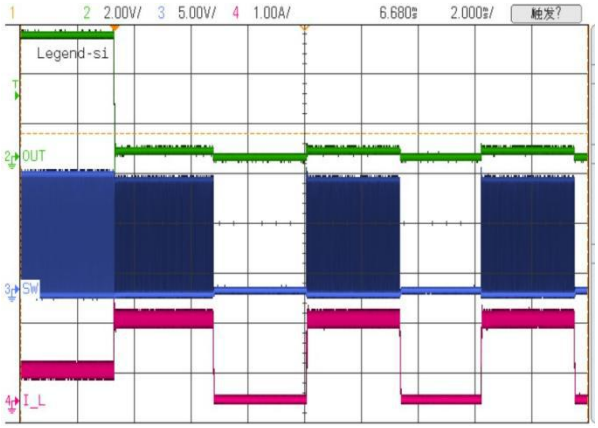
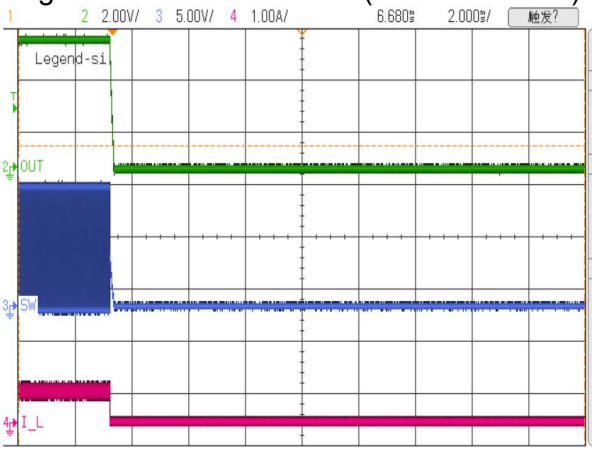


Figure 13. OTP verification(LOAD=600mA)



8 Functional Description

Overview

The ZCC5145 regulators are easy-to-use, non-synchronous, step-down DC/DC converters with a wide input voltage range up to 45 V. The devices are capable of delivering up to 600 mA DC load current with excellent line and load regulation. This devices are available in fixed frequency of 1.2 MHz. The family requires few external components, and the pin arrangement was designed for simple, optimum PCB layout.

Enable

EN is a digital control pin that turns the BUCK on and off. Pull to GND to disable the device and pull high to enable the device.

Protection

The ZCC5145 have dedicated protection circuitry running during normal operation to protect the IC. The thermal shutdown circuitry turns off the power device when the die temperature reaches excessive levels.Thermal protection disables BUCK when the junction temperature rises to approximately 150°C; allowing the device to cool down. When the junction temperature cools to approximately 120°C; the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

The UVLO comparator protects the power device during supply power start-up and shutdown to prevent operation at voltages less than the minimum input voltage. A gate drive (BST) undervoltage lockout is included to ensure that there is enough gate drive voltage to drive the MOSFET before the device tries to start switching. The ZCC5145 also feature a shutdown mode decreasing the supply current to approximately 3 μA.

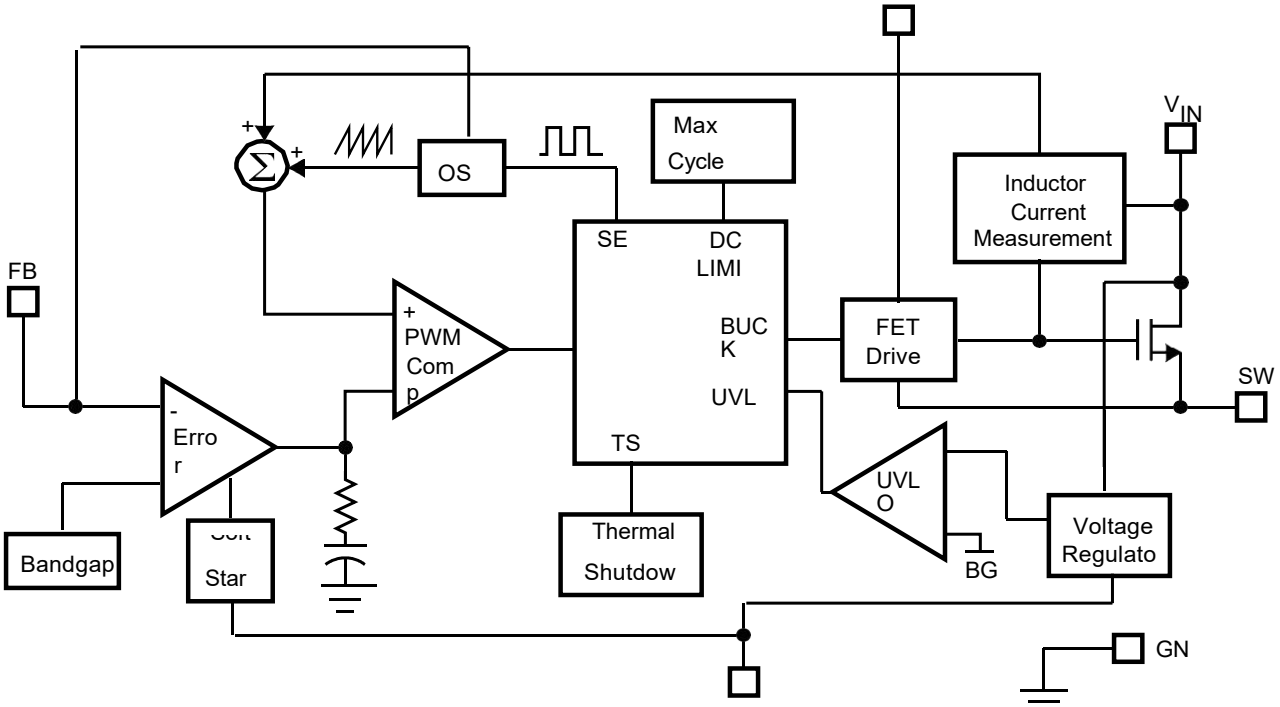


Figure 1 Functional Block Diagram

9 APPLICATION INFORMATION

NOTE

The information in the following application part is not part of the zcc-china component specification, and ZCC-Chinadoes not guarantee its accuracy or completeness. ZCC-Chinacustomers are responsible for determining the suitability of the components for their purposes. Customers should verify and test their design and implementation to confirm system functionality.

9.1 Setting Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Table 1 lists resistors for common output voltages. The feedback pin voltage 0.8 V, so the ratio of the feedback resistors sets the output voltage according to Equation 1:

$$VOUT = 0.8\ V\ (1 + (R1 / R2)) \quad (1)$$

Table 1: Resistor Selection for Common **Output Voltages**

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	102 (1%)	124 (1%)
2.5	59 (1%)	124 (1%)
3.3	40.2 (1%)	124 (1%)
5	23.7 (1%)	124 (1%)
12	8.2 (1%)	113 (1%)

9.2 Selecting the Inductor

Use an inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For best efficiency, the inductor's DC resistance should be less than 200m .

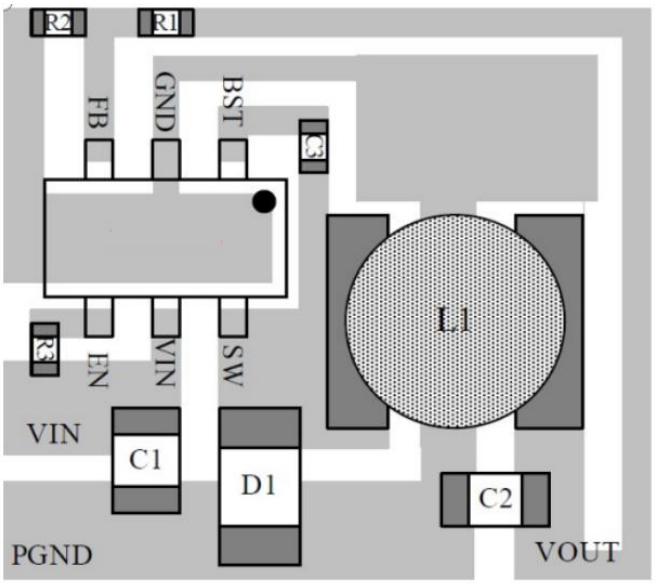
9.3 Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing through the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESRs and small temperature coefficients. For most applications, a 4.7μF effective capacitor will sufficient.

9.4 PCB Layout Guide

PCB layout is very important to stability. Please follow these guidelines and use Figure 2 and Figure 3 as reference.

1) Keep the path of switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.
2) Keep the connection from the power ground→Schottky diode→SW pin as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND to large copper areas to cool the chip for improved thermal performance and long- term reliability. For single layer PCBs, avoid soldering the exposed pad.



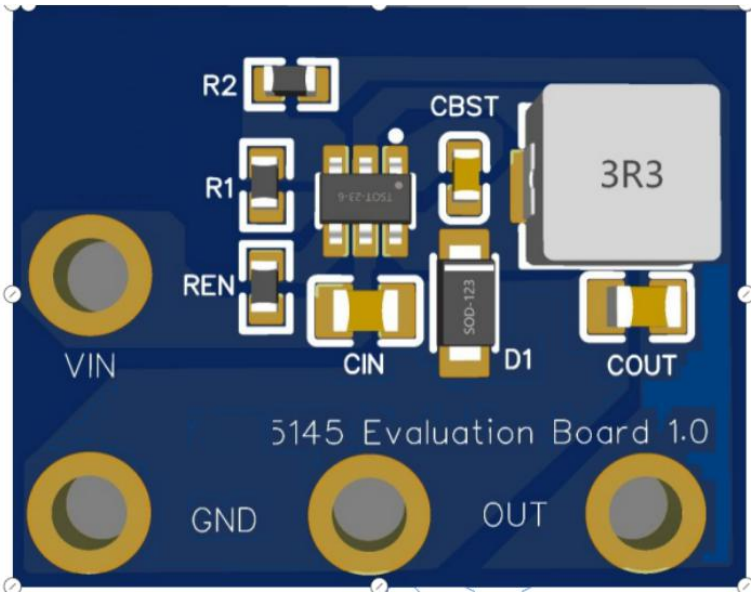


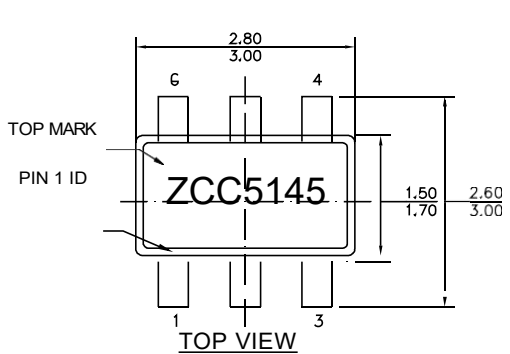
Figure 2 PCB Layout

Figure 3 PCB Layout With Example

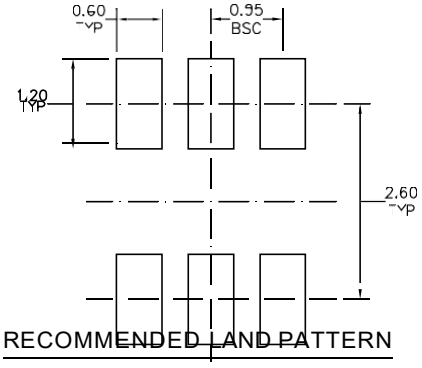
9.5 TYPICAL APPLICATION CIRCUIT

9.6 PACKAGE INFORMATION

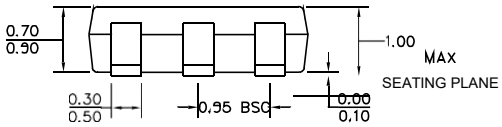
SOT23-6



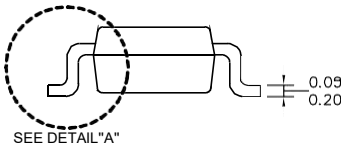
TOP VIEW



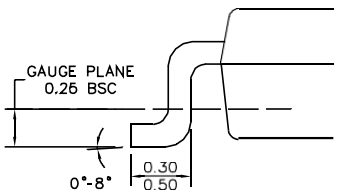
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) DRAWING IS NOT TO SCALE
4) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTICE: The information in this document is subject to change without notice.