100V Input, Ultra-Low I_Q, Synchronous Buck Converter

1 DESCRIPTION

The MK9019 operates over a wide input voltage range from 4.5V to 100V. With integrated the main MOSFET and a synchronous MOSFET, the MK9019 delivers up to 1A output current. With the 3A current limit, MK9019 can deliver 3A peak current for some special applications.

The MK9019 adopts a constant on-time (COT) control architecture to achieve excellent transient response.

With patented standby circuits, the device can achieve ultra-low I_Q, and exit the standby mode fast.

2 APPLICATIONS

- BMS (E-Bike, Electric Tools)
- Automotive and Industry Systems
- Motor Drives, Telecom

3 FEATURES

- Wide Input Voltage 4.5V-100V
- 3A Current limit
- Low $R_{DS(ON)}$ for Internal MOSFETS 500mΩ/240mΩ
- <200μA Supply Current under I_{LOAD}=100μA
- MK9019 Adjustable F_{SW} up to 1MHz
- Internal 3ms Soft-start
- Smart power saving and ultra-Fast Transient Response
- Precision ±1% Feedback Reference
- Open-Drain Power Good Indicator
- OC, OT Protection with Hiccup Mode
- No Loop Compensation Components
- ESOP8 Package with Thermal PAD

4 TYPICAL APPLICATION

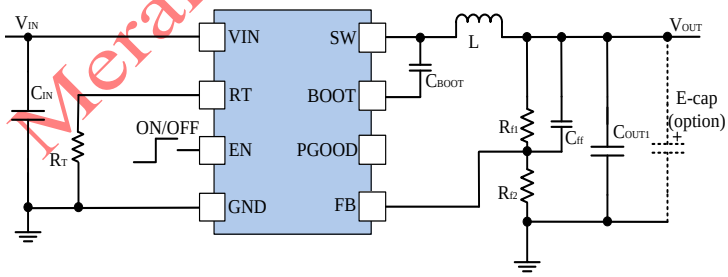


Figure 1. Typical Application Diagram

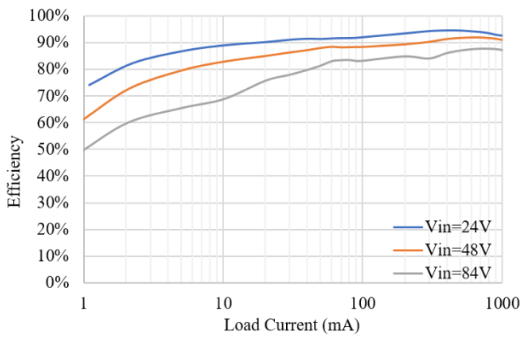
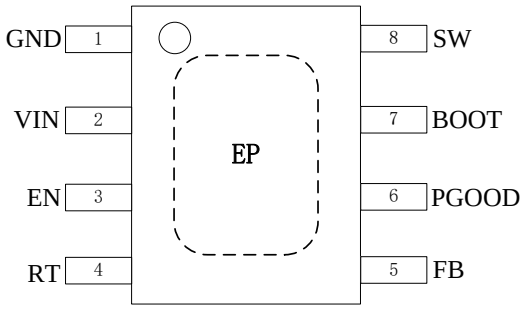


Figure 2. Efficiency at 12Vout

5 PACKAGE REFERENCE AND PIN FUNCTION



ESOP8(top view)

Order No.	Description
MK9019GAD	ESOP-8, tape, 4k/reel

Pin #	Name	Description
1	GND	Ground pin.
2	VIN	Input pin. Decouple this pin to GND with a low ESR ceramic capacitor.
3	EN	Enable control pin. The device has accurate 1.24V rising threshold and a programable falling threshold. This pin also can be used for programming the VIN turn on voltage with the resistor divider.
4	RT	On-time programming pin. A resistor between this pin and GND sets the buck switch on-time. $F_{SW}(kHz) = \frac{2.56 \times Vout(V)}{R_T(M\Omega)}$
5	FB	Output feedback pin. Connect this pin to the center point of the output resister divider to program the output voltage: $V_{OUT}=1.2\times(1+R_{f1}/R_{f2})$
6	PGOOD	Power good indicator pin. This pin is an open-drain output pin. Connect to a source voltage through an pull-up resistor.
7	BOOT	Boot-strap pin. Decouple this pin to SW pin with a 10nF ceramic capacitor.
8	SW	Inductor pin. Connect to the switch node of the power inductor.
EP	Thermal PAD	Exposed pad of the package. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

6 ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN, SW to GND ····· -0.3V to 110V
SW to GND (20ns pulse) ····· -3V to 110V
BS to GND ····· SW+6.6V
RT to GND ····· -0.3V to 6.6V
FB to GND ····· -0.3V to 6.6V
PGOOD to GND ····· -0.3V to 30V
Power Dissipation, P_D @T_A=25℃, ESOP8 ····· 3.3W
Package Thermal Resistance
θ_{JA} (Junction to ambient) ····· 30℃/W
θ_{JC} (Junction to case) ····· 10℃/W
Operating Junction Temperature, T_J ····· -40℃ to 160℃
Storage Temperature，T_{stg} ····· -65℃ to 160℃
Soldering Temperature(10 second)，T_{sld} ····· 260℃

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 RECOMMENDED OPERATING CONDITIONS

VIN Voltage ····· 4.5V to 100V
EN Voltage ····· -0.3V to 100V
SW Voltage ····· -0.3V to 100V
Ambient Temperature ····· -40℃ to 85℃

8 ESD RATINGS

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, SW, BOOT, EN, RT, FB, PGOOD (1).	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, SW, BOOT, EN, RT, FB, PGOOD (2).	±500	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

9 ELECTRICAL CHARACTERISTICS

V_{IN}=48V, V_{OUT}=5V, L=22μH, C_{OUT}=22uF, T_A=25℃, unless otherwise specified

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Input Voltage						
V_{IN}	Input Voltage		4.5		100	V
Supply Current						
$I_{SHUTDOWN}$	Shutdown Current	V_{EN}=0V		7.7		μA
$I_{STANDBY}$	Standby Current	V_{EN}=V_{IN}, I_{OUT}=0A,		155		μA
Feedback						
V_{REF}	Feedback reference voltage			1.2		V
EN/UVLO						
V_{ENH}	EN rising threshold	V_{IN}=48V, I_{OUT}=0.1A		1.24		V
$I_{EN\ Hysteresis}$	Hysteresis Input Current	V_{IN}=48V, I_{OUT}=0.1A		-2		μA
PGOOD						
V_{PGH}	FB rising threshold for PGOOD low to high	V_{FB} rising		1.187		V
V_{PGL}	FB falling threshold for PGOOD high to low	V_{FB} falling		1.138		V
Frequency						
F_{SW} MK9108S	Programmable Switching Frequency Range	$F(kHz) = \frac{2.56xV_{OUT}(V)}{R_T(M\Omega)}$	100		500	kHz
F_{SW} MK9108F	Programmable Switching Frequency Range	$F(kHz) = \frac{2.56xV_{OUT}(V)}{R_T(M\Omega)}$	100		1000	kHz
Timing						
t_{ON-MIN}	Minimum on-time			50		ns
$t_{OFF-MIN}$	Minimum off-time			270		ns
Power Switches						
$R_{DSON-HS}$	High-side MOSFET RDSON			0.5		Ω
$R_{DSON-LS}$	Low-side MOSFET RDSON			0.24		Ω
Current Limit						
$I_{PEAK-HS}$	High-side MOSFET Peak Current limit			4		A
$I_{VALLEY-LS}$	Low-side MOSFET Valley Current limit			2		A
Soft Start						
t_{SS}	Soft-start time			3		ms
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold	T_J rising		160		℃
T_{HYS}	Thermal Shutdown Hysteresis			25		℃

10 BLOCK DIAGRAM

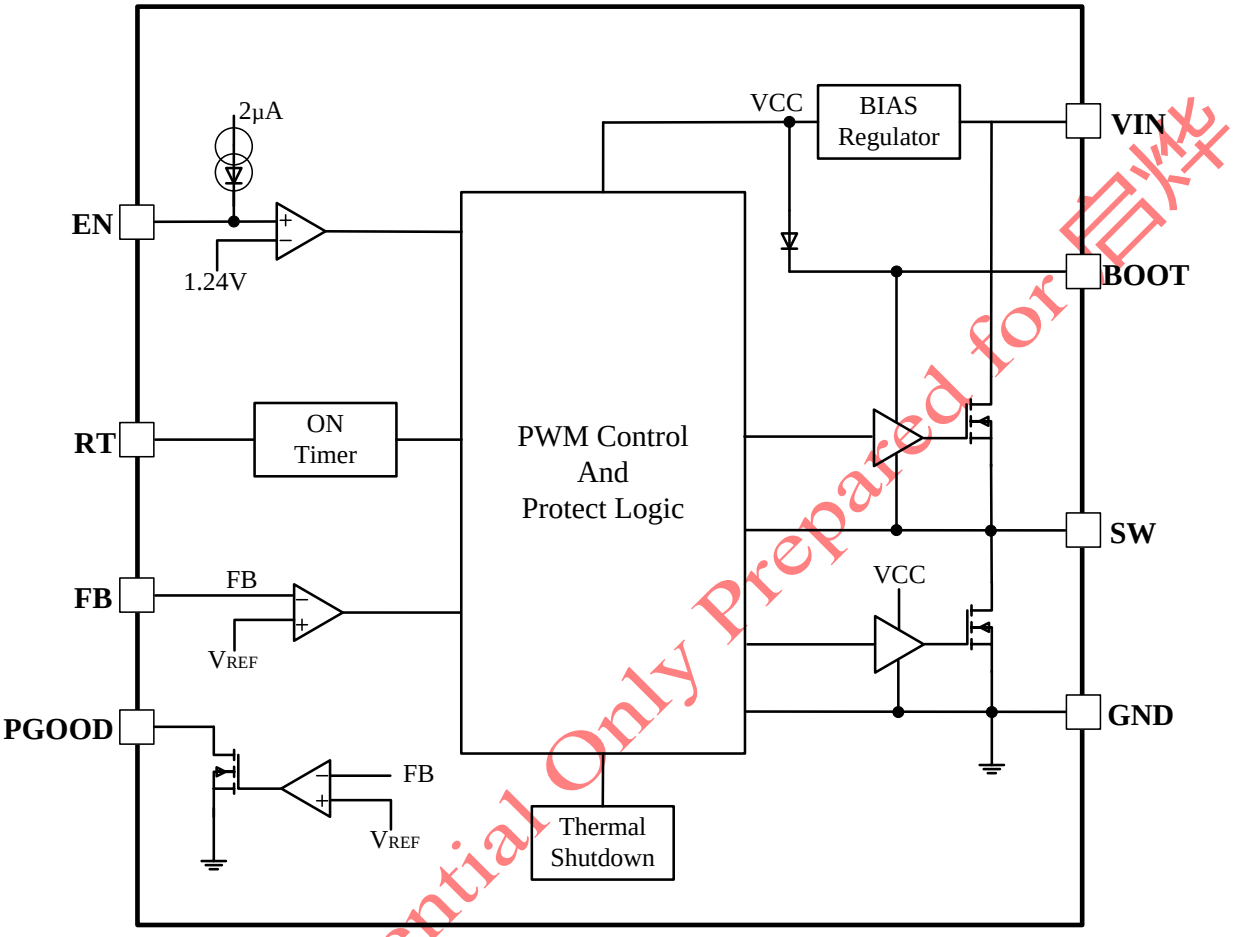


Figure3. Block Diagram

11 TYPICAL CHARACTERISTICS

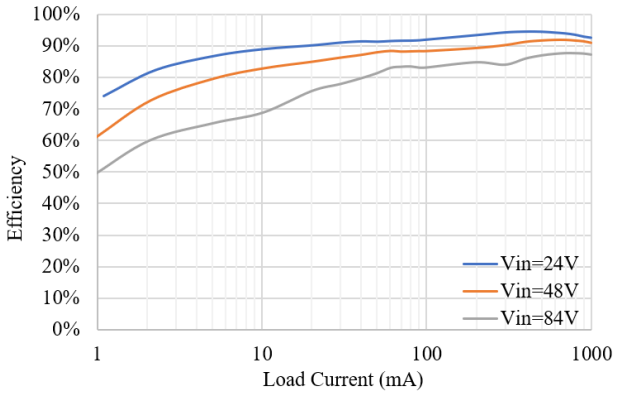


Figure4. Efficiency at 12Vout

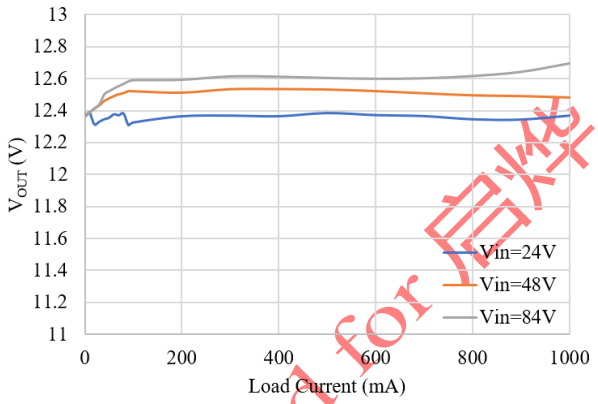
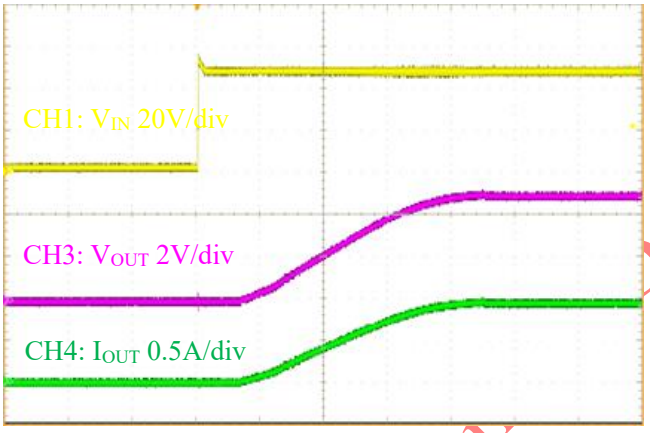
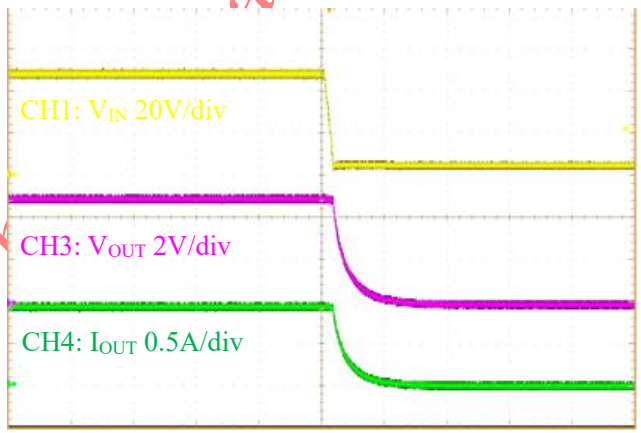


Figure5. Load and Line Regulation



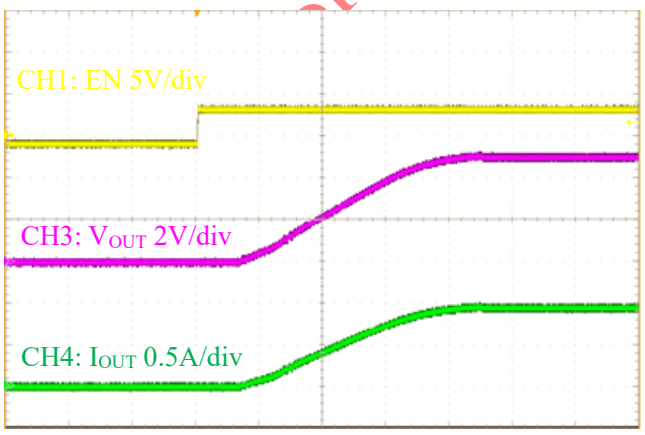
Time(1ms/div)

Figure6. Startup from VIN



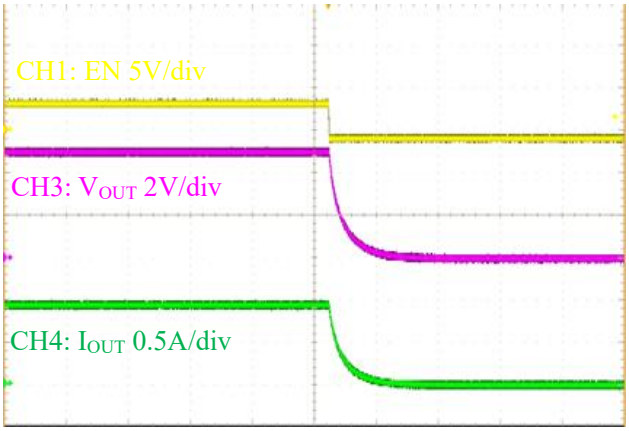
Time(1ms/div)

Figure7. Shutdown from VIN



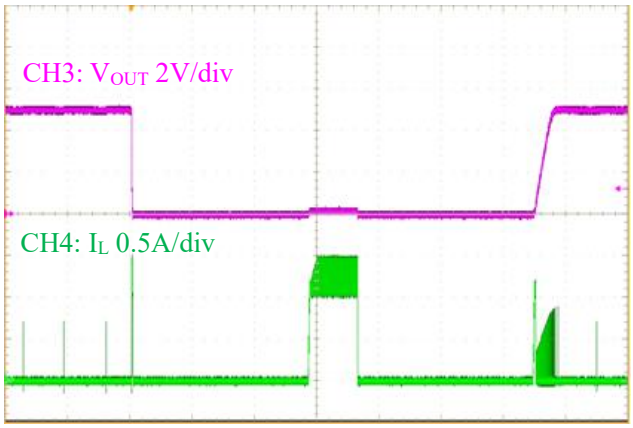
VIN=48V Time(1ms/div)

Figure8. Startup from EN



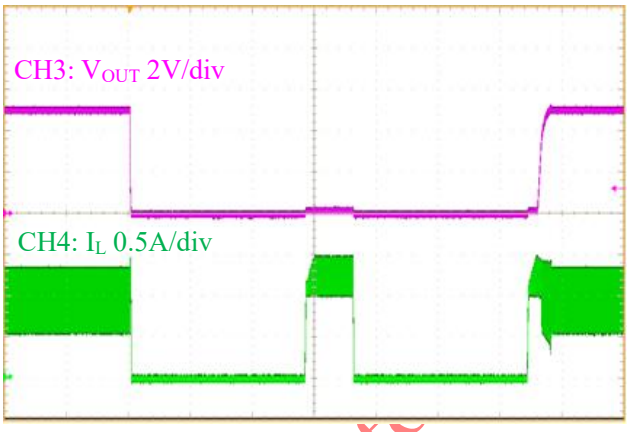
VIN=48V Time(1ms/div)

Figure9. Shutdown from EN



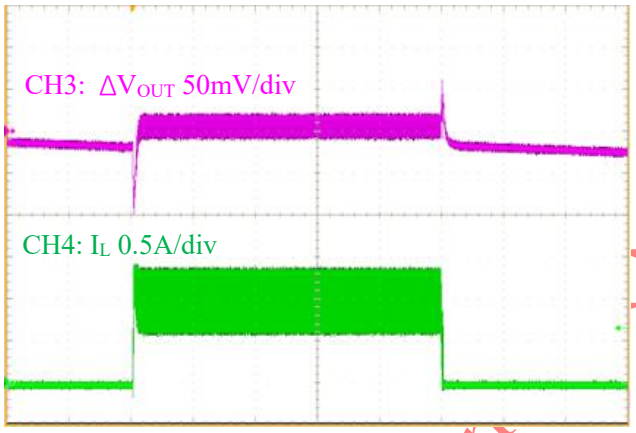
V_{IN}=48V I_{OUT}=0A Time(10ms/div)

Figure10. Short Protection and Recovery



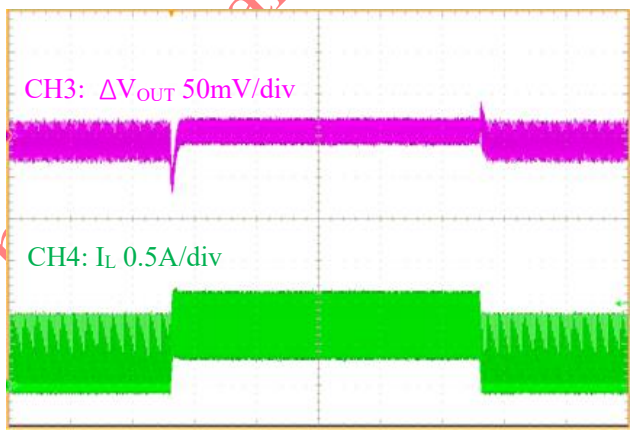
V_{IN}=48V I_{OUT}=1A Time(10ms/div)

Figure10. Short Protection and Recovery



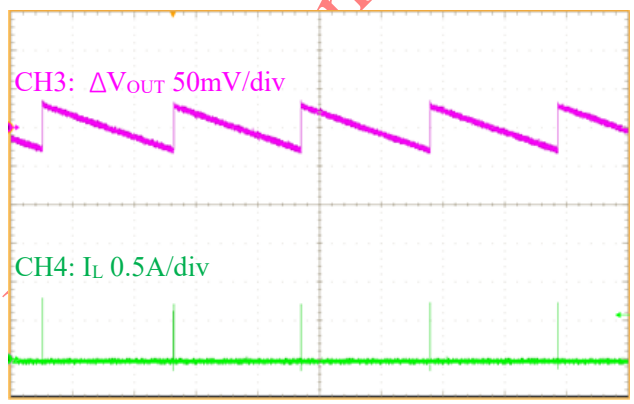
V_{IN}=48V V_{OUT}=5V Time(500μs/div) I_{OUT}:0A ~ 1A

Figure12. Load Transient



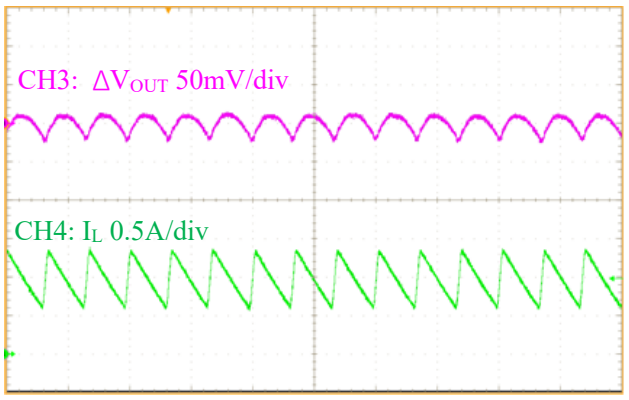
V_{IN}=48V V_{OUT}=5V Time(500μs/div) I_{OUT}:0.25A ~ 0.75A

Figure13. Load Transient



V_{IN}=48V V_{OUT}=5V Time(500μs/div) I_{OUT}=0A

Figure14. Out Ripple



V_{IN}=48V V_{OUT}=5V Time(5μs/div) I_{OUT}=1A

Figure15. Out Ripple

12 AIPPLICATIONS

12.1 Operation Overview

The MK9019 is a ultra-low I_Q synchronous buck converter. With very low $R_{DS(ON)}$ MOSFETs, the MK9019 can achieve very high efficiency. This converter operates over a wide input voltage range from 4.5V to 100V delivering up to 1A DC load current or 3A peak current. As adopting constant on-time (COT) mode, MK9019 can achieve fast transient responses for high voltage step down applications. Control loop compensation is not required for this regulator for this converter, reducing design time and external component count. And the pin arrangement is designed for a simple layout requiring only a few external components.

Because of high integration in the MK9019, the application circuit is very simple. Only the on-timer resister R_T, the feedback resistors (R_{f1} and R_{f2}), the BOOT capacitor C_{BOOT}, the feedforward capacitor C_{ff}, the input capacitor C_{IN}, the output capacitor C_{OUT} and the output inductor L need to be selected for the targeted applications.

12.2 Switching Frequency (R_T)

The switch frequency of MK9019 is set by the on-time resistor RT. As shown below, in $5V_{OUT}$ application a 43kΩ resistor sets the switching frequency at 300kHz.

$$F_{SW}(kHz) = \frac{2.56xV_{OUT}(V)}{R_T(M\Omega)}$$

Note that the final switching frequency is not only affected by component tolerant but also $t_{ON\text{-}MIN}$ and $t_{OFF\text{-}MIN}$.

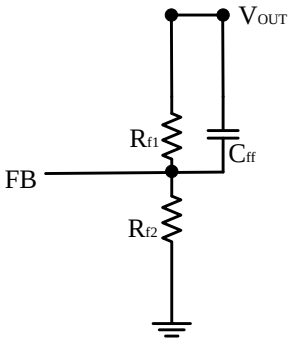
12.3 Output Voltage Program

Choose R_{f1} and R_{f2} to program the output voltage. For target V_{OUT} setpoint, calculate Rf1 and Rf2 using below equation:

$$V_{OUT} = 1.2V \times (1 + \frac{R_{f1}}{R_{f2}})$$

R_{f1} in the range of 100kΩ to 500kΩ is recommended for most applications. Larger feedback resistors consumes less DC current, which is important if light-load efficiency is critical. But too large resistors is not recommended as the feedback path would become more susceptible.

The feedforward capacitor C_{ff} is strongly recommended, which can improve the system stability and transient responses.



12.4 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X5R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 1μF low ESR ceramic capacitor is recommended.

12.5 Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current I_{OUT}(max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the I_L(peak). An inductor whose saturation current is above the current limit setting of the MK9019 will be best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

12.5 Output Capacitor (C_{OUT})

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only take the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X5R or better grade ceramic capacitor larger than 22μF is recommended. For high peak current applications, an E-cap larger than 100uF is recommended too.

12.6 Enable Operation

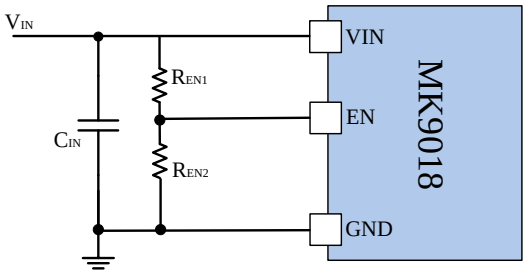
Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}}) \times V_{ENH}$$

V_{ENH} is EN rising threshold voltage, typical is 1.24V.

The UVLO hysteresis is accomplished with an internal 2μA current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN1} \times 2\mu\mathrm{A}$$



12.7 Boot-strap capacitor

This capacitor provides the energy for high-side gate driver. A high quality 10nF ceramic capacitor connected between the BS pin and the SW pin is recommended. Also a RC series net can be used for slow down the turn-on speed of high side MOSFET.

12.8 Power Good (PGOOD)

MK9019 provides a PGOOD flag pin to indicate whether the output voltage is within the regulation level. PGOOD is an open-drain output that requires a pullup resistor to a DC source. The typical range of pullup resistance is about 10kΩ. When the FB voltage exceeds 96% of the reference, the internal switch will be turned off and PGOOD can be pulled high by the pullup resistor. If the FB voltage falls below 92% of the reference, the switch will be turned on and PGOOD is pulled low to indicate the output voltage is out of regulation.

13 LAYOUT

13.1 Layout Guideline

To achieve high performance of the MK9019, the following layout tips must be followed.

(1) At least one low-ESR ceramic bypass capacitor C_{IN} must be used. Place the C_{IN} as close as possible to the MK9019 VIN and GND pins.

(2) Minimize the loop area formed by C_{IN} connections to VIN and GND pins.

(3) Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.

(4) Maximize the PCB area connecting to the GND pin and thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.

(5) Place the feedback resistors, R_{f1} and R_{f2}, close to the FB pin. Route the feedback V_{OUT} sense path away from noisy nodes such as the SW net.

(6) The RT pin is sensitive to noise. The on-time set resistor R_T must be close to the device.

13.2 Layout Example

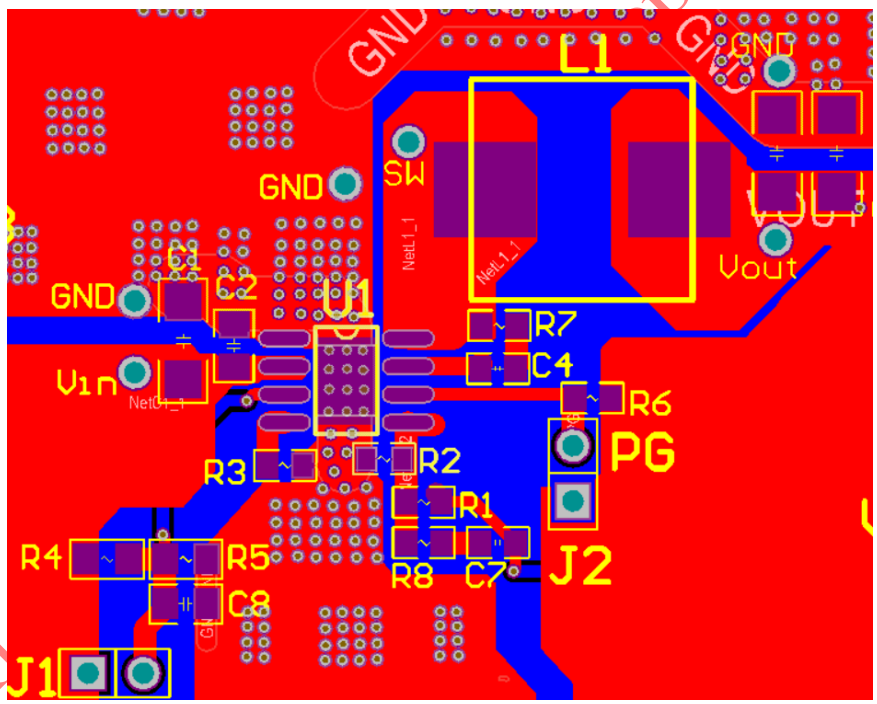


Figure16. Layout Example

14 PACKAGE SIZE

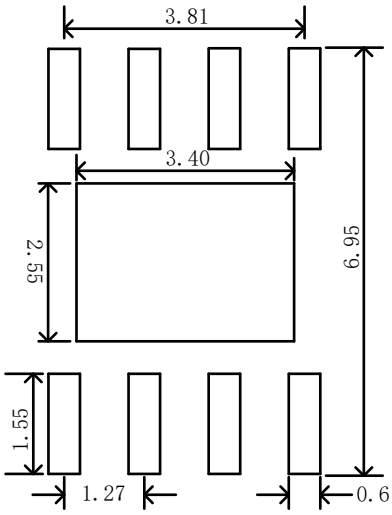


Figure17. Recommended Land Pattern (mm)

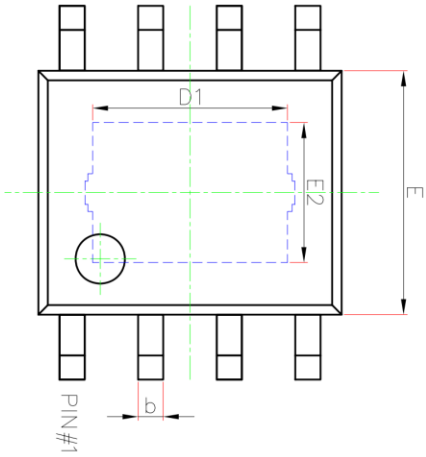


Figure18. MK9019 Top View

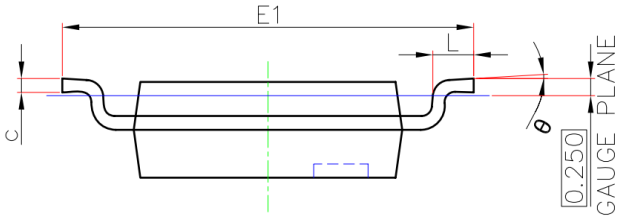


Figure19. MK9019 Side View

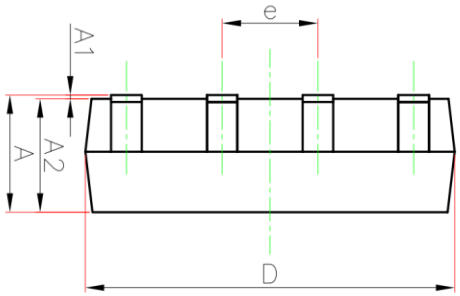
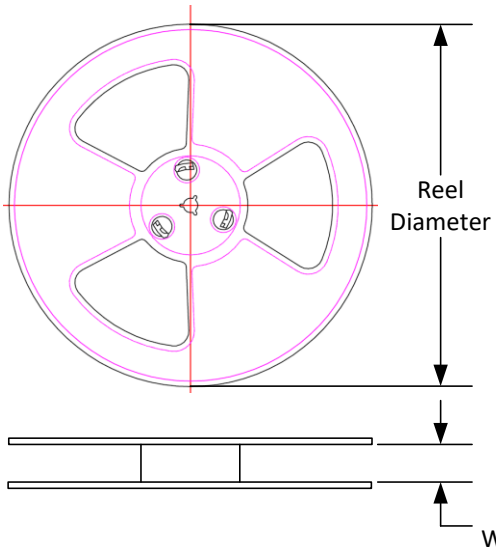


Figure20. MK9019 Side View

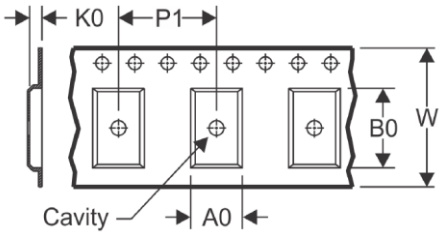
SYMBOL	Millimeter	
	MIN	NOM
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

15 REEL AND TAPE INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	Quantities	Reel Diameter (mm)	Reel Width W1(mm)
MK9019	ESOP8	8	4000	332	12.5
A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	
4.0	3.3	1.1	8.0	12.0	

16 TAPE AND REEL BOX DIMENSIONS