NEXGEN POWER

NSF65R600C

N-channel 650V Super Junction MOSFET

Description

NSF65R600C is a N-channel power MOSFET designed according to super junction technology. This device has very low on-resistance and hard ruggedness for switching applications. It's very low conduction loss and fast switching can make applications more efficient and faster.

Features

- Low gate charge
- Low $R_{DS(on)}$ per chip area(Low FOM)
- Very low switching and conduction loss
- Extremely high commutation ruggedness

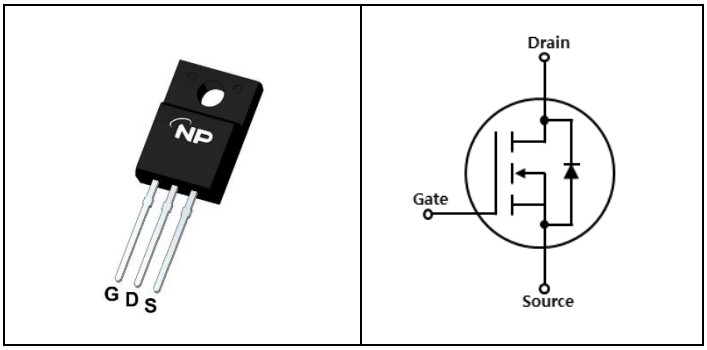
Applications

- TV and PC Power
- Adopter and Lighting
- Telecom and UPS(Uninterruptible Power Supply)

Key parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$Q_{g,typ}$	13	nC
I_D	8	A
$R_{DS(on),max}$	0.60	Ω

Package & Internal circuit



Ordering Information

Ordering Code	Package	Marking	Packing type
NSF65R600C	TO-220F	65R600C	Tube

Absolute maximum ratings at T_C=25ºC unless otherwise specified

Symbol	Parameter	Value	Unit	Test condition
V_{DS}	Drain-source voltage	650	V	-
V_{GS}	Gate-source voltage	±30	V	-
I_D(1)	Continuous drain current	8	A	T_C = 25˚C
	Continuous drain current	4.5	A	T_C = 100˚C
I_{DM}(2)	Pulsed drain current	24	A	T_C = 25˚C
E_{AS}	Single pulsed avalanche energy	129	mJ	Starting T_j = 25˚C, I_{AS} = 2.0A, V_{DD} = 50V, I_D = I_{AR}
P_{tot}	Total power dissipation	28	W	T_C = 25˚C
dv/dt	MOSFET dv/dt ruggedness	50	V/ns	V_{DS} = 0…400V
dv/dt	Reverse diode dv/dt	15	V/ns	V_{DS} = 0…400V, T_j = 25˚C, I_{SD}≤I_D
T_{stg}	Storage temperature	-55 to 150	˚C	-
T_j	Operating junction temperature	-55 to 150	˚C	-

1. limited by $T_{j,max}$
2. Pulse width limited by $T_{j,max}$

Thermal characteristics

Symbol	Parameter	Value	Unit	Test condition
R_{thJC}	Thermal resistance, junction - case	4.5	˚C/W	-
R_{thJA}	Thermal resistance, junction - ambient	80	˚C/W	-

Static characteristics at T_C=25ºC unless otherwise specified

Symbol	Parameter	Maximum value			Unit	Test condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	-	-	V	V_{GS} = 0V, I_D = 0.25mA
$V_{GS(th)}$	Gate threshold voltage	2	-	4	V	V_{GS} = V_{DS}, I_D = 0.25mA
I_{GSS}	Gate-body leakage current	-	-	100	nA	V_{GS} = ±30V, T_j = 25ºC
I_{DSS}	Zero gate voltage drain current	-	-	1	uA	V_{DS} = 650V, V_{GS} = 0V, T_j = 25˚C
		-	-	100		V_{DS} = 650V, V_{GS} = 0V, T_j = 150˚C
$R_{DS(on)}$	Drain-source on-resistance		0.52	0.60	Ω	V_{GS} = 10V, I_D = 2.0A

Dynamic characteristics

Symbol	Parameter	Values			Unit	Test condition
		Min.	Typ.	Max.		
C_{iss}	Input capacitance	-	471	-	pF	V_{DS} = 50V, V_{GS} = 0V, f = 400kHz
C_{oss}	Output capacitance	-	35	-	pF	
C_{rss}	Reverse transfer capacitance	-	1.7	-	pF	
$t_{d(on)}$	Turn-on delay time	-	17	-	ns	V_{DD} = 325V, I_D = 8A, V_{GS} =10V, R_G =25Ω
t_r	Rise time	-	26	-	ns	
$t_{d(off)}$	Turn-off delay time	-	53	-	ns	
t_f	Fall time	-	38	-	ns	
R_G	Gate resistance	-	22	-	Ω	f = 1MHz, I_D = 0A(open drain)
Q_g	Total gate charge	-	13	-	nC	V_{DS} = 520V, V_{GS} = 10V, I_D = 8A
Q_{gs}	Gate-source charge	-	2.1	-	nC	
Q_{gd}	Gate-drain charge	-	6.9	-	nC	

Reverse diode characteristics

Symbol	Parameter	Values			Unit	Test condition
		Min.	Typ.	Max.		
V_{SD}	Diode forward voltage	-	-	1.4	V	V_{GS} = 0V, I_{SD} = 8A, T_j = 25˚C
t_{rr}	Reverse recovery time	-	306	-	ns	I_{SD} = 8A, V_{DD} = 100V, di/dt = 100A/us
I_{rr}	Reverse recovery current	-	13	-	A	
Q_{rr}	Reverse recovery charge	-	2	-	uC	

Characteristic Graph

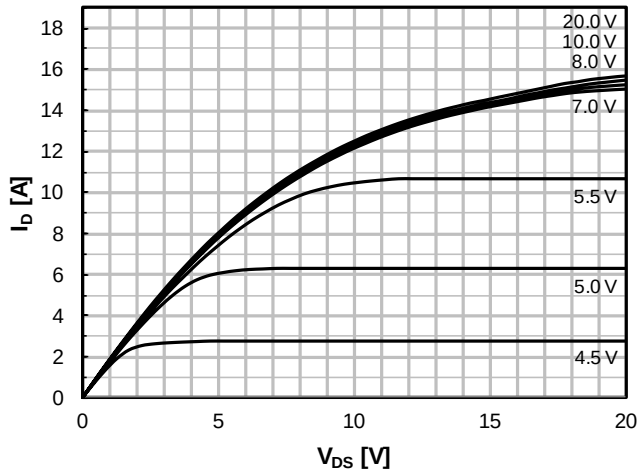


Fig. 1 Output Characteristics

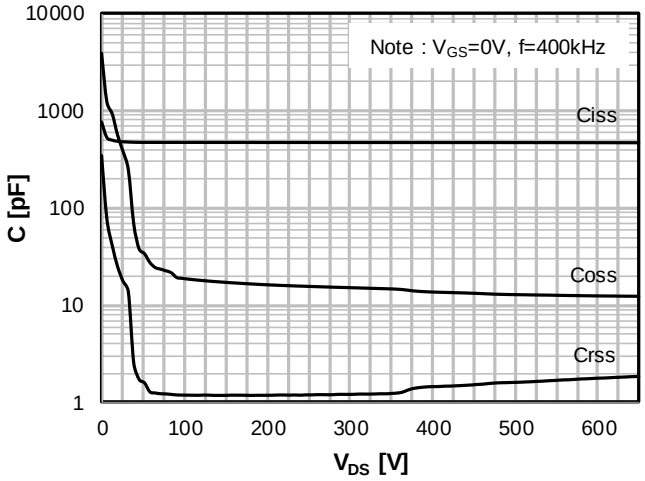


Fig. 2 Capacitances

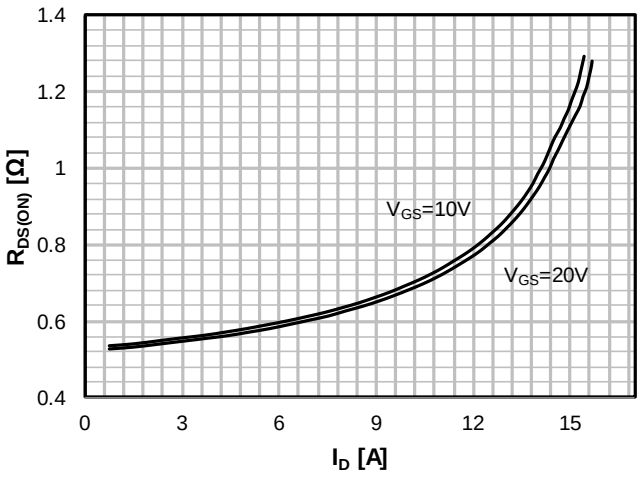


Fig. 3 On-state Resistance

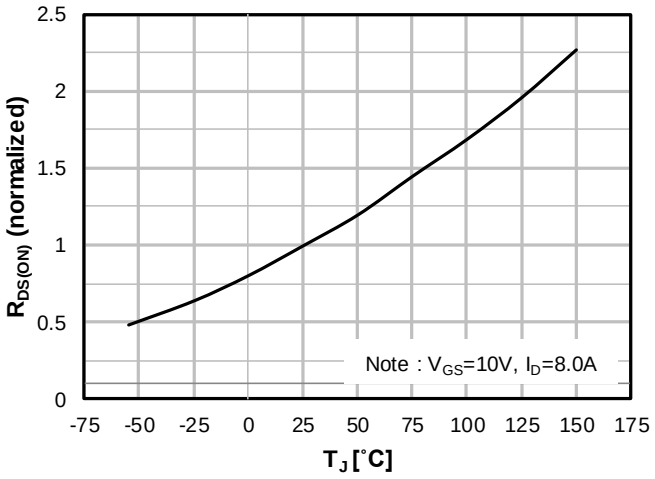


Fig. 4 On-state Resistance with Temperature

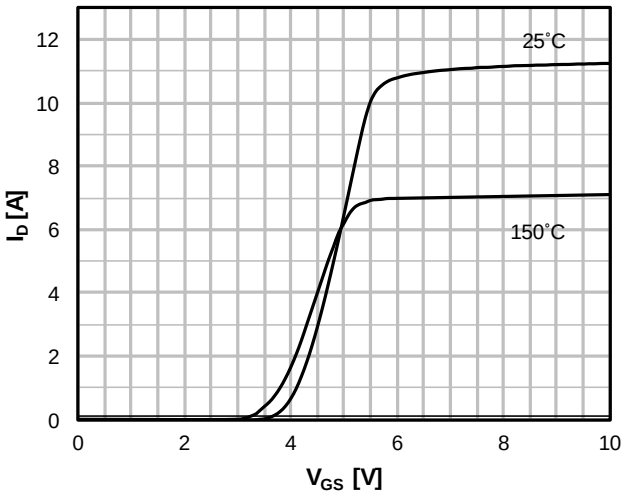


Fig 5. Transfer Characteristics

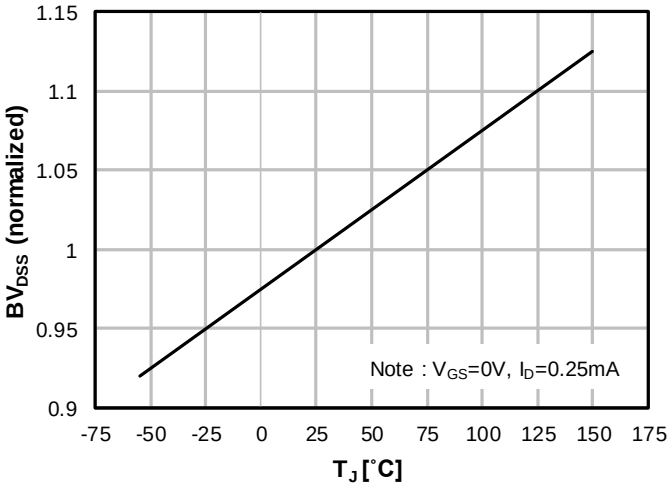


Fig 6. Breakdown Voltage with Temperature

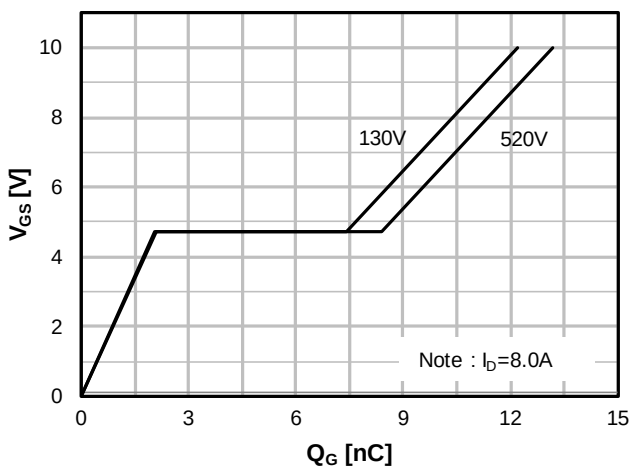


Fig 7. Gate Charge

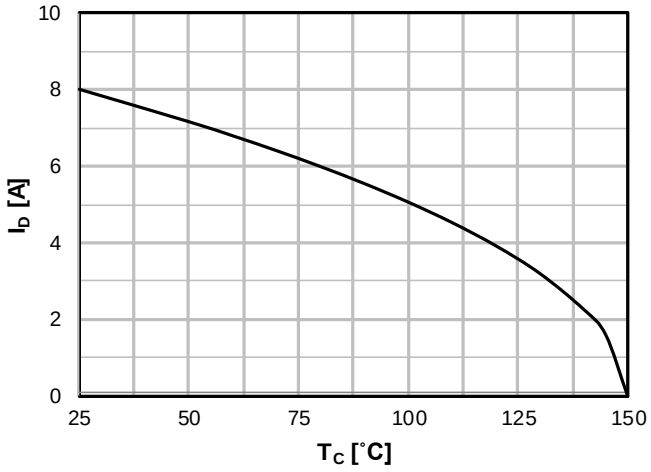


Fig 8. Maximum Drain Current

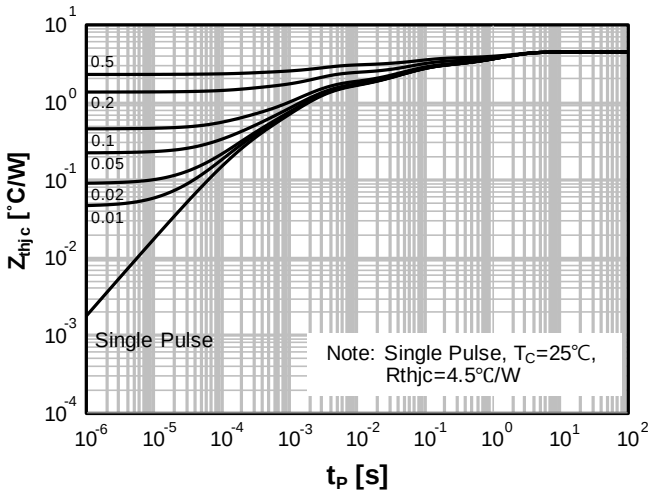


Fig 9. Maximum Transient Thermal Characteristics

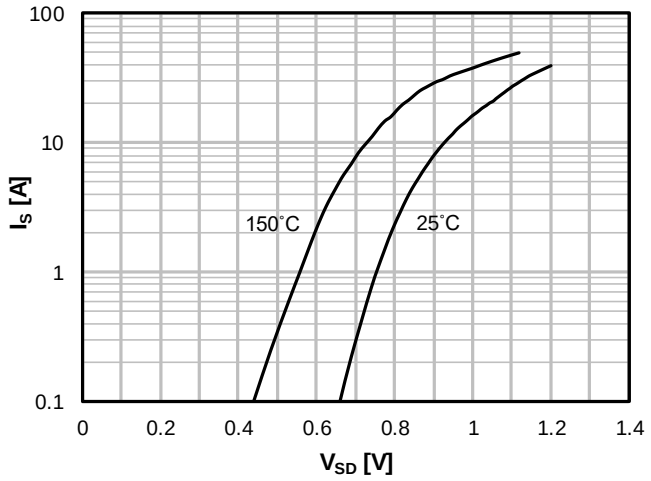


Fig 10. Body Diode Characteristics

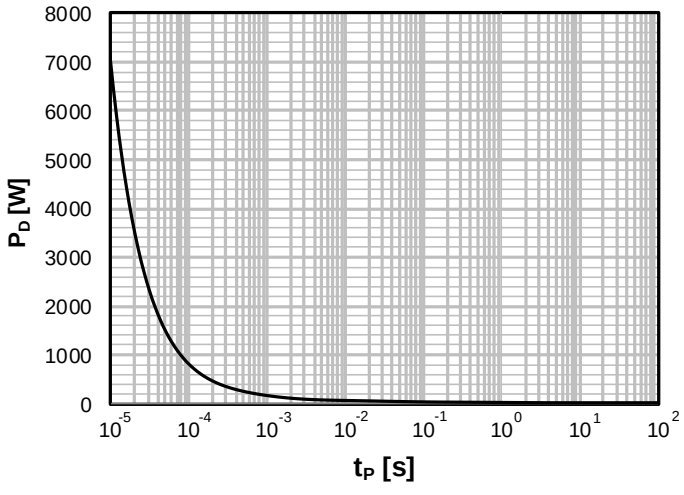


Fig 11. Power Dissipation

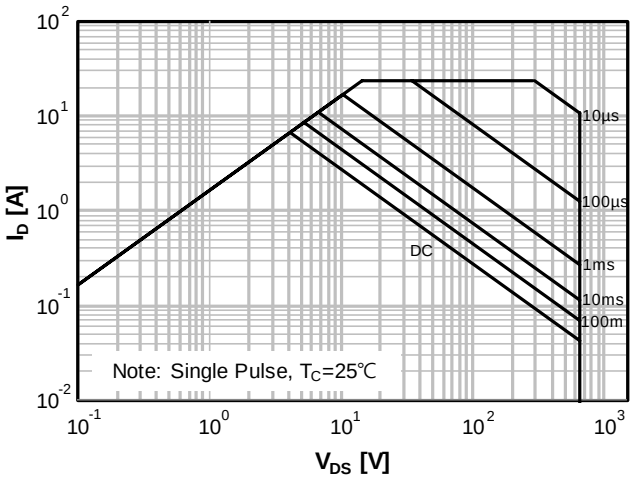


Fig 12. Safe Operating Area

Test Circuits

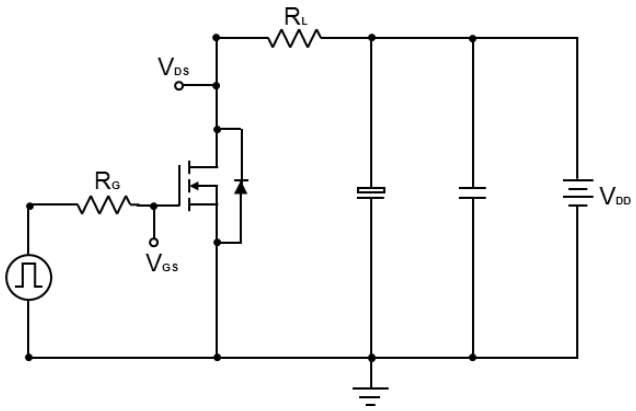


Fig 13. Test circuit for resistive load switching times

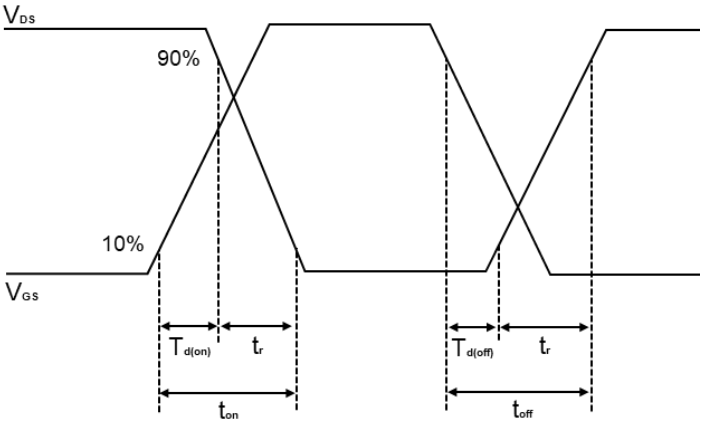


Fig 14. Switching times waveform

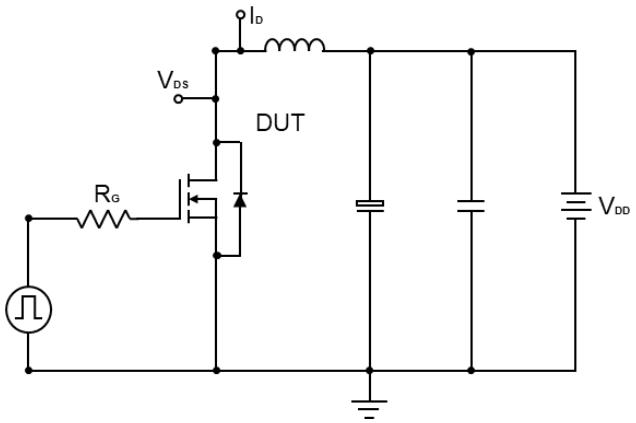


Fig 15. Test circuit for unclamped inductive load

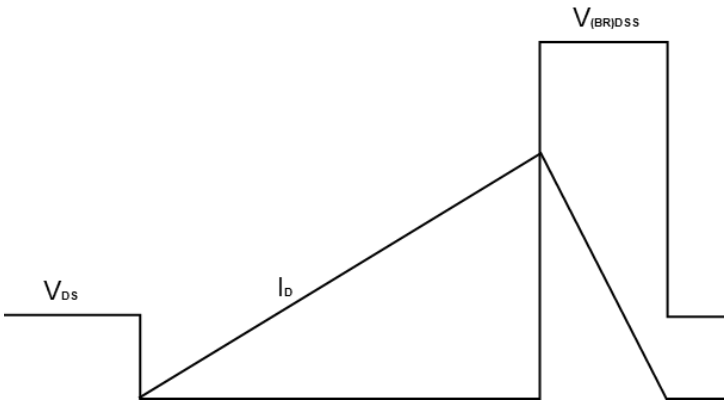


Fig 16. Unclamped inductive waveform

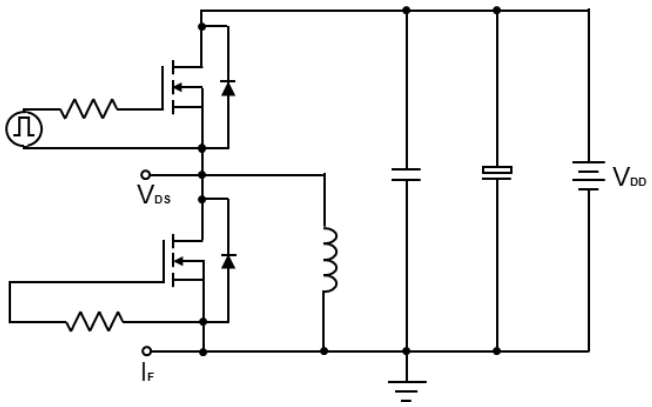


Fig 17. Test circuit for diode

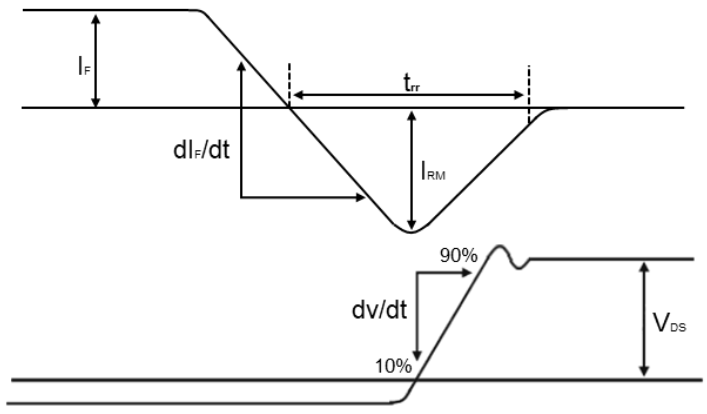
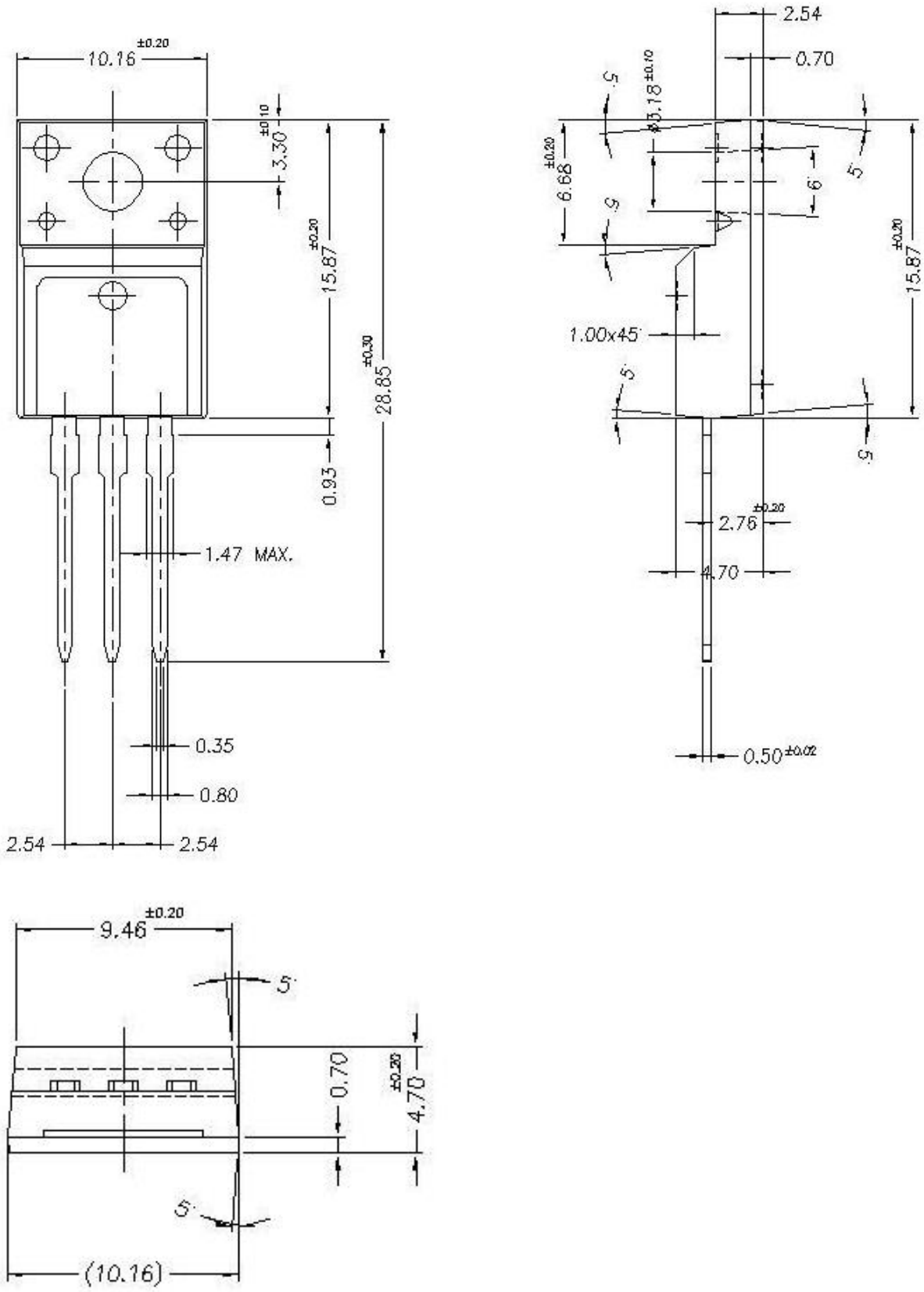


Fig 18. Diode recovery

Package Information

TO-220F Package Outline



RESTRICTIONS ON PRODUCT USE

Nexgen Power Ltd. and its subsidiaries and affiliates are collectively referred to as “Nexgen Power”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

• Nexgen Power Ltd. reserves the right to make changes to the information in this document and related Product without notice.
• This document and any information herein may not be reproduced without prior written permission from Nexgen Power Ltd. Even with Nexen Power Ltd.'s written permission, reproduction is permissible only if reproduction is without alteration/omission.