2016 High performance Power Technology Seminar

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IPC division

Segment Marketing Manager

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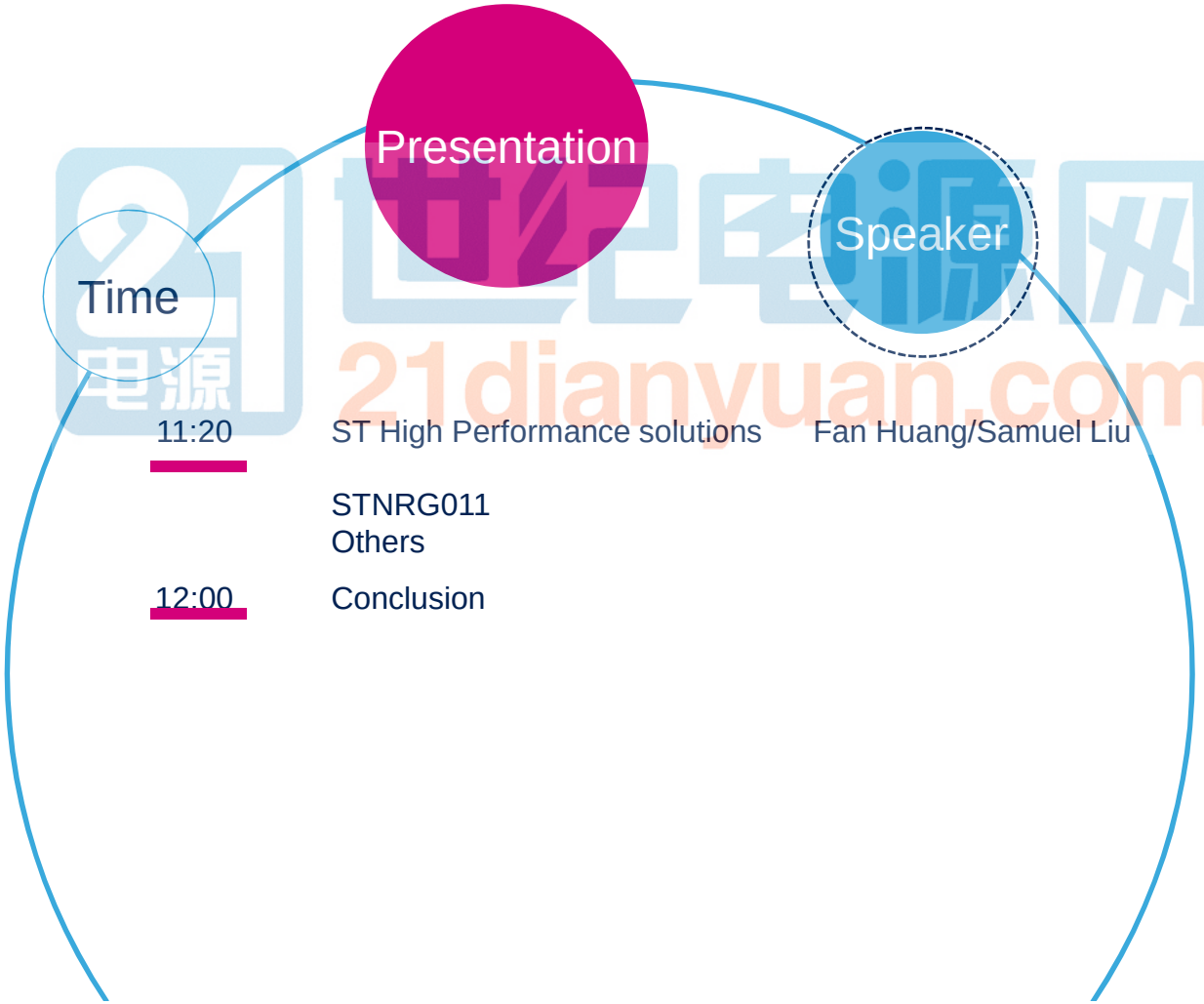
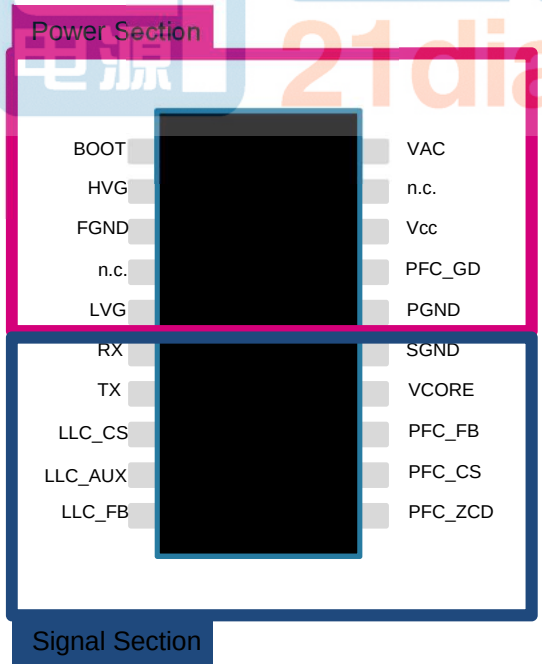
Agenda



Time	Presentation	Speaker
11:20	ST High Performance solutions	Fan Huang/Samuel Liu
	STNRG011 Others	
12:00	Conclusion	

STNRG011:digital combo with all analog peripherals and drivers integrated for LLC

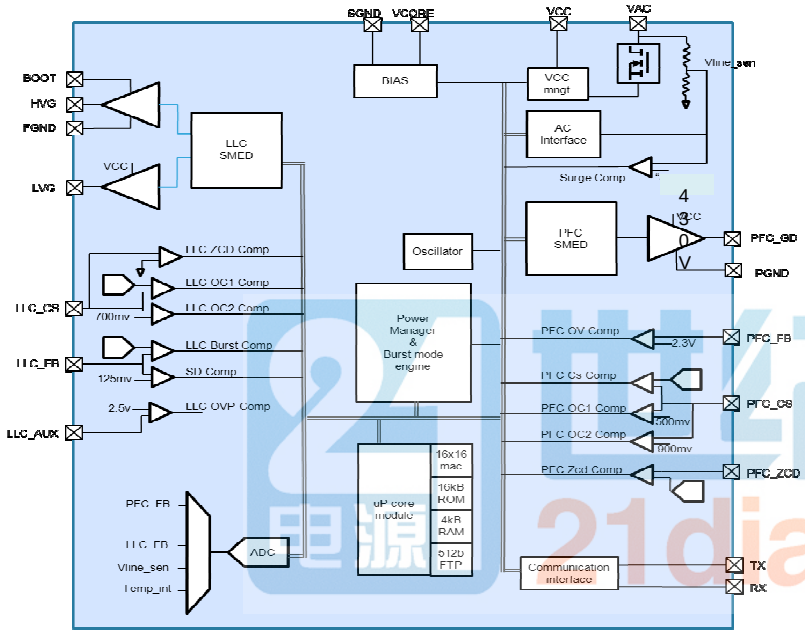
STNRG011 represents high voltage fully integrated Digital Combo ROM based Time Shift LLC controller with Multimode PFC Functionality



STNRG011 K-competitive advantages

- Lower part count
  - BOM reduction due to dedicated resources and 800V start-up Circuit, line Sense and Xcap Discharge integration
- Low pin count
  - SO20 package
- No-Load Power (Target <100mW)
  - Low power mode and X-cap discharge function
- Better light load efficiency
  - Enhanced Burst-mode. Improved PFC functionality
- Better dynamic response
  - Time Shift LLC control
- Optimized PFC section
  - Ramp enhanced constant-on-Time (reCOT) multimode with input voltage feedforward, THD optimizer, frequency limitation and Skipping area
- Safe operation
  - Complete set of PFC and Half bridge protections
- Flexibility, programmability and communication functions
  - FPGA emulator to develop and validate algorithms and software
  - Monitoring Function by UART Interface and Black Box recording

STNRG011 hardware

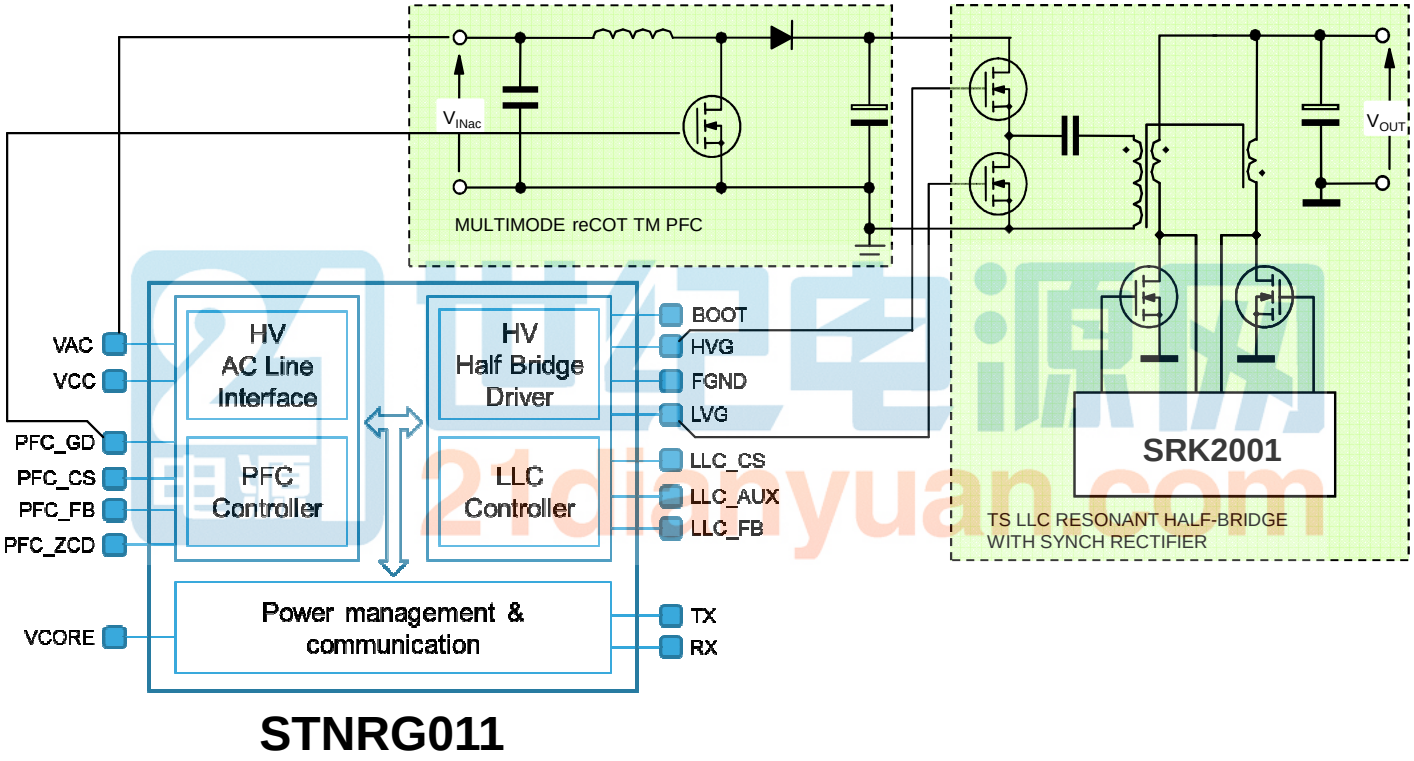


- ON-CHIP HV Half Bridge DRIVER
  - Dedicated for LLC topology
  - Up to 600V
  - 1A Peak Current Drive Capability
  - Matched Propagation Delays between Both Channels
  - dV/dt immunity +/- 50V/nsec
- Integrated HV start up & HV sense for AC line sense
- AC disconnection detection & Xcap discharge
- Brown out detection
- Surge detection

- Embedded µP
- 4 SMEDs (**S**tate **M**achine **E**vent **D**riven) for PWM generation
- Communication interfaces (UART & I2C)

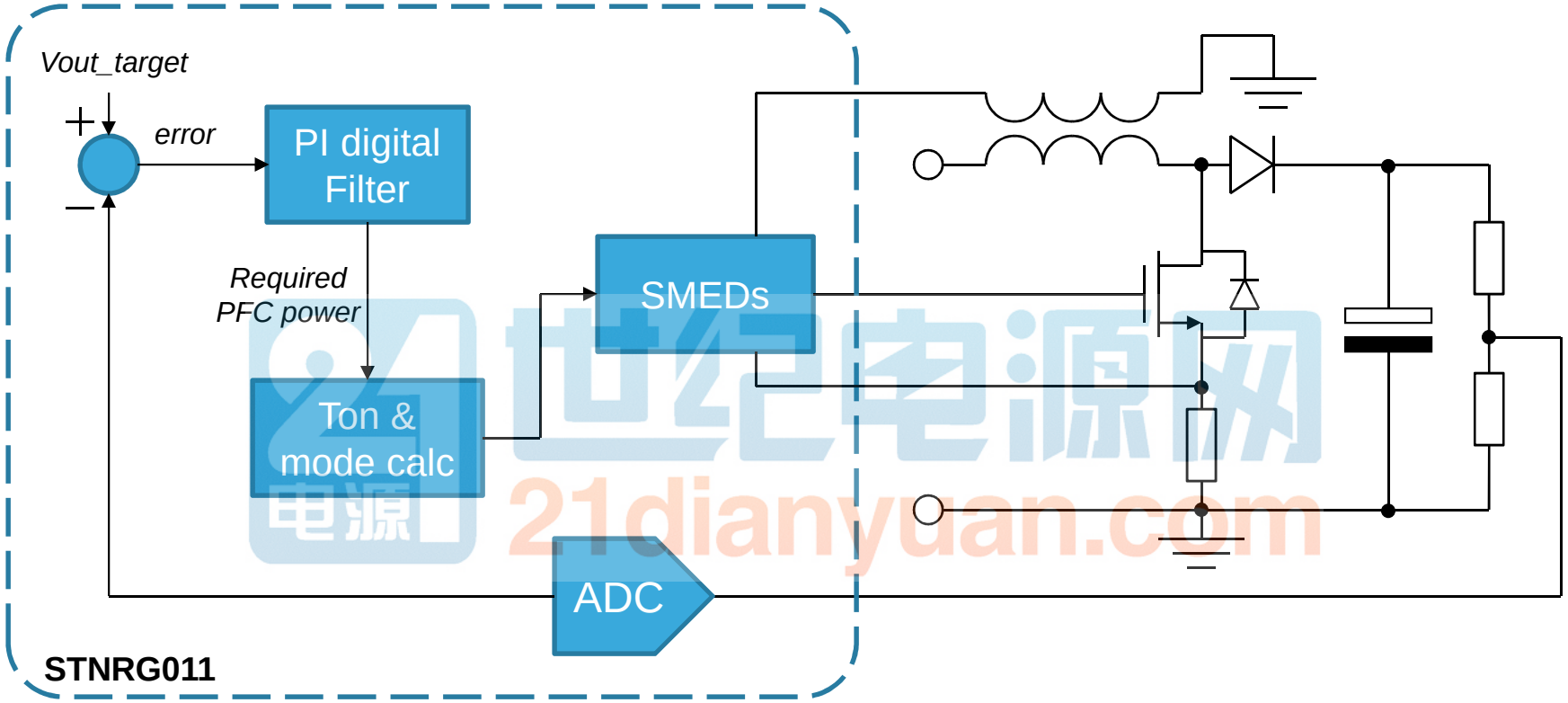
- ON-CHIP LV LS DRIVER:
- PFC topology
- Up to 20V
- 1A Peak Current Drive Capability

STNRG011 system concept



- STNRG011 addresses SMPS made of 2 stages:
  - TM PFC pre-regulator
  - Resonant LLC isolated DC/DC downstream converter

PFC control principle



- The PFC control loop is managed digitally
  - Vout is converted through the ADC
  - Compensation is done with a PI filter (calculation made by the core)
  - 2 coupled SMEDs generates the PWM signal

PFC algorithms

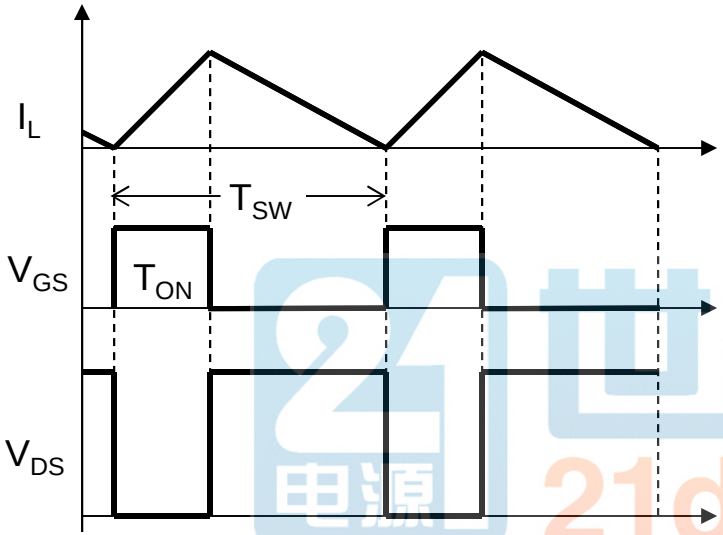
- Ramp Enhanced Constant On Time (ST patented) with 2 speed loop
  - Allows achieving very good PF & THD and dynamic performance
  - New “Ramp” compensation (patented) available: compensate input capacitive loads to achieve highest PF
- Multi mode operation
  - TM @ medium / high loads
  - TM, Valley skipping & skipping area @ low load
  - Burst mode @ very low load

ST Patents
US2013194842
US2013194845

ST Patent pending

PFC algorithm: the standard COT

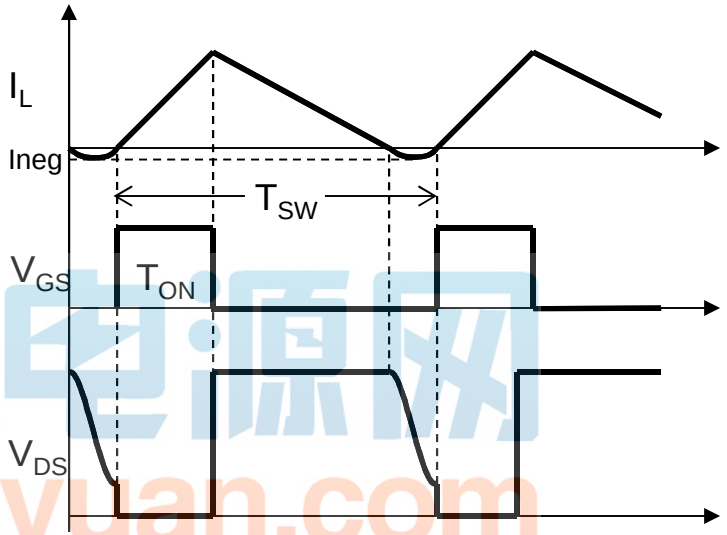
CCM / DCM boundary



$$\overline{Iin} = Vin_{pk} \cdot \sin\theta \cdot \frac{T_{ON}}{2 \cdot L}$$

- PRO & CON
  - Sinusoidal input current ➔ High PF & THD
  - High Vds @ turn-on ➔ high switching losses

TM

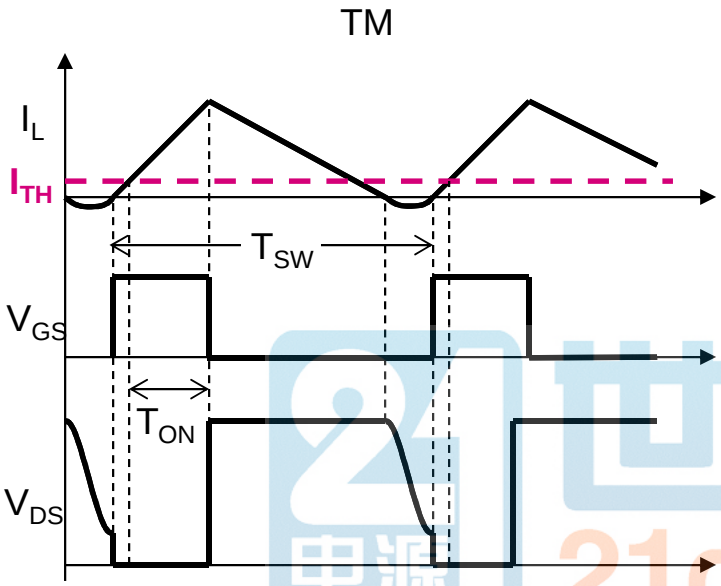


$$\overline{Iin} \approx Vin_{pk} \cdot \sin\theta \cdot \frac{T_{ON}}{2 \cdot L} - Ineg$$

$$Ineg = (Vo - Vin_{pk} \cdot \sin\theta) \cdot \sqrt{\frac{Coss}{L}}$$

- PRO & CON
  - Input current distortion ➔ Lower PF & THD
  - Lower Vds @ turn-on ➔ Lower switching losses

The eCOT



The GD is turned on like in the usual TM operation. The Ton is applied from the crossing of I_L of a threshold I_{TH}. By selecting an appropriate I_{TH}:

$$I_{TH} = Vo \cdot \sqrt{\frac{Coss}{L}} \qquad I_{pk} = I_{TH} + Vin_{pk} \cdot \sin\theta \cdot \frac{T_{ON}}{L}$$

$$\overline{Iin} \approx Vin_{pk} \cdot \sin\theta \cdot \frac{T_{ON}}{2 \cdot L} - Ineg + I_{TH}$$

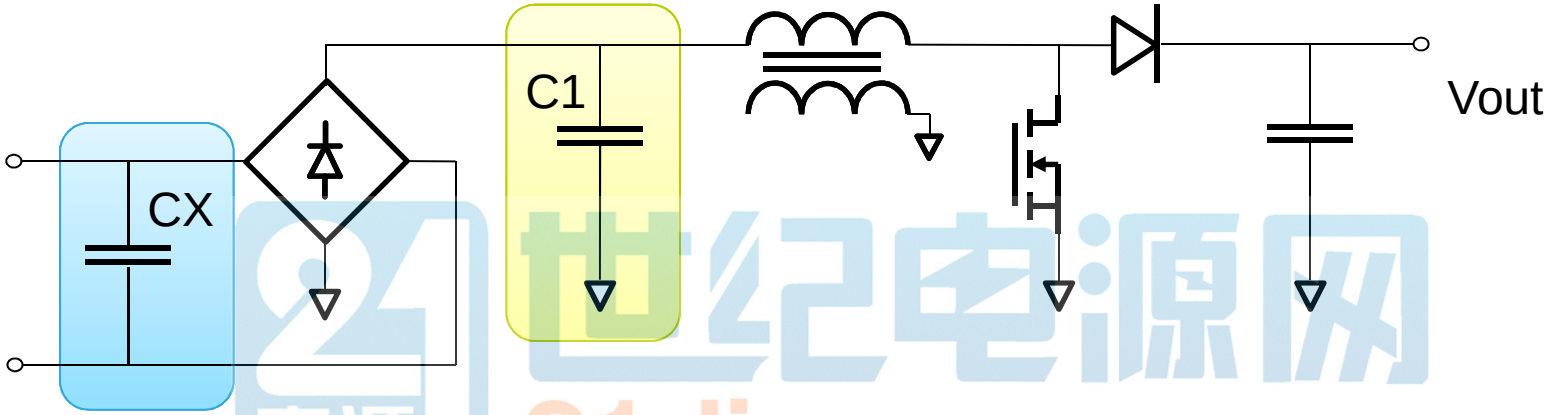
$$\overline{Iin} \approx Vin_{pk} \cdot \sin\theta \cdot \frac{T_{ON}}{2 \cdot L} - Ineg + Vin_{pk} \cdot \sin\theta \cdot \sqrt{\frac{Coss}{L}}$$

$$\boldsymbol{\overline{Iin} \approx K \cdot Vin_{pk} \cdot \sin\theta}$$

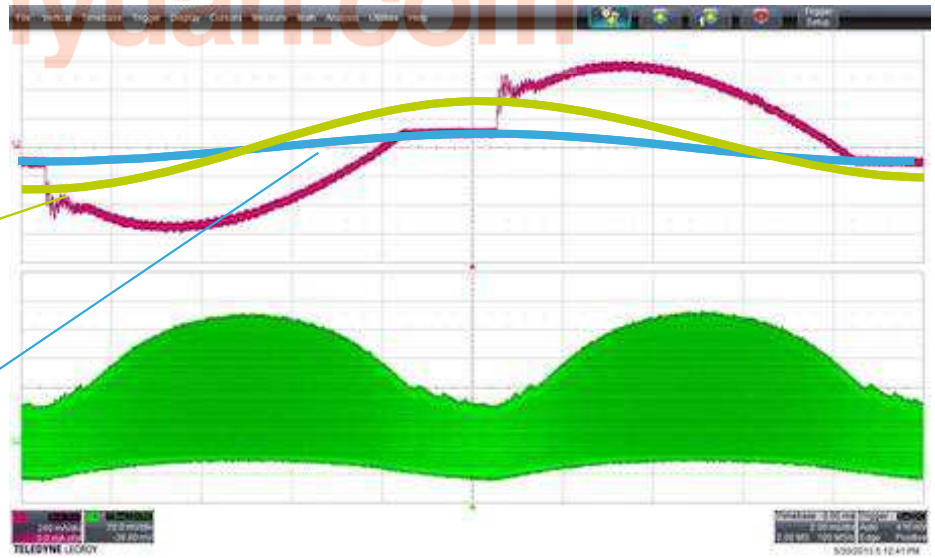
- Using eCOT is it possible to join the benefit of COT and TM:
  - Easy implementation
  - Low switching losses
  - High PF & THD

EMI capacitor

- All PFCs have one or more capacitors to filter current ripple



- Capacitor current is 90° out of phase
  - Power factor and distortion are impacted

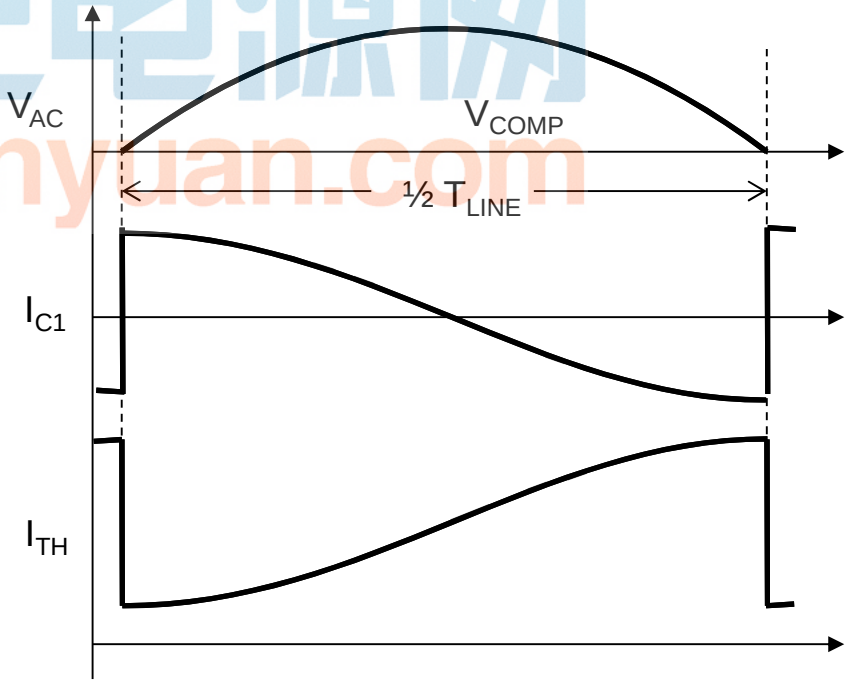


Ramp enhanced COT (ReCOT)

- I_{TH} can be used to shape PFC input current
- EMI capacitor current can be compensated by applying an opposite compensation
  - A linear ramp can be applied instead of a sinusoid
- Higher EMI capacitor can be used without affecting distortion and PF

$$v_{AC} = V_{PK} \sin \omega t$$

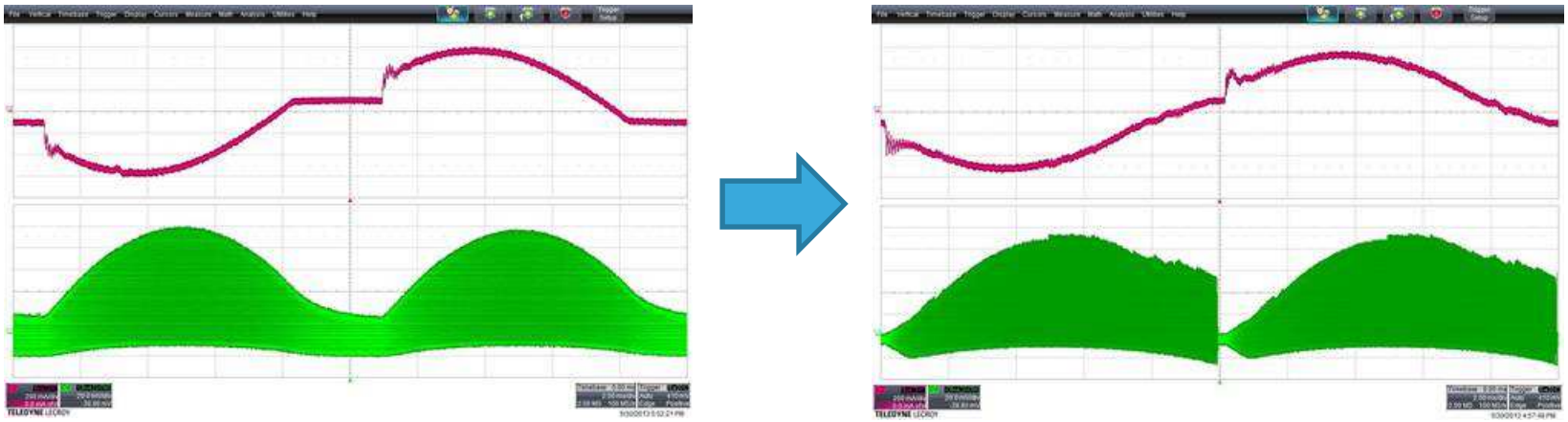
$$i_{C1} = C V_{PK} \omega \cos \omega t$$



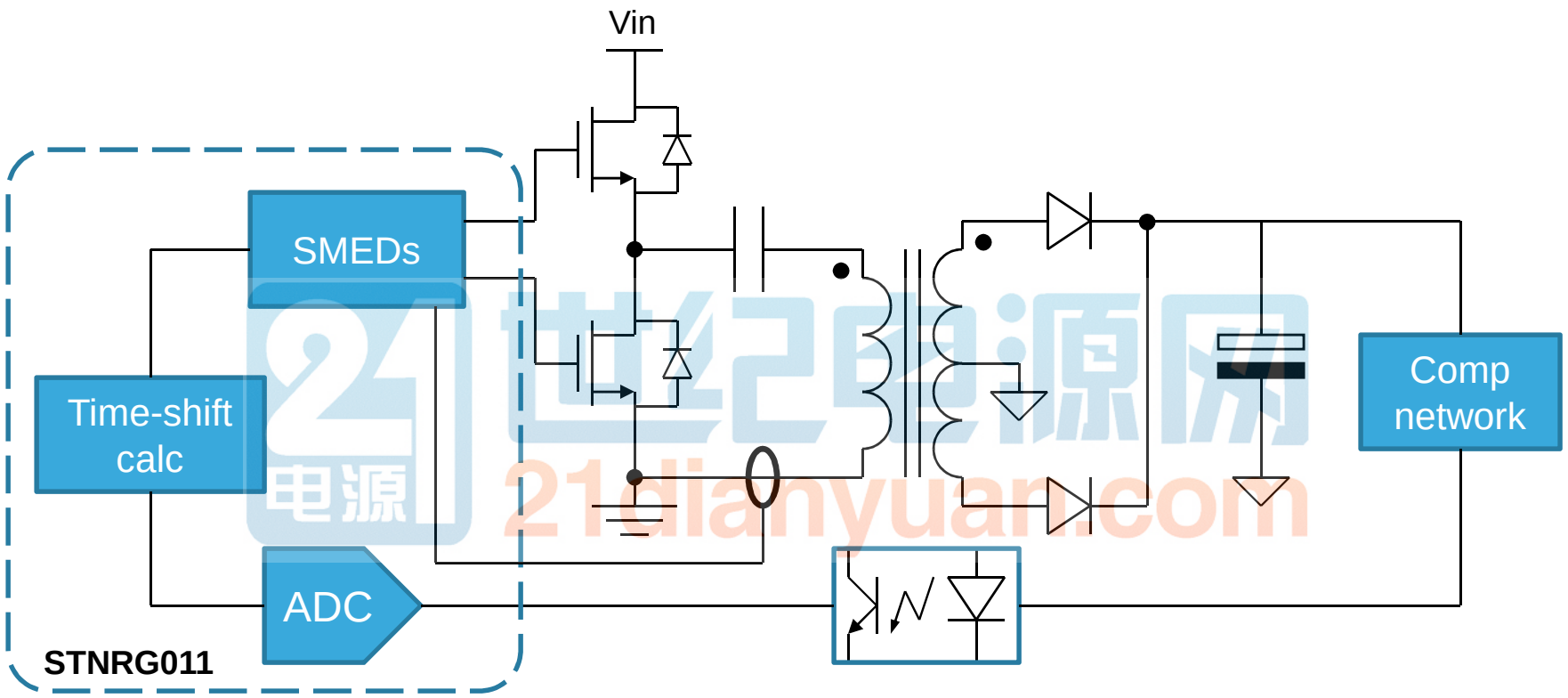
THD optimizer

- Enhanced Constant on time control allows also to considerably reduce the cross-over distortion due to the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage:
  - Defining the minimum current level before to start calculated Ton period allows PFC to process more energy as compared to that calculated by the control loop compensating not only the energy lost in MOS charging but also the inability of the system to transfer energy effectively when the instantaneous line voltage is very low

- Moreover Ramp E-COT allows compensating reactive energy (current) generated by big input filtering capacitor



LLC control principle



- The LLC control loop is managed in mixed mode
  - Compensation is done at secondary side with standard analog circuitry
  - The information from the optocoupler is sampled with the ADC
  - The core calculates the time shift and the SMEDs generates the HS & LS PWM

LLC algorithms

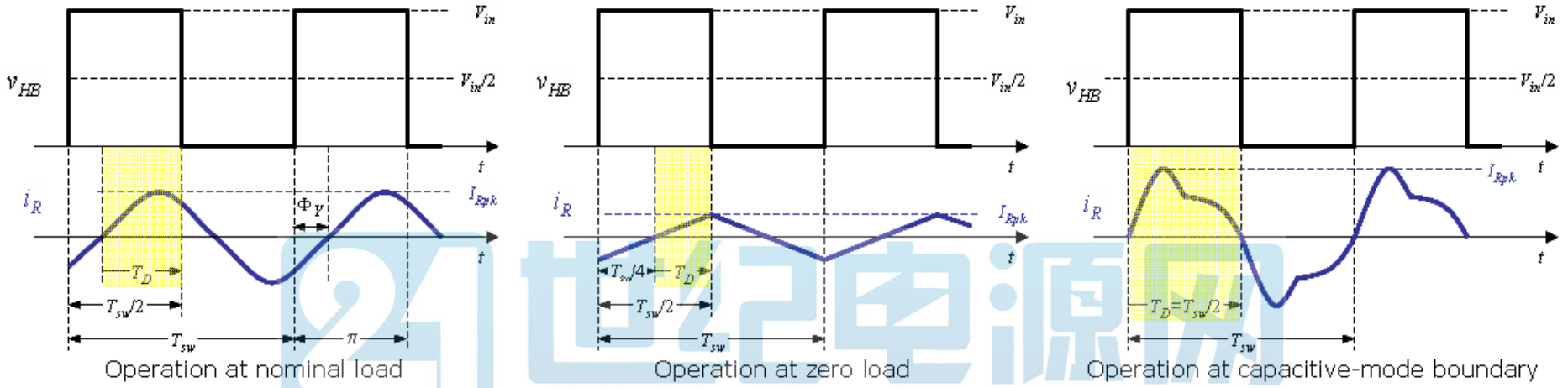
- Time-shift control (ST patented)
  - Improved dynamic performance
  - Easy compensation
  - Great input voltage ripple rejection (> 50dB)

- Advanced features & protections
  - Safe start
  - Anti Capacitive Protection
  - 2 levels Over Current management

- LLC stage drives Burst mode operation

Time shift concept

ST Patented



Operation at nominal load | Operation at zero load | Operation at capacitive-mode boundary

- Time-shift T_D is defined as **time elapsing from zero-crossing of tank current to next half-bridge toggling**
- A relationship exists between T_D and tank current phase-shift Φ_Y:

$$\Phi_Y = 180° \left(1 - 2\frac{T_D}{T_{SW}}\right)$$

- PWM is toggled T_D after tank current zero crossing
- T_D is calculated by µC based on ADC reading from FB

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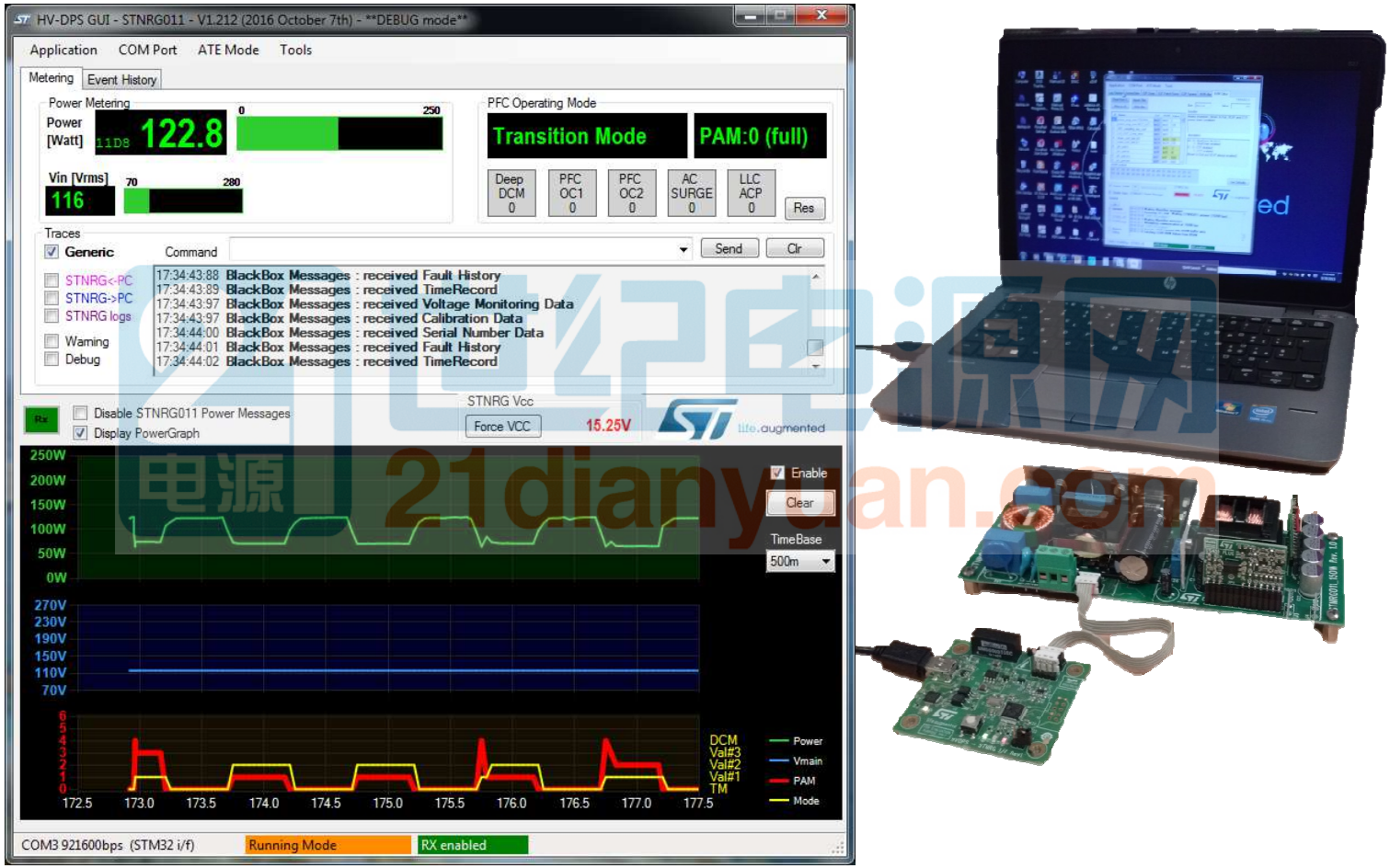
Time shift benefits vs DFC

- TSC makes LLC resonant converter dynamics very close to that of a first-order system
  - Frequency compensation is much easier
  - Response to perturbations is overdamped
- TSC improves load transient response
  - Overshoots and undershoots are nearly halved
  - Settling time is reduced 3-4 times
- TSC improves input ripple rejection
  - 100 Hz gain can be increased considerably
  - Rejection ratio increases by more than 15 dB
- TSC prevents hard switching at start-up
  - Converter reliability is improved

STNRG011 configurability

- STRNG011 allows the user to configure and optimize the system setting several parameters on its NVM (**N**on **V**olatile **M**emory)
- A complete tools system is available
  - Interface board to connect the STNRG011 board communication connector with the PC USB port
  - PC GUI
- A PC tool for PFC tuning

STNRG011 Ecosystem



STNRG011 NVM key parameters

- STNRG011 key parameters that can be adjusted via NVM (no HW changes)
  - Protections behavior (latch / autorestart)
  - Protections levels & timings
  - Comparators filtering & hysteresis
  - PFC soft start
  - PFC loop compensation
  - PFC light load behavior
  - PFC RECOT parameters (on the fly THD adjustment)
  - PFC maximum frequency
  - PFC nominal, minimum (UVP) and maximum (OVP) output voltages
  - LLC dead-time
  - LLC safe start & soft start parameters
  - Burst mode operation (in/out thresholds, burst pulses definition)

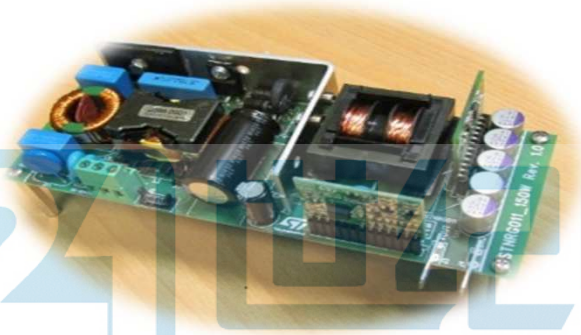
150W-12V STNRG011 evaluation board

Maximum efficiency: state of the art algorithms for PCF & LLC

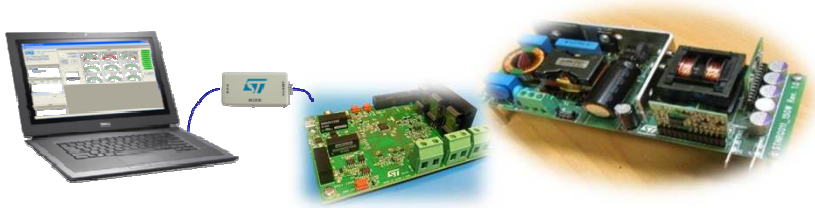
Communication: programmability and data monitoring

Fully Integrated solution: HV start-up & drivers

150W-12V adapter based on STNRG011 and SRK2001



GUI interface for easier configurability



STNRG011 → ***Eng Samples available*** → ***Board prototype available***

Industrial PS

All-in-One

High power adapters

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150W-12V STNRG011 evaluation board

- Board characteristics:
  - Input: 90 ÷ 264 Vac, 45 ÷ 65 Hz
  - Output: 12Vdc – 12.5A
  - No load: Pin < 100mW
  - MHR acc. EN61000-3-2 class D and JEITA-MITI class D
  - EMI acc. EN55022 class B
  - Black box & factory data features
  - I/F board & PC GUI available

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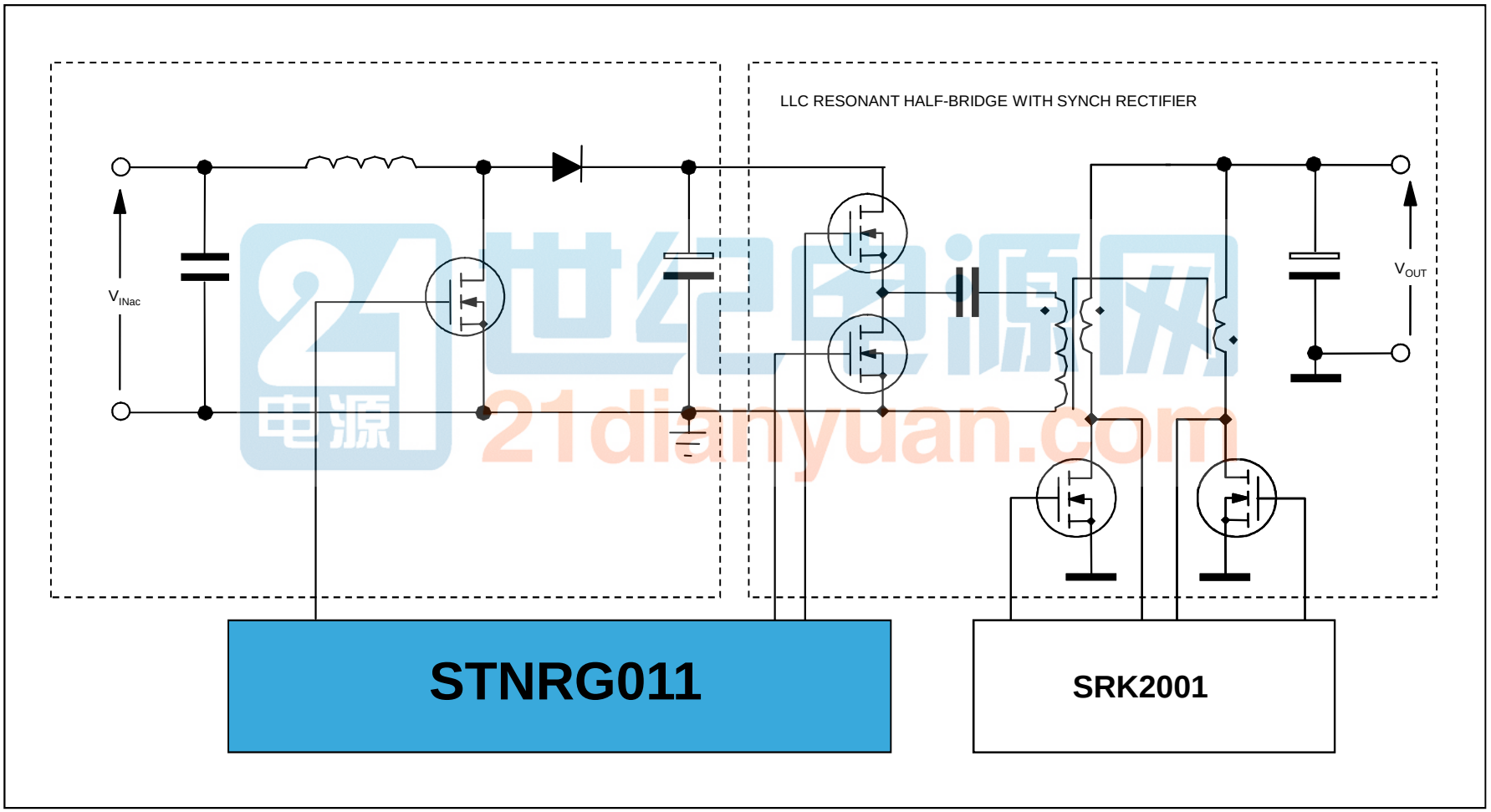
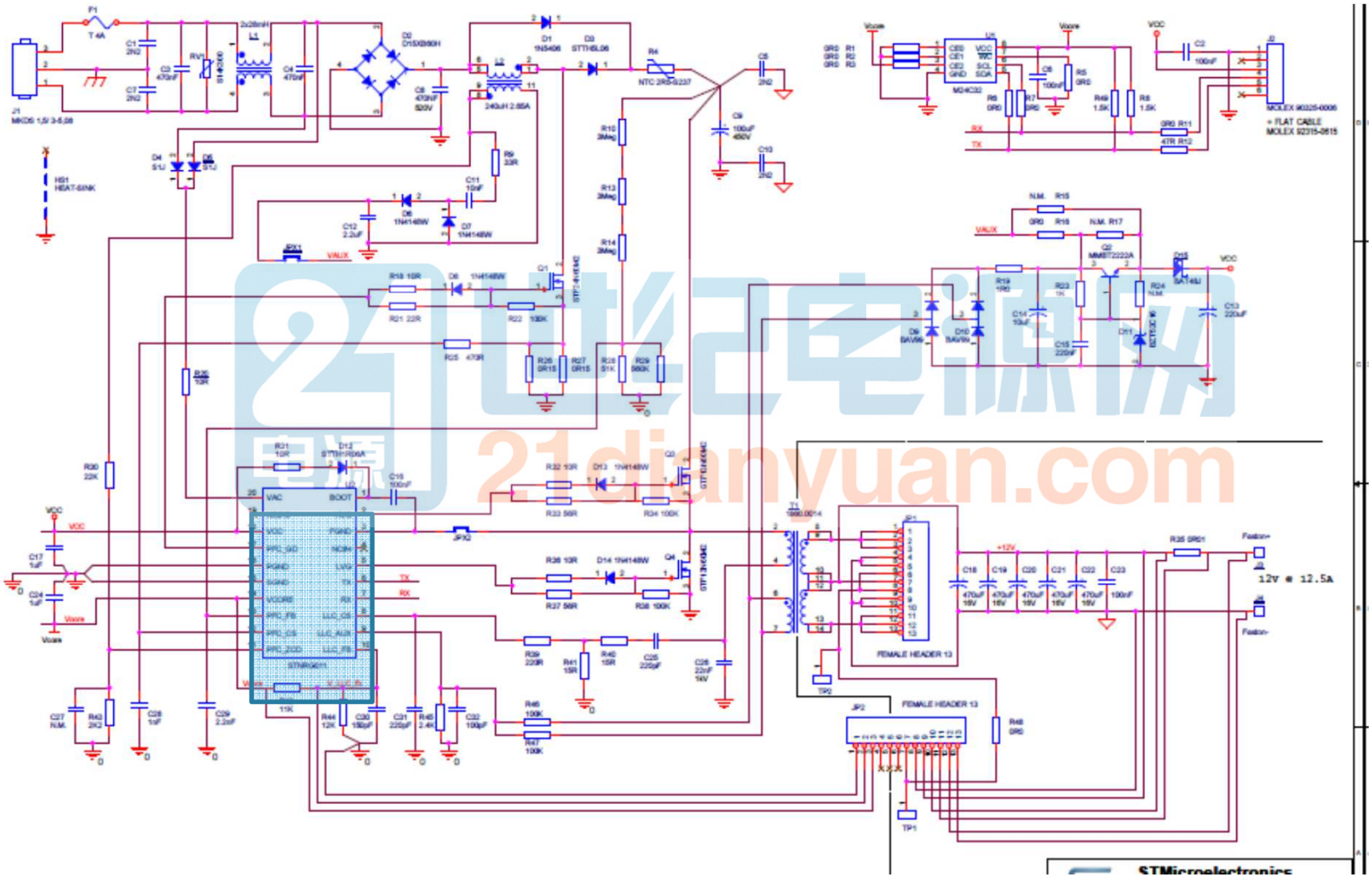
150W-12V Adapter block diagram



150W-12V Adapter schematic (MB)



150W adapter performance (preliminary)

115Vac	Vout	Iout	Pout	Pin	Eff	PF	THD
100mW	12.28	0.00887	0.108924	0.18	**60.51%**		
250mW	12.26	0.02082	0.255253	0.417	**61.21%**		
500mW	12.25	0.04178	0.511805	0.746	**68.61%**		
10%	12.03	1.2481	15.01464	17.95	**83.65%**		
20%	12.03	2.4975	30.04493	35.05	**85.72%**		
25%	12.03	3.1275	37.62383	43.11	**87.27%**		
50%	12.01	6.2418	74.96402	83.12	**90.19%**	0.984	6.10%
75%	11.99	9.3731	112.3835	122.99	**91.38%**		
100%	11.97	12.502	149.6489	163.66	**91.44%**	0.994	3.47%

No load	Pin
115 Vac	70 mW
230 Vac	93.4 mW

Excellent no load consumption!

4 points avg
90.03 %

230Vac	Vout	Iout	Pout	Pin	Eff	PF	THD
100mW	12.27	0.00887	0.108835	0.232	**46.91%**		
250mW	12.26	0.02087	0.255866	0.421	**60.78%**		
500mW	12.24	0.04179	0.51151	0.737	**69.40%**		
10%	12.02	1.2496	15.02019	17.48	**85.93%**		
20%	12.03	2.5125	30.22538	34.89	**86.63%**		
25%	12.03	3.1275	37.62383	42.44	**88.65%**		
50%	12.01	6.1237	73.54564	80.71	**91.12%**	0.933	8.55%
75%	11.99	9.3731	112.3835	121.47	**92.52%**		
100%	11.97	12.503	149.6609	161.07	**92.92%**	0.982	2.55%

4 points avg
91.30 %

Performance check

Eu Coc 5 EPS Tier 2	Limits	Result 115Vac	Result 230Vac	Status
4 points avg	> 0.87	0.900	0.913	Pass
Eff @ 10%	> 0.79	0.836	0.859	Pass
No load	< 0.15 W	0.07	0.0934	Pass

Energy star 6.0 for computer	Limits	Result 115Vac	Result 230Vac	Status
Eff @ 20%	> 0.82	0.857	0.866	Pass
Eff @ 50%	> 0.85	0.902	0.911	Pass
Eff @ 100%	> 0.82	0.914	0.929	Pass
PF @ 100%	> 0.9	0.994	0.982	Pass

DOE – EISA 2007 (from 2016)	Limits	Result 115Vac	Result 230Vac	Status
4 points avg	> 0.88	0.900	0.913	Pass
No load	< 0.15 W	0.07	0.0934	Pass

ErP Lot 7	Limits	Result 115Vac	Result 230Vac	Status
4 points avg	> 0.87	0.900	0.913	Pass
No load	< 0.5 W	0.07	0.0934	Pass

Additional ST Innovative solutions

ST new analog solution for SMPS up to 250W

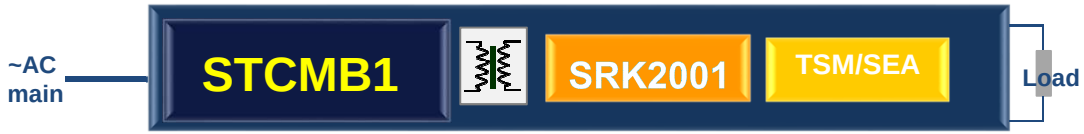
Consumer - TV, gaming

Computer - Adapters, AIO, ATX, Printers

Lighting - LED SMPS, Street Lighting

Other - Medical SMPS, open frame SMPS

Higher integration with smaller pin count vs. competition



competition

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ST Qualcomm® Quick Charge™

STQC30
QC 3.0 & QC2.0 (CLASS A)

ST chipset for Qualcomm® Quick Charge™

MP now!

STCH02

STCH03

SRK1000 (optional)

Samples now!

STQC30

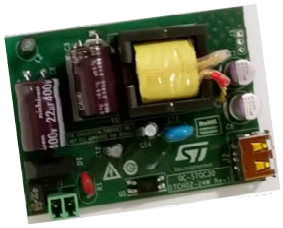
STQC30 COMPETITIVE ADVANTAGES

LESS COMPONENTS

- Full features in a compact package
- Discharge bleeder integrated
- Programmable current profiles

HIGH PERFORMANCE

- Low standby consumption
- Adaptive overvoltage protection
- Extended Vcc range (for operation lower than 3V)



[24W QuickCharger based on STQC30]

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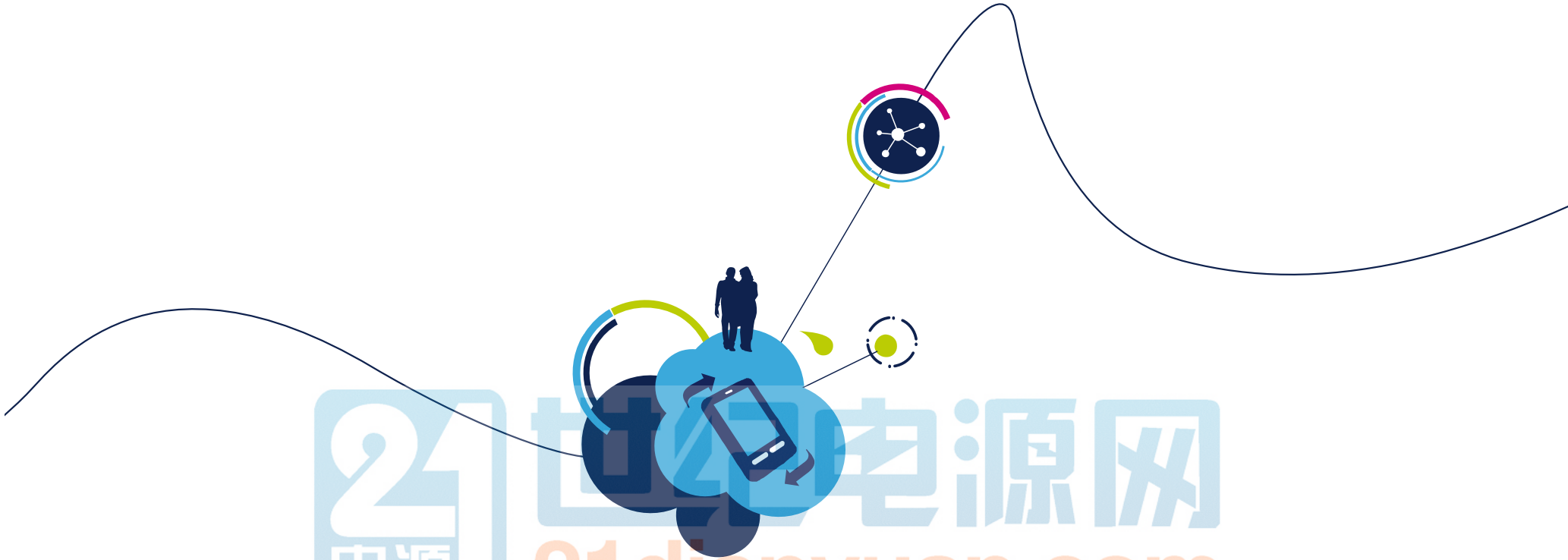

Thank You

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