

如何查看数据手册

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AHEAD OF WHAT'S POSSIBLE™

ADI 智库

一站式电子技术宝库

概述

- ▶ 数据手册的作用
- ▶ 如今您需要哪些信息?
- ▶ 产品选型
- ▶ 技术规格和条件
- ▶ 绝对最大额定值
- ▶ 热分析
- ▶ 工作原理和应用
- ▶ 封装和引脚排列
- ▶ 找到所需信息的方法
- ▶ 数据手册不包含的信息

数据手册的作用

▶ 产品描述

- 这款产品是否适合我的应用
- 功能和技术规格

▶ 用户手册

- 如何实现各种功能
- 如何连接
- DSP等复杂产品常常具有单独的编程手册

▶ 创意产生器

- 这款产品还可以做些什么
- 我可以实现哪些新应用

▶ 质保文档

- 保证何种性能
- 什么情况下质保失效

当下我需要做什么？

▶ 创意产生器

- 这款产品还可以做些什么
- 我可以实现哪些新应用

▶ 产品选型

- 这款产品是否适合我的应用
- 功能和技术规格

▶ 用户手册

- 如何实现各种功能
- 如何连接
- 我还需要什么
 - 软件
 - 连接产品
- 文档

选择产品 - 流程

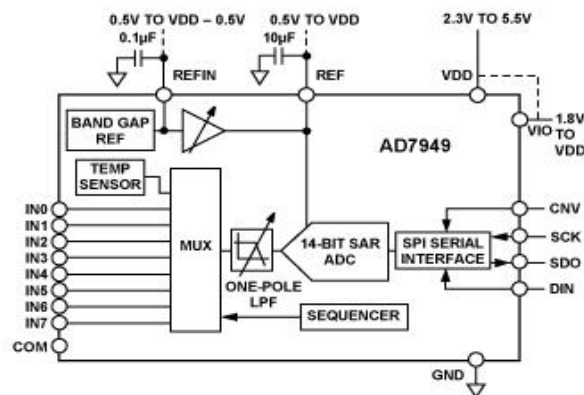
- ▶ 产品类型的一般描述
- ▶ 产品选型表

Apply Filters to this Table

Part#	Reference Circuit	Small Signal Bandwidth	Slew Rate	V Noise Density	Vos	Ib	Amplifiers Per Package	US Price 1000-4999
ADA4817-1	-	1.05GHz	870V/μs	4nV/rtHz	400μV	2pA	1	\$2.95
ADA4817-2	-	1.05GHz	870V/μs	4nV/rtHz	2mV	2pA	2	\$4.98
AD8067	-	54MHz	640V/μs	6.6nV/rtHz	200μV	600fA	1	\$1.89
AD8033	-	80MHz	80V/μs	11nV/rtHz	1mV	1.5pA	1	\$1.03
AD8066	YES	145MHz	180V/μs	7nV/rtHz	400μV	2pA	2	\$2.32
AD8034	YES	80MHz	80V/μs	11nV/rtHz	1mV	1.5pA	2	\$1.61
AD8065	YES	145MHz	180V/μs	7nV/rtHz	400μV	2pA	1	\$1.61
AD825	-	46MHz	140V/μs	12nV/rtHz	1mV	10pA	1	\$1.84

FEATURES	SPECIFICATIONS
<ul style="list-style-type: none"> 14-bit resolution with no missing codes 8-channel multiplexer with choice of inputs: Unipolar single ended Differential (GND sense) Pseudobipolar Throughput: 250 kSPS INL/DNL: ±0.5/±0.25 LSB typical Analog input range: 0 V to V_{REF} with V_{REF} up to VDD Multiple reference types Internal selectable 2.5 V or 	<p>AD7949-EP: SUPPORTS DEFENSE AND AEROSPACE APPLICATIONS (AQEC STANDARD)</p> <ul style="list-style-type: none"> Download AD7949-EP (Rev 0) Data Sheet Military temperature range (-55°C to +125°C) Controlled manufacturing baseline Enhanced product change notification Qualification data available on request


FUNCTIONAL BLOCK DIAGRAM FOR AD7949



Other Diagrams | Symbols and Footprints

选择产品 - 流程

- ▶ 一般技术规格和特性看起来不错
- ▶ 前往数据手册
- ▶ 完整技术规格
- ▶ 框图
- ▶ 详细说明
- ▶ 应用

**ANALOG
DEVICES**

**14-Bit, 8-Channel,
250 kSPS PulSAR ADC**

AD7949

Data Sheet

FEATURES

14-bit resolution with no missing codes
8-channel multiplexer with choice of inputs
Unipolar single-ended
Differential (GND sense)
Pseudobipolar
Throughput: 250 kSPS
INL/DNL: $\pm 0.5/\pm 0.25$ LSB typical
SINAD: 85 dB @ 20 kHz
THD: -100 dB @ 20 kHz
Analog input range: 0 V to V_{REF} with V_{REF} up to V_{DD}
Multiple reference types
Internal selectable 2.5 V or 4.096 V
External buffered (up to 4.096 V)
External (up to V_{DD})
Internal temperature sensor (TEMP)
Channel sequencer, selectable 1-pole filter, busy indicator
No pipeline delay, SAR architecture
Single-supply 2.3 V to 5.5 V operation with
1.8 V to 5.5 V logic interface
Serial interface compatible with SPI, MICROWIRE,
QSPI, and DSP
Power dissipation
2.9 mW @ 2.5 V/200 kSPS
10.8 mW @ 5 V/250 kSPS
Standby current: 50 nA
20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

Multichannel system monitoring
Battery-powered equipment
Medical instruments: ECG/EKG
Mobile communications: GPS
Power line monitoring
Data acquisition
Seismic data acquisition systems
Instrumentation
Process control

FUNCTIONAL BLOCK DIAGRAM

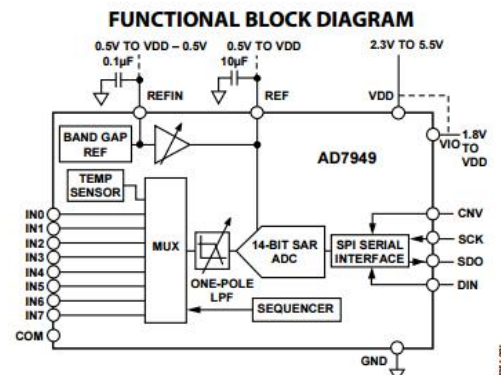


Figure 1.

0728 1001

Table 1. Multichannel 14-/16-Bit PulSAR* ADCs

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-1
16-Bit	4	AD7682		ADA4841-1
16-Bit	8	AD7689	AD7699	ADA4841-1

GENERAL DESCRIPTION

The **AD7949** is an 8-channel, 14-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, V_{DD} .

The **AD7949** contains all components for use in a multichannel, low power data acquisition system, including a true 14-bit SAR ADC with no missing codes; an 8-channel, low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The **AD7949** uses a simple SPI interface for writing to the

技术规格

- ▶ 产品性能详情
- ▶ 芯片公司可保证什么性能
- ▶ 所有重要且可测量的参数
 - 精度和速度
 - 时序
 - 电源要求

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		+V _{REF}	V
	Bipolar mode	-V _{REF} /2		+V _{REF} /2	V
Absolute Input Voltage	Positive input, unipolar and bipolar modes	-0.1		V _{REF} + 0.1	V
	Negative or COM input, unipolar mode	-0.1		+0.1	V
	Negative or COM input, bipolar mode	V _{REF} /2 - 0.1	V _{REF} /2	V _{REF} /2 + 0.1	V
Analog Input CMRR	f _{IN} = 250 kHz		68		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance ¹					
THROUGHPUT					
Conversion Rate					
Full Bandwidth ²	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
¼ Bandwidth ²	VDD = 4.5 V to 5.5 V	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8	µs
	Full-scale step, ¼ bandwidth			14.5	µs

技术规格 - 定义

- ▶ 许多数据手册具有“定义”或“术语”部分。
- ▶ 最常出现在专用产品中

TERMINOLOGY

Least Significant Bit (LSB)

The LSB is the smallest increment that can be represented by a converter. For an analog-to-digital converter with N bits of resolution, the LSB expressed in volts is

$$LSB (V) = \frac{V_{REF}}{2^N}$$

Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 24).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

- ▶ 否则，请搜索[ADI公司术语表](https://wiki.analog.com/university/courses/electronics/text/glossary)
 - <https://wiki.analog.com/university/courses/electronics/text/glossary>

技术规格 - 型号

- ▶ 产品系列中的不同型号
 - 不同技术规格、不同温度范围
 - 不同封装、不同发货包装（卷、盘、管等）
- ▶ 技术规格差异分列显示

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, VREF = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		+V _{REF}	V
	Bipolar mode	-V _{REF} /2		+V _{REF} /2	
Absolute Input Voltage	Positive input, unipolar and bipolar modes	-0.1		V _{REF} + 0.1	V
	Negative or COM input, unipolar mode	-0.1		+0.1	
	Negative or COM input, bipolar mode	V _{REF} /2 - 0.1	V _{REF} /2	V _{REF} /2 + 0.1	
Analog Input CMRR	f _{IN} = 250 kHz		68		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance ¹					
THROUGHPUT					
Conversion Rate					
Full Bandwidth ²	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
¼ Bandwidth ²	VDD = 4.5 V to 5.5 V	0		62.5	kSPS

测试条件 - 一般和特殊

- ▶ 技术规格页面上方的一般条件
- ▶ 适用于所有技术规格，除非被各技术规格的具体条件取代
 - 电源
 - 工作温度——通常为25°C
 - 输入信号范围
 - 基准电平、负载、增益设置等
- ▶ 运算放大器较为简单

(@ 25°C, $V_S = 5\text{ V}$, $R_L = 100\ \Omega$, $R_F = R_G = 750\ \Omega$ unless otherwise noted.)

- ▶ 数据转换器和其他产品则较为复杂

($V_{DD} = 5\text{ V} \pm 5\%$, $AGND = DGND = 0\text{ V}$, $V_{REF} = \text{Internal}$. Clock = Internal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

测试条件 - 一般和特殊

- ▶ 特殊条件显示在各技术规格所在行
- ▶ 说明测试和性能保证的条件
- ▶ 典型工作性能图显示较宽范围的性能

Intermodulation Distortion ³				fa = 49 kHz, fb = 50 kHz
2nd Order Terms	-95	-95	dB typ	
3rd Order Terms	-95	-95	dB typ	
Channel-to-Channel Isolation ^{3, 5}	-88	-88	dB max	f _{IN} = 50 kHz Sine Wave

OPEN-LOOP GAIN	V _{OUT} = ±10 V	±15 V	70	76	dB
	R _{LOAD} = 1 kΩ				
	V _{OUT} = ±7.5 V	±15 V	70	76	dB
	R _{LOAD} = 1 kΩ				
	V _{OUT} = ±7.5 V	±15 V			
	R _{LOAD} = 150 kΩ (50 mA Output)		68	74	dB

测试条件 - 一般和特殊

电源的具体参数指标

参数	符号	最小值	典型值	最大值	单位	测试条件/注释
欠压闭锁					V	下降阈值, V_{VIN} 和 V_{BAT_SNS} 中的较高值
迟滞		50	100	150	mV	迟滞, V_{VIN} 和 V_{BAT_SNS} 上升中的较高值 ¹
总输入电流	I_{LIM}	74	92	100	mA	标称USB初始化电流电平
		114		150		USB超高速
				300		USB枚举电流电平 (中国技术规格)
		425	470	500		USB枚举电流电平
				900		专用充电器输入
				1500		专用壁式充电器
VINx功耗	I_{QVIN}		2		mA	充电或LDO模式
	I_{QVIN_DIS}		280	450	μ A	DIS_IC1 = 高电平, $V_{ISO_B} < V_{VINx} < 5.5$ V
电池功耗	I_{QBATT}		20		μ A	LDO模式, $V_{ISO_S} > V_{BAT_SNS}$
				5	μ A	待机, 包括ISO_Sx引脚漏电流, $V_{VIN} = 0$ V, $T_J = -40^{\circ}\text{C}$ 至 $+85^{\circ}\text{C}$
			0.5	0.9	mA	待机, 电池监控器激活

测试条件 - 注释

- ▶ 页面底部的注释提供定义、说明和额外条件
- ▶ 小号字体

¹ See the Analog Inputs section.

² The bandwidth is set in the configuration register.

³ LSB means least significant bit. With the 5 V input range, one LSB = 305 μ V.

⁴ See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.

⁵ With VDD = 5 V, unless otherwise noted.

⁶ All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

⁷ This is the output from the internal band gap.

⁸ The output voltage is internal and present on a dedicated multiplexer input.

⁹ Unipolar mode: serial 14-bit straight binary.

Bipolar mode: serial 14-bit twos complement.

¹⁰ Conversion results available immediately after completed conversion.

¹¹ With all digital inputs forced to VIO or GND as required.

¹² During acquisition phase.

¹³ Contact an Analog Devices, Inc., sales representative for the extended temperature range.

最小值/最大值/典型值

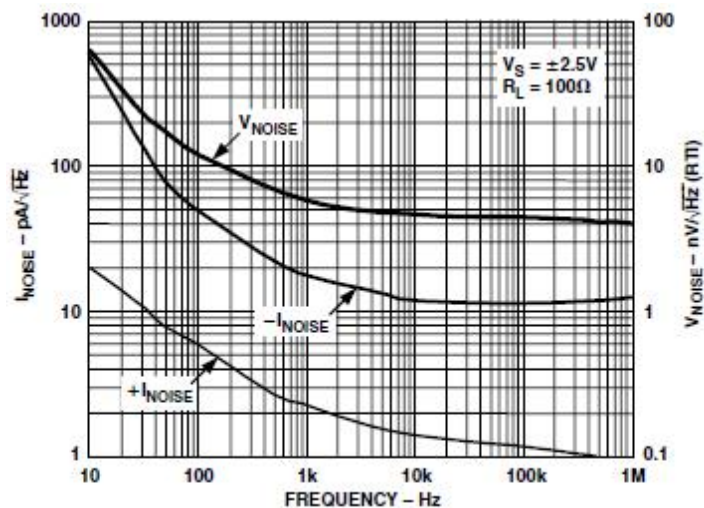
- ▶ 所有技术规格都有一系列分布值
- ▶ 如果说是典型值，常常不会进行测试
 - 产品发布时进行过特性测试
 - 某些器件高于该规格，某些器件低于该规格
 - 某些分布较为松散，某些则较为集中
 - 典型值技术规格由QA筛检
- ▶ 如果说是最小值或最大值，可能未经100%测试
 - 整个温度范围内的技术规格通过特性测试和保护带来保证
- ▶ 测试和技术规格由统计数据决定
 - 所有测试都有高斯分布噪声
 - 设置保护带的目的是将失效率保持在低ppm范围

All limits are determined to be at least four standard deviations away from mean value. At $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$ unless otherwise noted.

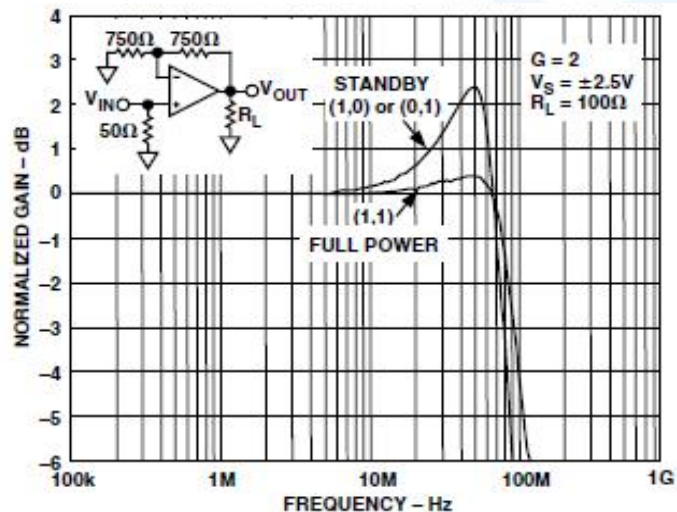
典型性能曲线(TPC)

- ▶ 典型性能曲线显示整个工作范围内的性能
 - 极有可能涵盖了您的目标工作范围
 - 对大量器件进行特性测试
 - 常常难以由用户测试
- ▶ 常常是产品选型的一个重要组成部分
 - 应用可能是非标准、不在技术规格的最佳使用条件下
 - 数据手册作者往往预设最常见的使用情形和工作条件

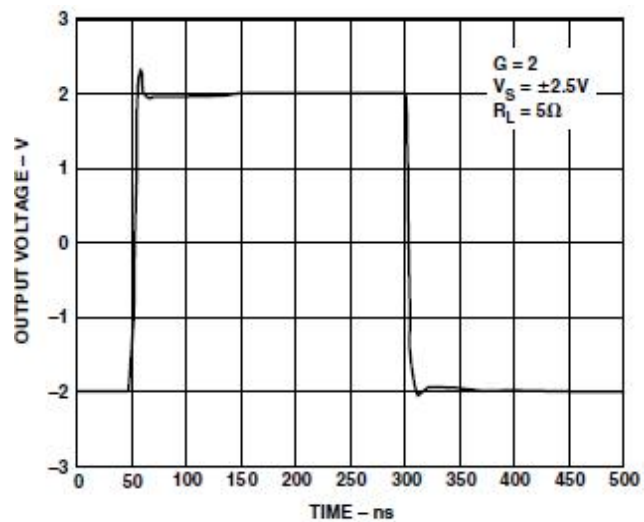
典型性能曲线(TPC)



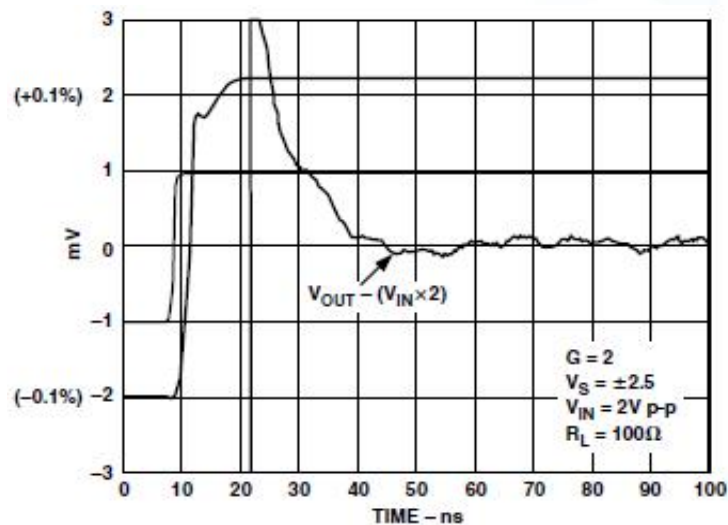
TPC 4. I_{NOISE} and V_{NOISE} vs. Frequency



TPC 11. Small Signal Frequency Response



TPC 3. Large Signal Step Response



TPC 6. 0.1% Settling Time

绝对最大额定值

- ▶ 该部分一般位于技术规格之后
- ▶ 描述会导致器件受损的限值
- ▶ 引脚之间的最大电压
- ▶ 流入/流出引脚的最大电流
- ▶ 使用和存储的最高温度
- ▶ 焊接和组装条件

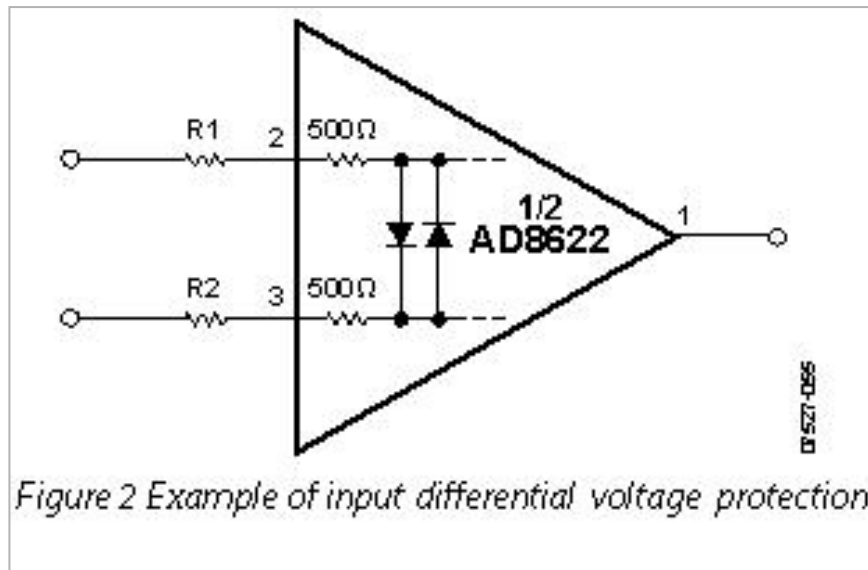
绝对最大额定值 - 建议

- ▶ 如果某一器件超过了绝对最大值，但仍能工作时该怎么办
 - 性能以隐蔽的方式受到损害
 - 如果是进行关键的性能测量，请更换器件
 - 不要将含有此类器件的评估设备发送给客户
- ▶ 不要采用接近最大额定值的电源供电
 - 电源噪声或瞬变可能导致电源供电超过最大额定值
 - 即使时间极短也会损坏绝缘氧化物并感应漏电路径，导致器件失效或性能受损

绝对最大额定值 - 难以觉察的问题

敏感的输入级

- 低压输入晶体管具有高增益和低噪声
- 保护电阻较小以便降低约翰逊噪声
- 差分输入被二极管限制在0.6V，因而大输入电压会产生大电流
- 外部电阻可以限制电流，但会增大误差
- 细致分析，在保护与精度之间取得平衡



散热考虑

- ▶ 所有IC都有一个芯片最大工作温度
 - 最高工作结温
 - 通常为125°C至150°C
 - 超过此温度会导致高漏电流，器件可能永久损坏
- ▶ 结温等于环境温度加自发热导致的温度升幅

自发热

▶ 自发热由功耗和热阻决定

▶ 示例:

- 芯片采用5V电源供电, 功耗为5mA

- $5V \times 5mA = 25mW = .025W$

- 热阻 $\Theta_{ja} = 115^{\circ}C/W$ (TSSOP)

- $0.025W \times 115^{\circ}C/W = 2.88^{\circ}C$ 温度升幅

- (不算大)

▶ 高电源时情况变得严重, 30V、10mA下为0.3W, 温度升幅为 $34.5^{\circ}C$

(请勿触摸)

自发热

- ▶ 自发热会降低器件可用的最大环境温度
- ▶ 通过降额曲线显示

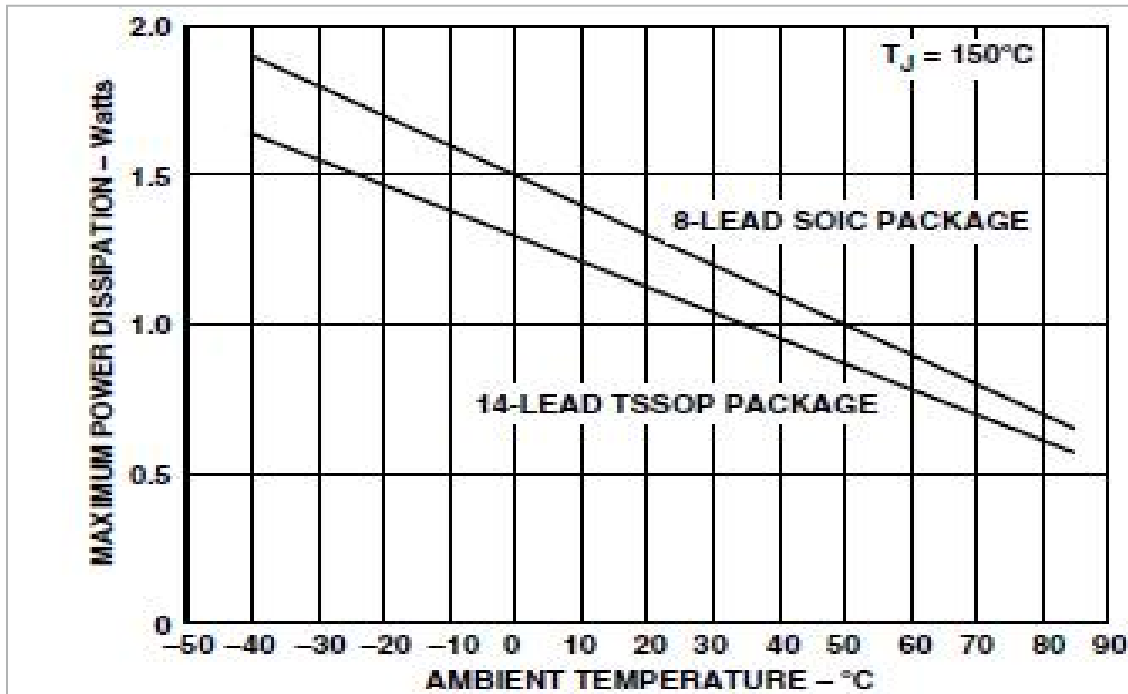


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

绝对最大额定值中的ESD警告

- ▶ ESD - 静电放电 - 所有数据手册
- ▶ 产品越新，ESD保护性能也越好，特别是那些采用外部连接的产品
- ▶ 在原型开发和测试期间，ESD防范措施仍然重要
- ▶ ESD故障可能不是灾难性的，只是会影响最高性能

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7865 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



封装吸湿性

- ▶ 数据手册中一般不提供
- ▶ 如果不是存储在受控环境下，小封装可能会吸收引脚下的水分
- ▶ 在300C回流焊周期中，引脚与封装之间的水分会汽化，导致封装开裂
- ▶ 产品经过烘烤，存储在干燥的运输材料中
- ▶ 最终组装之前，器件有一段时间会暴露在空气中
- ▶ 打开的包装仍然有未使用的产品，必须在时限内重新密封并干燥

湿气敏感度(MSL)

- ▶ 数据手册中一般不提供
- ▶ 材料声明中提供
- ▶ 通过报价/封装表获取
- ▶ MSL显示在包装材料上

MATERIAL DECLARATION SEARCH RESULTS

[RUN A NEW SEARCH](#) Go to Product Page

RoHS Compatible | Disclaimer Export to:

Showing 1-2 of 2 Product Matches Display 10 << < Page 1 of 1 > >

Remove	ADI Part Number	Family	PACKAGE TYPE	Lead Count	Body Size	Plating or Solder Sphere Finish	Tin/Lead Percentage	High Temp Compatible	MSL Rating	Peak Reflow Temperature (°C)	RoHS Compatible	Component Weight (milligrams)
<input type="checkbox"/>	AD7865	AD7865ASZ-1	MQFP	44	10X10X2.0(+3.9)	Matte Sn	100% Sn	Yes	3	260	Y	513
<input type="checkbox"/>	AD7865	AD7865ASZ-1REEL	MQFP	44	10X10X2.0(+3.9)	Matte Sn	100% Sn	Yes	3	260	Y	513

工作原理- 第一部分

- ▶ 详细说明器件如何工作及能做什么
- ▶ 有助于选择复杂的产品
 - 它可能不是像您需要的那样工作
 - ADC具有高吞吐速率，但延迟也长 - 应用要求立即返回数据
- ▶ 肯定有助于设置产品
 - 可回答它为什么这样工作之类的问题
- ▶ 可能会引发新的想法和应用产生

工作原理 - 第二部分

- ▶ 用户手册部分
- ▶ 工作原理再功能和设置描述部分
- ▶ 产品功能各方面的详细说明
- ▶ 描述每个功能
 - 电源与接地
 - 信号处理和负载
 - 接口
 - 软件支持 (如有)

框图和原理图

- ▶ 原理图显示输入和输出级以及一般结构

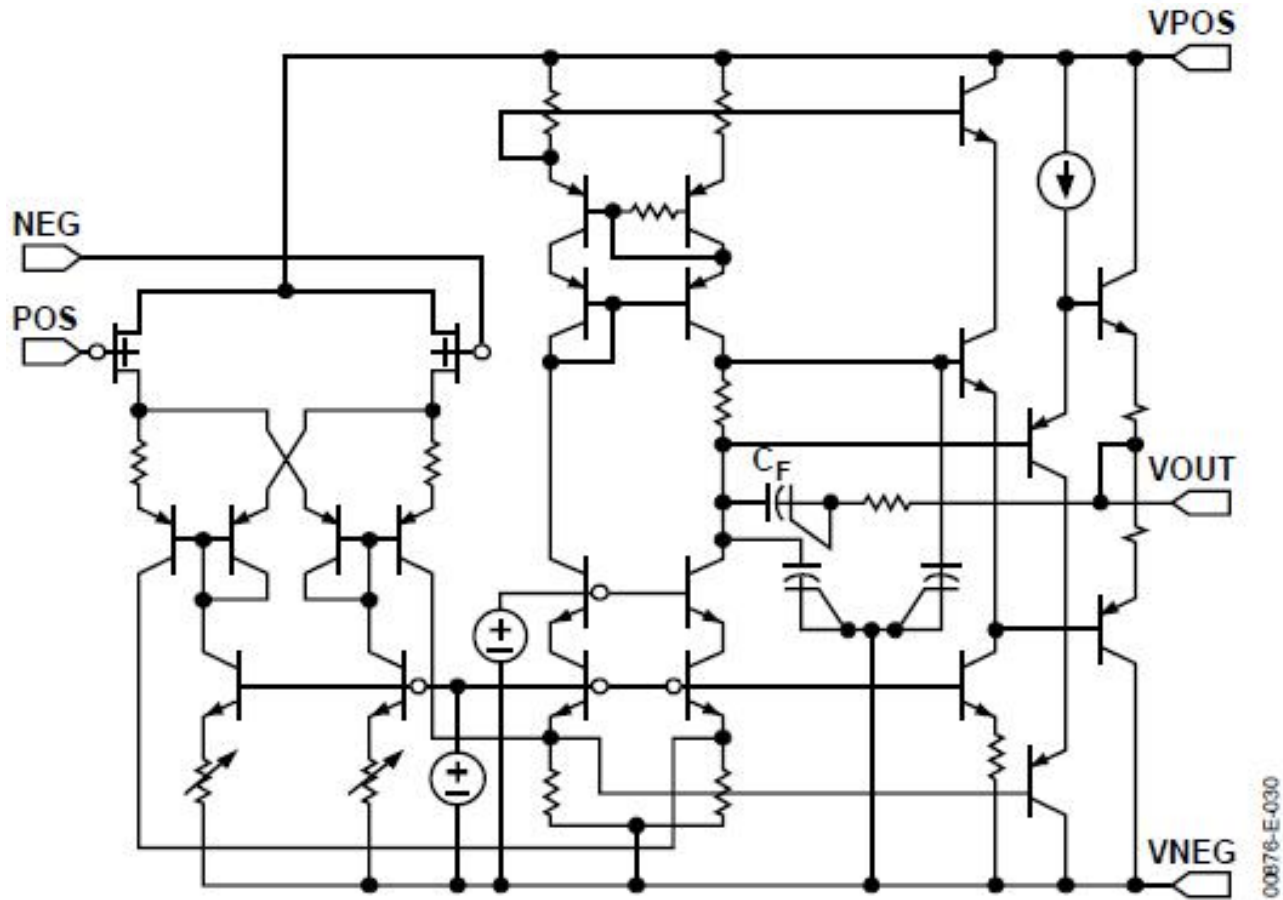
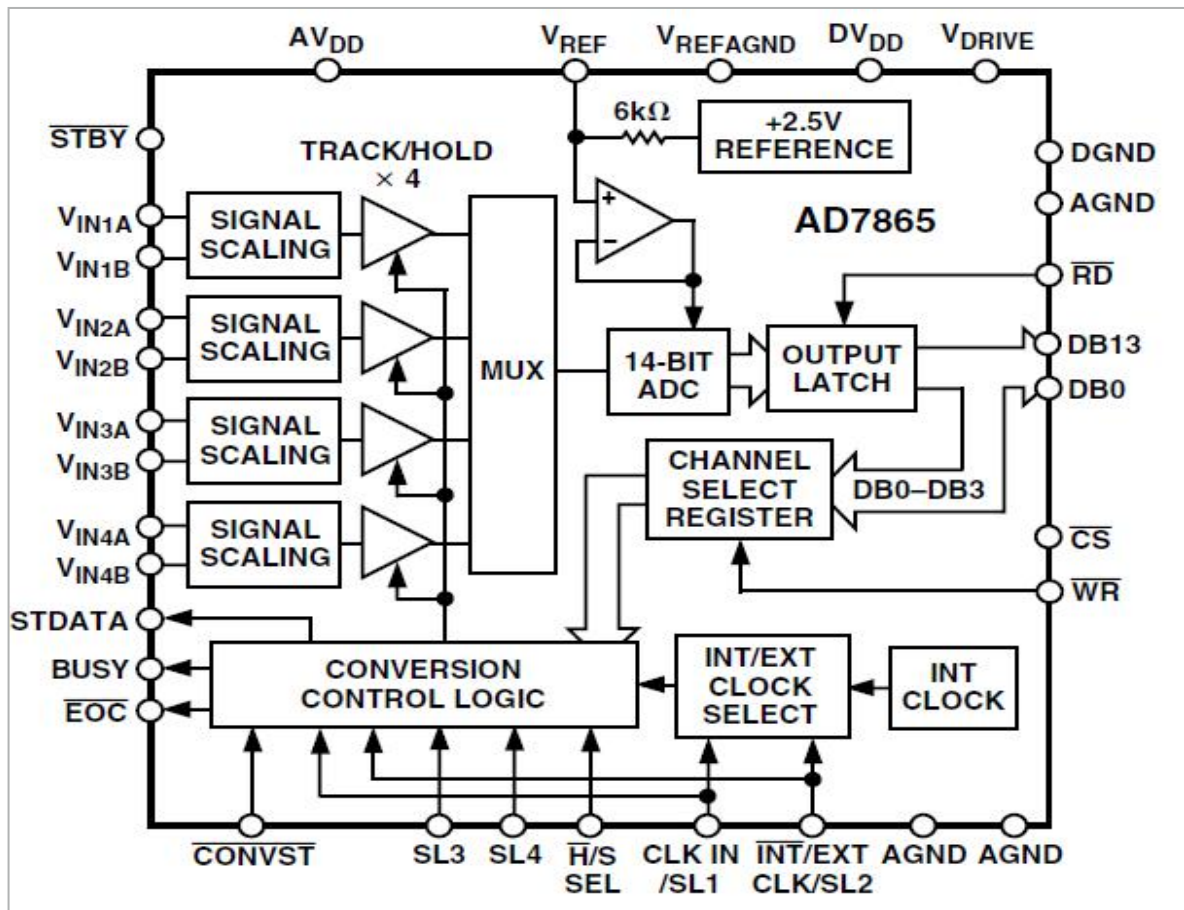


Figure 32. Simplified Schematic

框图和原理图

- ▶ 包含产品选型所需的大部分功能信息
- ▶ 内部结构和接口



引脚排列图

- ▶ 显示所有功能的连接
- ▶ 接地
 - 如果模拟地和数字地分别显示，切勿将引脚连接到错误的地
 - 一般在电源处连接模拟地和数字地
- ▶ 无连接或NC引脚
 - 有疑问时不要连接
 - 新标准 -- DNC
 - NC - 无内部连接 - 最好接地以实现低噪声性能
- ▶ 裸露散热焊盘
 - 检查连接点 - 可能不是地
 - 焊接到更大的铜焊盘以实现最佳散热效果

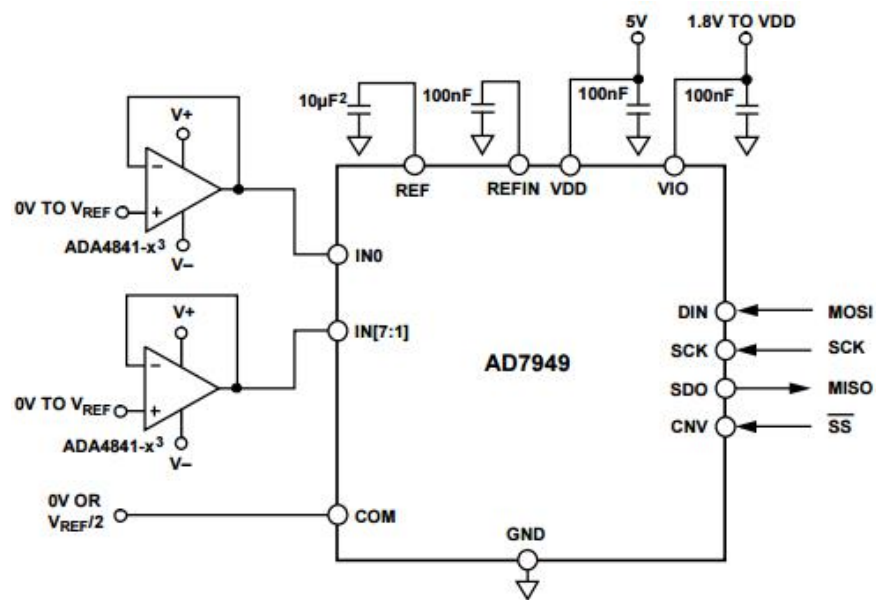
引脚排列描述

- ▶ 各引脚的详细说明
- ▶ 关于引脚连接的注释

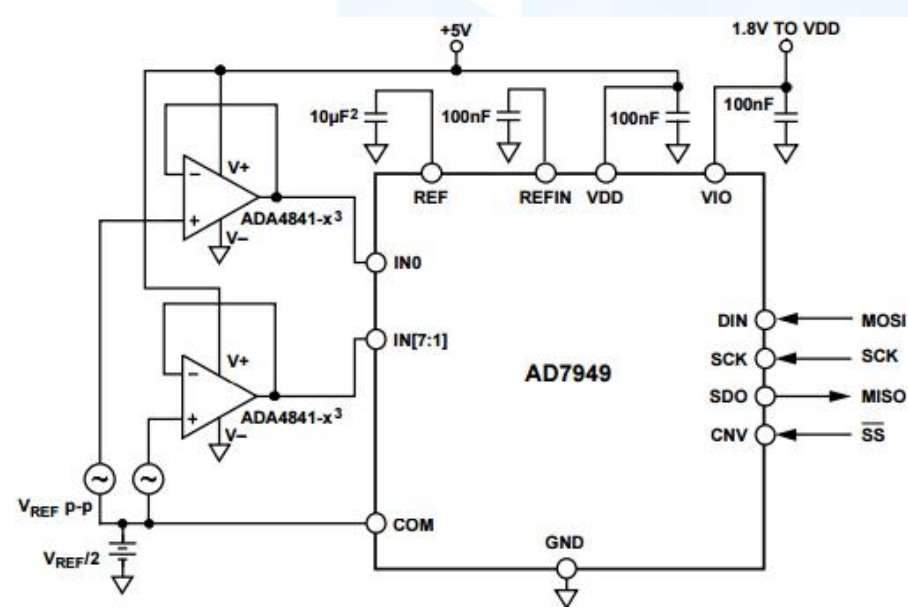
Pin No.	Mnemonic	Type ¹	Description
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 μ F and 100 nF capacitors. When using the internal reference for 2.5 V output, the minimum should be 3.0 V. When using the internal reference for 4.096 V output, the minimum should be 4.5 V.
2	REF	A/I/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference = 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096 V maximum), useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 μ F capacitor connected as close to REF as possible. See the Reference Decoupling section.
3	REFIN	A/I/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1 μ F capacitor. When using the internal reference buffer, apply a source between 0.5 V and 4.096 V that is buffered to the REF pin as described above.
4, 5	GND	P	Power Supply Ground.

典型应用

- ▶ 产品的最常见连接
- ▶ 常常显示技术规格的测试配置



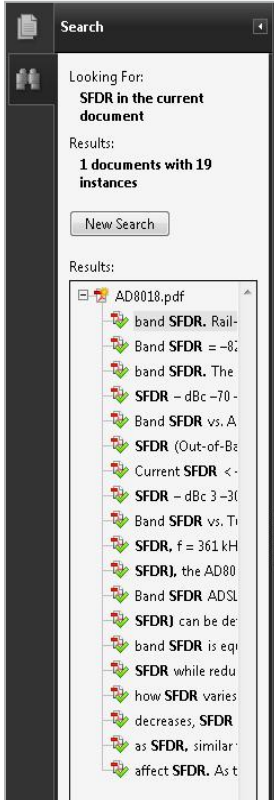
多个电源




双极性输入

Adobe Reader中的数据手册搜索工具

- ▶ 在左栏中打开搜索工具
- ▶ 点击“搜索”，输入搜索内容，在数据手册中查找相关内容





5 V, Rail-to-Rail, High-Output Current, xDSL Line Drive Amplifier

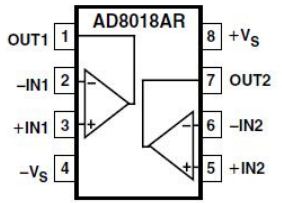
AD8018

FEATURES

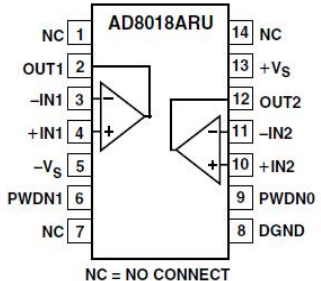
- Ideal xDSL Line Drive Amplifier for USB, PCMCIA, or PCI-Based Customer Premise Equipment (CPE). The AD8018 provides maximum reach on 5 V supply, driving 16 dBm of power into a back-terminated, transformer-coupled 100 Ω while maintaining -82 dBc of out-of-band SFDR.
- Rail-to-Rail Output Voltage and High Output Current Drive
- 400 mA Output Current into Differential Load of 10 Ω @ 8 V p-p
- Low Single-Tone Distortion
- -86 dBc Worst Harmonic, 6 V p-p into Differential 10 Ω @ 100 kHz

PIN CONFIGURATIONS

8-Lead SOIC (Thermal Coastline)



14-Lead TSSOP



NC = NO CONNECT

PRODUCT DESCRIPTION

Adobe Reader中的数据手册搜索工具

▶ 许多数据手册提供目录标签

Bookmarks

- FEATURES
- APPLICATIONS
- GENERAL DESCRIPTION
- FUNCTIONAL BLOCK DIAGRAM
- SPECIFICATIONS
- ABSOLUTE MAXIMUM RATINGS
- PIN CONFIGURATION
- MAXIMUM POWER DISSIPATION
- ORDERING GUIDE
- Typical Performance Characteristics
- THEORY OF OPERATION
 - Choice of Feedback and Gain Resistors
- PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS
- POWER SUPPLY BYPASSING
- DC ERRORS AND NOISE
- POWER CONSIDERATIONS
 - Other Power Considerations
 - Parallel Operation
 - Differential Operation
 - Creating Differential Signals
 - Direct Single-Ended-to-Differential Conversion
 - Two-Channel Video

ANALOG DEVICES

High Output Current Differential Driver

AD815

FEATURES

- Flexible Configuration**
 - Differential Input and Output Driver or Two Single-Ended Drivers
- Industrial Temperature Range**
- High Output Power**
 - Thermally Enhanced SOIC
 - 400 mA Minimum Output Drive/Amp, $R_L = 10 \Omega$
- Low Distortion**
 - 66 dB @ 1 MHz THD, $R_L = 200 \Omega$, $V_{OUT} = 40 \text{ V p-p}$
 - 0.05% and 0.45° Differential Gain and Phase, $R_L = 25 \Omega$
 - (6 Back-Terminated Video Loads)
- High Speed**
 - 120 MHz Bandwidth (-3 dB)
 - 900 V/ μs Differential Slew Rate
 - 70 ns Settling Time to 0.1%
- Thermal Shutdown**

APPLICATIONS

- ADSL, HDSL, and VDSL Line Interface Driver
- Coil or Transformer Driver
- CRT Convergence and Astigmatism Adjustment
- Video Distribution Amp
- Twisted Pair Cable Driver

GENERAL DESCRIPTION

The AD815 consists of two high speed amplifiers capable of supplying a minimum of 500 mA. They are typically configured as a differential driver enabling an output signal of 40 V p-p on $\pm 15 \text{ V}$ supplies. This can be increased further with the use of a coupling transformer with a greater than 1:1 turns ratio. The low harmonic distortion of -66 dB @ 1 MHz into 200 Ω

FUNCTIONAL BLOCK DIAGRAM

NC = NO CONNECT
*HEAT TABS ARE CONNECTED TO THE POSITIVE SUPPLY.

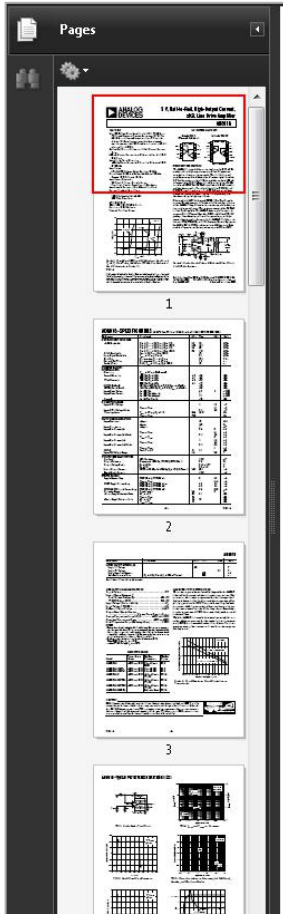
combined with the wide bandwidth and high current drive make the differential driver ideal for communication applications such as subscriber line interfaces for ADSL, HDSL and VDSL.


The AD815 differential slew rate of 900 V/ μs and high load drive are suitable for fast dynamic control of coils or transformers, and the video performance of 0.05% and 0.45° differential gain and phase into a load of 25 Ω enable up to 12 back-terminated loads to be driven.

The 24-lead SOIC (RB) is capable of driving 26 dBm for full rate ADSL with proper heat sinking.

Adobe Reader中的数据手册搜索工具

- ▶ 点击“页面”以获得各页的缩略图，从而执行快速搜索



 **ANALOG
DEVICES**

5 V, Rail-to-Rail, High-Output Current, xDSL Line Drive Amplifier

AD8018

FEATURES
Ideal xDSL Line Drive Amplifier for USB, PCMCIA, or PCI-Based Customer Premise Equipment (CPE). The AD8018 provides maximum reach on 5 V supply, driving 16 dBm of power into a back-terminated, transformer-coupled 100 Ω while maintaining -82 dBc of out-of-band SFDR.

Rail-to-Rail Output Voltage and High Output Current Drive
400 mA Output Current into Differential Load of 10 Ω @ 8 V p-p

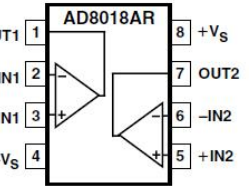
Low Single-Tone Distortion
-86 dBc Worst Harmonic, 6 V p-p into Differential 10 Ω @ 100 kHz

Low Noise
4.5 nV/ $\sqrt{\text{Hz}}$ Voltage Noise Density, 100 kHz
Out-of-Band SFDR = -82 dBc, 144 kHz to 500 kHz,
 $R_{\text{LOAD}} = 12.5 \Omega$, $P_{\text{LINE}} = 13 \text{ dBm}$

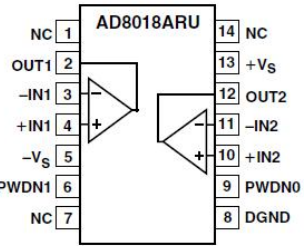
Low-Power Operation
3.3 V to 8 V Power Supply Range

PIN CONFIGURATIONS

8-Lead SOIC (Thermal Coastline)



14-Lead TSSOP



NC = NO CONNECT

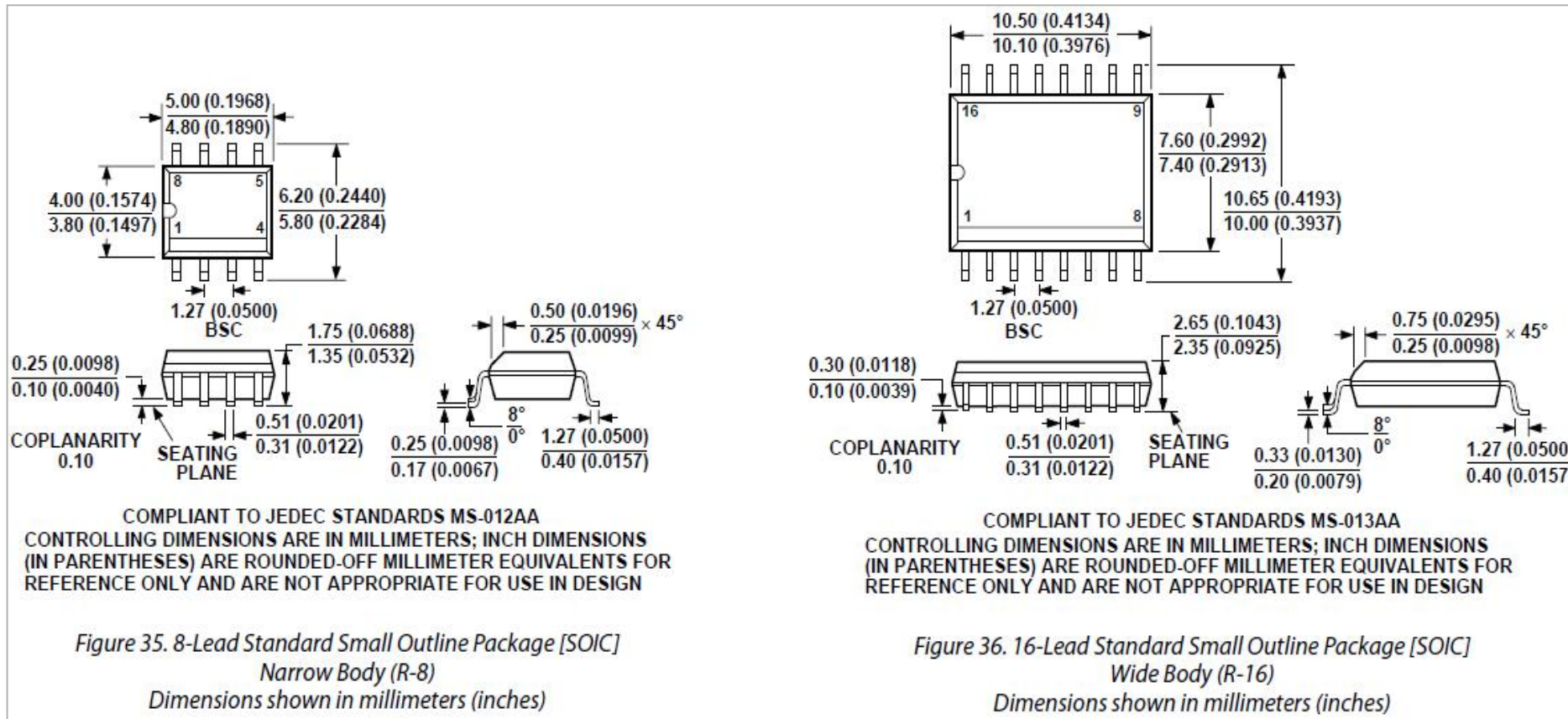
PRODUCT DESCRIPTION
The AD8018 is intended for use in single-supply (5 V) xDSL modems where high-output current and low distortion are essential to achieve maximum reach. The dual high-speed amplifiers are capable of driving low distortion signals to within 0.5 V of the power supply rail. Each amplifier can drive 400 mA of current into 10 Ω (differential) while maintaining -82 dBc

修订历史

- ▶ 并非所有制造商都提供
- ▶ ADI公司在第2页提供修订历史（较早数据手册是在最后一页）
- ▶ 列出各版本的出版日期
- ▶ 简要列出相对于上一版的修改项目
- ▶ 技术规格变更也会通过PCN发送

REVISION HISTORY	
10/04—Data Sheet Changed from Rev. E to Rev. F	
Changes to Figure 1.....	1
Changes to Figure 4.....	5
Changes to Figure 21.....	8
3/04—Data Sheet Changed from Rev. D to Rev. E	
Changes to Specifications.....	3
Addition of 16-Lead SOIC Pin Configuration	5
Changes to Figure 27.....	9
Updated Outline Dimensions.....	12
Updated Ordering Guide.....	12
2/01—Data Sheet Changed from Rev. C to Rev. D	
Addition of 16-lead SOIC package (R-16)	
Connection Diagram	4
Addition to Absolute Maximum Ratings	4

封装图纸 - 外形尺寸

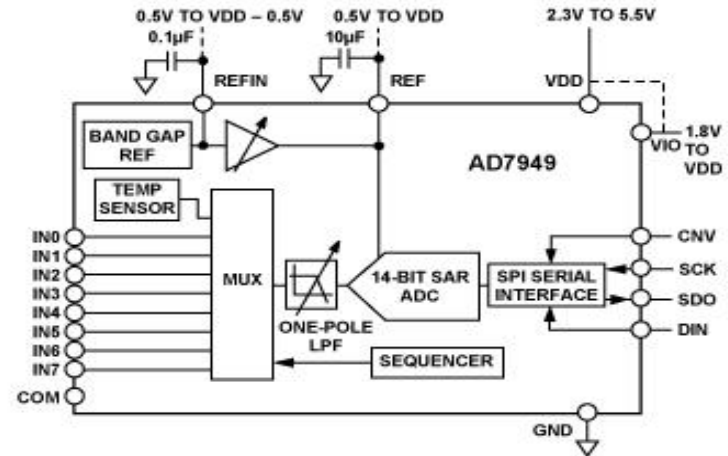


产品所有可用封装的比例图

封装图纸 - 外形尺寸

- ▶ 通常位于数据手册的末尾
- ▶ 您需要的是封装的尺寸
 - 每个产品和封装均提供
 - 利用Ultra Librarian和BXL文件支持多PCB布局封装
 - ORCAD、PCAD、PowerPCB、Eagle、BoardStation、AutoCAD等
- ▶ 可通过网站访问
- ▶ 产品页面
- ▶ 包括原理图
- ▶ 布局图

FUNCTIONAL BLOCK DIAGRAM FOR AD7949



[Other Diagrams | Symbols and Footprints](#)



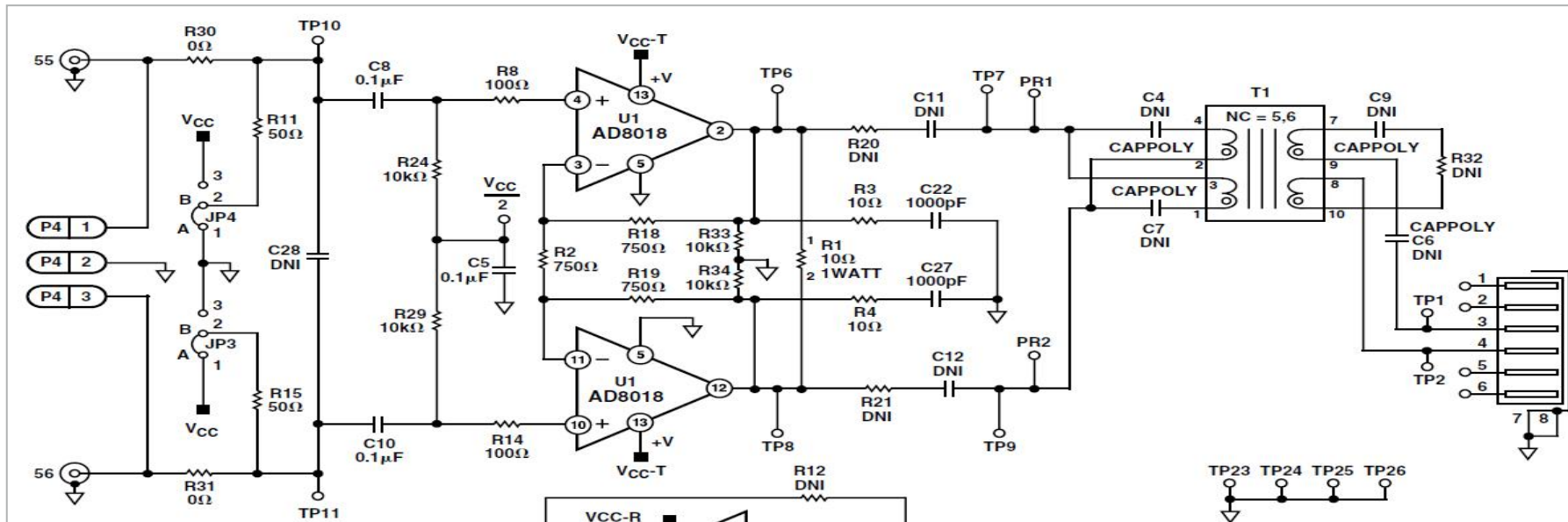
订购指南

- ▶ 通常在数据手册的最后一页
- ▶ 列出所有可供销售的型号及完整的订购代号
- ▶ 包括温度范围、封装类型、主要技术规格
- ▶ 网站上的产品页面显示同样的型号以及报价和供货情况
- ▶ 小型封装显示标识码

ORDERING GUIDE				
Model	Temperature Range	Package Description	Package Option	Branding
AD8038AR	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AR-REEL	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AR-REEL7	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ-REEL ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038ARZ-REEL7 ¹	-40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8038AKSZ-R2 ¹	-40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C
AD8038AKSZ-REEL ¹	-40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C
AD8038AKSZ-REEL7 ¹	-40°C to +85°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	H1C

评估板

- ▶ 几乎所有产品都提供评估板，以使用户在各种工作模式下快速、准确地测试产品
- ▶ 大多数评估板的操作说明是通过单独的数据手册或用户指南提供
- ▶ 评估板的布局优化了产品性能
- ▶ 提供大多数评估板的Gerber文件
- ▶ 布局和BOM在数据手册或用户指南中提供



数据手册不包含的信息

- ▶ 报价
 - 报价不固定，取决于地域和订货量
 - 订购指南列出供货的型号
- ▶ 库存
- ▶ 湿气敏感度
- ▶ 质量和可靠性
- ▶ 评估板操作
 - 单独的数据手册
- ▶ 最新的技术支持信息
 - 查看网站 - ADI [EngineerZone中文技术论坛](http://ez.analog.com) 等版块 (<http://ez.analog.com>)

其他有用信息

- ▶ 数据手册的末尾一般有空白页。出于印刷格式需要，空白页4页一组。
- ▶ 可以找到旧版数据手册，但不能立即获得
- ▶ 数据手册中显示的软件一般可供下载

其他信息来源

▶ 网站

- 产品页面
 - 类似产品
 - 报价
- 封装详细信息 - 材料
- 应用笔记和技术文章
 - 有关特定应用的更详细说明
- 参考设计
- 在线和可下载功能模型
- 质量和可靠性
- 仿真模型
 - SPICE
 - IBIS
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 - 技术支持

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- ADL5567 & AD9625 Analog Signal Chain Evaluation and ADF4355-2 Wideband Synthesizer with VCO
- ADL5567 Evaluation Board

Documentation

Data Sheet

- ADL5567: 4.3 GHz, Ultrahigh Dynamic Range, Dual Differential Amplifier Data Sheet

Reference Materials

Technical Articles

- Designing High Speed Analog Signal Chains from DC to Wideband
-

Design Resources

- ADL5567 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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Submit a technical question or find your regional support number

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