

12V Synchronous Buck PWM Controller

General Description

EM5301F/G is a synchronous rectified PWM controller operating with 12V supply voltage. This device operates at 160/200 kHz and provides an optimal level of integration to reduce size and cost of the power supply.

This part includes internal soft start, over current protection, under voltage protection, over voltage protection, and shutdown function. This part is available in PSOP-8 package.

Ordering Information

Part Number	Package	Frequency
EM5301FGE	PSOP-8	160kHz
EM5301GGE	PSOP-8	200kHz

Features

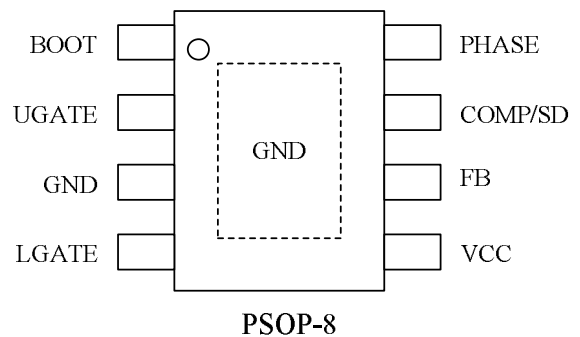
- Operate from 12V Voltage Supply
- 0.8V V_{REF} with 1.0% Accuracy
- Voltage Mode PWM Control
- 160kHz or 200kHz Fixed Frequency Oscillator
- 0% to 80% Duty Cycle
- Internal Soft Start
- Over Current Protection
- Integrated Bootstrap Diode
- Adaptive Non-Overlapping Gate Driver
- Under Voltage Protection
- Over Voltage Protection

Applications

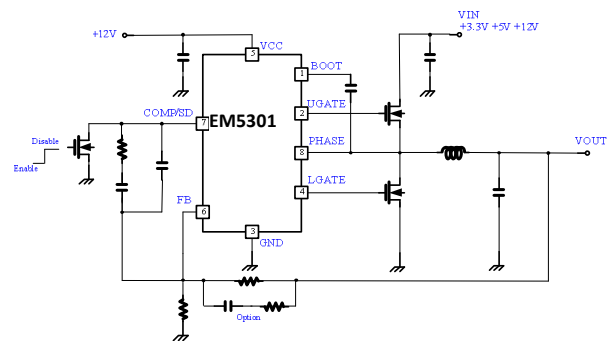
- Notebook & Netbook
- Graphic Cards & MB
- Low Voltage Logic Supplies



Pin Configuration



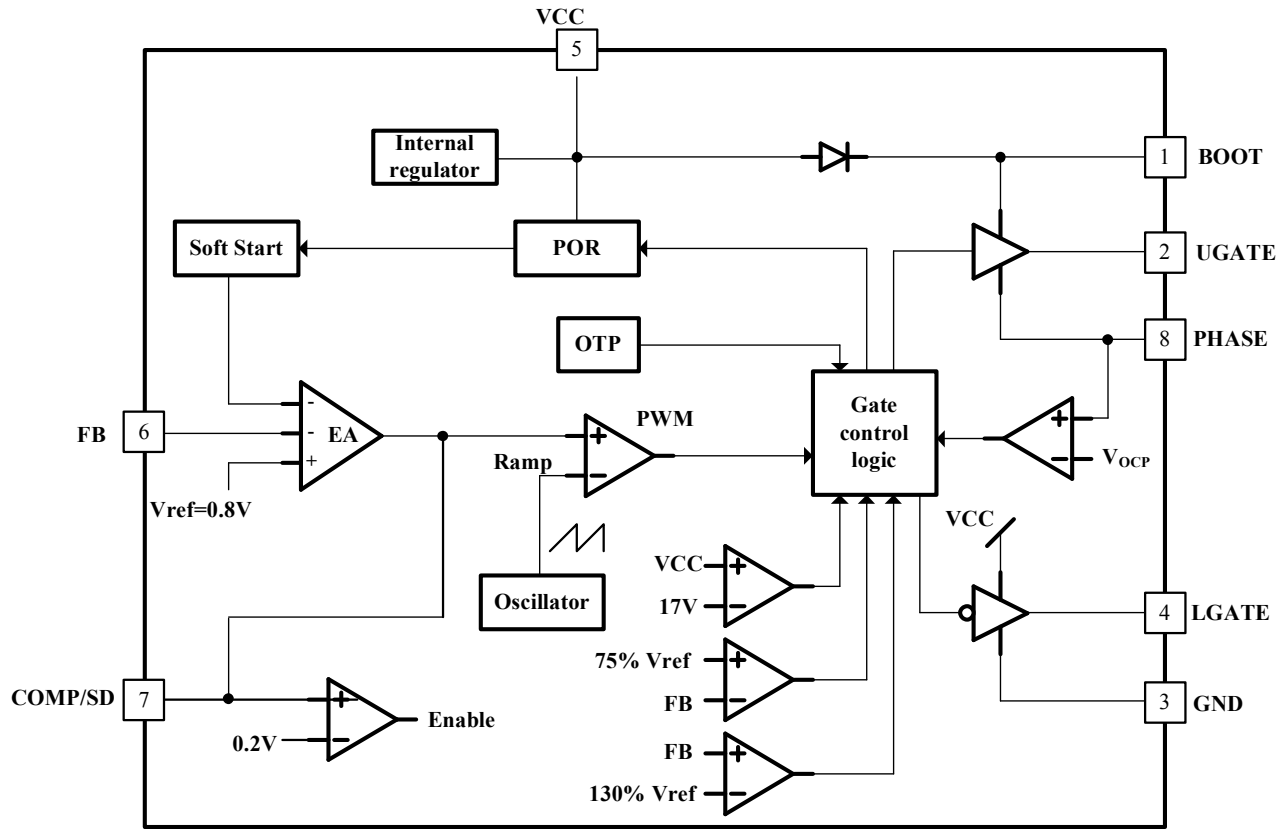
Typical Application Circuit



Pin Assignment

Pin Name	Pin No.	Pin Function
BOOT	1	Bootstrap Supply for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
UGATE	2	Upper Gate Driver Output. Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
GND	3	Signal and Power Ground for the IC. All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
LGATE	4	Lower Gate Driver Output. Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
VCC	5	Supply Voltage. This pin provides the bias supply for the EM5301F/G and the lower gate driver. The supply voltage is internally regulated to 5VDD for internal control circuit. Connect a well-decoupled 10V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC.
FB	6	Feedback Voltage. This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage.
COMP/ SD	7	Error Amplifier Output. This pin is the output of error amplifier and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage control feedback loop of the converter. Pulling this pin lower than 0.2V disables the controller and causes the oscillator to stop, the UGATE and LGATE outputs to be held low.
PHASE	8	PHASE Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

● Supply voltage, VCC-----	-0.3V to 16V
● PHASE to GND	
DC-----	-5V to 16V
<200nS-----	-10V to 32V
● BOOT to PHASE-----	16V
● BOOT to GND	
DC-----	-0.3V to PHASE+16V
<200nS-----	-0.3V to 42V
● UGATE	
DC-----	$V_{PHASE} - 0.3V$ to $V_{BOOT} + 0.3V$
<200ns-----	$V_{PHASE} - 5V$ to $V_{BOOT} + 5V$
● LGATE	
DC-----	-0.3V to VCC + 0.3V
<200ns-----	-5V to VCC+5V
● COMP/SD & FB-----	-0.3V to 6V
● Power Dissipation, PD @ TA = 25°C, PSOP-8 -----	1.33W
● Package Thermal Resistance, θ_{JA} , PSOP-8 (Note 2)-----	75°C/W
● Junction Temperature-----	150°C
● Lead Temperature (Soldering, 10 sec.)-----	260°C
● Storage Temperature Range-----	-65°C to 150°C
● ESD susceptibility (Note3)	
HBM (Human Body Mode)-----	2KV
MM (Machine Mode)-----	200V

Recommended Operating Conditions (Note4)

● Supply Voltage, V _{CC} -----	10V to 13.2V
● Junction Temperature -----	-40°C to 125°C
● Ambient Temperature -----	-40°C to 85°C

Electrical Characteristics

V_{CC}=12V, T_A=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Input Section						
Supply Voltage	V _{CC}		10		13.2	V
Supply Current	I _{CC}	LGATE, UGATE open, Switching.		2.5		mA
Quiescent Supply Current	I _{CCQ}	No Switching.		2		mA
Power on Reset Threshold	V _{CCRTH}			8.8		V
Power on Reset Hysteresis	V _{CCHYS}			0.8		V
Internal Oscillator						
Free Running Frequency	f _{OSC}	EM5301F	130	160	190	kHz
		EM5301G	170	200	235	kHz
Ramp Amplitude	ΔV_{OSC}			1.5		V _{pp}
Error Amplifier						

Open Loop DC Gain	A_o		88			dB
Gain-Bandwidth Product	GBW		15			MHz
Maximum Duty	D_{MAX}		80			%
PWM Controller Gate Drivers						
Upper Gate Sourcing Current	I_{UG_SRC}	$V_{BOOT} - V_{PHASE} = 12V,$ $V_{BOOT} - V_{UGATE} = 6V$		-1.2		A
Upper Gate Sinking Current	I_{UG_SNK}	$V_{BOOT} - V_{PHASE} = 12V,$ $V_{UGATE} - V_{PHASE} = 6V$		1.5		A
Upper Gate $R_{DS(ON)}$ Sinking	R_{UG_SNK}	$V_{BOOT} - V_{PHASE} = 12V,$ $V_{UGATE} - V_{PHASE} = 0.1V$		2	4	Ω
Lower Gate Sourcing Current	I_{LG_SRC}	$V_{CC} - V_{LGATE} = 6V$		-1.2		A
Lower Gate Sinking Current	I_{LG_SNK}	$V_{LGATE} = 6V$		1.5		A
Lower Gate $R_{DS(ON)}$ Sinking	R_{LG_SNK}	$V_{LGATE} = 0.1V$		1	2	Ω
PHASE Falling to LGATE Rising Delay		$V_{CC} = 12V; (V_{UGATE} - V_{PHASE}) < 1.2V$ to $V_{LGATE} > 1.2V$		30	90	ns
LGATE Falling to UGATE Rising Delay		$V_{CC} = 12V; V_{LGATE} < 1.2V$ to $(V_{UGATE} - V_{PHASE}) > 1.2V$		30	90	ns
Reference Voltage						
Nominal Feedback Voltage	V_{FB}		0.792	0.8	0.808	V
Protection section						
FB Under Voltage Protection	V_{FB_UVP}	FB falling	68	75	82	%
FB Over Voltage Protection	V_{FB_OVP}	FB rising	115	130	145	%
LGATE OC Setting Current	I_{OCSET}		22	25	28	μA
Over Current Threshold1	V_{PHA_OC1}	$R_{LGATE} = 8Kohm$		-400		mV
Soft-Start Interval	T_{SS}			3.6		ms
COMP Enable Threshold	$V_{COMP/EN}$				0.2	V
Temperature Shutdown	T_{SD}			165		$^{\circ}C$

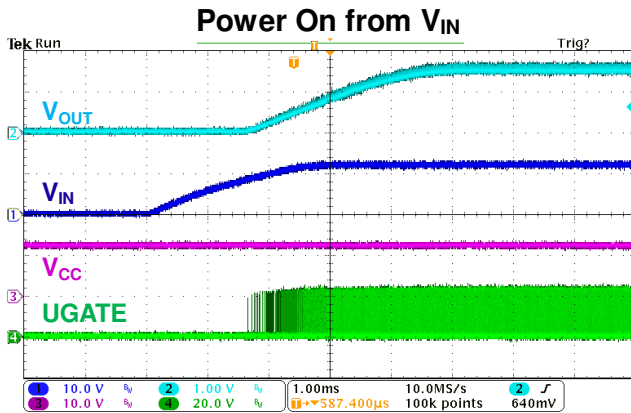
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} PSOP-8 packages is $52^{\circ}C/W$ on JEDEC 51-7 (4 layers,2S2P) thermal test board with $50mm^2$ copper area.

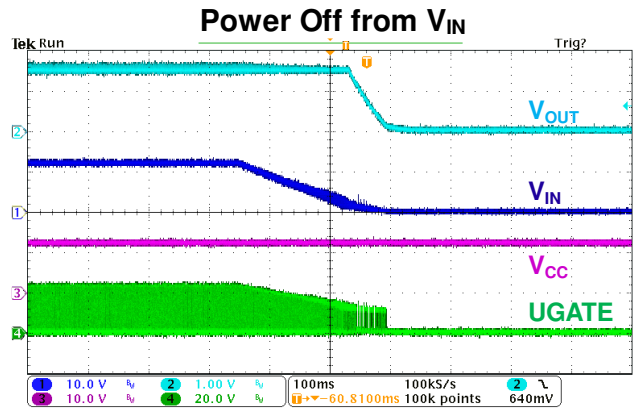
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

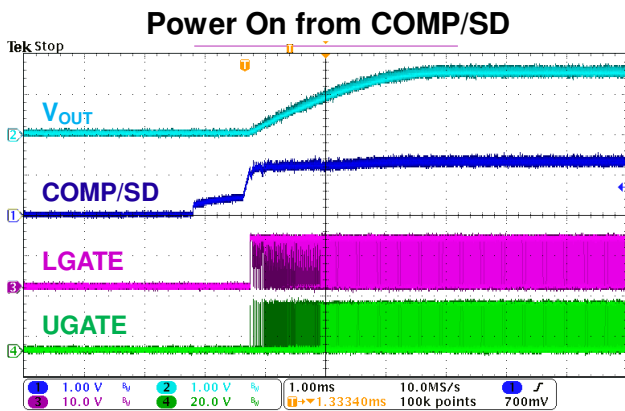
Typical Operating Characteristics



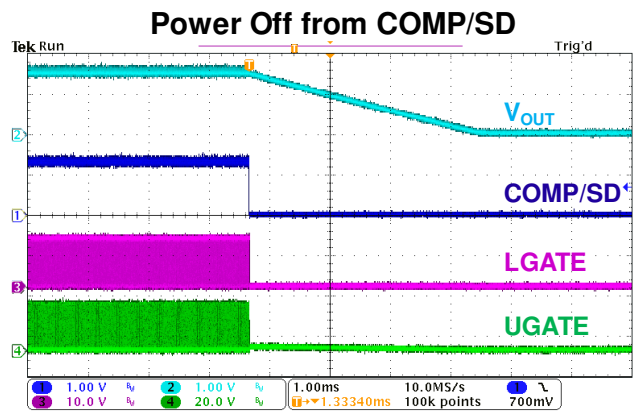
$V_{IN}=12V$, $V_{CC}=12V$, No Load.



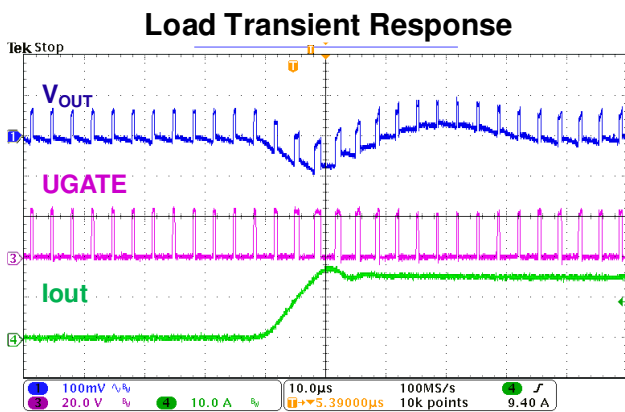
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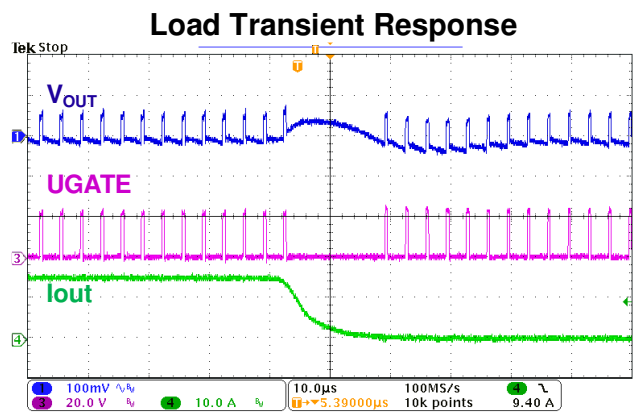
$V_{IN}=12V$, $V_{CC}=12V$, No Load.



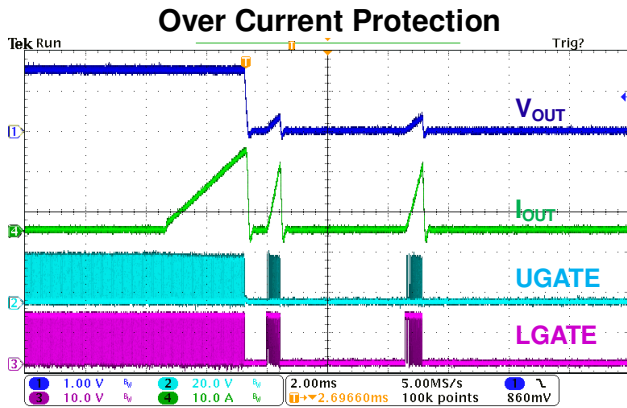
$V_{IN}=12V$, $V_{CC}=12V$, No Load.



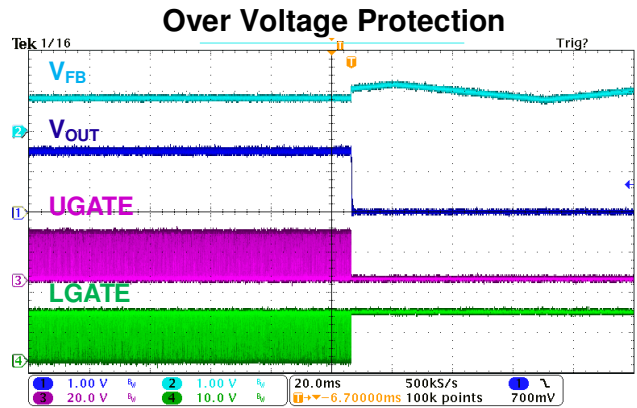
$V_{IN}=12V$, $V_{CC}=12V$, $C_{OUT}=1360\mu F$, $L=1.2\mu H$
 $I_{OUT}=0A$ to $15A$.



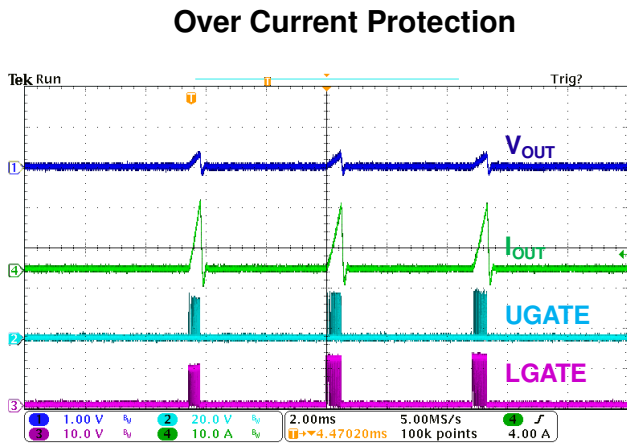
$V_{IN}=12V$, $V_{CC}=12V$, $C_{OUT}=1360\mu F$, $L=1.2\mu H$
 $I_{OUT}=15A$ to $0A$.



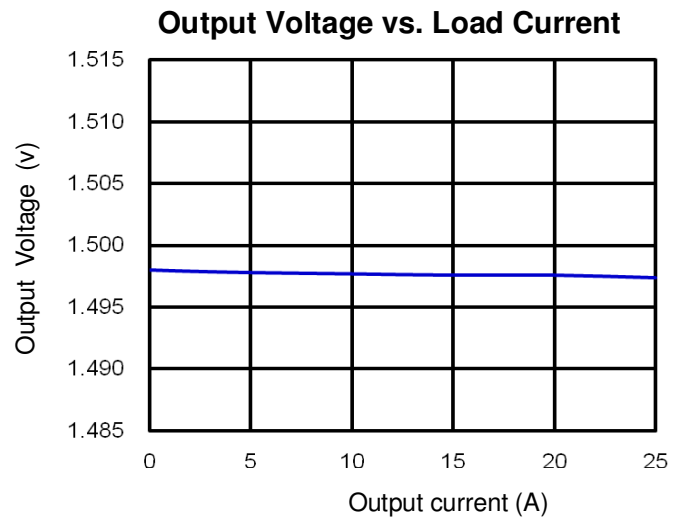
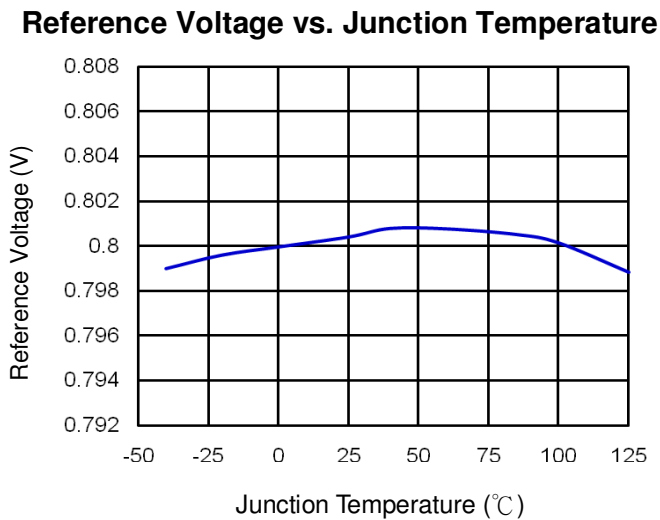
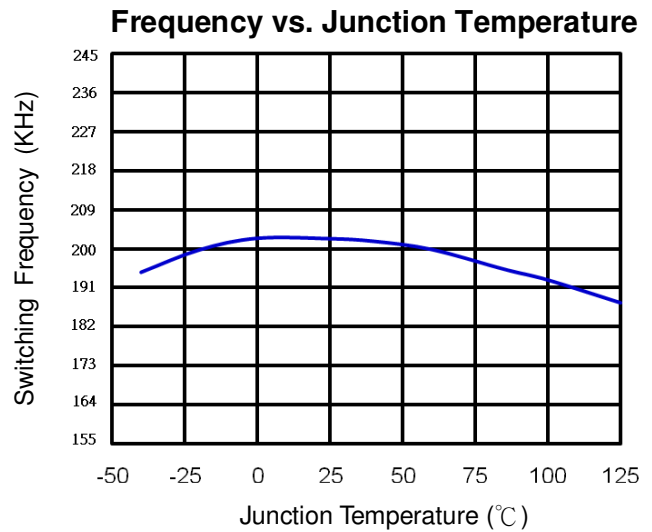
$V_{IN}=12V$, $V_{CC}=12V$, $I_{OCSET}=20A$.



$V_{IN}=12V$, $V_{CC}=12V$, No Load.

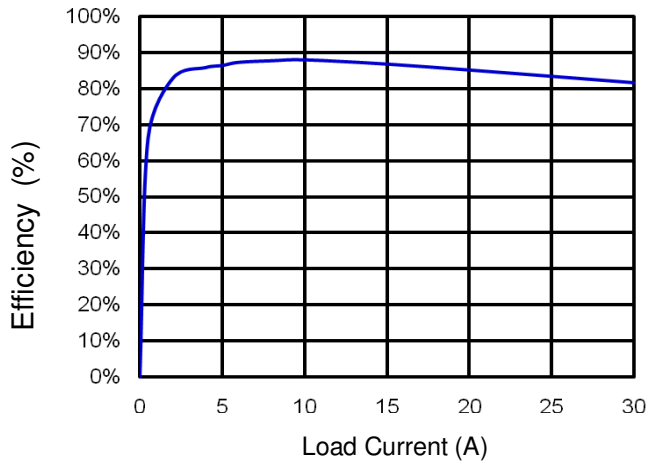


$V_{IN}=12V$, $V_{CC}=12V$, $I_{OCSET}=20A$.
Turn On to Short Circuit





Efficiency vs. Load Current



Functional Description

EM5301F/G is a voltage mode synchronous buck PWM controller. This device provides complete protection function such as over current protection, under voltage protection and over voltage protection.

Supply Voltage

The V_{CC} pin provides the bias supply of EM5301F/G control circuit, as well as lower MOSFET's gate and the BOOT voltage for the upper MOSFET's gate. A minimum 0.1uF ceramic capacitor is recommended to bypass the supply voltage.

Power ON Reset

To let EM5301F/G start to operation, V_{CC} voltage must be higher than its POR voltage even when REFIN voltage is pulled higher than enable high voltage. Typical POR voltage is 8.8V.

Shutdown

The COMP/SD pin can be used to enable or disable EM5301F/G. Pull down COMP/SD pin below 0.2V can disable the controller.

Soft Start

EM5301F/G provides soft start function internally. The FB voltage will track the internal soft start signal, which ramps up from zero during soft start period.

OCP, Over Current Protection

The over current function protects the converter from a shorted output by using lower MOSFET's on-resistance to monitor the current. The OCP level can be calculated as the following equation:

$$I_{OCP} = \frac{V_{OCP}}{R_{DS(ON)}}$$

When OCP is triggered, EM5301F/G will shut down the converter and cycles the soft start function in a hiccup mode. If over current condition still exist after 3 times of hiccup, EM5301F/G will shut down the controller and latch.

UVP, Under Voltage Protection

The FB voltage is monitored for under voltage protection. The UVP threshold is typical 0.6V. When UVP is triggered, EM5301F/G will shut down the converter and cycles the soft start function in a hiccup mode.

OVP, Over Voltage Protection

The FB voltage is monitored for over voltage protection. The OVP threshold is typical 1.04V. When OVP is triggered, EM5301F/G will turn off upper MOSFET and turn on lower MOSFET.

Feedback Compensation

Fig.1 shows the voltage mode control loop for a synchronous-rectified buck converter. The compensation network consists of the error amplifier and the impedance networks Z_{IN} and Z_{FB} . The goal of the compensation network is to provide a closed loop transfer function with adequate phase margin.

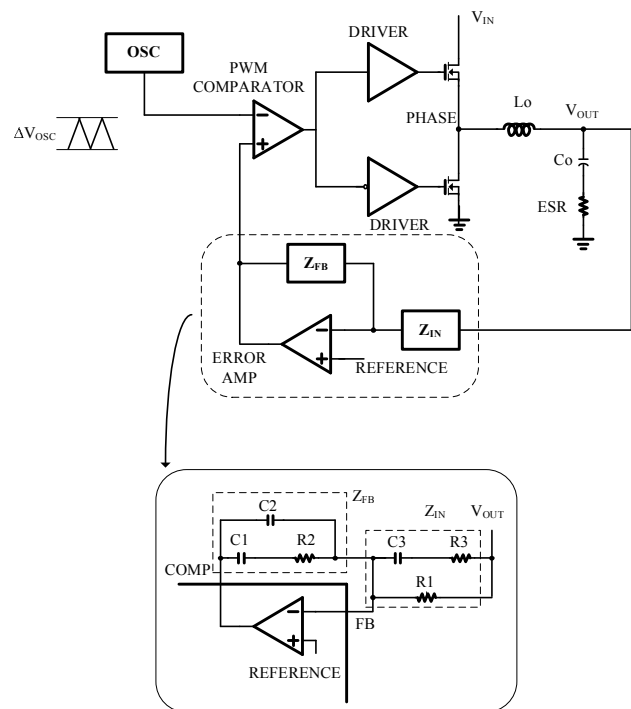


Fig.1 Compensation for Voltage Mode Buck Converter

The equations below relate the compensation network's poles and zeros to the components (R1, R2, R3, C1, C2 and C3).

$$F_{Z1} = \frac{1}{2\pi * R_2 * C_1} \quad F_{P1} = \frac{1}{2\pi * R_2 * (\frac{C_1 * C_2}{C_1 + C_2})}$$

$$F_{Z1} = \frac{1}{2\pi * (R_1 + R_3) * C_3} \quad F_{P2} = \frac{1}{2\pi * R_3 * C_3}$$

Fig.2 shows the Bode plot for the control loop. The compensation gain uses external impedance networks Z_{IN} and Z_{FB} to provide a stable loop. A stable control loop has a gain crossing with -20db/decade slope and phase margin greater than 45 degrees.

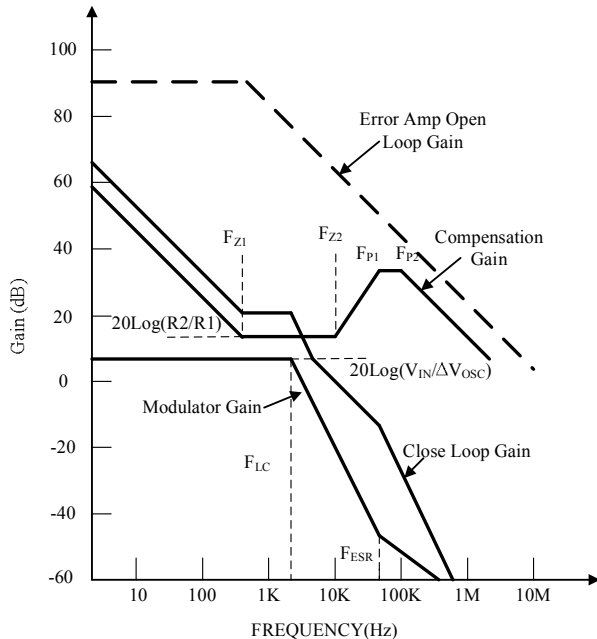


Fig.2 Bode Plot of Voltage Mode Buck Converter

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the response time to the load transient. The inductor value determines the current ripple and voltage ripple. The ripple current is approximately the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} * \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient. The selection of output capacitor depends on the output ripple voltage. The output ripple voltage is approximately bounded by the following equation:

$$\Delta V_{OUT} = \Delta I_L * (ESR + \frac{1}{8 * F_{SW} * C_{OUT}})$$

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFET. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turn on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of the upper MOSFET and the source of the lower MOSFET. The important parameters of the input capacitor are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement can be expressed as the following equation:

$$I_{RMS} = I_{OUT} \sqrt{D(1-D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Power MOSFET Selection

The EM5301F/G requires two N-Channel power MOSFETs. These should be selected based upon on-resistance, breakdown voltage, gate supply requirement, and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection and heat sink are the dominate design factor. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor.

The power dissipations in the two MOSFETs are approximately the following equation:

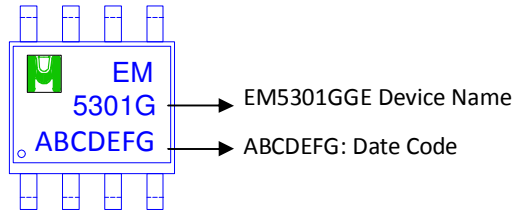
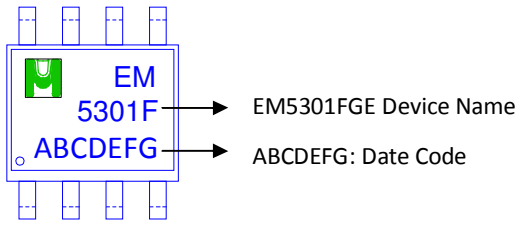
$$PD_{UPPER} = I_{OUT}^2 * R_{DS(ON)} * D + 0.5 * I_{OUT} * V_{IN} * F_{SW} * t_{SW}$$

$$PD_{LOWER} = I_{OUT}^2 * R_{DS(ON)} * (1 - D)$$

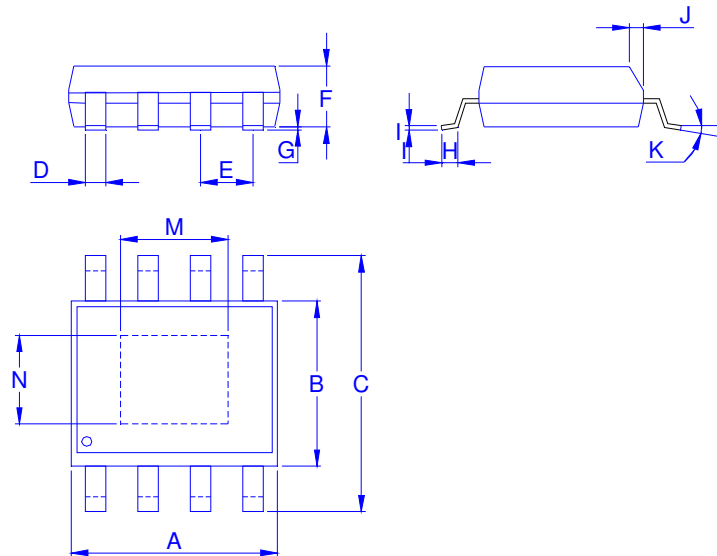
Where D is the duty cycle, t_{SW} is the combined switch ON and OFF time.

Ordering & Marking Information

Device Name: EM5301FGE;EM5301GGE for PSOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	M	N
Min.	4.70	3.70	5.80	0.33		1.20	0.02	0.40	0.19	0.25	0°	1.94	1.94
Typ.					1.27								
Max.	5.10	4.10	6.20	0.51		1.62	0.15	0.83	0.26	0.50	8°	2.49	2.49