iW3605 design Guide

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1. Introduction to iW3605

The iW3605 is a single-stage, high-performance AC/DC offline power supply controller for dimmable LED luminaires. It applies advanced digital control technology to detect the dimmer type, which provides dynamic impedance to interface with the dimmer and control the LED brightness at the same time.

With advanced dimmer detection technology, the iW3605 can operate with most wall dimmers including leading-edge dimmers (R-type or R-L type) and trailing-edge dimmers (R-C type). In addition, the iW3605's cycle-by-cycle waveform analysis technology allows for fast dimmer setting response. When no dimmer is on the line, the iW3605 optimizes the power factor and minimizes the current harmonic distortion to the AC line. Furthermore, in no dimmer condition, output current is regulated at nominal output current value over a wide input voltage range.

The iW3605 operates the main power converter that delivers current to the LED load in quasi-resonant mode to provide high power efficiency and minimize electro-magnetic interference (EMI). The commonly utilized converter topologies for iW3605 are buck-boost and flyback. It uses Dialog's patented PrimAccurate™ primary-side sensing technology to achieve excellent LED current regulation under different AC line and LED load voltages, without using a secondary-side feedback circuit and thus eliminating the need for an opto-coupler.

The iW3605 minimizes the external components count by eliminating the secondary feedback circuit and bleeder circuit. Additionally, the digital control loop of the iW3605 maintains stable overall operating conditions without the need for loop compensation components.

2. Design Example: low line 10W dimmable LED driver

2.1 Photograph

Figure 2.1: 120Vac 30V350mA LED Driver Photograph

2.2 LED Driver Design Specifications

Parameter	Symbol	Range
Input Voltage	Vin	108~132Vrms
Frequency	f_{IN}	45~66Hz
Output Voltage	Vout	30V
Output Current	Iout	350mA

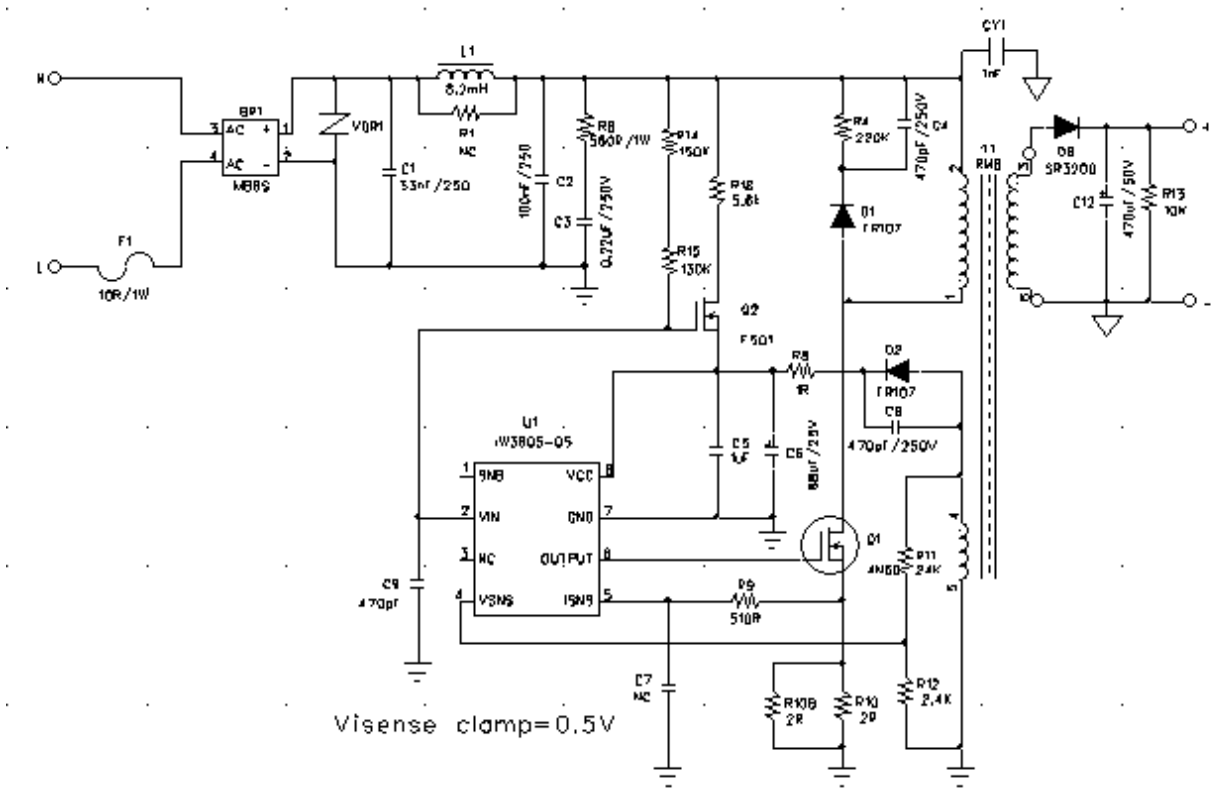
Efficiency	η	85%
Output Ripple	Vripple*	<30%*Iout

Table 2.1: Design specifications

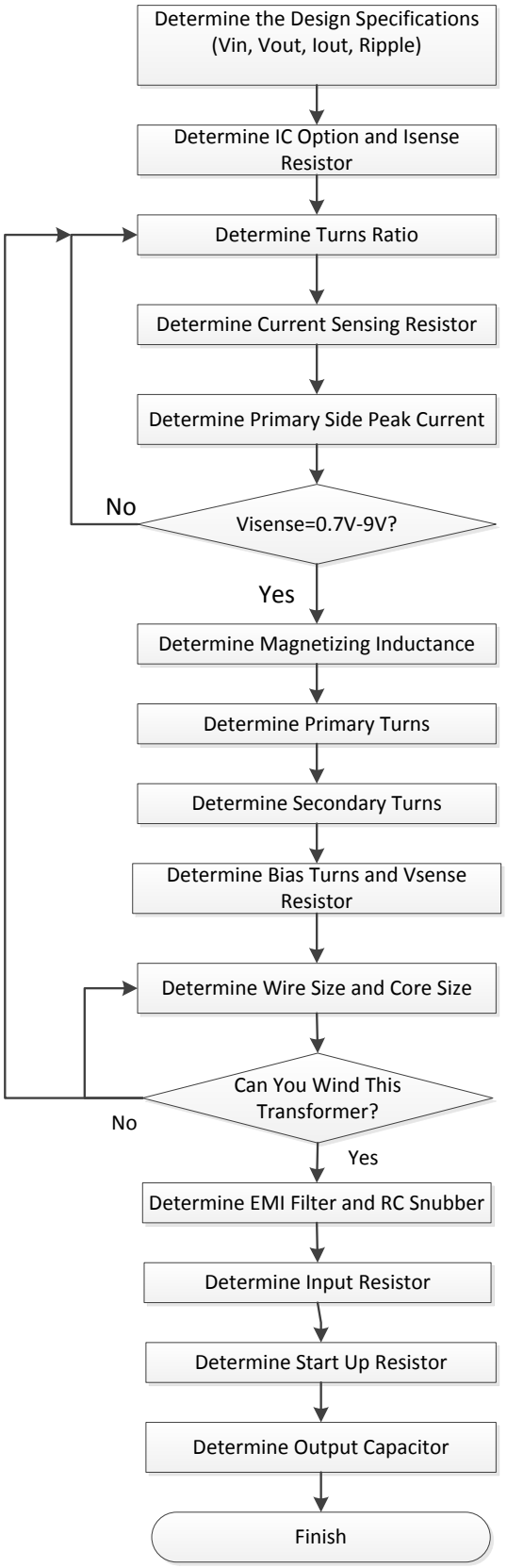
*Note: Vripple is defined as output current peak to peak value divided by 2*Iout

2.3 Major IC Design Control Parameters

2.4 Schematic



3. Design Procedure



3.1 Determine IC Option and Isense Resistor

There are two IC options -02 and -05 in iW3605 family. The difference between them is the Isense pin clamp voltage. Higher Isense clamp voltage will has higher output power at minimum dimmer phase which will help to hold leading edge dimmer. Typically one can chose iW3605-05 for 5W to 10W applications and iW3605-02 for 10W to 25W applications.

Application	IC option	Isense Clamp Voltage
Low Line 5W	-05	0.5V
Low Line 10W	-05	0.5V
Low Line 20W	-02	0.4V
High Line 10W	-05	0.5V
High Line 20W	-02	0.4V

Table 3.1: IC Option and Power Level

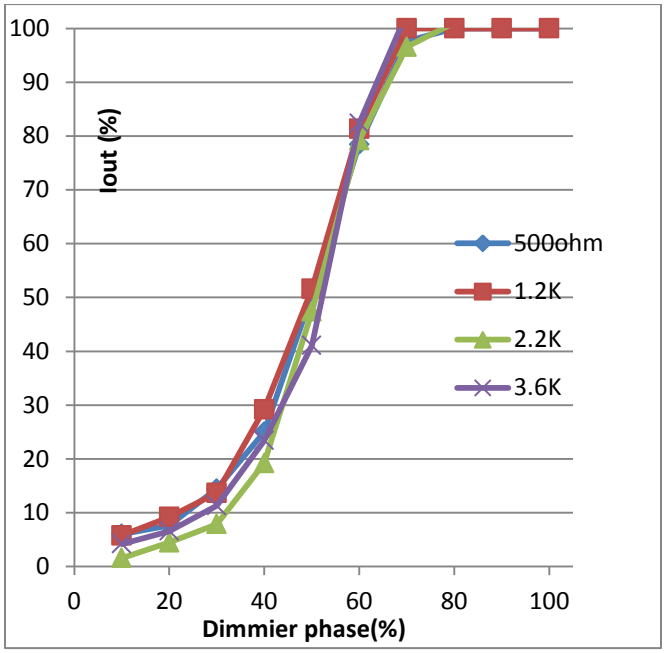
For this low line 10W design, we can chose iW2605-05 with Isense clamp to 0.5V.

Isense clamp voltage is configured by the Isense pin filter resistor R9. Below is the relationship between R9 and Isense clamp voltage for -02 and -05 IC options.

R9	Vclamp(-02)	Vclamp(-05)
510	0.3V	0.5V
1.2K	0.4V	0.6V
2.2K	0.3V	0.5V
3.6K	0.4V	0.6V

Table 3.2: R9 and Isense Clamp Voltage

R9 not only affects Isense clamp voltage but also affect Iout versus dimmer phase. It is shown in below curve.



3.2 Determine Turns Ratio

Turns ratio can affect the MOSFET drain to source voltage and also the Isense pin voltage at peak of line. The typical value of Nps is chosen so that Nps*Vout is between 50V to 120V and Isense pin voltage is around 0.9V.

At start point, we can choose

$$Nps = \frac{70V}{Vout} \qquad (3.1)$$

For this example, Vout=30V. So we choose

$$Nps = \frac{70V}{30V} = 2.33$$

3.3 Determine Current Sensing Resistor

The output current regulation is determined by the transformer turn ratio n, the primary current sense resistor Ris, and the flyback converter efficiency η by equation (3.2)

$$I_{out} = \frac{0.175V}{R_{is}} \times Nps \times \eta \qquad (3.2)$$

For this example, if the target output current is 350mA, the turn ratio is selected to be equal to 2.33, assuming the transformer efficiency is 85%, the current sense resistor is calculated:

$$R_{is} = \frac{0.175V}{0.35A} \times 2.33 \times 0.85 = 1\Omega$$

3.4 Determine Primary Side Peak Current

The primary peak current can be determined by the equations (3.3) and (3.4)

$$Iin\_rms = \frac{Vout * Iout}{\eta * \mathrm{Vin}} \qquad (3.3)$$

$$Ipk\_pri = \frac{4 * \sqrt{2} * Iin\_rms}{\int_0^{\pi} \frac{\sin\theta}{1 + \frac{\sqrt{2} * Vin * \sin\theta}{Nps * Vout}} d\theta} \qquad (3.4)$$

For this example,

$$Iin\_rms = \frac{30V * 0.35A}{85\% * 120V} = 0.103A$$

$$Ipk\_pri = \frac{4 * \sqrt{2} * 0.103A}{\int_0^{\pi} \frac{\sin\theta}{1 + \frac{\sqrt{2} * 120V * \sin\theta}{2.33 * 30V}} d\theta} = 0.805A$$

We can now check Isense pin voltage Visense at peak of line:

$$Visense = Ipk\_pri * Ris = 0.805A * 1\Omega = 0.805V$$

The recommend value for Visense is between 0.7V to 0.9V. Visense too high corresponds to high Ris, which will lower the minimum output current which is not good for holding LE dimmer. Visense too low corresponds to low Ris. It will increase minimum output current but induces high ripple voltage on bulk capacitor which will cause dimmer unbalance. One can increase Nps if Visense is less than 0.7V or decrease Nps if Visense is higher than 0.9V. After change Nps, go through step 3.3 and 3.4 again. It may take several iterations to get desired Visense.

3.5 Determine Magnetizing Inductance

The transformer should be designed to work in valley switching mode. The target switching frequency is selected to be below maximum clamped frequency 90 kHz. Typically switch frequency is chosen between 65 kHz to 75 kHz at peak of line with no dimmer connected. Lower switch frequency means higher magnetizing inductance which will is good for hold dimmer. Higher frequency means lower magnetizing inductance which is good for decrease transformer size.

Under valley mode switching condition, Lm determines the switching frequency by Equation (3.5). Equation (3.5) shows how to calculate the transformer inductance based on the desired switching frequency fs, the valley resonant frequency fres, the input voltage Vin, Nps*Vo value and the peak primary current Ipri_pk. The Vin and Ipri_pk are selected at lowest operating line voltage and full load condition.

$$Lm = \frac{\frac{1}{fs} - \frac{1}{2\,fres}}{(\frac{1}{\sqrt{2} * Vin} - \frac{1}{Nps * Vout}) * Ipk\_pri} \qquad (3.5)$$

For this example, we chose fs=75khz,assuming fres=500kHz,

$$Lm = \frac{\frac{1}{75kHz} - \frac{1}{2 * 500kHz}}{(\frac{1}{\sqrt{2} * 120V} - \frac{1}{2.33 * 30V}) * 0.805A} = 759\mu H$$

3.6 Determine Primary Turns

The number of primary winding turns is limited by the transformer physical structure as well as the maximum allowed flux density Bmax. The minimum number of turns is calculated according to equation (3.6)

$$N_p = \frac{L_m \times I_{pk}}{B_{max} \times A_e} \qquad (3.6)$$

Here Ae is the cross-sectional area of the core. Ipk should consider normal operation maximum flux density, Isense OCP threshold 1.3V.

For this example, RM6 core is used. With Ae=36.6mm^2, Bmax=0.35T, we get

$$Np = \frac{759uH * \frac{1.3V}{1\Omega}}{0.35T * 36.6mm^2} = 77$$

3.7 Determine Secondary Turns

The number of the secondary winding turns is obtained from equation (3.7)

$$Ns = \frac{Np}{Nps} \qquad (3.7)$$

For this example, Np is chosen to be 77 turns and Nps=2.33. So

$$Ns = \frac{77}{2.33} = 33$$

3.8 Determine Bias Turns and Vsense Resistor

VCC supply voltage is determined by the auxiliary winding and it should be below 16 V. The number of bias winding turns is obtained from equation (3.8)

$$Nbias = Ns * \frac{Vcc + VFD}{Vout + VFD} \qquad (3.8)$$

Here V_{FD} is the forward voltage drop of diode.

For this example, we chose Vcc to be 12V. Assume VFD=1V and we get:

$$Nbias = 33 * \frac{12V + 1V}{30V + 1V} = 13.8$$

14 turns will be used for Nbias.

The output voltage sense is determined by the feedback signal Vsense

$$V_{sense} = V_{out} \times \frac{R_{12}}{(R_{11}+R_{12})} \times \frac{N_{bias}}{N_s} \qquad (3.9)$$

Vsense should be kept below the OVP threshold 1.7V. The recommended Vsense voltage under normal operation is 1.538V.

iW3605 also uses Vsense resistor to configure the internal over temperature derating theshold. The vsense resistor value vs. the over temperature derating thresholds are shown in Table 2.

Table 3.3 Typical Vsense resistor options

Temperature derating Start Point (°C)	100	110	120	130
R11//R12 (ohm)	0.72k	1.38k	2.3k	3.6k

For this example, R12=2.4K, R11=24K,

$$Vout * \frac{R12}{R11 + R12} * \frac{Nbias}{Ns} = 30 * \frac{2.4K}{2.4K + 24K} * \frac{14}{33} = 1.16V$$

And OVP point is:

$$Vout\_ovp = 1.7V * \frac{24K + 2.4K}{2.4K} * \frac{33}{14} = 44V$$

While R11//R12=2.4K//24K=2.2K. so OTP starts at 120C.

3.9 Determine wire size and core size

At this moment, we can choose suitable core and wires to fit the design requirement. Keep in mind that after checking no dimmer and dimmer performance it may need to go back change the transformer design to achieve good thermal and dimmer performance.

3.10 Determine EMI filter and RC Snubber

The RC snubber R6 and C3 are used to damp the ringing from EMI filter during the phase-cut time for the leading edge dimmer. When a step input voltage appears, RC circuit generates an additional input current pulse. The height is determined by input voltage divided by R6. The time during is controlled by the time constant C3. This input current pulse is necessary to overcome the ringing appears in the dimmer and EMI filter.

As a rule of thumb, the capacitor C3 is typically selected as 1 to 5 times of the input filtering capacitor C2. The snubber resistor R6 provides enough damping to the ringing. The typically values are 1kΩ for 230V design and 560Ω for 120V design.

C2 should be bigger enough to avoid voltage ring when input is near zero crossing. Typical value of C2 is 100nF for lower line and 47nF for high line. C1 has to be as small as possible to avoid input current ringing during leading edge dimmer turn on time. If C1 cannot be too small to pass EMI, a secondary RC snubber or inrush limit circuit must be used.

3.11 Determine Input Resistor

Input resistor is used to sense bulk voltage and it is used to control output current with dimmer and input OVP level.

The default scale factor from bulk voltage to Vin pin voltage is 0.008 for low line and 0.004 for high line.

With Vin internal resistor Zin=2.5kΩ, we have

$$Rin_{lowline} = \left(\frac{1}{0.008} - 1\right) * Zin = 310k\Omega$$

$$Rin_{highline} = \left(\frac{1}{0.004} - 1\right) * Zin = 622.5k\Omega$$

Change Rin from default value will affect dimming curve and input OVP threshold. For this example, Rin (R14+R15 in schematic) uses 280kΩ.

3.12 Determine Startup Resistor

Startup resistor R18 is used for fast charge Vcc capacitor at start up through a DFET Q2. Q2 gate will be pulled down by Vin once Vcc reaches start up threshold so Q2 turns off during normal operation.

R18 is designed so that it can provide about 20mA c harge current which is required by some digital dimmer.

For this example,

$$R18 = \sqrt{2} * 120V * \frac{2}{\pi} * \frac{1}{20mA} = 5.4k\Omega$$

A 5.6kΩ resistor is used.

3.12 Determine Output Capacitor

Output capacitor affects the output current ripple. The output capacitor C12 can be estimated as:

$$C12 > \frac{1}{4 * \pi * fac * Rled} \quad (3.10)$$

Rled is the dynamic resistor of LED. It can be obtained from V-I curve of LED data sheet.

For this example, f_{ac}=60Hz, Vripple=30%, Rled=5Ω, we get:

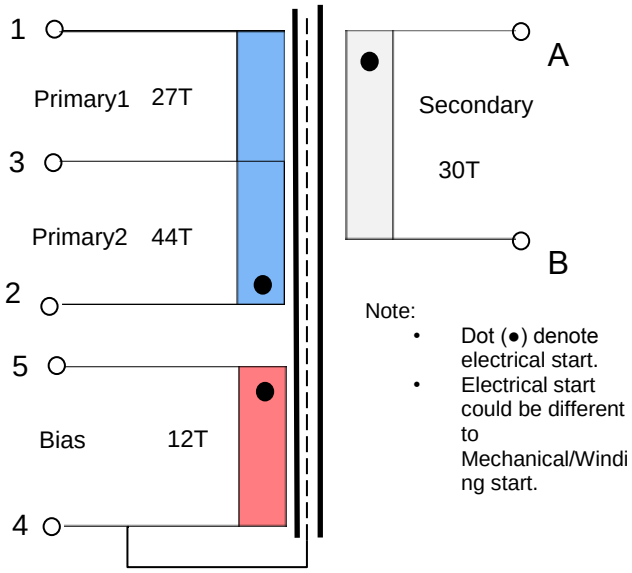
$C12 > \frac{1}{4*\pi*60Hz*5\Omega}$=265uF

A 470uF electrolytic capacitor is used in the design.

4. Bill of Material

Qty	Ref.	Description		
1	U1			iW3605-05
1	C1	0.033uF	250V	CL21
1	C2	0.1	250V	CL21
1	C3	0.22uF	250V	CL21
1	C9	470pF	50V	X7R
1	C4	220pF	250V	NPO
1	C8	470pF	250V	NPO
1	C12	470UF	50V	E-CAP,105℃
1	C6	68UF	25V	E-CAP,105℃
1	C5	1UF	25V	Ceramic, X7R
1	BR1	1A	1000V	B10S
2	D1,D2	1A	1000V	FR107
1	D8	3A	150V	SB315
1	Q1	4A	700V	NDD04N60
1	Q2	10mA	500V	F501
1	R4	220KΩ	+/-5%	R0805
1	R8	1Ω	+/-5%	R0805
1	R9	510Ω	+/-5%	R0805
1	R18	5.6K	+/-5%	MOF, 1/2W
1	R13	10K	+/-5%	R1206
1	R14	150KΩ	+/-5%	R0805
1	R15	130KΩ	+/-5%	R0805
2	R10,R10B	2Ω	+/-5%	R0805
1	R6	560Ω	+/-1%	MOF,1W
1	R12	2.4KΩ	+/-1%	R0805
1	R11	24KΩ	+/-1%	R0805
1	CY1	1000PF	250V	Y2 Capacitor
1	VDR1	150Vac		VDRS07H150
1	F1	10R		
1	L1	8.2mH		Renco 5480-3
1	T1	Transformer		RM6

SCHEMATIC



Note:
- Dot (●) denote electrical start.
- Electrical start could be different to Mechanical/Winding start.

ELECTRICAL SPECIFICATIONS:

1. Primary Inductance (Lp) = 0.76mH @10KHz
2. Primary Leakage Inductance (Lk)< = 100uH @10KHz

MATERIALS:

1. Core : RM6(Ferrite Material TDK PC40 or equivalent)
2. Bobbin :RM6Horizontal. Primary=3, Secondary=3
3. Magnet Wires (Pri) : Type 2-UEW
4. Magnet Wire (Sec) : Triple Insulated Wires
5. Layer Insulation Tape :3M1298 or equivalent.