ZCC6908HV

Fast Turn-off Intelligent Rectifier

DESCRIPTION

The ZCC6908HV is a Low-Drop Diode Emulator IC that, combined with an external switch, replaces Schottky diodes in high-efficiency Flyback converters. The chip regulates the forward drop of an external Synchronous Rectifier (SR) MOSFET to about 40mV and switches it off as soon as the voltage becomes negative. ZCC6908HV can generate its own supply voltage for battery charging applications with low output voltage or high side rectification applications. A programmable ringing detection circuitry prevents ZCC6908HV false turn-on during DCM and Quasi-Resonant operations.
ZCC6908HV is available in space saving TSOT23-6 packages.

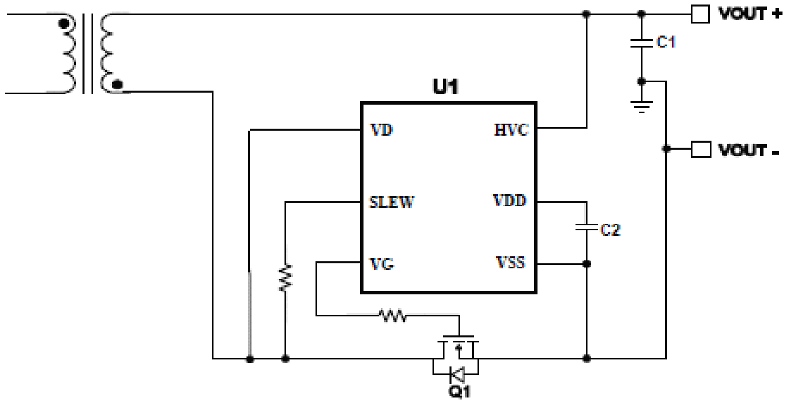
FEATURES

- Operates in a wide output voltage range down to 0V
- Self-supplying for operation with low output voltage rectification without an auxiliary winding
- Works with 12V Standard and 5V Logic Level SR MOSFETS
- Compatible with Energy Star, 1W Standby Requirements
- <30ns Fast Turn-off and Turn-on Delay
- <100uA Quiescent Current
- Supports DCM, Quasi-Resonant and CCM Operations
- Supports both High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter
- TSOT23-6 Package Available

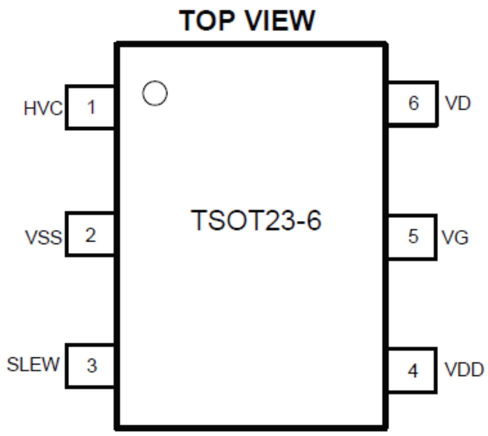
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

TYPICAL APPLICATION



PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} .... –0.3V to +14V
V_G to V_{SS} .... –0.3V to +14V
V_D to Vss .... –1V to + 200V
HVC to V_{SS} ....–1V to + 80V
SLEW to VSS .... –0.3V to +6.5V
Continuous Power Dissipation (TA = +25°C)
Junction Temperature .... 150°C
Lead Temperature (Solder) .... 260°C
Storage Temperature .... –55°C to +150°C

Recommended Operation Conditions

VDD to VSS .... 3.6 to 13V
Maximum Junction Temp. (TJ) .... +125°C

Thermal Resistance ϑ_{JA} ϑ_{JC}

TSOT23-6 .... 220 ....110 °C /W

ELECTRICAL CHARACTERISTICS

VDD=5V. TJ=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY MANAGEMENT SECTION						
VDD UVLO Rising				4		V
V_{DD} UVLO Hysteresis			0.1	0.2	0.35	V
VDD Maximum Charging Current	IVDD	VDD=7V,HVC=40V		60		mA
		VDD=4V, VD=30V		30		
VDD Regulation Voltage		VD=12V,HVC=12V		9.5		V
		HVC=3V, VD=12V		5.2		
Operating Current	ICC	VDD=9V, C_{LOAD}=2.2nF, F_{SW}=100kHz		2.9		mA
		VDD=5V, C_{LOAD}=2.2nF, F_{SW}=100kHz		1.72		
Quiescent Current	Iq(VDD)	VDD=5V		100	130	uA
Shutdown Current	ISD(VDD)	VDD=UVLO-0.05V			100	uA
CONTROL CIRCUITRY SECTION						
V_{SS}–V_D Forward Regulation Voltage	Vfwd			40		mV
Turn-On Threshold (V_{DS})	VLL-DS			-86		mV
Turn Off Threshold (VSS-VD)				0		mV
Turn-On Delay	TDon	CLOAD = 2.2nF		30		ns
Turn-Off Delay	TDoff	CLOAD = 2.2nF		30		ns
Turn On Blanking Time	TB-ON	CLOAD = 2.2nF		1.97		us
Turn Off Blanking V_{DS} Threshold	VB-OFF		2		3	V
Turn On Slew Rate Detection Timer		Rslew=100kohm, Vds from 2.5V step down.		60		ns
GATE DRIVER SECTION						
VG (Low)	VG-L	ILOAD=10mA or 100mA		0.02	0.1	V
VG (High)	VG-H	ILOAD=10mA or 100mA		VDD		V
Maximum Source Current				0.5		A
Maximum Sink Current				3		A

Pull Down Impedance		Same as VG(Low)		1		Ω

PIN FUNCTIONS

Pin #	Name	Description
1	HVC	HV Linear Regulator Input
2	VSS	Ground, also used as FET source sense reference for VD
3	SLEW	Programming for turn on signal slew rate detection. To prevent SR controller false turn on by ringing below turn on threshold at VD in DCM and QR modes, any signal slower than pre-set slew rate is not going to turn on VG
4	VDD	Linear Regulator Output, supply ZCC6908HV
5	VG	Gate drive output
6	VD	FET drain voltage sense

BLOCK DIAGRAM

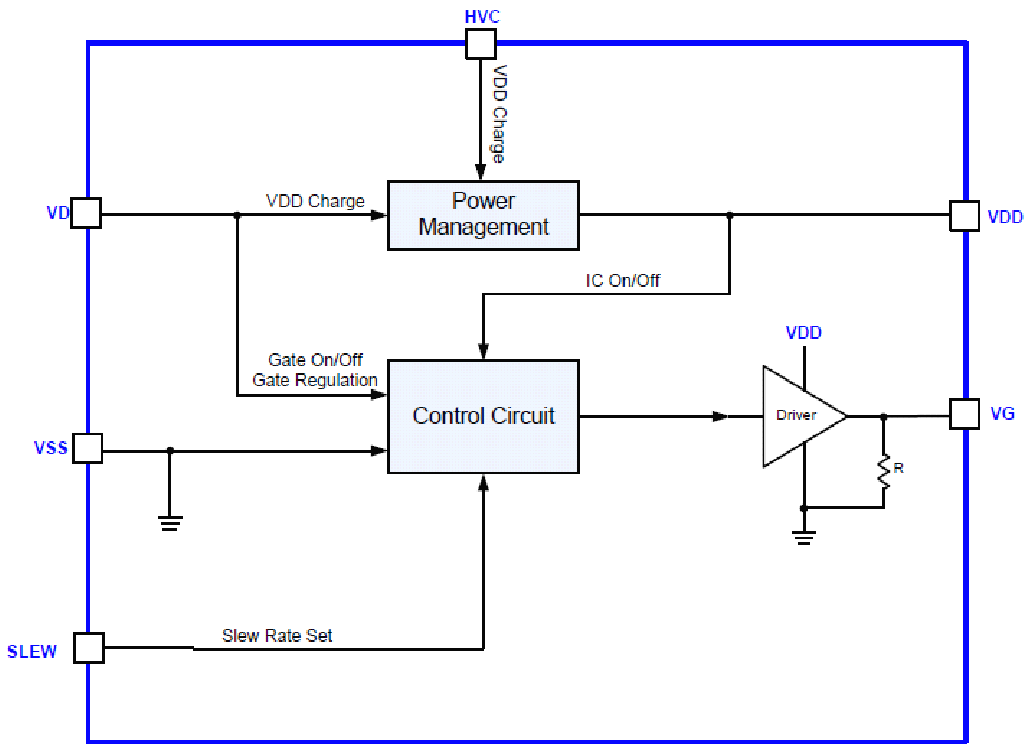


Figure 1—Functional Block Diagram

OPERATION

The ZCC6908HV supports operation in DCM and Quasi-Resonant Flyback converters as well as in CCM mode. The control circuitry controls the gate in forward mode and will turn the gate off when SR MOSFET current drops to zero.

Start-up and VDD Generation

HVC is the input for linear regulator which output is VDD. VDD is regulated at 9.5V which supplies ZCC6908HV including VG. Here HVC can be a DC voltage such as VOUT for low side rectification or an AC voltage such as Drain of SR MOSFET. When HVC is above 4.7V, linear regulator's maximum charging current is 70mA to charge the external 1uF capacitor at VDD. VDD is regulated to 9.5V when HVC is above 10.5V. Then VDD follows HVC with 0.7V dropout (i.e. VDD=HVC- 0.7V) until HVC drops to 4.7V. Once HVC drops below 4.7V, a 40mA current source from VD will charge up VDD and regulate at 5.2V.

Under-Voltage Lockout (UVLO)

When VDD is increased above 4V, ZCC6908HV goes out of UVLO and is enabled. ZCC6908HV goes into sleep mode and VG keeps at low once VDD drops below 3.6V.

Turn-on Phase

While VDS (VD-VSS) falls through 2V, a turn-on timer starts. This turn-on timer can be programmed by external resistor at SLEW pin. If VDS reaches -86mV turn-on threshold from 2V within this time set by the timer, MOSFET will be turned on after a turn-on delay which is around 30ns for ZCC6908HV (as showed in Fig.2). If VDS across -86mV after the timer times off, gate voltage VG is going to stay off. This turn-on timer is to prevent ZCC6908HV from false turn-on due to ringing from DCM and QR operations. TSLEW can be programmed by the following equation:

$$T_{SLEW} = R_{SLEW} \times \frac{20ns}{100k\Omega}$$

Turn On Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on, it makes sure that the on state at least lasts for some time. The turn on blanking time is ~1.97us to prevent accidently turn-off because of ringing, during which the turn off threshold is blanked (as showed in Fig.2) and sink ability is limited at ~2.5mA. However if Vds not only reaches turn-off threshold of 0mV, but also all the way up to 2-3V, VG is pulled low immediately even though ~1.97us minimum on time has not been satisfied.

Conduction Phase

When VDS rises above the forward voltage drop (- 40mV) according to the decrease of switching current, ZCC6908HV will pull down the gate voltage level to make the on resistance of synchronous MOSFET larger to ease the rise of VDS.

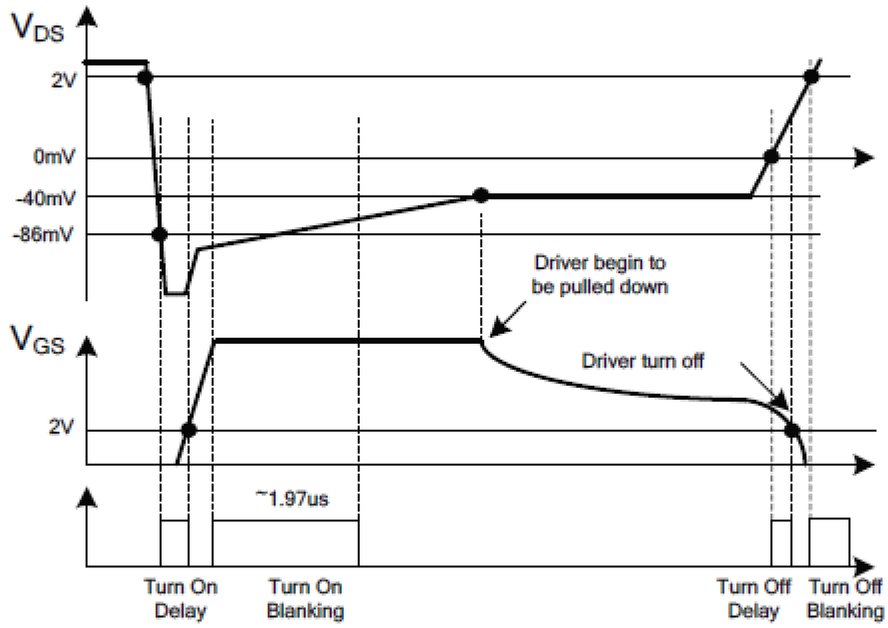


Figure 2—Turn on/off Timing Diagram

See Fig.2, with this control scheme, VDS is adjusted to be around -40mV even when the current through the MOSFET is fairly low, this function can make the driver voltage at very low level when synchronous MOSFET is going to be turned off, which boosts the turn off speed.

Turn-off Phase

When VDS rises to trigger the turn off threshold (0mV), the gate voltage is pulled to zero after a very short turn off delay which is 15ns, see Fig.2.

Turn-off Blanking

After gate driver VG is pulled to zero by VDS touching the turn-off threshold (0mV), a turn-off blanking time will be applied during which the gate driver signal is latched off, the turn-off blanking will be removed when VDS voltage rises to above 2V (as showed in Fig.2)

Typical System Implementations

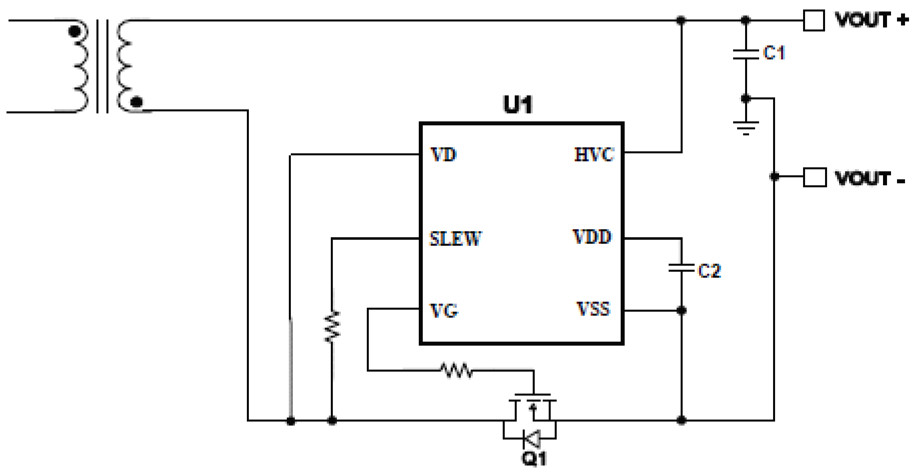


Figure 3— ZCC6908HV in Low-Side Rectification

Fig.3 shows the typical system implementation for the IC power supply derived from output voltage VOUT, which is available in low-side rectification.

Since HVC operating range is from 0V to 180V, ZCC6908HV can support most applications even when VOUT is down to 0V for low-side rectification. When VOUT (HVC) is above 10.5V, VDD will be regulated at 9.5V. VDD follows VOUT (HVC) with 0.7V dropout until VOUT is below 4.7V. Once VOUT drops below 4.7V, another 40mA current source from Drain of SR MOSFET Q1 (VD) is going to charge VDD up and regulate at 5.2V again.

SR MOSFET Selection

The Power MOSFET selection proved to be a tradeoff between RDS(ON) and Qg. To achieve higher efficiency, the MOSFET with smaller RDS(ON) is always preferred, while Qg is usually larger with RDS(ON) smaller, which makes the turn-on/off speed lower and lead to larger power loss including driver loss. For ZCC6908HV, because VDS is adjusted at ~-40mV during the driving period when switching current is fairly small, the MOSFET with too low RDS(ON) is not recommend, because the gate driver will started to be pulled to low when VDS=-ISDxRDS(ON) becomes larger than -40mV, which makes MOSFET's RDS(ON) no contribution to conduction loss then (conduction loss PCON=-VDSxISD≈ISDx40mV).

Fig.4 shows the typical waveform of QR flyback. Assume 50% duty cycle and the output current is IOUT.

To achieve fairly high usage of the MOSFET's RDS(ON), it is expected that the MOSFET be fully turned on at least 50% of the SR conduction period:

$$Vds = -Ic \times Ron = -2 \cdot I_{OUT} \times Ron \leq -Vfwd$$

Where VDS is Drain-Source voltage of the MOSFET and Vfwd is the forward voltage threshold of ZCC6908HV, which is ~40mV.

So the MOSFET's RDS(ON) is recommended to be no lower than ~20/IOUT (mΩ). (For example, for 5A application, the RDS(ON) of the MOSFET is recommended to be no lower than 4mΩ).

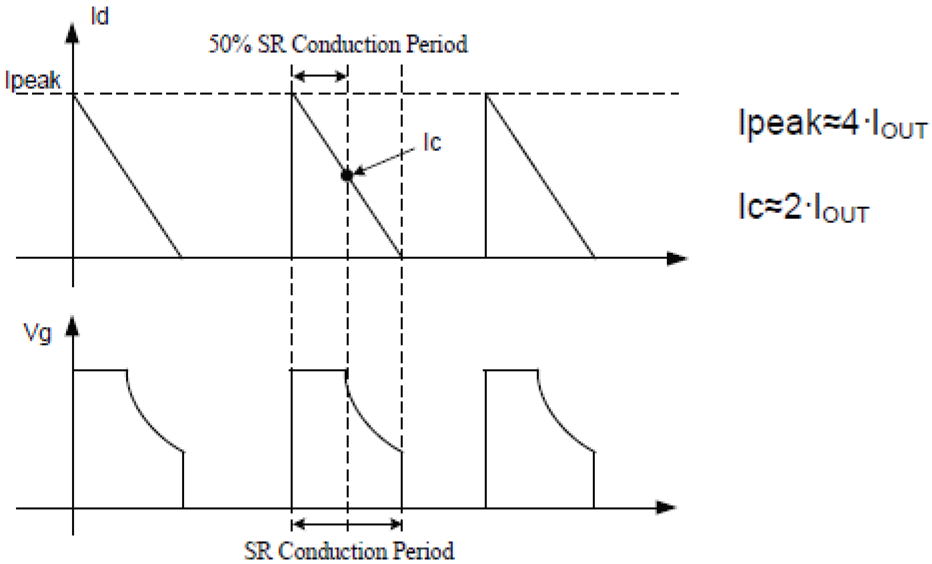
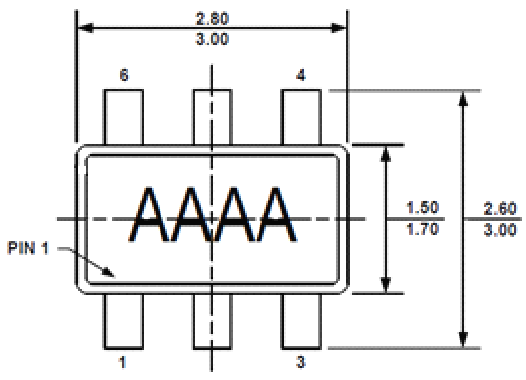


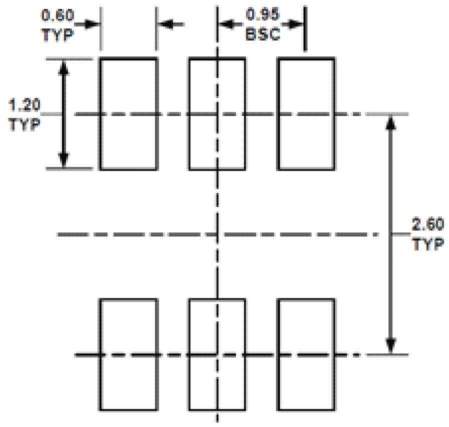
Figure 4—Synchronous Rectification typical waveforms in QR Flyback

PACKAGE INFORMATION

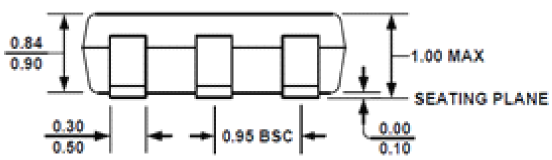
TSOT23-6



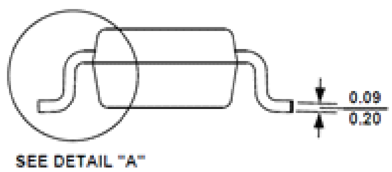
TOP VIEW



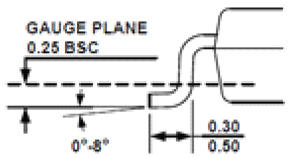
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"