



ALGOLTEK

AG6310

**DP to HDMI
Converter**

Data Sheet

Official Version

V1.2

October, 2017



Revision History

Version	Date	Notes
0.1.0	2017/6/205	Preliminary
0.2.0	2017/9/29	Modify pin description.
1.0.0	2017/10/25	First release
1.1.0	2018/10/15	Added another package
1.2	2019/4/29	Update Table4: Add T_j / θ_{JC} , / θ_{JA}

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I. General Description

ALGOLTEK AG6310 is a single chip solution to implement DisplayPort to HDMI data converter. AG6310 is a single chip solution which transmits both the video and audio streams via single DisplayPort connector. Its DisplayPort 1.2 receiver supports configurable 1, 2 and 4 lanes @ 1.62Gbps, 2.7Gbps and 5.4Gbps input, and the HDMI supports up to 4K2K@30Hz output. AG6310 Series also support the external SPI flash for the firmware upgrade for better compatibility and flexibility. It's a good fit for the applications of docking stations, extended display adaptors and dongles for the laptop PC, tablet and smartphone accessory markets.

II. Features

- Embedded 16 bit MCU
- EDID and MCCS pass-through supported
- Supports Hot Plug Detection
- External SPI flash supported for firmware upgrade
- Embedded HDCP 1.4 supported
- HDMI 1.4b TX supports 4K@30Hz output
- 2KV ESD performance
- Down Spread Spectrum Clock (SSC) supported

III. Device Information

Part Number	Package	Body Size	Note
AG6310-MAQ	QFN-64	8x8 mm ²	/w I ² S audio output
AG6310-MBQ	QFN-48	6x6 mm ²	/wo I ² S audio output /w USB DP_DM

IV. Application

- DisplayPort dongle

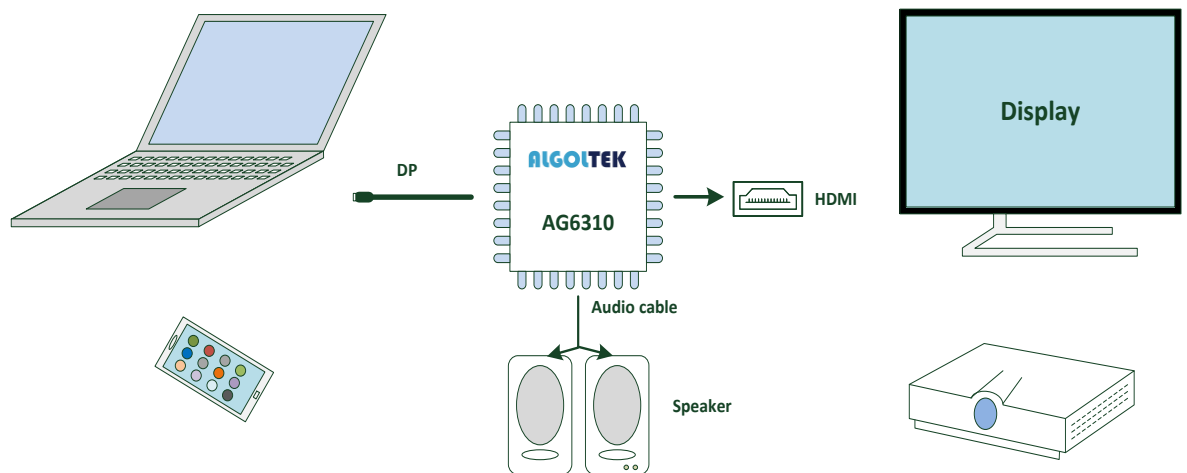


Figure 1 Application for DisplayPort to HDMI Dongle



V. System Block Diagram

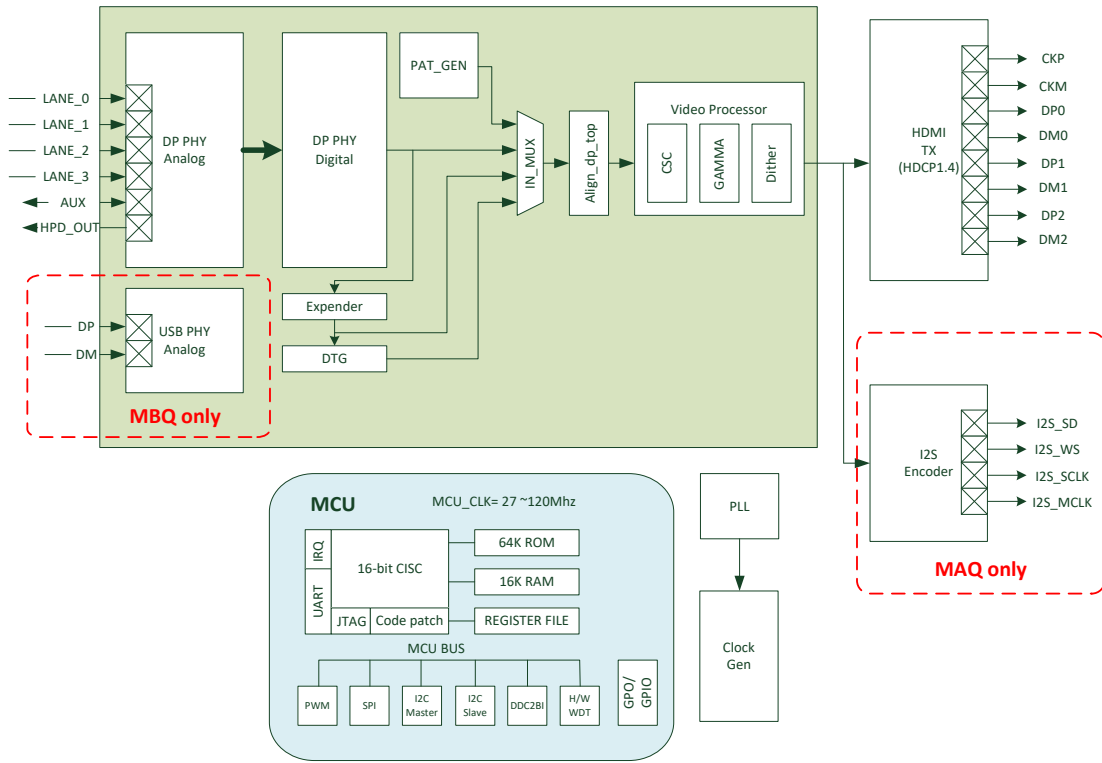


Figure 2 System Block Diagram

VI. Pin Mapping and Description

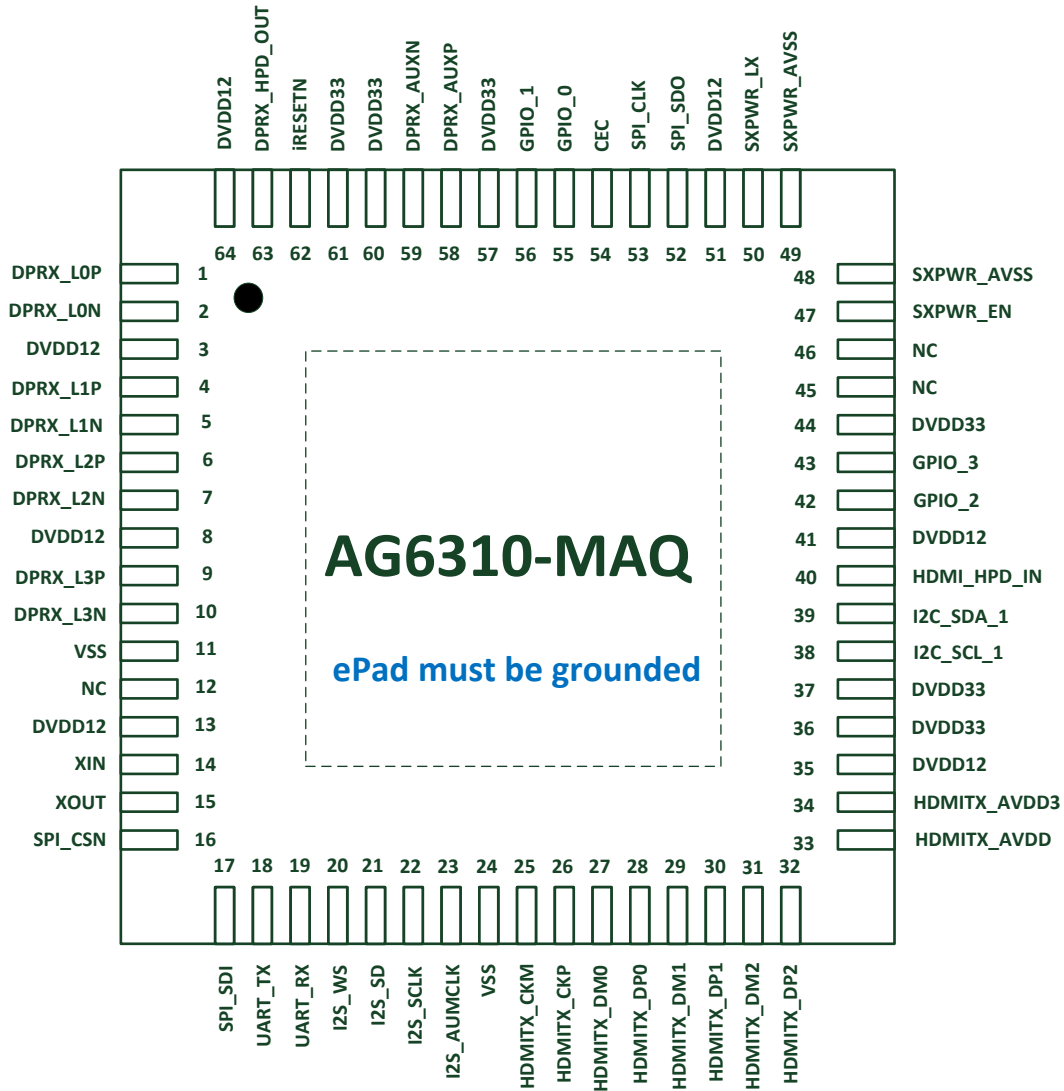


Figure 3 AG6310-MAQ PIN Mapping



Table 1 AG6310-MAQ PIN Description

Pin Name	PIN NO.	Type	Description
POWER SUPPLY			
DVDD33	36, 37, 44, 57, 60, 61	Power	Digital 3.3V I/O power input
DVDD12	3, 8, 13, 35, 41, 51, 64	Power	Digital 1.2V core power input
VSS	11, 24,	Power	Digital ground
HDMITX_AVDD	33	Power	Analog 1.2V power for HDMI TX
HDMITX_AVDD3	34	Power	Analog 3.3V power for HDMI TX
SXPWR_AVSS	48, 49	Power	Analog ground.
SXPWR_LX	50	Power	NC
DIFFERENTIAL HIGH-SPEED IO			
DPRX_LOP	1	Input	DP RX lane0 positive
DPRX_LON	2	Input	DP RX lane0 negative
DPRX_L1P	4	Input	DP RX lane1 positive
DPRX_L1N	5	Input	DP RX lane1 negative
DPRX_L2P	6	Input	DP RX lane2 positive
DPRX_L2N	7	Input	DP RX lane2 negative
DPRX_L3P	9	Input	DP RX lane3 positive
DPRX_L3N	10	Input	DP RX lane3 negative
HDMITX_CKM	25	Output	HDMI TX clock channel negative
HDMITX_CKP	26	Output	HDMI TX clock channel positive
HDMITX_DM0	27	Output	HDMI TX data channel 0 negative
HDMITX_DP0	28	Output	HDMI TX data channel 0 positive
HDMITX_DM1	29	Output	HDMI TX data channel 1 negative
HDMITX_DP1	30	Output	HDMI TX data channel 1 positive
HDMITX_DM2	31	Output	HDMI TX data channel 2 negative
HDMITX_DP2	32	Output	HDMI TX data channel 2 positive
DPRX_AUXN	59	Bidirectional	DisplayPort AUX channel N
DPRX_AUXP	58	Bidirectional	DisplayPort AUX channel P
Digital IO			



XIN	14	Input	Crystal oscillator clock input
XOUT	15	Output	Crystal oscillator clock output
SPI_CSN	16	Output	SPI chip select.
SPI_SDI	17	Input	SPI data input
UART_TX	18	Output	UART TX
UART_RX	19	Input	UART RX
I2S_WS	20	Output	I2S Left Right Clock
I2S_SD	21	Output	I2S Serial Audio Data Output
I2S_SCLK	22	Output	I2S Continuous Serial Clock
I2S_AUMCLK	23	Output	I2S System Clock
I2C_SCL_1	38	Bidirectional	HDMI I2C SCL
I2C_SDA_1	39	Bidirectional	HDMI I2C SDA
HDMI_HPD_IN	40	Input	HDMI cable detection
GPIO_2	42	Bidirectional	General Purpose I/O
GPIO_3	43	Bidirectional	General Purpose I/O
SXPWR_EN	47	Input	Pull down to ground
SPI_SDO	52	Output	SPI data output.
SPI_CLK	53	Output	SPI clock.
CEC	54	Input	HDMI CEC
GPIO_0	55	Bidirectional	General Purpose I/O
GPIO_1	56	Bidirectional	General Purpose I/O
iRESETN	62	Input	H/W Reset signal, active low. Need connect to Resistor and Capacitor on board.
DPRX_HPD_OUT	63	Output	DP RX Hot Plug Detect

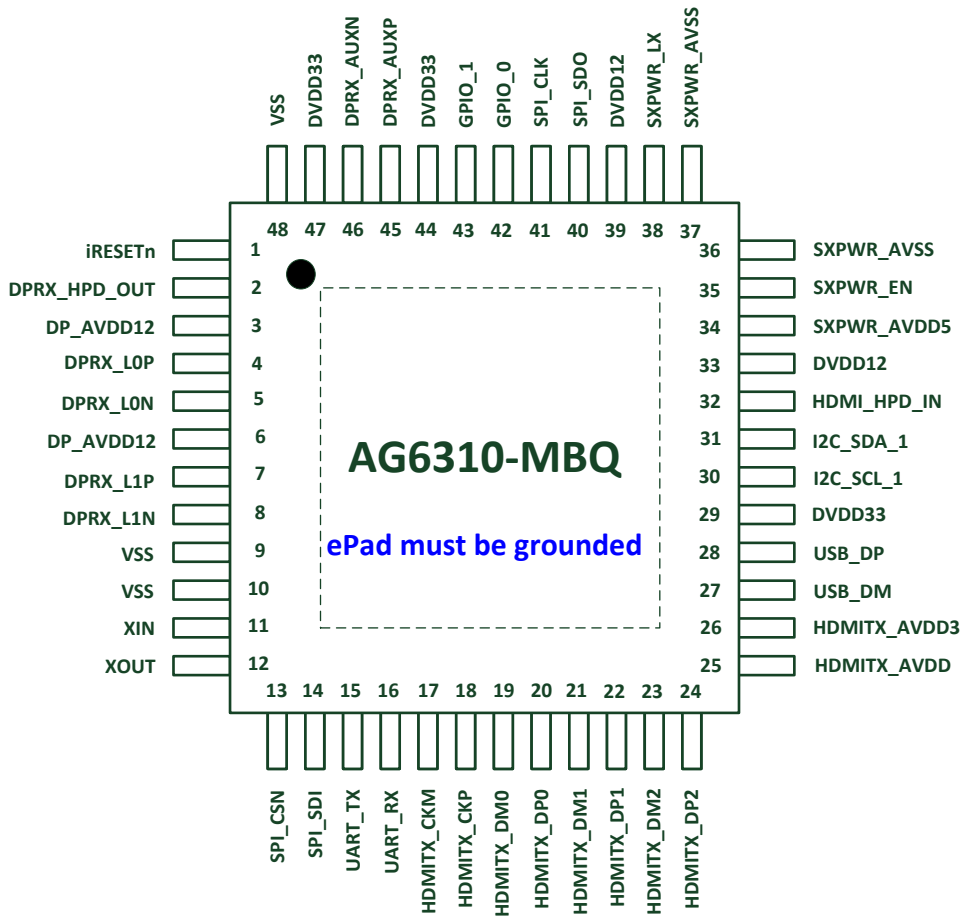


Figure 4 AG6310-MBQ PIN Mapping

Table 2 AG6310-MBQ PIN Description

Pin Name	PIN NO.	Type	Description
POWER SUPPLY			
DP_AVDD12	3,6	Power	Analog 1.2V power input for DP RX
DVDD33	29, 44, 47	Power	Digital 3.3V I/O power input
DVDD12	33, 39	Power	Digital 1.2V core power input
VSS	9, 10, 48	Power	Digital ground
HDMI_TX_AVDD	25	Power	Analog 1.2V power for HDMI TX
HDMI_TX_AVDD 3	26	Power	Analog 3.3V power for HDMI TX



SXPWR_AVDD5	34	Power	5.0V power input. Input voltage range: 3.0V ~ 5.5V
SXPWR_AVSS	36, 37	Power	Analog ground.
SXPWR_LX	38	Power	NC
DIFFERENTIAL HIGH-SPEED IO			
DPRX_LOP	4	Input	DP RX lane0 positive
DPRX_LON	5	Input	DP RX lane0 negative
DPRX_L1P	7	Input	DP RX lane1 positive
DPRX_L1N	8	Input	DP RX lane1 negative
HDMITX_CKM	17	Output	HDMI TX clock channel negative
HDMITX_CKP	18	Output	HDMI TX clock channel positive
HDMITX_DM0	19	Output	HDMI TX data channel 0 negative
HDMITX_DP0	20	Output	HDMI TX data channel 0 positive
HDMITX_DM1	21	Output	HDMI TX data channel 1 negative
HDMITX_DP1	22	Output	HDMI TX data channel 1 positive
HDMITX_DM2	23	Output	HDMI TX data channel 2 negative
HDMITX_DP2	24	Output	HDMI TX data channel 2 positive
USB_DM	27	Bidirectional	USB Type-C D-
USB_DP	28	Bidirectional	USB Type-C D+
DPRX_AUXN	46	Bidirectional	DisplayPort AUX channel N
DPRX_AUXP	45	Bidirectional	DisplayPort AUX channel P
Digital IO			
XIN	11	Input	Crystal oscillator clock input
XOUT	12	Output	Crystal oscillator clock output
SPI_CSN	13	Output	SPI chip select.
SPI_SDI	14	Input	SPI data input
UART_TX	15	Output	UART TX
UART_RX	16	Input	UART RX
I2C_SCL_1	30	Bidirectional	HDMI I2C SCL
I2C_SDA_1	31	Bidirectional	HDMI I2C SDA
HDMI_HPD_IN	32	Input	HDMI cable detection
SXPWR_EN	35	Input	Pull down to ground
SPI_SDO	40	Output	SPI data output.
SPI_CLK	41	Output	SPI clock.



GPIO_0	42	Bidirectional	General Purpose I/O
GPIO_1	43	Bidirectional	General Purpose I/O
iRESETN	1	Input	H/W Reset signal, active low. Need connect to Resistor and Capacitor on board.
DPRX_HPD_OUT	2	Output	DP RX Hot Plug Detect

VII. Specification

i. Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDD5	5V Power Input	-0.5	5.5	V
VDD33/AVDD33	3.3V supply voltage	-0.5	3.63	V
VDD/AVDD	1.2V supply voltage	-0.5	1.32	V

Table 3 Absolute Maximum Rating

ii. DC Characteristics/Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
VDD5	5V Power Input	4.5	5	5.5	V
VDD33	Digital I/O supply voltage	3	3.3	3.6	V
VDD	Digital core supply voltage	1.16	1.2		V
AVDD3	Analog I/O supply voltage	3	3.3	3.6	V
AVDD	Analog core supply voltage	1.16	1.2		V
I _{VDD33+AVDD3}	3.3V I/O Supply Current (4K2K/30Hz)		80		mA
I _{VDD+AVDD}	1.2V Core supply Current (4K2K/30Hz)		380		mA
V _{OH}	Output High Voltage	2.4			V
V _{OL}	Output Low Voltage			0.4	V
V _{IH}	Input High Voltage	2.0		5.5	V
V _{IL}	Input Low Voltage	-0.3		0.8	V
I _{LI}	Input leakage Cur.			±1	uA
θ _{JC}	Thermal Resistance of QFN48L (Junction to Case)		2.0		°C/W
	Thermal Resistance of QFN64L (Junction to Case)		1.2		°C/W
θ _{JA}	Thermal Resistance of QFN48L (Junction to Ambient)		33		°C/W
	Thermal Resistance of QFN64L		24		°C/W



	(Junction to Ambient)				
T _J	Junction Temperature	0		125	°C
T _A	Ambient Temperature	0		70	°C

Table 4 Digital I/O Specification

iii. AC Characteristics

DisplayPort Main Link AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UI_HBR2	Unit interval for HBR2(5.4-Gbps/lane)		185		ps
UI_HBR	Unit interval for HBR(2.7-Gbps/lane)		370		ps
UI_RBR	Unit interval for RBR(1.62-Gbps/lane)		617		ps
Down_Spread_Amp.	Link clock down-spreading	0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency	30		33	kHz
T _{RX-MEDIAN-to-MAX-JITTER}	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)			0.265	UI
T _{RX-MEDIAN-to-MAX-JITTER}	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)			0.39	UI
V _{RX-DC-CM}	RX DC Common Mode Voltage	0		2	V
I _{RX-SHORT}	RX Short Circuit Current Limit			50	mA

Table 5 DisplayPort Input Timing

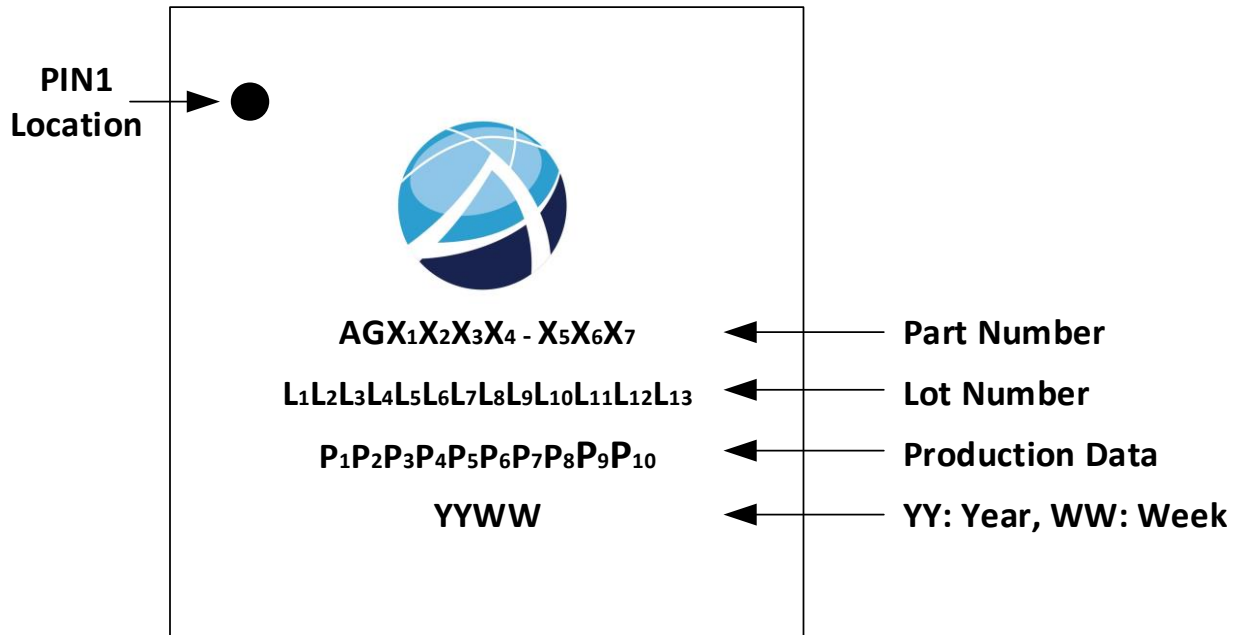
DisplayPort AUX-CH AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UIMAN	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	us
Pre-charge Pulses	Number of pre-charge pulses	10		16	
T _{AUX-BUS-PEAK}	AUX CH bus park time	10			ns
T _{cycle-to-cycle jitter}	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
V _{AUX-DIFFp-p RX}	AUX peak-to-peak voltage at a transmitting device when receiving	0.29		1.38	V
V _{AUX-DIFFp-p RX}	AUX peak-to-peak voltage at a receiving device when receiving	0.27		1.36	V
V _{AUX_TERM_R}	AUX CH termination DC resistance		100		Ω
V _{AUX_DC_CM}	AUX DC common mode voltage	0		2.0	V
V _{AUX_TURN_CM}	AUX turn around common mode voltage			0.3	V
I _{AUX_SHORT}	AUX short circuit current			90	mA
C _{AUX}	AUX AC coupling	75		200	nF

Table 6 DisplayPort AUX Channel I/O Specification

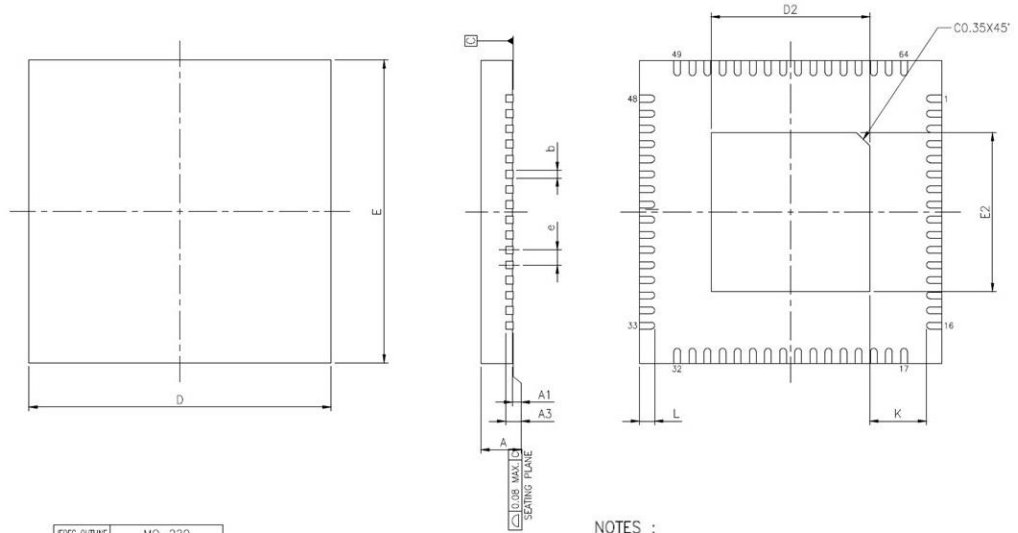
VIII. Packing and Marking Specification

- Marking





● **Package Dimension**
AG6310-MAQ: QFN-64L 8x8mm



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X864)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

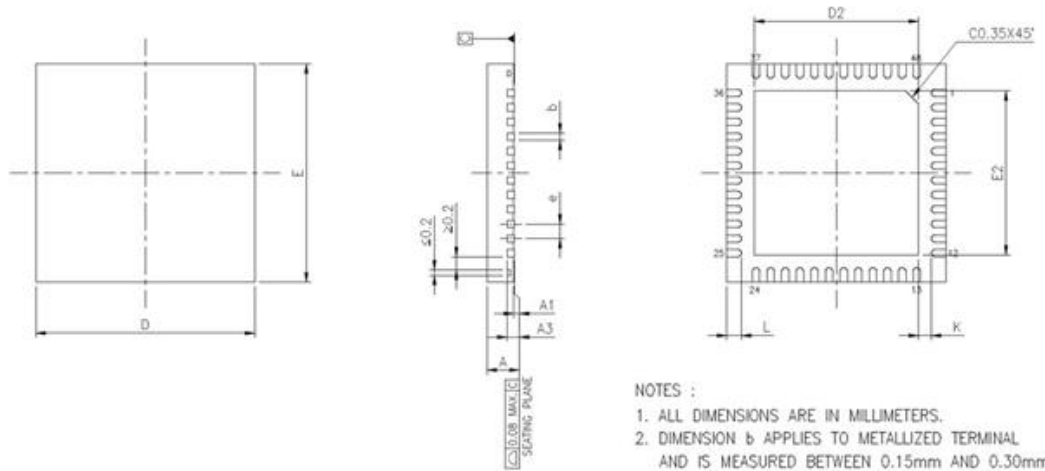
PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
268X26* ML	6.40	6.50	6.60	6.40	6.50	6.60	V	X	W(V)LLE-2

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 5 AG6310-MAQ Package Dimension

AG6310-MBQ: QFN-48L 6x6mm



A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Sn	PPF	
185x18° ML	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	v	x	(W)VJJE-1

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 6 AG6310-MBQ Package Dimension



IX. References

- DisplayPort™ Standard 1.2b Specification
- HDMI 1.4b Specification

X. Contact Information

ALGOLTEK, INC.
www.algotek.com.tw
Sales@algotek.com.tw

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