A Novel Zero-Voltage and Zero-Current-Switching PWM Full-Bridge Converter Using Two Diodes in Series With the Lagging Leg

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***Abstract*—This paper proposes a novel phase-shifted zero-voltage and zero-current-switching (ZVZCS) pulsewidth modulation full-bridge converter, which realizes ZVS for the leading leg and ZCS for the lagging leg. A blocking capacitor is added in series with the primary winding of the transformer to make the primary current decay to zero during zero state to ensure ZCS for the lagging leg. In order to prevent the primary current from reversing during zero state, two diodes in series with the lagging leg are added. The principle of operation, steady-state analysis, and design procedures are presented. The experimental results are also included to verify the theoretical analysis.**

***Index Terms*—Full-bridge converter, pulsewidth modulation, soft-switching technique.**

I. Introduction

In RECENT years, soft-switching pulsewidth modulation (PWM) full-bridge (FB) converters have attracted increased attention, and a number of topologies and modulation strategies have been proposed. Phase-shifted (PS) zero-voltage-switching (ZVS) PWM FB converters achieve ZVS for both the leading leg and the lagging leg with the use of the leakage inductor of the main transformer and the output capacitors of the power switches [1], [2]. PS zero-voltage and zero-current-switching (ZVZCS) PWM FB converters achieve ZVS for the leading leg and ZCS for the lagging leg [3]–[7]. Chen and Stuart [8] and Masserant *et al.* [9] proposed two kinds of PWM FB converters, which achieve ZVS for one leg and ZCS for the other leg.

In order to reveal the relationship among the aforementioned soft-switching PWM FB converters and modulation strategies, [10] systematically proposed a family of PWM modulation strategies. It includes nine modulation strategies containing all the modulation strategies previously proposed. The nine modulation strategies can be classified into two categories depending on the turn-off sequence of the diagonal power switches. If the two power switches turn off at different time, FB converters can achieve PWM soft switching without adding any auxiliary power switch, thus introducing the concept of leading leg and lagging leg. The leading leg can only achieve ZVS, which is easily achieved. Depending on the operation mode of the zero state in the FB converter, the lagging leg has two kinds of soft-switching mechanisms. If the zero state operates in current constant mode (CCM), the lagging leg can achieve ZVS; and if the zero state operates in current reset mode (CRM), the lagging leg can achieve ZCS. Therefore, soft-switching PWM FB converters can be classified into two types: ZVS and ZVZCS. ZVS PWM FB converters' zero state operates in CCM, and both the leading leg and the lagging leg achieve ZVS; ZVZCS PWM FB converters' zero state operates in CRM, and the leading leg achieves ZVS and the lagging leg achieves ZCS. Reference [10] also points out three kinds of modulation strategies suited for ZVS PWM FB converters and two kinds of modulation strategies suited for ZVZCS PWM FB converters. PS modulation strategy suits both types of soft-switching PWM FB converters.

Concerning ZVZCS PWM FB converters, in order to achieve ZCS for the lagging leg, it is important to make the primary current decay to zero and then keep it at zero during the zero state. Section II proposes the current reset strategies, and then a novel ZVZCS PWM FB converter is derived. Section III analyzes the principle of operation of the novel converter, Section IV presents the theoretical analysis, Section V presents simplified design procedures and a design example, and Section VI gives the experimental results to verify the principle of operation of the novel converter.

II. Derivation of a Novel ZVZCS PWM FB Converter

A. Current Reset Strategies

In order to make the primary current i_p decay to zero in zero state, a blocking voltage source $v_{\rm block}$ can be inserted in series with the primary winding as shown in Fig. 1(a). In zero state, if i_p flows in the positive direction, the blocking voltage source is positive, as shown in Fig. 1(b), and if i_p flows in the negative direction, the blocking voltage source is negative, as shown in Fig. 1(c). The blocking voltage source can be simply realized by a capacitor C_b , named a blocking capacitor, as shown in Fig. 2(a). When Q_1 and Q_4 conduct, i_p charges C_b, and when Q_2 and Q_3 conduct, i_p discharges C_b. During zero state, the voltage of C_b keeps constant and resets i_p, as shown in Fig. 2(b).

B. Blocking the Reverse Flowing Path

During zero state, in order to achieve ZCS for the lagging leg, i_p should be prevented from turning negative after it decays to zero. Therefore, the reverse path for i_p should be blocked. As seen from Fig. 2(a), there are three possible places to block

Manuscript received May 9, 2000; revised February 1, 2001. Abstract published on the Internet June 6, 2001.

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Publisher Item Identifier S 0278-0046(01)06279-7.

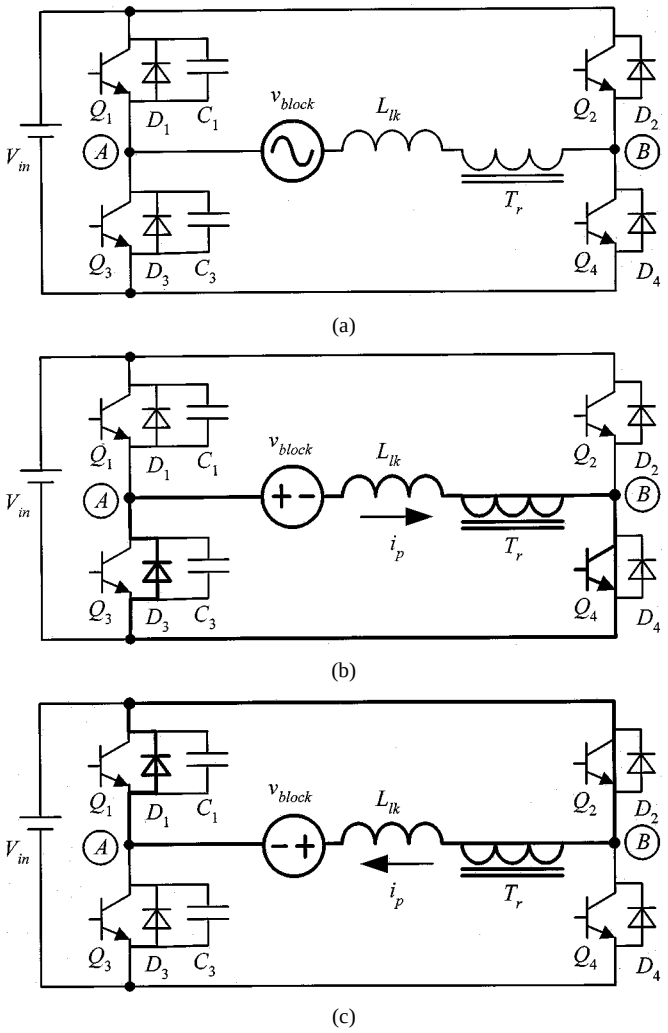

Fig. 1. The requirement of the blocking voltage source. (a) Blocking voltage source. (b) $i_p > 0$. (c) $i_p < 0$.

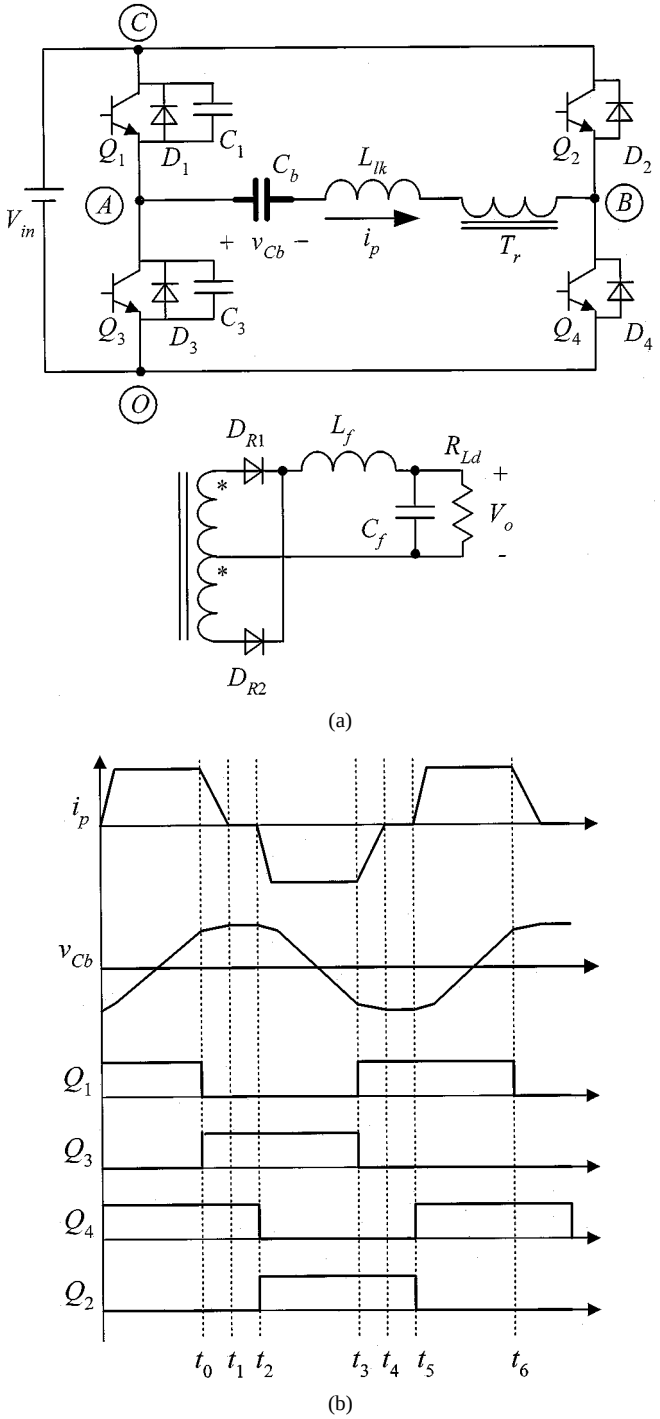

Fig. 2. ZVZCS PWM FB converter. (a) Main circuit. (b) Key waveforms.

the reverse path: 1) segment AO/AC; 2) segment AB; and 3) segment BO/BC.

In order to achieve ZVS for the leading leg, either Q_1 or Q_3 has been turned on during zero state, which makes it impossible to prevent i_p from flowing in the reverse direction in the AO/AC segment.

In segment AB, the simplest way to block the reverse flowing path is to add a saturable inductor as shown in Fig. 3(a) [3]. During zero state, the saturable inductor behaves as a high-impedance device to prevent i_p from flowing in the reverse direction. As in $+1$ or -1 state, it is saturated. In segment AB, there are additional four methods as shown in Fig. 3(b)–(e) [4]–[7].

In segment BO/BC, we can add D_2 and D_4 in series with the lagging switches Q_2 and Q_4, respectively, to make Q_2 and Q_4 conduct only in the positive direction. A novel ZVZCS PWM FB converter is thereby proposed, as shown in Fig. 3(f).

C. Comparison of the ZVZCS PWM FB Converters

The converter in Fig. 3(a) is very simple because only one saturable inductor is needed. However, the use of the saturable inductor results in two drawbacks. First, it causes a secondary duty cycle loss. In general, as the input voltage $V_{\rm in}$ has a certain variation range, L_s should be designed according to $V_{\rm in\,max}$ to prevent L_s from saturation during zero state, thus, the effective secondary duty cycle is reduced as $V_{\rm in}$ decreases. The lower the $V_{\rm in}$, the larger the secondary duty cycle loss. Second, the saturable inductor causes high core loss since it saturates in both directions.

In Fig. 3(b), the blocking capacitor is shifted to the secondary side and also an active switch is introduced, which cannot only reset the primary current, but also clamp the rectified voltage to depress the parasitic voltage oscillation. However, the converter requires an additional active switch and the associated control circuitry.

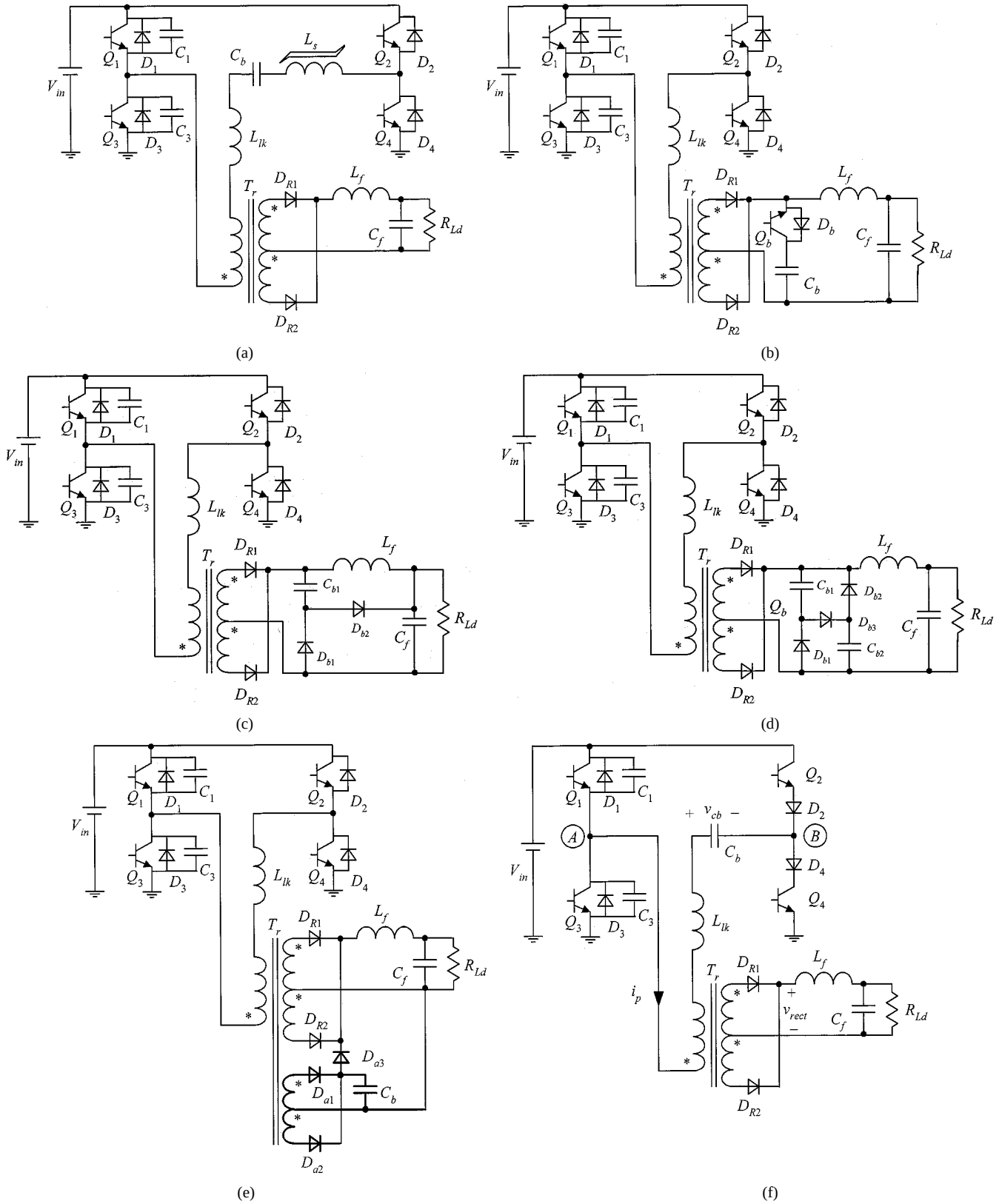

Fig. 3. Topologies for ZVZCS PWM FB converters. (a) Using the saturable inductor. (b) Using the active clamp circuit. (c) Number 1 secondary reset circuit. (d) Number 2 secondary reset circuit. (e) Adding an auxiliary winding. (f) Adding two series diodes.

In Fig. 3(c)–(e), the blocking capacitor is also shifted to the secondary side, the primary current reset mechanisms of all three converters are similar. The energy stored in the blocking capacitor is delivered to the load during zero state. The converter in Fig. 3(c) is better than the other two in terms of simplicity. Furthermore, the peak secondary rectified voltage is inversely proportional to the duty cycle and lower than twice the reflected input voltage. For example, if duty cycle is 0.8, the peak recti-

fied voltage is 1.2 times the reflected input voltage. However, this converter also has three drawbacks.

1) In zero state, the blocking capacitor has been fully discharged, so when the lagging leg turns on, the primary current has an excess high current spike due to charging of the blocking capacitor. The larger the blocking capacitor, the larger the current spike.
2) When the leading leg turns off, the rectified voltage ramps down. As it becomes lower than the blocking capacitor voltage, the blocking capacitor will supply the rectified output filter inductor current. Thus, only the energy stored in the leakage inductor (instead of the output filter inductor) to charge and discharge the paralleled capacitor of the leading leg. In general, the leakage inductor is too small to fully discharge the remaining charge of the paralleled capacitors of the leading leg, which may results in hard turn-on of the leading leg.
3) As the converter operates in zero state, the blocking capacitor not only needs to reset the primary current, but also provides the rectified output current. If the blocking capacitor is not sufficiently large, its energy will not be enough to reset the primary current.

The novel converter in Fig. 3(f) only introduces two diodes and does not have the drawbacks mentioned above. When the leading leg turns on, there is no excess current spike because the blocking capacitor is in series with the load (including L_f, C_f and R_{Ld}) instead of being in parallel with the load. During the switching interval of the leading leg, the output filter inductor is in series with the leakage inductor, the energy of the leakage inductor and the output filter inductor is used to achieve ZVS for the leading leg, so it is easy to realize ZVS. In zero state, the output current freewheels via two secondary rectifier diodes, and the voltage of the blocking capacitor is fully used to reset the primary current. As will be explained later, the lagging leg can achieve ZCS under any load condition. One drawback of this converter is that the primary-side conduction losses are slightly increased due to the series diodes. However, these increased losses are not very significant.

III. Principle of Operation

In this section, the principle of operation of the novel ZVZCS PWM FB converter is presented. Fig. 4 shows the key waveforms of the novel converter employing PS modulation strategy.

The following assumptions are made in this analysis: 1) all power devices and diodes are ideal; 2) all capacitors and inductors are ideal; 3) output filter inductor L_f is large enough to be treated as a constant current source during a switching period; and 4) $C_1 = C_3 = C_r$.

During a switching period, there are ten switching modes, as described in the following. The equivalent circuits are shown in Fig. 5.

1) Mode 0 [Prior to t_0] [Fig. 5(a)]: Prior to t_0, Q_1 and Q_4 are conducting, and primary current i_p charges the blocking capacitor C_b. $I_p(t_0) = I_{p0} = I_o/K$, where I_o is output current, K is the turns ratio of the transformer, $V_{cb}(t_0)$ is the voltage of C_b at t_0.

2) Mode 1 [t_0, t_1] [Fig. 5(b)]: Q_1 is turned off at t_0, i_p charges C_1 and discharges C_3. Q_1 is turned off with ZVS

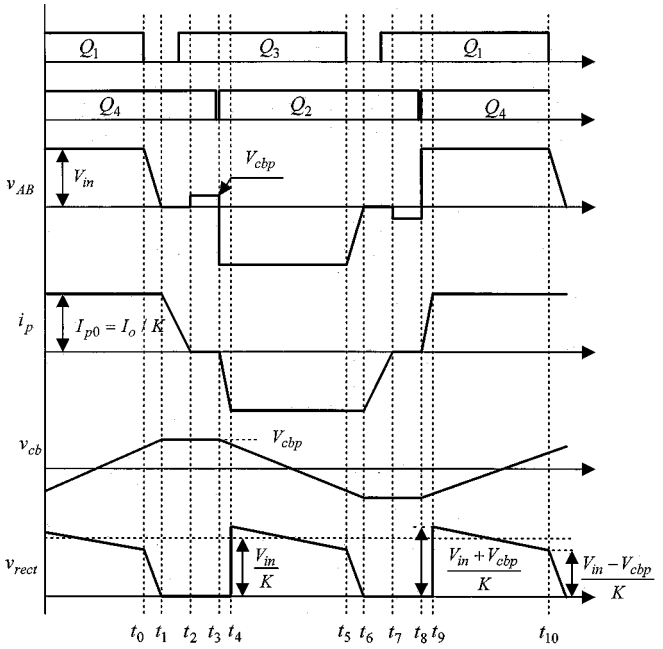

Fig. 4. Key waveforms of the novel ZVZCS PWM FB converter.

because C_3 and C_1 limit the rising rate of the voltage across Q_1. During this interval, the leakage inductor of transformer L_{lk} is in series with L_f. L_f is large enough to be treated as a constant current source so that i_p keeps the value $I_{p0} = I_o/K$. i_p continues charging C_b. The voltage of C_1 rises linearly and the voltage of C_3 decays linearly

$$v_{cb}(t) = V_{cb}(t_0) + I_{p0} \bullet \frac{t - t_0}{C_b} \tag{1}$$

$$v_{c1}(t) = \frac{I_{p0}}{2C_r}(t - t_0) \tag{2}$$

$$v_{c3}(t) = V_{\text{in}} - \frac{I_{p0}}{2C_r}(t - t_0). \tag{3}$$

At t_1, v_{c3} decays to zero, D_3 turns on naturally, and mode 1 ends. The time period for mode 1 is

$$t_{01} = 2C_r V_{\text{in}}/I_{p0}. \tag{4}$$

At t_1, the voltage of C_b is

$$V_{cb}(t_1) = V_{cb}(t_0) + 2 \bullet \frac{C_r V_{\text{in}}}{C_b}. \tag{5}$$

3) Mode 2 [t_1, t_2] [Fig. 5(c)]: As D_3 is conducting, Q_3 is turned on with ZVS. The delay time between Q_1 and Q_3 gate drive signals should be greater than the time period of mode 1, i.e., $t_d > t_{01}$. During this interval, D_3 and Q_4 conduct, $v_{AB} = 0$. v_{cb} is applied to L_{lk} and primary winding, which forces i_p to decrease. Therefore, i_p is not enough to provide the load current, and the secondary rectifier diodes D_{R1} and D_{R2} conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at zero, so v_{cb} is fully applied to L_{lk}. Since C_b is large enough to be treated as a constant voltage source during this mode, i_p decays linearly

$$v_{cb}(t) = V_{cb}(t_1) \equiv V_{cbp} \tag{6}$$

$$i_p(t) = I_{p0} - \frac{V_{cbp}}{L_{lk}}(t - t_1). \tag{7}$$

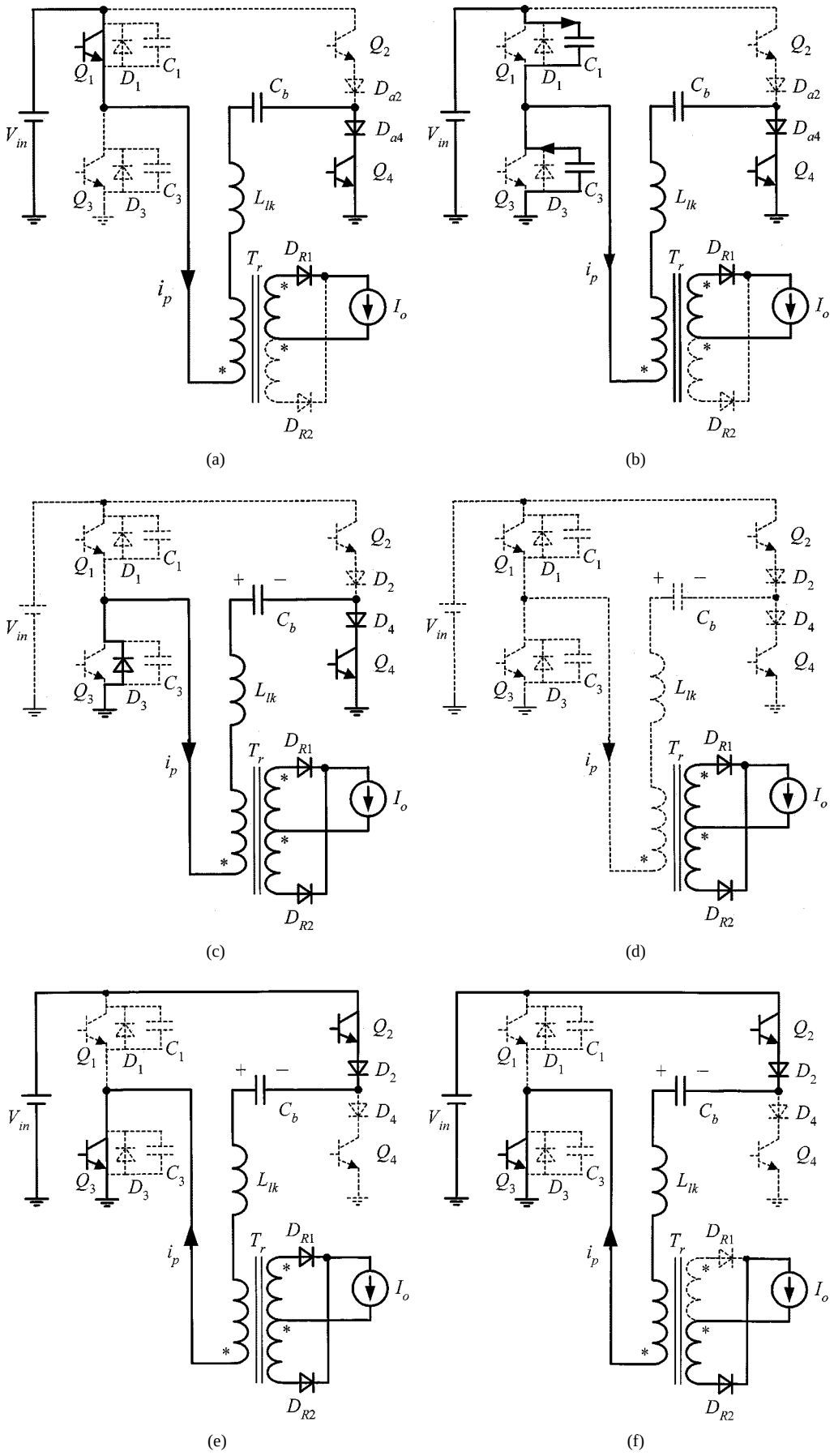

Fig. 5. Equivalent circuits of the switching modes. (a) Prior to t_0. (b) $[t_0, t_1]$. (c) $[t_1, t_2]$. (d) $[t_2, t_3]$. (e) $[t_3, t_4]$. (f) $[t_4, t_5]$.

At t_2, i_p decays to zero. The time period for mode 2 is t_{12}

$$t_{12} = L_{lk} \bullet I_{p0}/V_{cbp}. \tag{8}$$

4) Mode 3 [t_2, t_3] [Fig. 5(d)]: During mode 3, as the diode D_4 blocks the reverse path of i_p, i_p keeps at zero. $v_A = 0$, and $v_B = -V_{cbp}$. Both rectifier diodes conduct and they share the load current equally.

5) Mode 4 [t_3, t_4] [Fig. 5(e)]: At t_3, Q_4 is turned off. As $i_p = 0$, there is no current flowing in Q_4, and Q_4 is turned off with ZCS. After a very short delay, Q_2 is turned on with ZCS because L_{lk} limits di_p/dt. As reflected primary current i_p is lower than the load current, both secondary rectifier diodes conduct, which clamps both the primary and secondary voltage of transformer at zero, $-(V_{\text{in}}+V_{cbp})$ is applied on L_{lk}, i_p linearly rises in the negative direction

$$i_p(t) = -\frac{V_{\text{in}} + V_{cbp}}{L_{lk}}(t - t_3). \tag{9}$$

At t_4, i_p rises to the reflected load current. The time interval of this mode is

$$t_{34} = \frac{L_{lk} \bullet I_{p0}}{V_{\text{in}} + V_{cbp}}. \tag{10}$$

6) Mode 5 [t_4, t_5] [Fig. 2(f)]: From t_4, primary side powers the load and i_p discharges C_b. D_{R1} turns off naturally and D_{R2} carries all the output current

$$v_{cb}(t) = V_{cbp} - \frac{I_{p0}}{C_b}(t - t_4). \tag{11}$$

At t_5, Q_3 is turned off, the second half-cycle [t_5, t_{10}] starts, which is similar to the first half-cycle [$t_0\, t_5$]. At this time,

$$V_{cb}(t_5) = V_{cbp} - \frac{I_{po}}{C_b} \bullet t_{45}. \tag{12}$$

IV. Theoretical Analysis

A. Peak Voltage of the Block Capacitor

In (8), it is clear that the interval t_{12} and the voltage stress of the lagging switches are determined by V_{cbp}, so it is important to calculate V_{cbp}. v_{cb} reaches the negative peak value $-V_{cbp}$ at t_6. The operation during [t_5, t_6] is similar to [t_0, t_1], so we can get the following equation:

$$\begin{aligned} V_{cb}(t_6) &= V_{cb}(t_5) - \frac{2C_r V_{\text{in}}}{C_b} \\ &= V_{cbp} - \frac{I_{po}}{C_b} \bullet t_{45} - \frac{2C_r V_{\text{in}}}{C_b} \\ &= -V_{cbp}. \end{aligned} \tag{13}$$

In general, $C_r \ll C_b$, (13) can be simplified as (14)

$$V_{cbp} = \frac{I_{po}}{2C_b} \bullet t_{45}. \tag{14}$$

B. Achieving ZVS for the Leading Leg

Clearly, from the above analysis, ZVS of the leading leg is realized by utilizing the energy of the output filter inductor. In general, the output filter inductor is large enough that ZVS can be achieved for the leading leg over a wide load range.

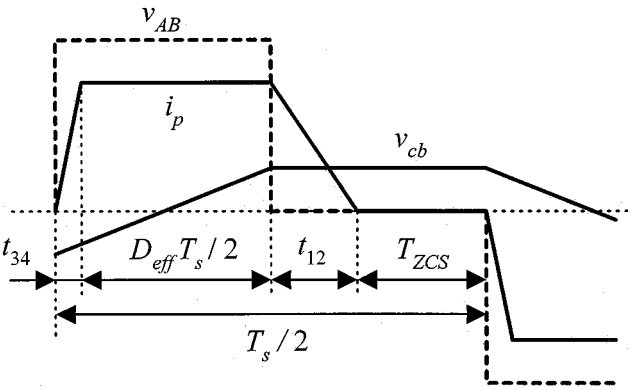

Fig. 6. Determination of $D_{\text{eff max}}$.

C. Maximum Effective Duty Cycle $D_{\text{eff max}}$

In order to achieve ZCS for the lagging leg, i_p should decay to zero before the switching of the lagging leg. t_{12} can be derived from (8) and (14)

$$t_{12} = \frac{2L_{lk}C_b}{t_{45}} = \frac{2L_{lk}C_b}{D_{\text{eff}} \bullet T_s/2} = \frac{4L_{lk}C_b}{D_{\text{eff}}T_s} \tag{15}$$

where D_{eff} is the effective duty cycle and T_s is the switching period.

According to Fig. 6, $D_{\text{eff max}}$ is determined by

$$D_{\text{eff max}} < 1 - D_{\text{reset}} - D_{\text{ZCS}} - D_{\text{loss}} \tag{16}$$

where $D_{\text{reset}} = t_{12}/(T_s/2)$, and $D_{\text{ZCS}} = t_{\text{ZCS}}/(T_s/2)$. ZCS is achieved during interval T_{ZCS}, which is determined by the turn-off characteristic of switching device, e.g., the minority carrier lifetime of the insulated gate bipolar transistors (IGBTs). $D_{\text{loss}} = t_{34}/(T_s/2)$ is the duty-cycle loss caused by the leakage inductor.

D. Achieving ZCS for the Lagging Leg

From (15), it can be seen that t_{12} is independent of load current and is inversely proportional to D_{eff}; if the condition (16) is satisfied, the lagging leg can achieve ZCS over the entire line and load range.

E. Voltage Stress of the Lagging Leg

During mode 3, $i_p = 0$, $v_B = -V_{cbp}$, and the lagging leg voltage is

$$V_{Q2} = V_{\text{in}} + V_{cbp} \tag{17}$$

$$V_{Q4} = -V_{cbp}. \tag{18}$$

From the above two equations, it is shown that the maximum voltage of the lagging leg is $V_{\text{in}} + V_{cbp}$ and the negative voltage $-V_{cbp}$ may be applied to the lagging leg. Therefore, series diodes are needed to prevent reverse breakdown.

F. Blocking Capacitor

The value of the blocking capacitor C_b is based on two factors: 1) in order to increase $D_{\text{eff max}}$, C_b should be minimized according to (15) and (16) and 2) in order to reduce the voltage stress of the lagging leg and the series diodes, C_b should be selected as large as possible. Therefore, there is a tradeoff in se-

lecting the C_b value. In general, C_b is designed to keep the peak voltage of C_b around 10% of $V_{\rm in}$, i.e., $V_{cbp} \approx 0.1V_{\rm in}$.

V. Simplified Design Procedure and Example

This section illustrates a simplified design procedure and example. The design of this converter involves complex interactions between circuit parameters and operation condition, therefore, we should make some assumptions and approximations.

1) Input specifications:

input voltage $V_{\rm in} = 537$ VDC $\pm$ 20%;
output voltage $V_o = 54$ Vdc;
output current $I_o = 100$ A;
switching frequency $f_s = 25$ kHz;
switching period $T_s = 40$ μs;
leakage inductor measured at the switching frequency $L_{lk} = 5$ μH.

2) Let $D_{\rm eff\,max} = 0.7$ at the lowest input voltage, then the turns ratio of the transformer K is determined by the following equation:

$$K = \frac{V_{\rm in\,min}}{(V_o + V_D)/D_{\rm eff\,max}} = 5.42 \tag{19}$$

where V_D is the voltage drop in the secondary rectifier diode; $V_D = 1.5$ V. The number of turns of the secondary and primary windings are selected at 4 and 22, respectively, thus, $K = 5.5$, and $D_{\rm eff\,max} = 0.71$.

3) In order to have $V_{cbp} \approx 0.1V_{\rm in}$, according to (14),

$$\begin{aligned} C_b &= \frac{I_o/K}{2 \times 0.1V_{\rm in}} \bullet D_{\rm eff\,max} \bullet \frac{T_s}{2} \\ &= \frac{100/5.5}{2 \times 0.1 \times 537} \bullet 0.71 \bullet \frac{40 \times 10^{-6}}{2} \\ &= 2.4\ \mu\text{F}. \end{aligned} \tag{20}$$

We choose $C_b = 2.2\ \mu F$ (930C2W2P2K from CDE Co.), so $V_{cbp} = 58.7$ V.

4) Once K and C_b are determined, $D_{\rm eff}$, $D_{\rm reset}$, and $D_{\rm loss}$ can be calculated from

$$D_{\rm eff} = \frac{K(V_o + V_D)}{V_{\rm in}} \tag{21}$$

$$D_{\rm reset} = \frac{t_{12}}{T_s/2} = \frac{8L_{lk}C_b}{D_{\rm eff}T_s^2} = \frac{8V_{\rm in}L_{lk}C_b}{K(V_o + V_D)T_s^2} \tag{22}$$

$$\begin{aligned} D_{\rm loss} &= \frac{t_{34}}{T_s/2} \\ &= \frac{2L_{lk}I_o}{KT_s(V_{\rm in} + V_{cbp})} \\ &= \frac{2L_{lk}I_o}{KT_s\left(V_{\rm in} + \dfrac{I_o}{2C_b} \bullet \dfrac{V_o + V_D}{V_{\rm in}} \bullet \dfrac{T_s}{2}\right)}. \end{aligned} \tag{23}$$

To meet the voltage and current requirements, IGBT Module (VII50-12Q3) is chosen. The current tail time is $T_{\rm tail} = 0.35$ μs, so $t_{\rm ZCS} = T_{\rm tail} = 0.35$ μs, then $D_{\rm ZCS} = 0.0175$.

We can define $D_{\rm sum}$ as follows:

$$D_{\rm sum} = D_{\rm eff} + D_{\rm reset} + D_{\rm loss} + D_{\rm ZCS}. \tag{24}$$

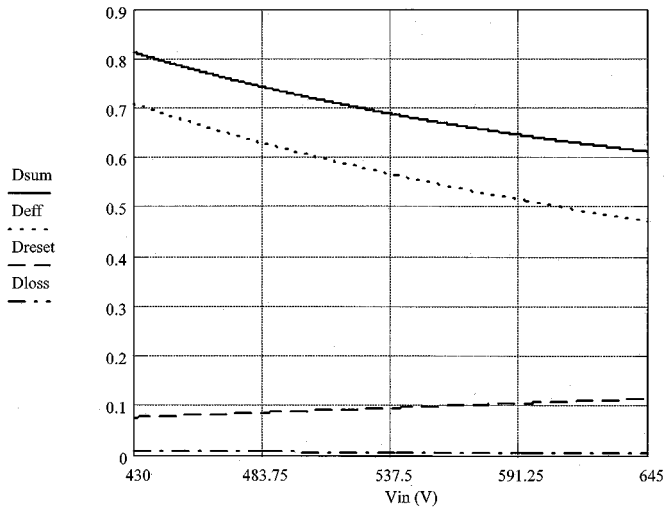

Fig. 7. $D_{\rm sum}$, $D_{\rm eff}$, $D_{\rm reset}$, and $D_{\rm loss}$ as functions of the input voltage $V_{\rm in}$.

$D_{\rm sum}$, $D_{\rm eff}$, $D_{\rm reset}$, and $D_{\rm loss}$ are dependent on the input voltage $V_{\rm in}$ and are shown in Fig. 7. $D_{\rm eff}$ and $D_{\rm sum}$ achieve their maximum values at minimum input voltage, i.e., $D_{\rm eff\,max} = 0.71$ and $D_{\rm sum\,max} = 0.82 < 1$, and condition (16) is satisfied, so the selected K and C_b values are reasonable.

5) Since condition (16) is satisfied, the lagging leg can achieve ZCS over the entire line and load ranges.

6) In order to achieve soft turn off for the leading leg, snubber capacitors are added in parallel with the switches. Based on the operation analysis in mode 1, t_{01} is the time it takes for the snubber capacitor voltage to rise from zero to $V_{\rm in}$. In order to reduce the turn-off loss, t_{01} is selected to be $(2 \sim 3)T_{tail}$ at full load. According to (4),

$$C_1 = C_3 = C_r = \frac{\dfrac{I_o}{K} \times 3 \times T_{tail}}{2V_{\rm in}} = 17.8\ \text{nF}. \tag{25}$$

We choose $C_1 = C_3 = C_r = 15$ nF.

In order to ensure zero-voltage turn-on, the voltage of the paralleled capacitor of the on-going turn-on leading switch should decay to zero prior to turn-on of the leading switch. The delay time between the gate drive signals of the switches in the leading leg is selected as $t_d = 2.4$ μs. If the load current is below $I_{o\,\rm min}$, the zero-voltage turn-on condition will be lost for the leading leg according to (4). Therefore, $I_{o\,\rm min}$ can be calculated as

$$\begin{aligned} I_{o\,\rm min} &= \frac{2 \times C_r \times V_{\rm in}}{t_d} \times K \\ &= \frac{2 \times 15 \times 10^{-9} \times 537}{2.4 \times 10^{-6}} \times 5.5 \\ &= 37 \end{aligned} \tag{26}$$

which represents 37% of the full-load current.

VI. Experimental Results

Following the design guidelines outlined above, a 54-V/100-A rectifier was developed. The following parameters

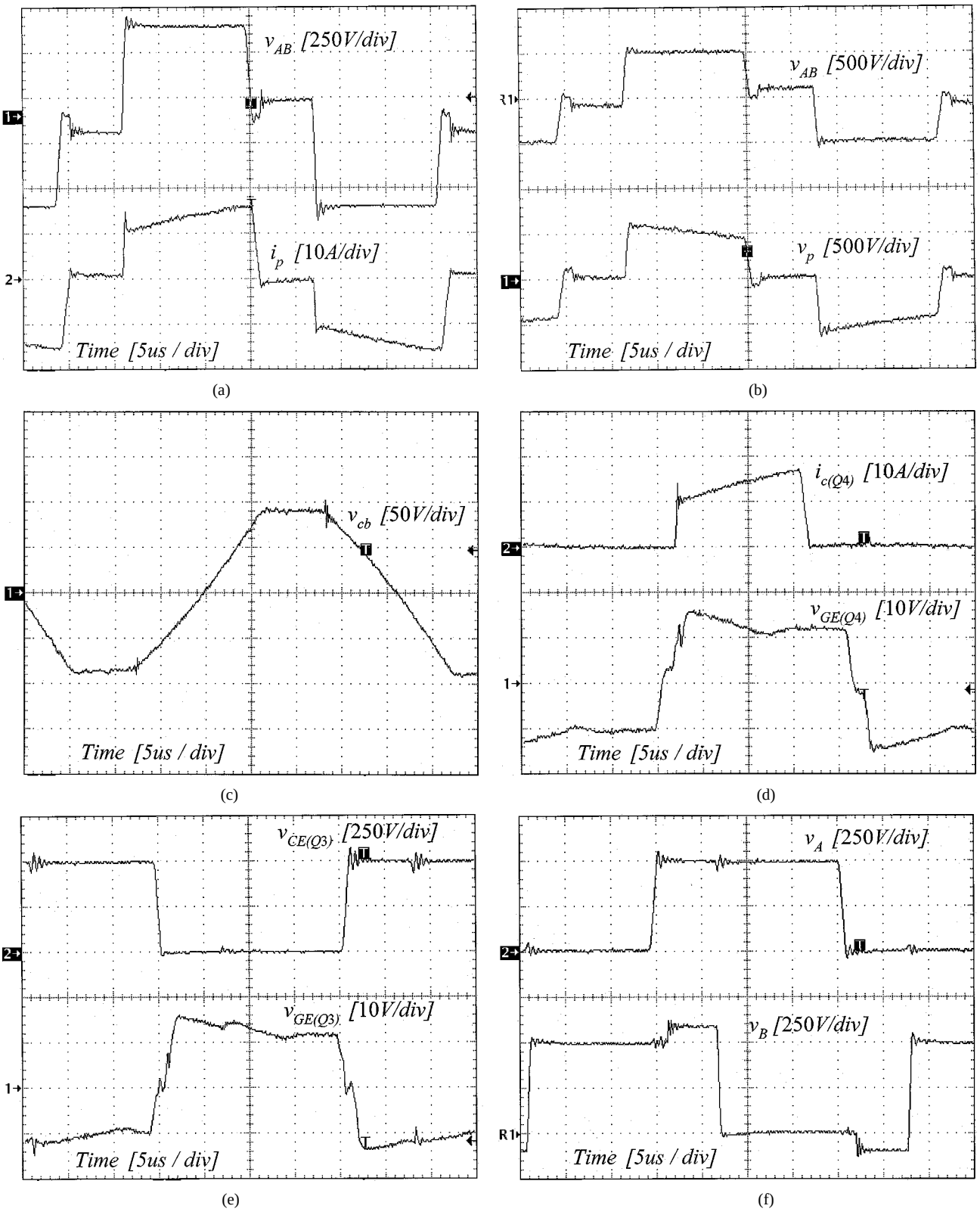

Fig. 8. Experimental results. (a) v_{AB} and i_p. (b) v_{AB} and v_p. (c) v_{cb}. (d) Current of lagging leg and its gate drive signal. (e) Voltage of leading leg and its gate drive signal. (f) v_A and v_B.

are used in the experiment: Input voltage $V_{\text{in}} = 537$ Vdc; output voltage $V_o = 54$ VdC; output current $I_o = 100$ A; turns ratio of the transformer $K = 5.5$; leakage inductor $L_{lk} = 5$ μH; block capacitor $C_b = 2.2$ uF; snubber capacitor $C_1 = C_3 = 15$ nF; output inductor $L_f = 30$ μH; output capacitor $C_f = 10\,000$ μF; power switches IGBT(VII50-12Q3); series diode DSEP2 $\times$ 31-03A; rectifier diode MEK95-06DA; and switching frequency $f_s = 25$ kHz.

Fig. 8 shows the experimental waveforms at full load. Fig. 8(a) shows the waveforms of v_{AB} and i_p, which illustrates

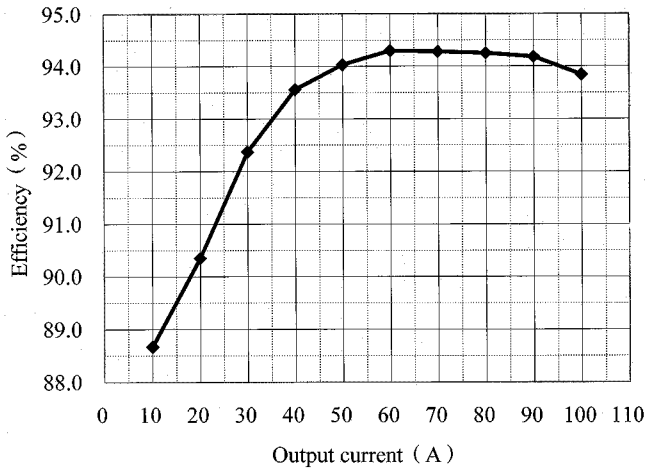

Fig. 9. Conversion efficiency.

that when $v_{AB} = 0$, the blocking capacitor voltage forces i_p to decay to zero to achieve ZCS for the lagging leg. Compared with the PS ZVS PWM FB converter, the ZVZCS PWM FB converter has no idle current during zero state. This helps increase the efficiency. Fig. 8(b) shows that the waveforms of v_{AB} and the primary voltage of transformer v_p. v_p is not square wave due to the existence of the blocking capacitor. However, the average value of v_p is the same as that of the PS ZVS PWM FB converter. Fig. 8(c) shows the waveform of blocking capacitor voltage. Fig. 8(d) shows the waveforms of lagging leg's current and its gate drive signal, which illustrates that the lagging leg operates with ZCS, and Fig. 8(e) shows the waveforms of the leading leg's voltage and its gate drive signal, which illustrates that the leading leg operates with ZVS. Fig. 8(f) shows the waveforms of the voltage of leading leg and lagging leg; the peak–peak voltage stress across the lagging leg is $V_{\text{in}} + V_{cbp}$. There is a negative voltage applied on the lagging switches, the series diodes D_2 and D_4 block the reverse breakdown of the lagging switches.

Fig. 9 gives the overall conversion efficiency at 380-Vac input voltage (which is rectified and filtered to the dc voltage $V_{\text{in}} = 537$ Vdc). The efficiency is 93.8% at full load. If the PS ZVS PWM FB converter is employed, the efficiency is 92% at full load. The higher efficiency is achieved because there is no idle current and there is no conduction loss in the power switches and transformer during zero state in the PS ZVZCS PWM FB converter.

VII. Conclusion

This paper has proposed a novel ZVZCS PWM FB converter which employs two additional diodes in series with the lagging leg. The leading leg can achieve ZVS over a wide load range, and the lagging leg can achieve ZCS over the entire line and load ranges. The principle of operation, steady-state analysis, and simplified design procedures were presented, and the experimental results were also included.

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