HT1335P

Digital Green-Mode Quasi-Resonant Primary-Side PWM Power Switch

DIGITAL PWM IC

1.0 General Description

The HT1335P is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device includes an internal power MOSFET and operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design and lowers the total bill of material cost. The HT1335P removes the need for secondary feedback circuit while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response for both one-time and repetitive load transients. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range. Hunch's innovative proprietary technology ensures that power supplies built with the HT1335P can achieve both highest average active efficiency and have fast dynamic load response in a compact form factor in typical applications.

Features

- ◆ Tight constant-voltage and constant-current regulation across line and load range
- ◆ Primary-side feedback eliminates opto-isolators and simplifies design
- ◆ Proprietary optimized 90 kHz maximum PWM switching frequency with quasi-resonant operation achieves best size, efficiency and common mode noise
- ◆ Adaptive Multi-mode PWM/PFM control improves efficiency
- ◆ No external loop compensation components required
- ◆ User-configurable 5-level cable drop
- ◆ Complies with CoC Version 5 Tier 2 and DOE level VI energy-efficiency specifications with ample margin
- ◆ Built-in single-point fault protection features: output short-circuit protection, output over-voltage protection, over-current protection ， current-sense-resistor fault protection and over temperature protection
- ◆ No audible noise over entire operating range

Applications

- ● Compact AC/DC adapter/chargers for media tablets and smart phones
- ● AC/DC adapters for consumer electronics

2.0 Products Information

2.1 Pin configuration

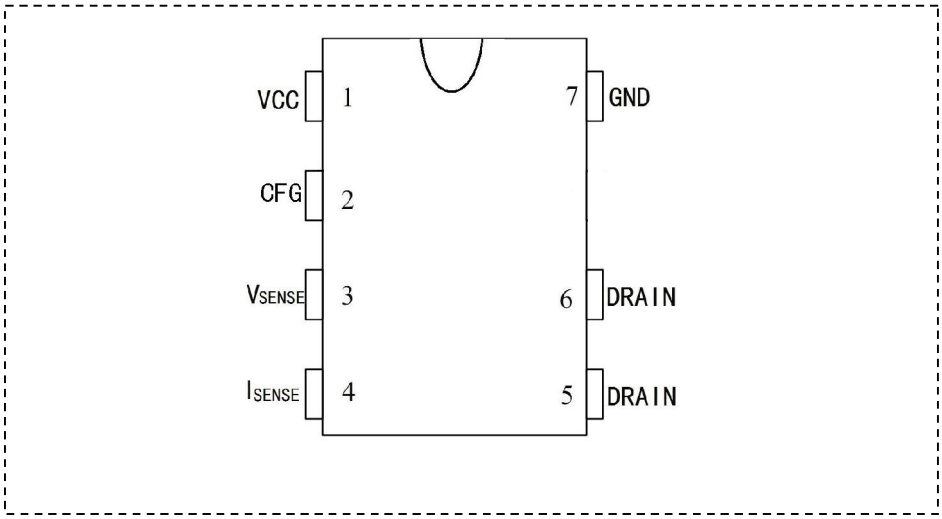


Figure2.1: HT1335P Series（ DIP7 Package ）

Pin#	Name	Type	Description
1	VCC	Power Input	Power supply for control logic.
2	CFG	Analog Input	Shared Multi-function pin. Used for external cable drop compensation (CDC) configuration and supplemental over-voltage protection (OVP).
3	Vsense	Analog Input	Auxiliary voltage sense (used for primary regulation)
4	Isense	Analog Input	Primary current sense. Used for cycle-by-cycle peak current control and limit.
5、6	Drain	MOSFET Drain	Drain of internal Power MOSFET .The Drain pin is connected to the primary lead of the transformer
7	GND	Ground	Ground.

2.3 Series description

Part Number	Description
HT1335P	DIP7, provides 3 levels of CDC configurations

2.3 Block diagram

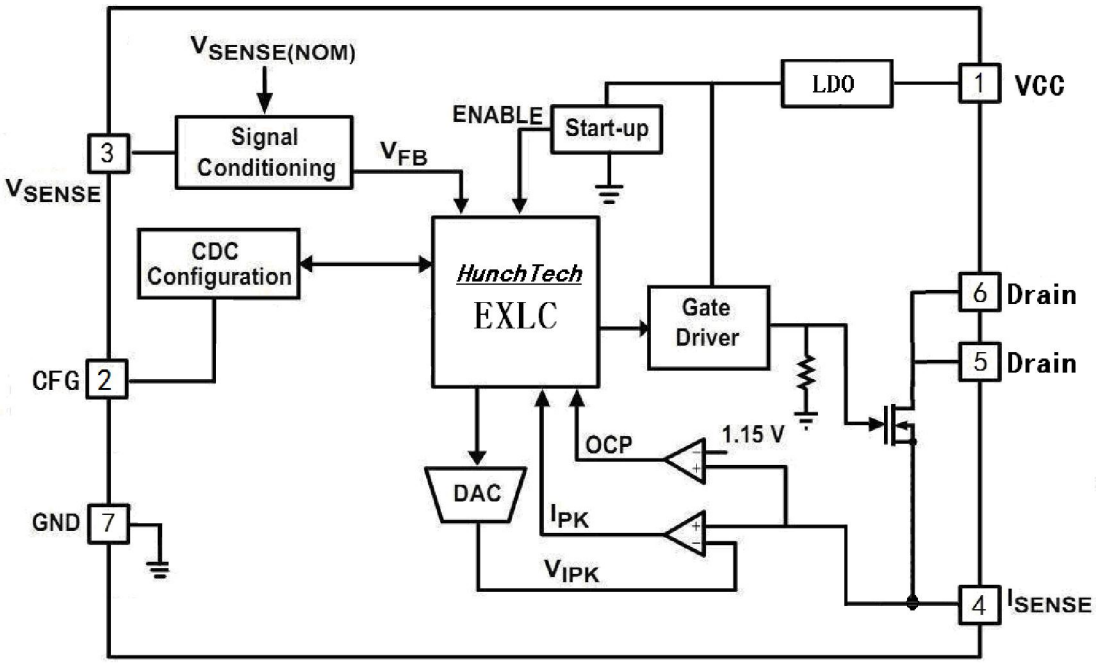


Figure2.1 HT1335P Functional Block Diagram

3.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Drain Voltage（off state）	V_{DRAIN}	-0.3 to Bvdss	V
DC supply voltage range (pin 1, I_{DD} = 20mA max)	V_{CC}	-0.3 to 25.0	V
Continuous DC supply current at VCC pin (VCC = 15 V)	I_{DD}	20	mA
V_{SENSE} input (Pin 2, I_{VENSE} ≤ 10mA)		-0.7 to 4.0	V
I_{SENSE} input (Pin 3)		-0.3 to 4.0	V
CFG(Pin 8, I_{CFG} ≤ 20mA)		-0.8 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	℃
Operating junction temperature	T_{JOPT}	-40 to 150	℃
Storage temperature	T_{STG}	–65 to 150	℃
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	℃
Thermal resistance junction-to-ambient	θ_{JA}	160	℃/W
ESD rating per JEDEC JESD22-A114		3,000	V
Latch-up test per JEDEC 78		±100	mA

4.0 Typical Application

The HT1335P contains a controller for a flyback circuit.

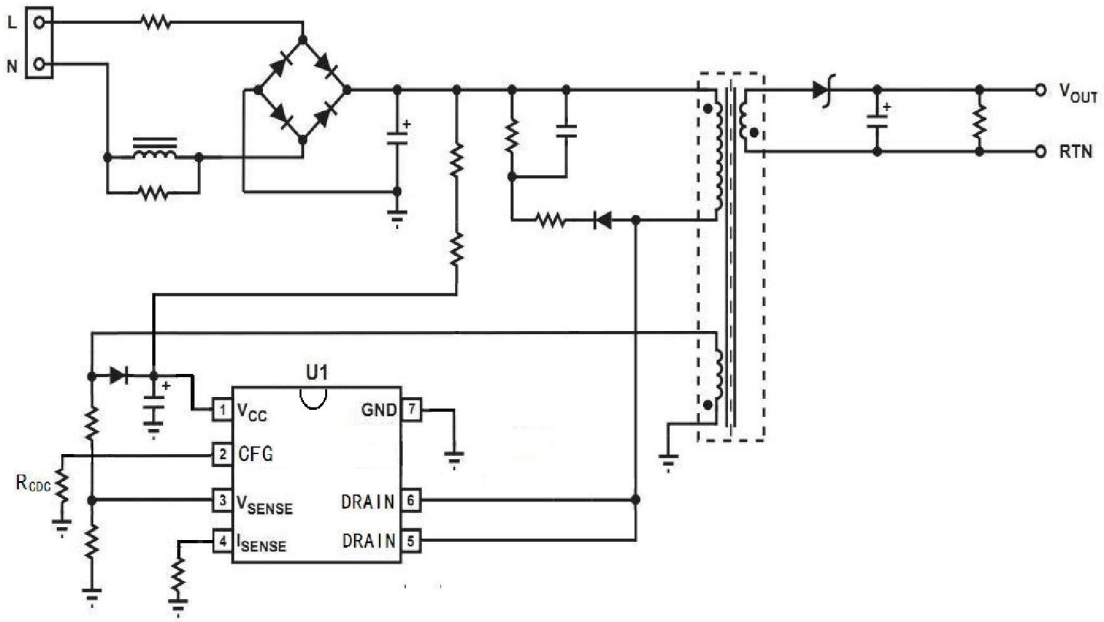


Figure4.1 HT1335P Typical Application

5.0 Electrical Characteristics

(TA = 25℃, VCC=12V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCC SECTION (Pin1)						
$VCC_{(MAX)}$	Maximum operating voltage (Note 2)	-	-	-	20	V
$VCC_{(ST)}$	Start-up threshold	VCC rising	13.0	14.0	15.0	V
$VCC_{(UVL)}$	Under-voltage lockout threshold	VCC falling	6.2	6.5	6.8	V
$VCC_{(RLS)}$	Latch release threshold	VCC falling	4.2	4.5	4.8	V
$I_{IN(ST)}$	Start-up current	VCC = 12V	-	7.8	-	uA
I_{CCQ}	Quiescent current	C_L=330pF,V_{SENSE}=1.5V	-	3.5	-	mA
CFG Section (Pin2)						
$V_{SD-TH(R)}$	OVP shutdown threshold (rising edge)	-	0.96	1.015	1.07	V
V_{SENSE} SECTION (Pin 3)						
I_{BVS}	Input leakage current	V_{SENSE} = 2 V	-	-	1	uA
$V_{SENSE(NOM)}$	Nominal voltage threshold	TA=25°C, negative edge	1.521	1.536	1.551	V
$V_{SENSE(MAX)}$	V_{SENSE}-based output OVP threshold	TA=25°C, negative edge	-	1.930	-	V
I_{SENSE} SECTION (Pin 4)						
V_{OCP}	Over-current threshold	-	1.11	1.15	1.19	V
$V_{IPK(HIGH)}$	ISENSE regulation upper limit (Note 2)	-	-	1.0	-	V
$V_{IPK(LOW)}$	ISENSE regulation lower limit (Note 2)	-	-	0.23	-	V
MOSFET SECTION						
BVdss	Mosfet Drain-Source Breakdown Voltage		650			V
Rdson	Static drain to source on resistance		--	0.95	1.2	Ω
Switching CHARACTERISTICS						
f_{SW}	Switching frequency	>50% load		90		kHz

Notes:

Note 1: The V_{SENSE}-based output OVP threshold depends on the CDC setup, see Section 7.10 for more details.

Note 2: These parameters are not 100% tested, guaranteed by design and characterization.

Note 3: Operating frequency varies based on the load conditions.

6. Typical Performance Characteristics

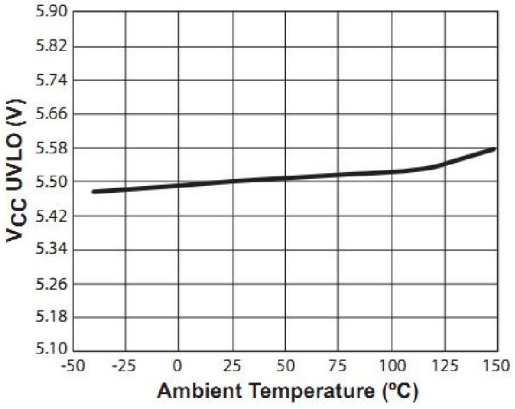


Figure 6.1 VCC UVLO vs. Temperature

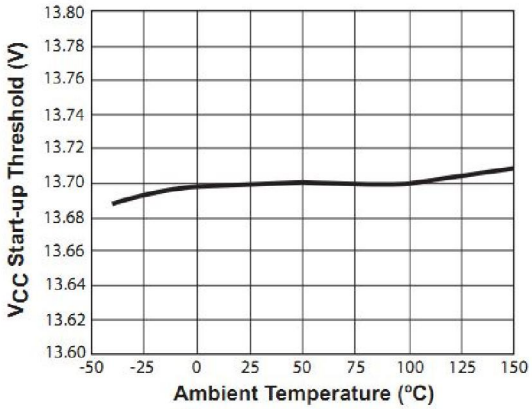


Figure 6.2 Start-Up Threshold vs. Temperature

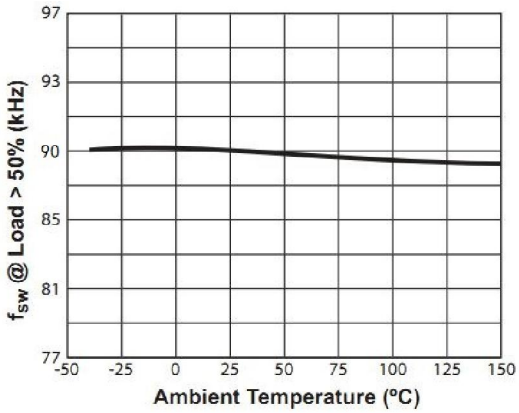


Figure 6.3 Switching Frequency vs. Temperature

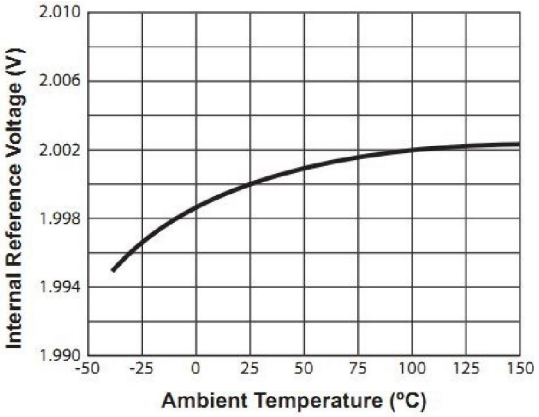


Figure 6.4 Internal Reference vs. Temperature

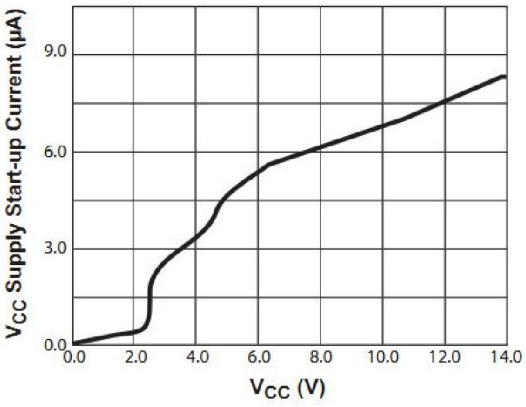


Figure 6.5 VCC vs. VCC Supply Start-up Current

Notes:

Note1: Operating frequency varies based on the load conditions, see Section 7.6 for more details.

7. Theory of Operation

The HT1335P is a digital power switch which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Hunch's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 2.1, the HT1335P operates in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The I_{SENSE} is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the I_{SENSE} to compare with, and it varies in the range of 0.23 V (typical) to 1.00 V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The HT1335P uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for any secondary-side sense and control circuits.
The HT1335P uses adaptive Multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency,EMI,and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and I_{SENSE} fault detection.

Hunch's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design.This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

7.1 Pin Detail

Pin1– VCC

Power supply for the controller during normal operation. The controller will start up when VCC reaches 14.0 V (typical) and will shut down when the VCC voltage drops below 5.5 V (typical). A decoupling capacitor of 0.1 μF or so should be connected between the VCC pin and GND.

Pin2 – CFG

MULTI-function pin. Used to configure external cable drop compensation (CDC) at the beginning of start-up and provide over-voltage protection during normal operation by sensing output voltage via auxiliary winding.

Pin3– V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation..

Pin4– I_{SENSE}

Primary current sense. Used for cycle-by-cycle peak current control and limit..

Pin5、6– DRAIN

Drain of internal power MOSFET.

Pin7– GND

Ground.

7.2 Soft-start

When the VCC bypass capacitor is charged to a voltage higher than the start-up threshold $VCC_{(ST)}$, the ENABLE signal becomes active and the HT1335P begins to perform initial OTP check, followed by CDC configuration. Afterwards, the HT1335P commences soft-start function. During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses will be small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator.If at any time the VCC voltage drops below under-voltage lockout (UVLO) threshold $VCC_{(UVL)}$ then the HT1335P goes to shutdown. At this time ENABLE signal becomes low and the VCC capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

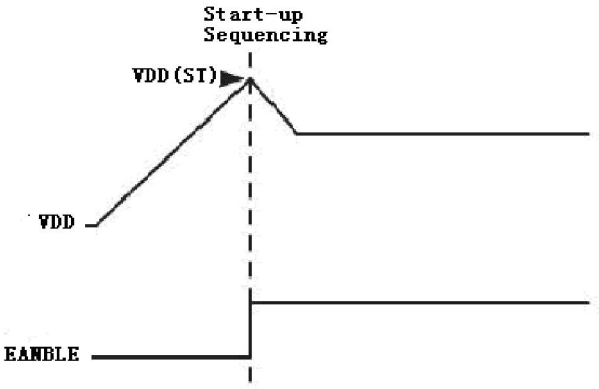


Figure 7.1: Start-up Sequencing Diagram

7.3 Understanding Primary Feedback

Figure 7.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M.The rectifying diode D1 is reverse biased and the load current I_O is supplied by secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

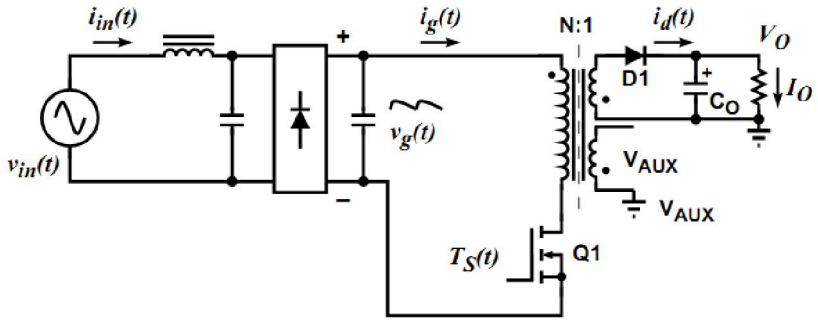


Figure 7.2: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor

C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (7.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (7.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (7.3)$$

When Q1 turns off at t_o, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_o, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (7.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave, and reflects the output voltage as shown in Figure 7.3.

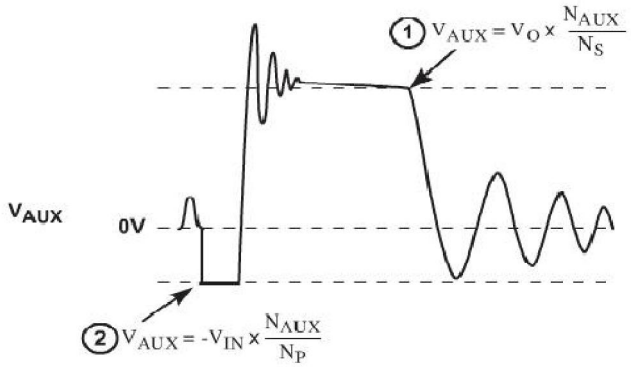


Figure 7.3: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (7.5)$$

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV.

Furthermore, if the voltage can be read when the secondary current is small, ΔV will also be small. With the HT1335P, ΔV can be ignored.

The real-time waveform analyzer in the HT1335P reads this information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

7.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (T_{ON}) and off time (T_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the HT1335P shuts down.

7.5 Constant Current Operation

The constant current (CC) mode is useful in battery charging applications.During this mode of operation the HT1335P will regulate the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode.
To achieve this regulation the HT1335P senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground.

The HT1335P also provides a product option to disable the CC mode operation. If the power supply enters into the CC mode during normal operation, this product option will shut down the power supply. This feature serves as an over-load protection and can be used in certain adapter applications.

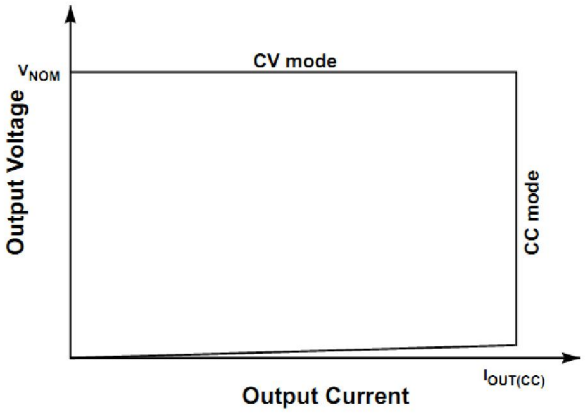


Figure 7.4: Power Envelope

7.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The HT1335P uses a proprietary adaptive Multi-mode PWM /PFM control to dramatically improve the light-load efficiency and thus the overall average efficiency.
During the constant voltage (CV) operation, the HT1335P normally operates in a pulse-width-modulation (PWM) mode during heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time T_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. During the PFM mode, the MOSFET is turned on for a set duration under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the HT1335P Transitions to a second level of PWM mode, namely Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 25KHz in order to avoid audible

noise.

As the load current is further reduced, the HT1335P transitions to a second level of PFM mode, namely Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across varying load conditions.

As the load current reduces to very low or no-load condition, the HT1335P transitions from the DPFM to the third level of PWM mode, namely Deep-Deep PWM mode (DDPWM), where the switching frequency is fixed at around 1.8 kHz. The HT1335P also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on

for every PWM/PFM switching cycle, during all PFM and PWM modes and in both CV and CC operations.This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply.Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. Together these innovative digital control architecture and algorithms enable the HT1335P to achieve highest overall efficiency and lowest EMI, without causing audible noise over entire operating range.

7.7 Variable Frequency Operation Mode

At each of the switching cycles, the falling edge of V_{SENSE} will be checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110 μs. When the transformer reset time reaches 110 μs, the HT1335P shuts off.

7.8 Internal Loop Compensation

The HT1335P incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20 dB of gain margin.

7.9 Voltage Protection Features

The secondary maximum output DC voltage is limited by the HT1335P. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 7.3 the HT1335P shuts down.

Although there is no pin available to directly sense the input voltage, the HT1335P uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of

the DC bulk capacitor voltage. This enables the HT1335P to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in and unplug, and to take appropriate actions. When the AC input voltage drops to below normal operation range and the power supply input is still connected to the AC source, the HT1335P initiates brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the HT1335P continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply. Also, the HT1335P monitors the voltage on the VCC pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold.

When any of these faults are met the IC remains biased to discharge the VCC supply. Once VCC drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed. For the latched OVP version, the controller can only start-up when the fault is removed and input is unplugged to allow VCC to drop 1.0 V below UVLO threshold.

7.10 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built-in to the HT1335P. With the I_{SENSE} pin the HT1335P is able to monitor the peak primary current.This allows for cycle-by-cycle peak current control and limit.When the peak primary current multiplied by the I_{SENSE} resistor is greater than 1.15 V,over-current is detected and the IC will immediately turn off the gate driver until the next cycle.The output driver will send out a switching pulse in the next cycle, and the switching pulse will continue if the OCP threshold is not reached; or, the switching pulse will turn off again if the OCP threshold is reached.If the OCP occurs for several consecutive switching cycles, the HT1335P shuts down.

If the I_{SENSE} resistor is shorted there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault after start-up and shut down immediately.The VCC will be discharged since the IC remains biased. Once VCC drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to startup, but does not fully start-up until the fault condition is removed.

7.11 CDC Configuration

The HT1335P incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally.This configuration is only performed once.It is completed after the initial OTP check but before the soft-start commences. During the CDC configuration, the internal digital control block senses the external resistance value between the CFG pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 4.1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC}, from the CFG pin to ground. The HT1335PC provides five levels of CDC configurations: 0, 75 mV, 150 mV, 300 mV, and 450 mV. Table 7.1 below shows the resistance range for each of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 7.1 refers to the voltage increment at PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the nominal output voltage of 5 V. For different output voltage, the actual voltage increment needs to be scaled accordingly. To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply by the maximum output current.

For each of the CDC levels, the internal V_{SENSE}-based OVP thresholds are different. Table 7.1 also lists the typical OVP thresholds for each CDC level.

Table7.1 Recommended resistance range and corresponding CDC levels for 5V output

CDC Level	1	2	3
R_{CDC} Range（kΩ）	0	8.5 – 10.5	NC
Cable Comp（mV）	0	75	150
V_{SENSE}-based OVP Threshold	1.838	1.861	1.884

7.12 External CFG-Based OVP

In the HT1335P, the CFG pin can also be used to provide the external over-voltage protection (OVP) besides fulfilling the CDC configuration. This external CFG-based OVP serves as a supplemental or extra protection in addition to the V_{SENSE}-based OVP. The circuit implementation can be found in Figure 7.5, where two resistors R1 and R2 form a voltage divider to sense output voltage via auxiliary winding, with the tapping point connected to the CFG pin. During the CDC configuration the HT1335P does not send out any drive signal at OUTPUT pin, and the switch Q1 remains in off-state. The resistors R1 and R2 are essentially connected in parallel since the bias winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 sets the CDC level. Meanwhile, during normal operation, the CFG pin reflects output voltage in real-time, in the similar fashion as the V_{SENSE} does at point 1 in Figure 7.3. The ratio of R1 to R2 sets the external OVP threshold.

The resistance values for the resistor divider, R1 and R2, can be derived as follows. First, for the given CDC level, the paralleled resistance of R1 and R2 should be within the range listed in Table 7.1:

$$R_{CDC} = \frac{R_1 \times R_2}{R_1 + R_2} \qquad (7.6)$$

Second, during normal operation the voltage divider, R1 and R2, sets the desired OVP threshold:

$$\left(\frac{N_{AUX}}{N_{SEC}}\right) \times V_{OVP} \times \left(\frac{R_2}{R_2 + R_1}\right) \geq V_{SD-TH(R)} \qquad (7.7)$$

where NAUX is the number of turns for the bias winding, N_{SEC} is the number of turns for the secondary winding, V_{OVP} is the desired OVP tripping point, and $V_{SD-TH(R)}$ is the internal comparator threshold (1.015 V typically) for OVP detection. The combination of Equations (9.6) and (9.7) leads to

$$R_1 = \left(\frac{N_{AUX}}{N_{SEC}}\right) \times R_{CDC} \times \left(\frac{V_{OVP}}{V_{SD-TH(R)}}\right)$$

$$R_2 = \left(\frac{R_1}{R_1 - R_{CDC}}\right) \times R_{CDC} \qquad (7.8)$$

It is recommended the R_{CDC} value is taken as the median value of the resistance range as given in Table7.1, and R1 and R2 can then be readily derived from Equation (7.8).

It should be noted when the CFG pin is used to provide external OVP, an additional constraint will be applied to the resistance range given in Table7.1. Since for the OVP configuration in Figure 7.5, a large negative voltage may occur to the auxiliary winding (V_X in Figure 7.5) during the switch on-time, which can cause a negative current flowing out of the CFG pin. Care needs to be taken to ensure R1 and R2 are large enough, so that the resulting negative current is less than the maximum allowed current, specified in Section 3.0.

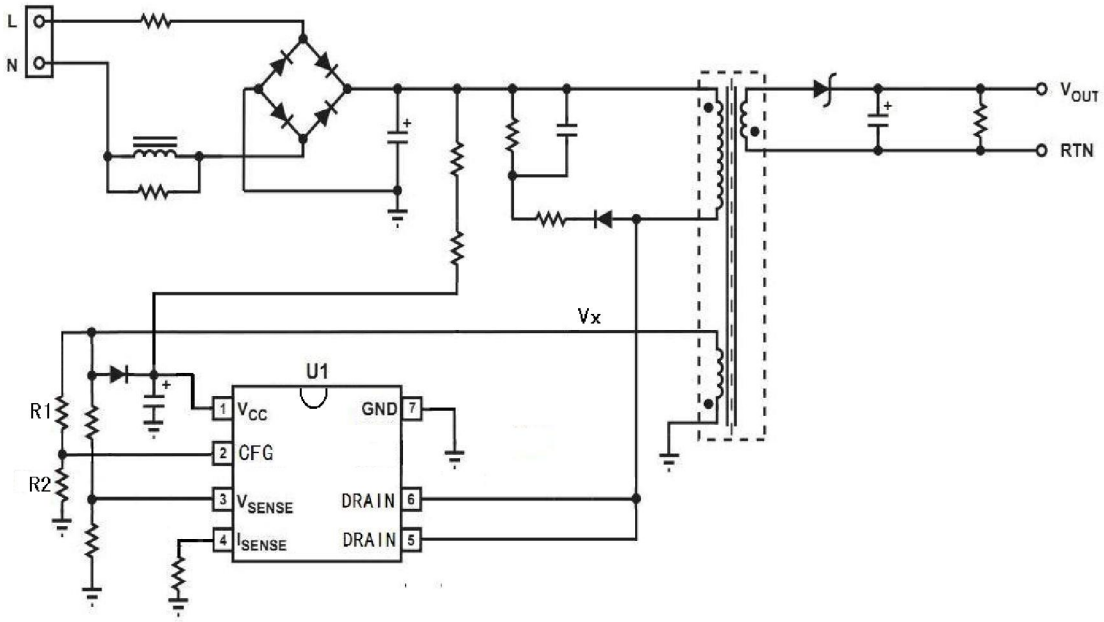
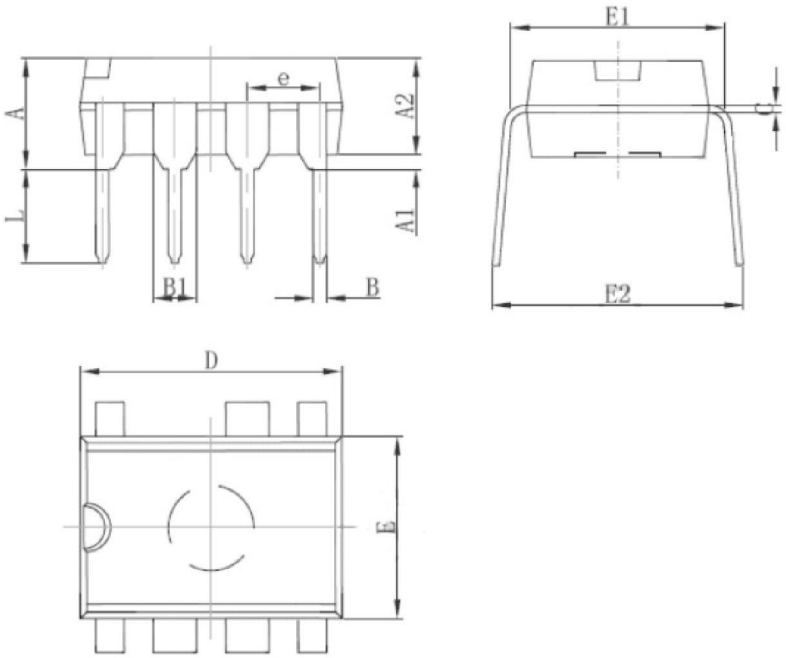


Figure 7.5: Typical Application Circuit with CDC,OVP

8. Package Information

DIP7 PACKAGE



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381	--	0.015	--
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524(BSC)		0.06(BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540(BSC)		0.1(BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430