2500 W full-bridge totem-pole power factor correction using CoolGaN™

Order code: EVAL_2500W_PFC_GAN_A

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About this document

Scope and purpose

This is an application note dedicated to Infineon's 2500 W totem-pole full-bridge Power Factor Correction (PFC) demo board comprising CoolGaN™ e-mode HEMTs, CoolMOS™ SJ MOSFETs and an ICE3 PFC controller in combination with 1EDi HV MOSFET drivers.

Intended audience

This application note is intended for Infineon customers and partners using Infineon's CoolGaN™ technology.

Table of contents

1 PFC demonstration platform

This demo board shows a high-efficiency PFC stage, which exploits the advantages of Infineon's CoolGaN™ technology to boost the system efficiency above 99 percent for efficiency-critical applications, such as server or telecom rectifiers.

One unique advantage within the enhancement-mode (e-mode) gallium nitride (GaN) semiconductors – with GaN being a wide-bandgap (WBG) material – is the complete absence of any reverse recovery charge. Therefore this technology enables new topologies in power classes that cannot be addressed by today's HV superjunction (SJ) power semiconductors. Based on these features, the totem-pole PFC topology is the perfect match to exploit the benefits of Infineon's CoolGaN™ technology.

Our demo board shows reliable operation up to 2500 W with benchmark efficiency of 99.2 percent. To achieve this, only two discrete 70 mΩ CoolGaN™ switches in combination with two discrete 33 mΩ 650 V CoolMOS™ C7 Gold switches are required. All power components are Surface Mount Devices (SMDs) enabling a faster and cheaper assembly process. The control is realized with Infineon's standard ICE3 Continuous Conduction Mode (CCM) control IC. The PWM switching frequency is set to 65 kHz.

Figure 1 The 2500 W totem-pole PFC demo board enabled by CoolGaN™ technology

1.1 Totem-pole full-bridge PFC

The totem-pole PFC is an AC-to-DC converter concept that replaces all diodes along the current path with semiconductor switches. In this way it is possible to increase the overall efficiency of the application as the voltage drop of the diode is being mitigated by the resistive behavior of the power semiconductor switches and the lower number of conducting devices in an on-state. Figure 2 shows this topology.

This PFC works in CCM, meaning the input current is commutated between transistors Q1 and Q2 depending on the duty cycle. This has the advantage that the input current ripples are significantly reduced compared to Discontinuous Current Mode (DCM) operation, so a better power factor and a better Total Harmonic Distortion (THD) factor can be achieved by CCM operation. This mode of operation is also called "hard-switching", as the commutation is performed with a positive load current across the transistors. This raises the requirement for rugged transistors suitable for commutation that do not suffer from reverse recovery issues. GaN High Electron Mobility Transistors (HEMTs) with zero recovery charge are therefore the perfect choice for this application. The absence of Q_{rr} also reduces the turn-on losses; the cross-over of voltage and current is minimized because the device can be turned on faster.

In contrast, soft-switching applications (such as LLC and ZVS) perform the commutation at zero current – or zero voltage – conditions. See Infineon product brochure "CoolMOS™ SJ MOSFETs benefits in both hard and soft switching SMPS topologies"[1] for a comparison of the techniques.

The phase rectification stage consisting of Q3 and Q4 is realized by two SJ 650 V CoolMOS™ C7 Gold devices offering a low $R_{DS(ON)}$ (33 mΩ) in a TOLL package. This latest generation of CoolMOS™ boosts the efficiency and, as these devices are switched at the zero-voltage crossing, power semiconductor devices with non-zero Q_{rr} values can be accepted (ZVS). For details about this device please refer to the IPT65R033G7 datasheet [2].

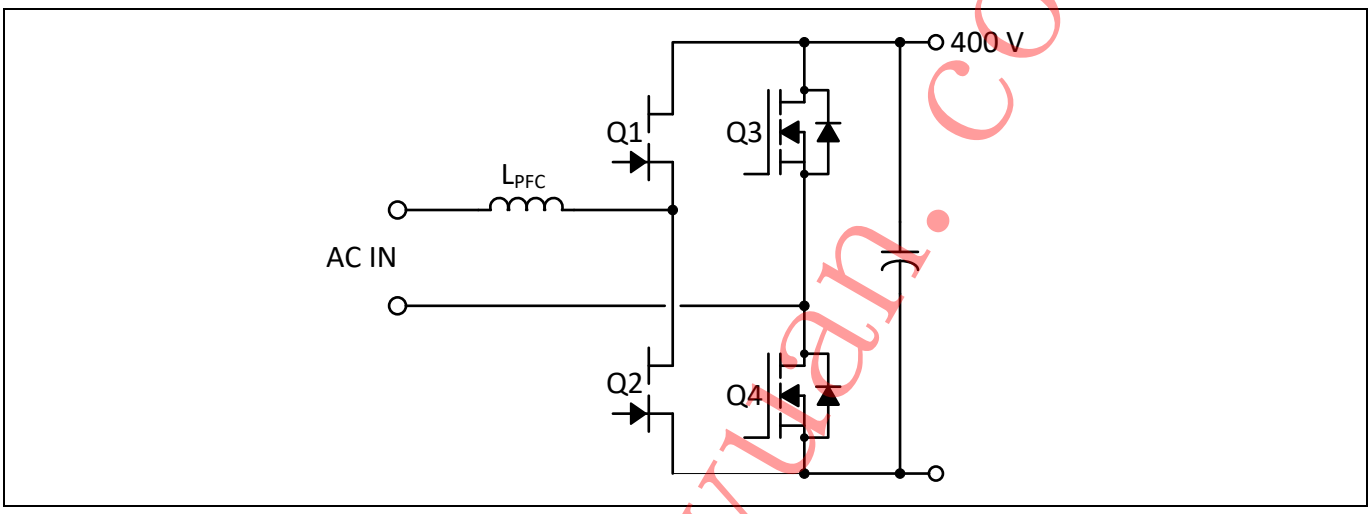

Figure 2 Schematic of full-bridge totem-pole PFC comprising GaN HEMTs and CoolMOS™

1.2 Schematic and implementation details

This section gives some brief practical advice regarding implementation.

1.2.1 PWM switching frequency

The purpose of the demo board is to show the efficiency boost enabled by using the totem-pole PFC with the latest-generation WBG power devices offering ultra-low switching losses. Nevertheless, the switching losses cannot be neglected in applications operating in CCM, and they scale linearly with the frequency. Thus, the PWM switching frequency of this application was set to 65 kHz – a standard frequency used in other hard-switching PFC topologies (like the conventional boost-PFC) – as a good balance between inductor size, permissible ripple current and target efficiency.

1.2.2 PFC inductor design

The target of the PFC design was to fulfill the ripple current requirements at the nominal switching frequency and to reduce parasitic capacitances. This demonstration comprises three stacked distributed airgap cores from Magnetics, Inc. This approach allows a high inductance value over a wide frequency range without overlaying windings in order to minimize the stray capacitances. Figure 5 shows a frequency sweep measurement for the main PFC inductor. The blue curve in this plot is the measured impedance in Ohms, while the yellow curve shows the phase in degrees against the frequency (on the x-axis). The result shows that the coil exhibits inductive behavior up to 700 kHz and a first resonance frequency above 1 MHz. Assuming an ideal inductance at the cursor's position, the initial inductance value L_0 can be calculated based on the following equation:

$$Z = \omega L_0 = 2\pi f L_0 \rightarrow L_0 = \frac{Z}{2\pi f}$$

Using the cursor information as displayed in Figure 3, this yields:

$$L_0 = \frac{2.182\ \Omega}{2\pi \cdot 523.86\ Hz} = \sim 663\ uH$$

Now the parasitic capacitor can be determined:

$$f_{res} = \frac{1}{2\pi\sqrt{L_0 \cdot C_{par}}} \rightarrow C_{par} = \frac{1}{4\pi^2 L_0 {f_{res}}^2}$$

Assuming a resonant frequency of 1 MHz would yield:

$$C_{par} = \frac{1}{4\pi^2 \cdot 663\ \text{uH} \cdot 1\ MHz^2} = \sim 38\ pF$$

The goal of this optimization was to allow fast switching and to reduce peak currents within the application. This result proves that the optimization was successful since the parasitic capacitor value is very small.

Figure 3 **Frequency sweep of PFC coil showing inductive behavior over a wide range and the first resonance above 1 MHz**

1.3 Gate driving

The PFC uses conventional gate drivers for the driving of the e-mode GaN power switches as well as the CoolMOS™ MOSFETs for the phase rectification.

To make full use of the Kelvin contact offered by the DSO20 power package, isolated gate drivers from Infineon's 1EDi family are used in this demo board. These drivers are available as 2 A and 6 A versions and offer separate source-and-sink paths for the gate currents. To optimize the performance, a 2 A driver is the best choice for the GaN HEMT, whereas a 6 A driver is preferred for the 650 V CoolMOS™ C7 Gold.

Since the GaN transistors are in the high-frequency half-bridge, they must be switched much faster than the CoolMOS™ devices. Due to the internal device structure, an Infineon HV MOSFET driver in combination with an RC network is used to turn the GaN devices on and off in the most optimal way. The RC network acts as a high-pass filter. It offers a low impedance path for fast signals, whereas slow signals experience a significantly higher resistance. Therefore the device is being turned on and off with a high current (several hundreds of milliamps) whereas the steady-state current, which is needed to keep the device in the on-state, is limited to a few milliamps. This means a standard MOSFET driver can be used to drive the GaN devices. The network is shown in Figure 4 and in the attached schematics. A more detailed explaination and dimensioning of the RC network can be found in the Infineon application note "Driving IGO60R070D1 enhancement-mode GaN HEMTs" [3]. One unique advantage of the CoolGaN™ technology is that the gate modules of the GaN HEMTs offer a non-isolated gate that is robust even against high voltage peaks.

Since the deployed 1EDi MOSFET drivers are isolated, a straightforward driving of the high-side transistors can be used. The power DSO package offers Kelvin contacts, which migitate the common source feedback to allow faster switching for this high-frequency half-bridge. For this reason, this demo board also uses the 1EDi isolated standard drivers from Infineon in the low-side configuration.

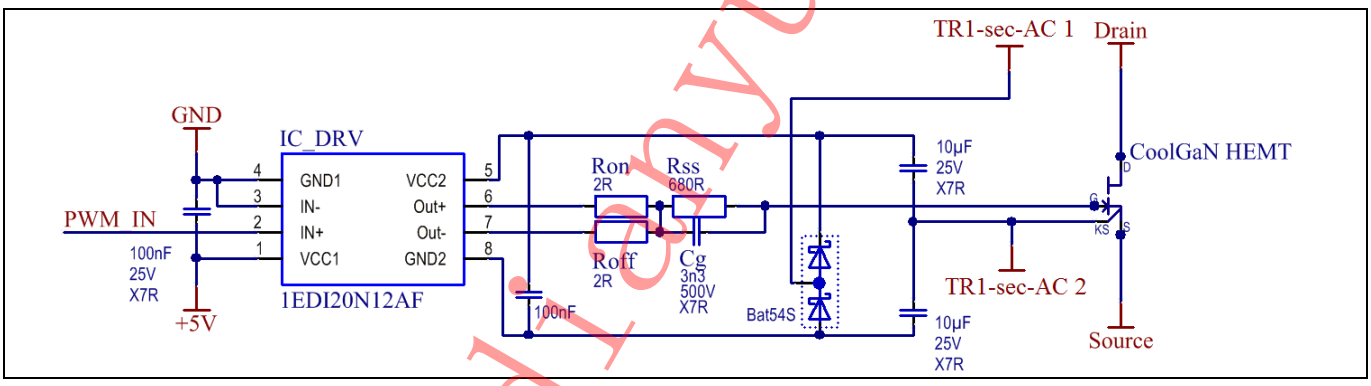

Figure 4 Schematic of generic driver stage for eMode GaN comprising Infineon's isolated 1EDi driver. The input side of the driver is supplied with 5 V and the isolated output is supplied with 12 V.

Figure 4 shows the principle of the driver stage. A rectangular ±6 V signal is provided from the output of a pulse transformer thru TR1-sec- AC 1 and TR1-sec-AC 2. This produces an isolated voltage of 12 V by using the BAT54S rectification diodes and the 10µF 25V capacitors.

The actual driving of the GaN is realized by splitting the +12 V into a positive and a negative contribution by biasing the Kelvin source contact in the middle. Thus, a positive voltage of 6 V is used to control the turn-on, whereas a -6 V voltage is available for safe turn-off. In practical terms, a +3.1 V value will result at the gate of the HEMT during steady-state turn-on, whereas a -5.9 V value is applied during turn-off. The advantage of this solution – compared to the classical RC drive (as shown in [3]) – is that the gate voltage of the GaN device is well defined with respect to the negative driver voltage. Even at small duty-cycle values (with dominant off-times) the voltage on the gate will not move toward 0 V – it will remain at -5.9 V and thus guarantee robustness against the C dv/dt that is induced by gate turn-on.

The input side of the 1EDi driver is supplied with 5 V, which is the same voltage that is used by the CCM PFC control IC. The isolated secondary side of the 1EDi driver is supplied by its own isolated 12 V domain (V_{CC2}, pin 5 and GND2, pin 8 as shown in Figure 4) whereas the reference ground for the GaN transistor is conditioned to TR1-sec-AC 2. This enables a well-defined positive output voltage during turn-on and also a well-defined

negative driver output voltage during the off-phase, as shown in Figure 5. This solution overcomes the limitation of the time constant given by R_{ss}*C_g as a negative level at the gate is always guaranteed by design.

Even if the off-time is longer than five times τ (e.g. at small duty cycles or in pulse-skipping mode), the capacitor will discharge toward the negative voltage level (-5.9 V) and not to 0 V. In this way it is guaranteed that the signal-to-noise ratio on the gate is high and robustness against dv/dt-triggered events is assured.

Figure 5 Typical gate-source voltage characteristic with proposed gate drive at a load current of 16 A. V_2 shows the steady-state turn-on voltage (+3.1 V) and V_1 shows the turn-off voltage (-5.9 V).

The driving of the CoolMOS™ devices is realized via separate turn-on and turn-off gate resistors. As the 33 mΩ 650 V CoolMOS™ C7 Gold devices are being turned on during the zero crossing of the AC input signal, the timing is not critical. Thus, the turn-on gate resistor is chosen to be fairly high (390 Ω) to allow smooth turn-on waveforms. The Kelvin contacts of the TOLL package are not required for the same reason. The turn-off resistor is set to 4R7 (the standard configuration), which allows a fast turn-off. This is an additional safety measure other than the dead-time to avoid cross-conduction under abnormal conditions. The nominal V_{GS} voltage during turn-on is approximately +13 V for the high-side transistor and +15 V for the low-side transistor respectively.

Note: The gate-driving functionality can easily be monitored under LV conditions. For that purpose, supply 35 V DC on the input of the PFC board. For debugging purposes, check the supply of the HV drivers on the primary side (+5 V) and on the secondary side (+12 V) and the respective V_{GS} signals under LV conditions.

1.4 Layout considerations

The mainboard of the demo board is a four-layer PCB with a total thickness of 1.66 mm. The advantage of this approach is that interlayer capacitances can be realized while having sufficient space for signal routing. The complete layer stack is shown in Figure 6.

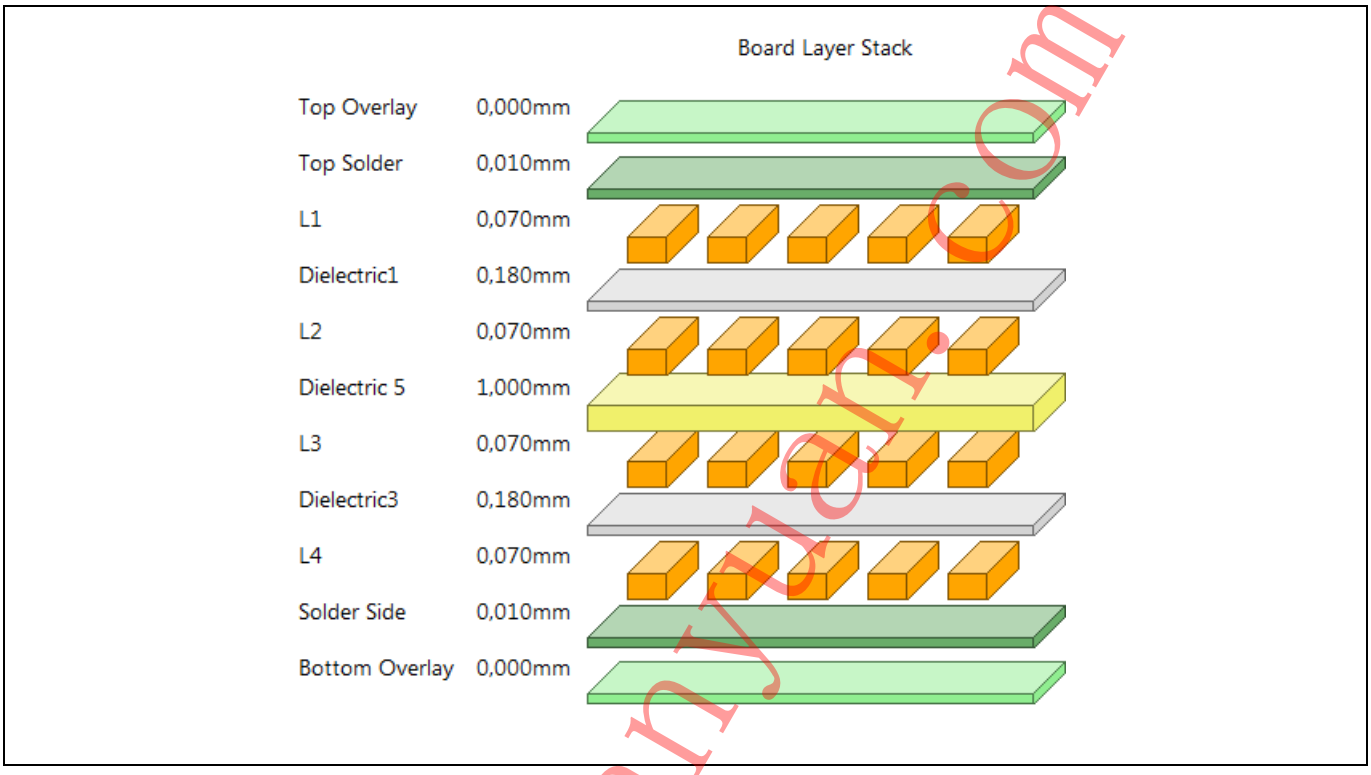

Figure 6 Layer stack of main PCB

One recommended way to minimize the voltage overshoots is to minimize the stray inductances along the current path in the power loop. One possible way to achieve reasonably small overshoots with the DSO packages is to minimize the area defined by the power-loop current. In practice, this means using the mid-layers as a current return path to route the current back as close as possible to the forward path. This concept is shown in Figure 7. The two layers are connected with vias.

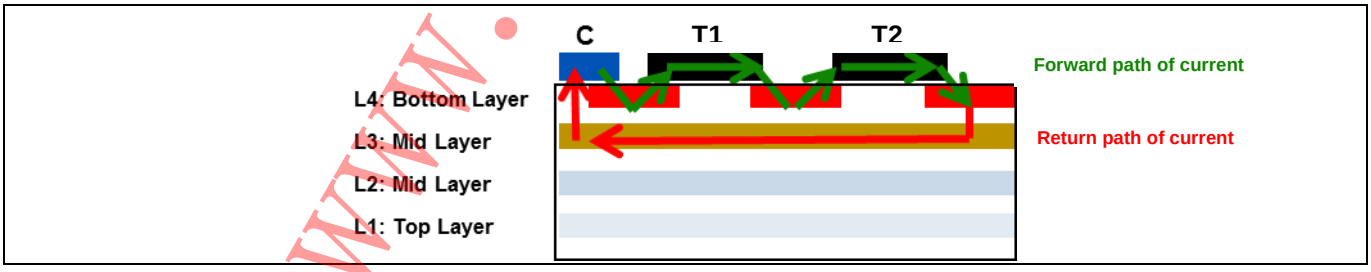

Figure 7 Principle of the power-loop concept with GaN in the DSO package (cross-section, rotated)

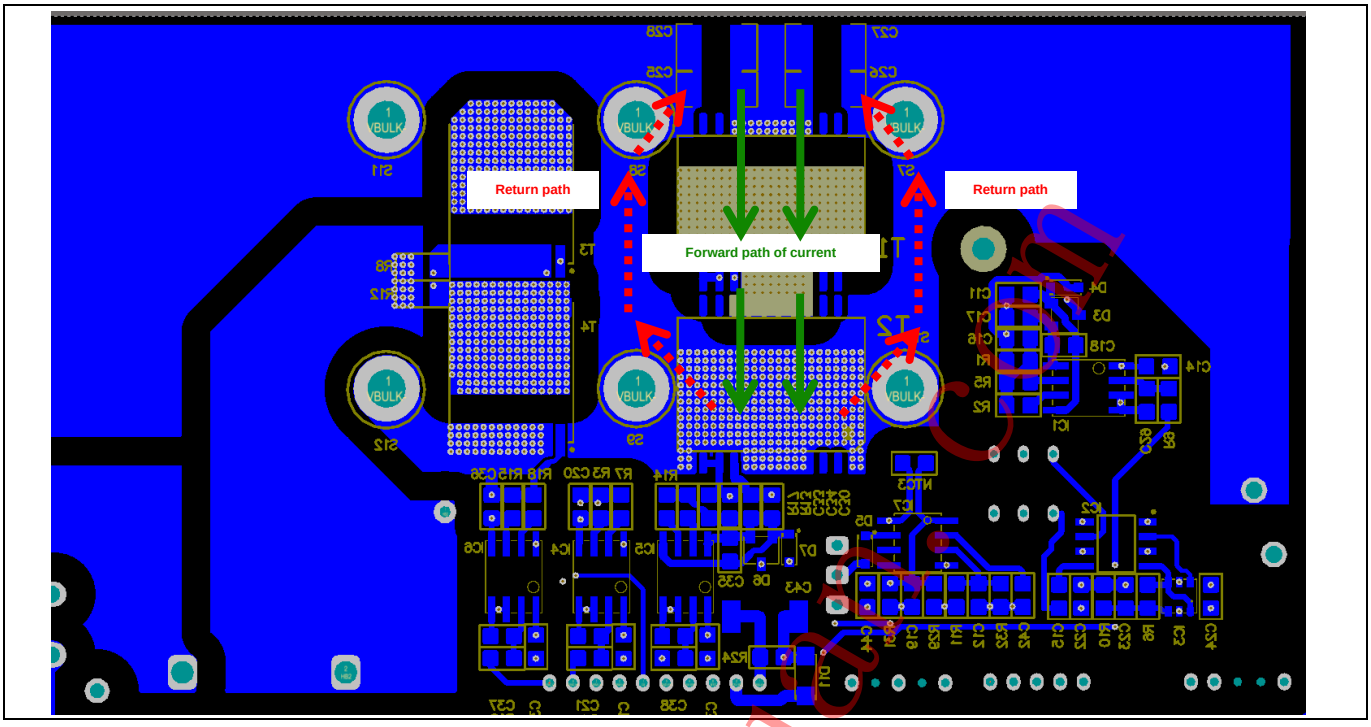

Figure 8 Layout of main PCB (bottom view) and indication of current path

1.5 Thermal concept

Efficient thermal management is a ongoing challenge in power electronic applications and is mostly contrary to low-parasitic designs. The power components on this demo board are exclusively SMDs with high thermal capabilities. The e-mode GaN power semiconductor is housed in a power DSO20 430 mil., which optimizes the thermal path from the chip to the heatsink while balancing the parasitic elements in the power loop. The heat generated in the GaN HEMT is transported through the PCB by thermal vias and dissipated by a common heatsink on the opposite side side of the PCB (i.e. the top side). The PCB uses 276 standard through-hole vias with a diameter of 0.6 mm and a drilling of 0.3 mm throughout the whole area of the heatslug provided by the DSO package.

The temperature of the heatsink is monitored by a PT100 sensor and this information is used to control the speed of the fan. We are currently using a Thermal Interface Material (TIM) from Bergquist or HALA to isolate the PCB from the heatsink. This configuration is able to achieve an $R_{th,junction\_to\_heatsink}$ of at least 5 K/W which allows a maximum output power of 2500 W with just two GaN devices:

$$R_{th,junction\_to\_heatsink} = R_{th,junction\_to\_case} + R_{th,case\_to\_PCB} + R_{th,PCB\_Vias} + R_{th,TIM}$$

Figure 9 shows a thermal measurement of the demo board operating at full output power. The two rectangular fields highlight the GaN power devices on the bottom side of the PCB that act as heat sources. The measurement shows that the maximum device temperature is about 74°C. The maximum permitted junction temperature of the power devices is 150°C. Consequently, the board could be operated at a higher ambient temperature, e.g. in a closed-chassis or high-temperature environment. This temperature measurement was performed at full load and the same conditions used for the efficiency measurement shown in Figure 25. The input voltage was set to 230 V_{rms} and the ambient temperature in this laboratory set-up was approximately 25°C. The efficiency analysis was performed with a Yokogawa WT3000 precision power analyzer and the case temperature was captured with a thermal camera from the FLIR A40 series.

The CoolMOS™ chips are accommodated in a TOLL package, which perfectly fits the $R_{DS(ON)}$ requirements for the phase-rectification half-bridge. Our full-SMD solution enables easier manufacturing as it reduces the manual soldering steps in the production line.

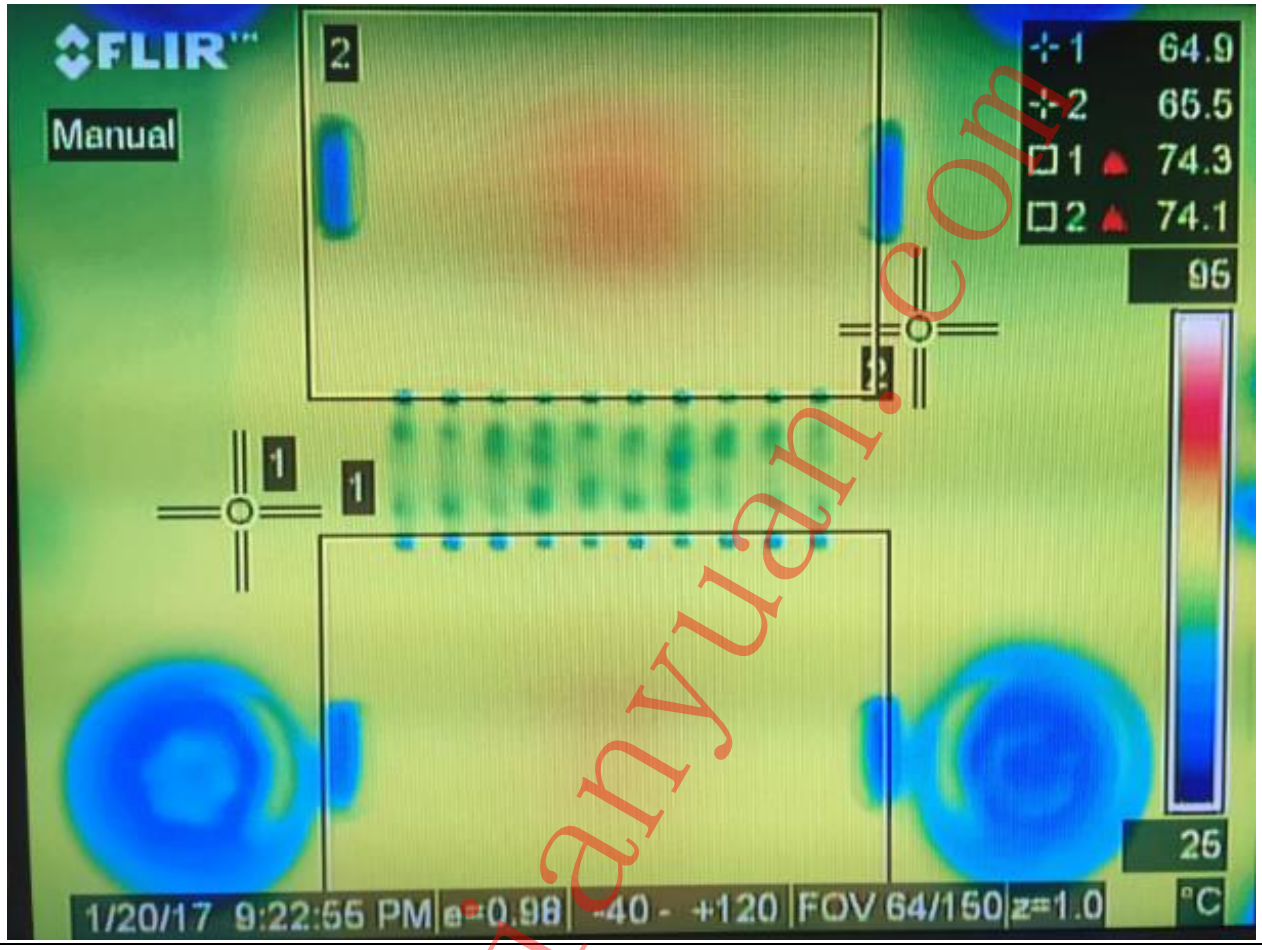

Figure 9 Temperature measurement of GaN devices at full load (2500 W, 230 V AC input)

1.6 EMI filters

The PCB is equipped with a three-stage input filter on the input and a single-stage filter on the output to suppress conducted disturbances. The concept of these filters is to suppress Common Mode (CM) and Differential Mode (DM) noise on the interface of the board toward the AC source and the active load.

1.7 Auxiliary power supply

The auxiliary power supply for the generation of the voltages for the driving stages, the controller daughter card and other auxiliary circuits is generated via a flyback circuit on a separate daughter card. The flyback itself is realized with Infineon's ICE2QR2280G – an integrated power-management IC with 800 V avalanche rugged CoolMOS™, start-up cell and QR current-mode flyback PWM controller in a DSO-16/12 package. More information about the ICE2QR2280G is available [4].

The circuit is supplied by the bulk voltage and generates the following output voltages:

- +15 V DC, non-isolated for driving the low-side 650 V CoolMOS™ C7 Gold
- +13 V DC, isolated for driving the high-side 650 V CoolMOS™ C7 Gold
- +5 V DC, isolated for the digital logic and the primary supply of the MOSFET drivers

Efficiency tests have shown that this flyback system runs at around 80 percent efficiency at 3 W output power. The new ICE5 family of Infineon will increase the efficiency further. The product will become available soon. Details will be available on our webpage [5] or by contacting your local sales office for more information.

If debugging of the functionality is required, we suggest supplying 35 V DC on the PFC input and measuring the output signals of the auxiliary board at the interface to the mainboard.

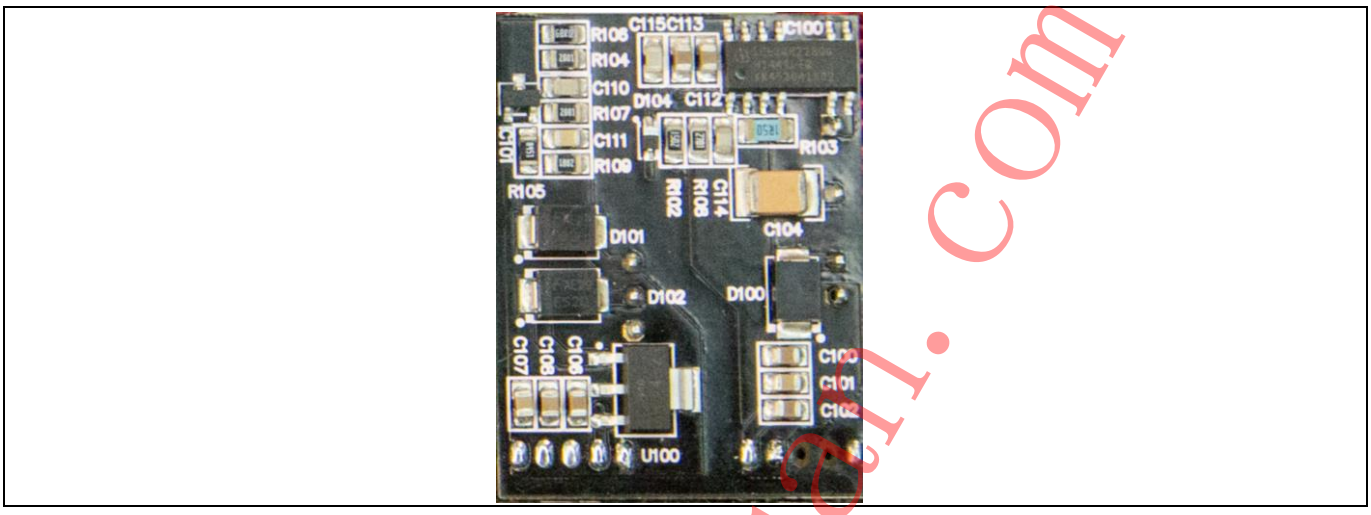

Figure 10 The auxiliary supply daughter board

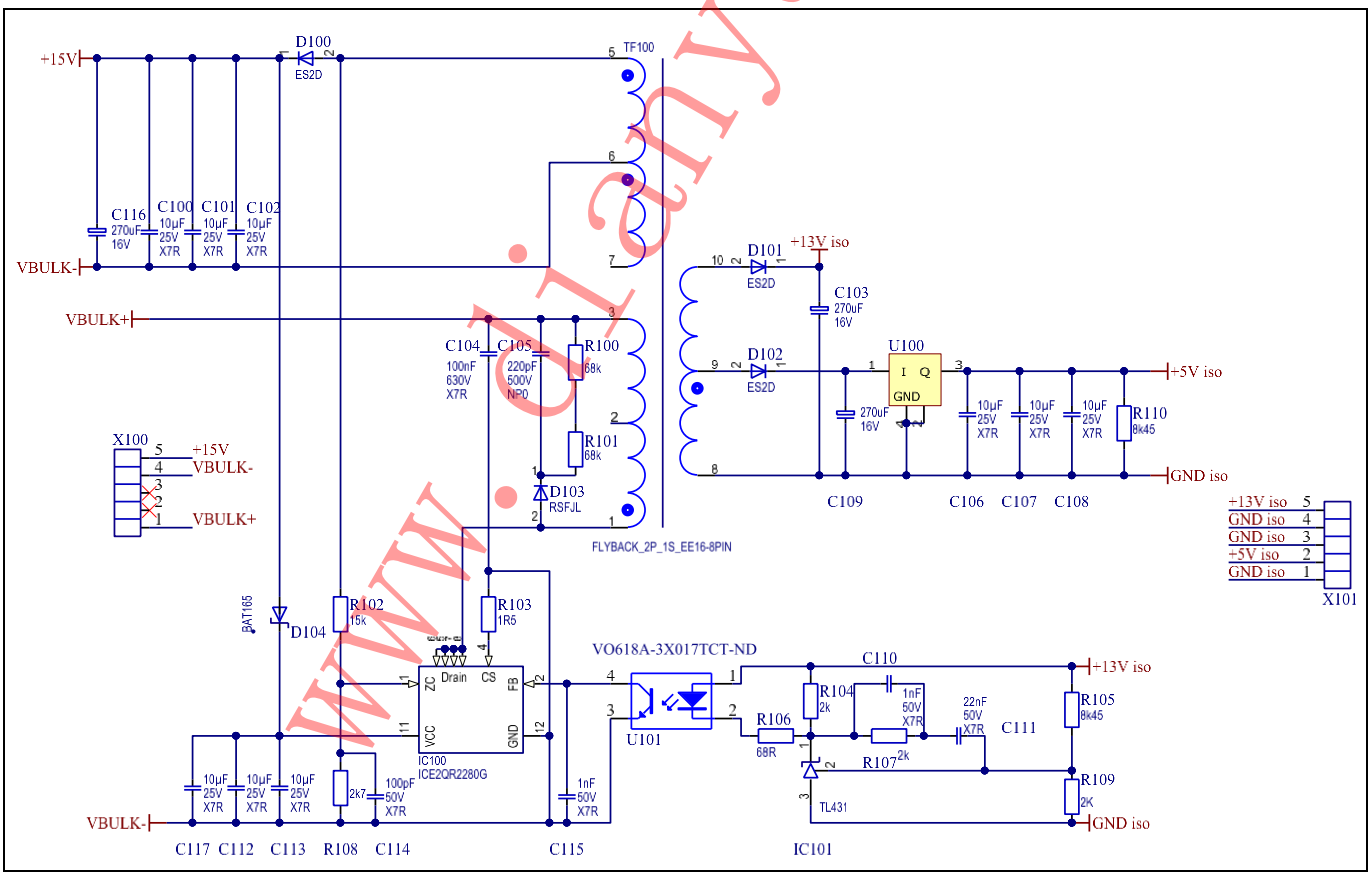

Figure 11 Schematic of the auxiliary supply daughter board

1.8 Control daughter boards

The control board represents the intelligence of the totem-pole PFC. The control is realized using an analog controller that achieves a stable operation across the complete load range and reasonable PFC, as well as handling of fault events. The analog control version shows the feasibility of having a standard PFC controller operating in the full-bridge totem-pole PFC circuitry at 65 kHz.

The analog control is realized with Infineon's ICE3PCS01G, which is a CCM PFC controller that is used for classic PFC circuits comprising a CoolMOS™ switch and a SiC diode. Infineon's latest CCM PFC controller was used due to the very low Current Sensing (CS) input voltage (0.2 V). This minimizes shunt losses under critical-line conditions. More information about the functionality and features of the ICE3 controller is available on our webpage [6].

To satisfy the special requirements of the totem-pole PFC circuit, the behavior of the classic PFC controller has been extended with additional logic gates. Thus, additional features such as the phase rectification of the low-frequency half-bridge (switching with 50 Hz or 60 Hz respectively) can be supported. A photograph of the analog control card is shown in Figure 12. The phase recification and the blanking of the PWM operation for the GaN half-bridge were realized with digital gates on the "gate" output of the ICE3 control IC. The dead-time settings are controlled with RC time constants and a comparator. The schematic is shown in Figure 13, with the extended functionality highlighted in red.

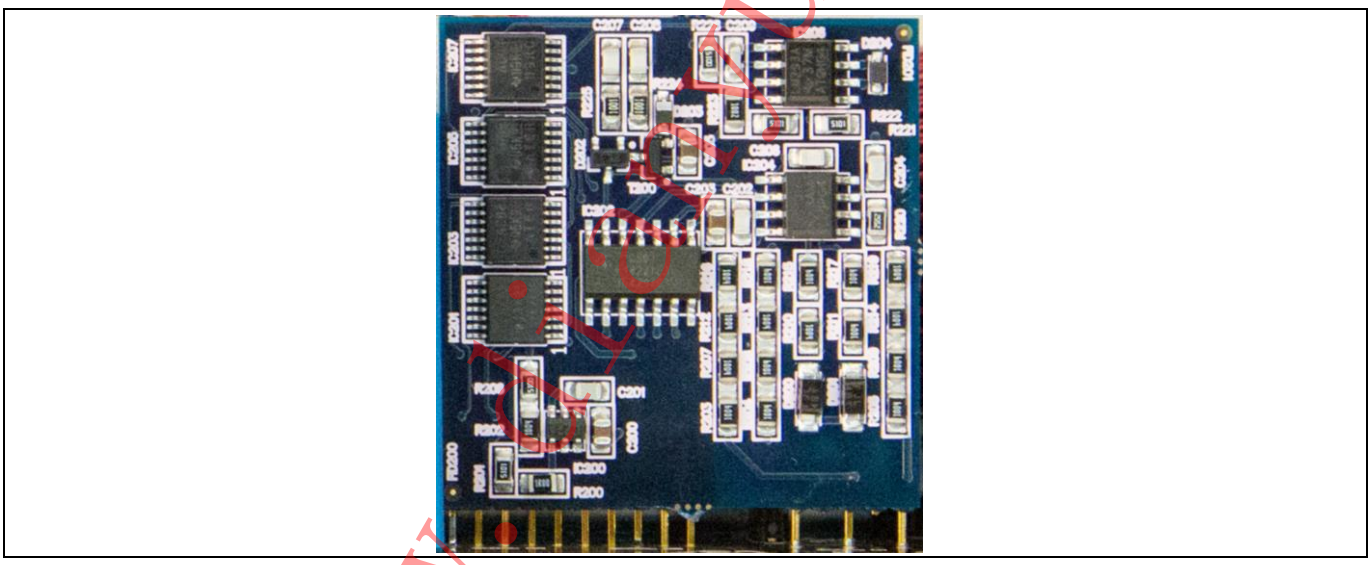

Figure 12 Control card used in the full-bridge totem-pole PFC

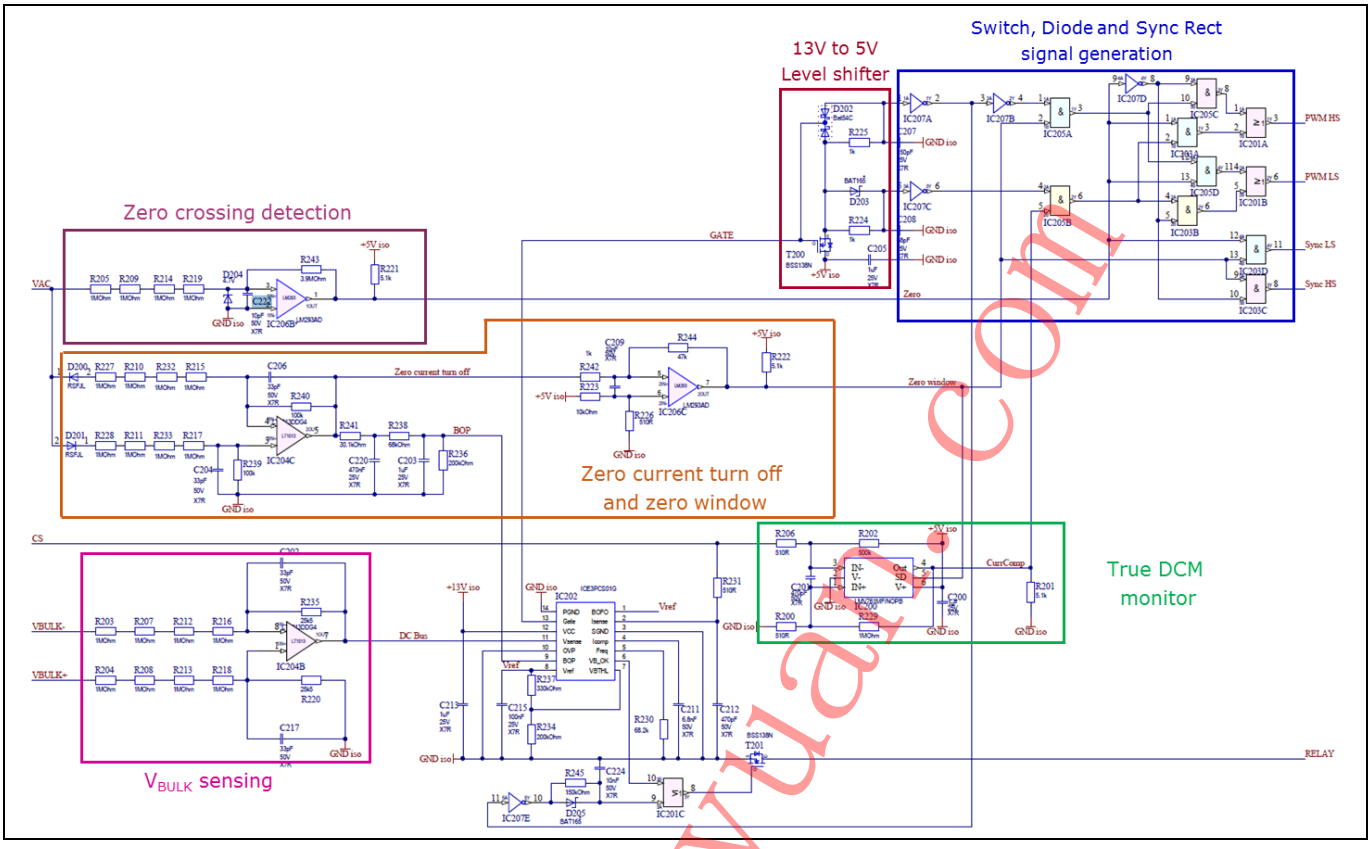

Figure 13 Schematic of the ICE3-based control board with extra functionality required for the totem-pole functionality.

1.8.1 Zero crossing detection

A simple V AC zero crossing circuit is used to provide the required signal to exchange the PWM signal between the high-side and low-side switch over the sinusoidal grid input voltage.

1.8.2 V_{BULK} sensing

As the signal ground is referenced to HB2 and not to V_{BULK}, a differential sensing circuit must be used to provide the V_{BULK} voltage information to the PFC controller.

1.8.3 Switch, diode and synchronous sectification signal generation

This block, represented by all logic circuitry at the top of the schematics shown in Figure 13, is used to accurately and correspondingly generate the switch and diode PWM signals from a single PFC gate signal for efficient utilization of the GaN devices. The proper PWM signals to the high frequency devices, i.e. GaN, and the low frequency ones, i.e. CoolMOS, depend on the grid voltage phase or semicycle.

1.8.4 Level shifter

This block is necessary to step down the 13 VDC voltage signal from the PFC controller to the necessary 5 VDC level that logic circuitry needs to work properly.

1.8.5 Zero current turn off and zero window comparator

This circuit prevents the PWM signal from being applied to the power switches for approximately 100 µs during a zero crossing of the grid voltage to maintain exchange of the high-side and low-side PWM signals. This leads to elimination of possible cross-conduction in the half-bridge configuration.

1.8.6 True DCM monitor / enabler

As the ICE3PCS01G controller is originally designed for a classic or traditional PFC topology where a MOSFET is switching against a SiC Shottky diode, in order to fit this controller to the CCM Totem Pole topology, a fast comparator is needed to prevent a negative current flow in the PFC choke during DCM operation.

1.8.7 Current sensing approach

A cost effective and simple approach to do the current sensing for the oper control is depicted in Figure 14

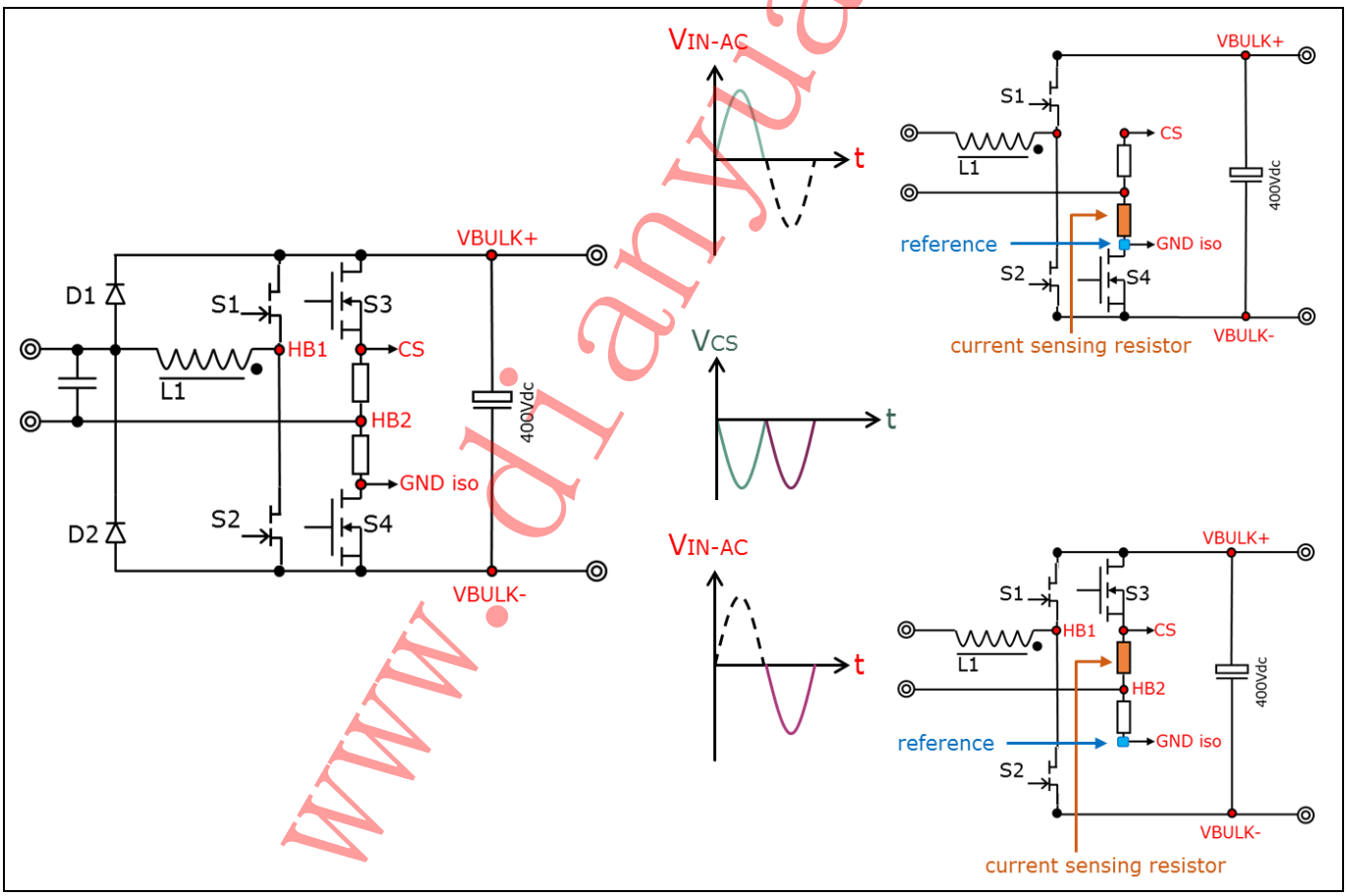

Figure 14 Reference point and active current sensing resistor according to the input voltage semi-cycle as well as voltage waveform that works as reference for the PFC controller.

As GND_iso is referenced to HB2 and not to V_{BULK}, a differential rectification sensing circuit must be used to provide the V AC voltage to the PFC controller.

2 Getting started with the hardware

This section describes how to use the hardware successfully for lab evaluations. Figure 15 shows the different sub-blocks of the demo board.

The auxiliary supply and the PFC control logic are on daughter boards that are connected to the PFC main board. This allows the user to exchange the daughter boards to perform a deeper investigation with (for example) a customized auxiliary supply or an external laboratory power supply.

This demo board is supplied with an analog controller board (Infineon ICE3 PFC controller) on a daughter board. This means that the controller could be easily replaced with another version once another version becomes available (e.g. a digital version).

Figure 16 shows a detailed view of the two different daughter boards that are connected to the main board.

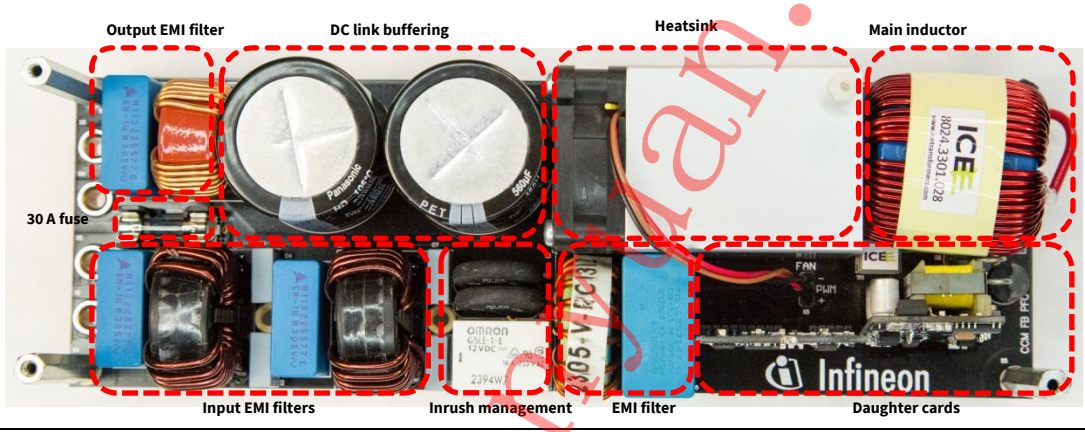

Figure 15 Top view of PCB with block description

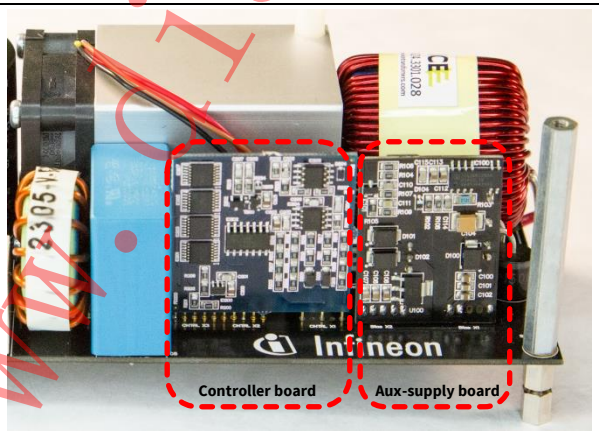

Figure 16 Detailed side view of the controller and auxiliary supply daughter cards

2.1 Basic wiring and connections

Figure 17 shows the principle of the power signal wiring. The AC inputs are shown in blue. The DC outputs are shown in red and black. Attention must be paid to the correct polarity of the DC output signal: the red signal indicates the positive terminal (+) whereas the negative terminal is marked black (-). The corresponding terminals are also marked directly on the bottom side of the PCB. Furthermore, Figure 19 shows the recommended wiring of the power signals. These are the minimum connections that are needed to start up the

hardware. Additional wiring is not required; all of the electronics are supplied via the AC input. Now, the set-up is fully functional and ready to perform efficiency investigations.

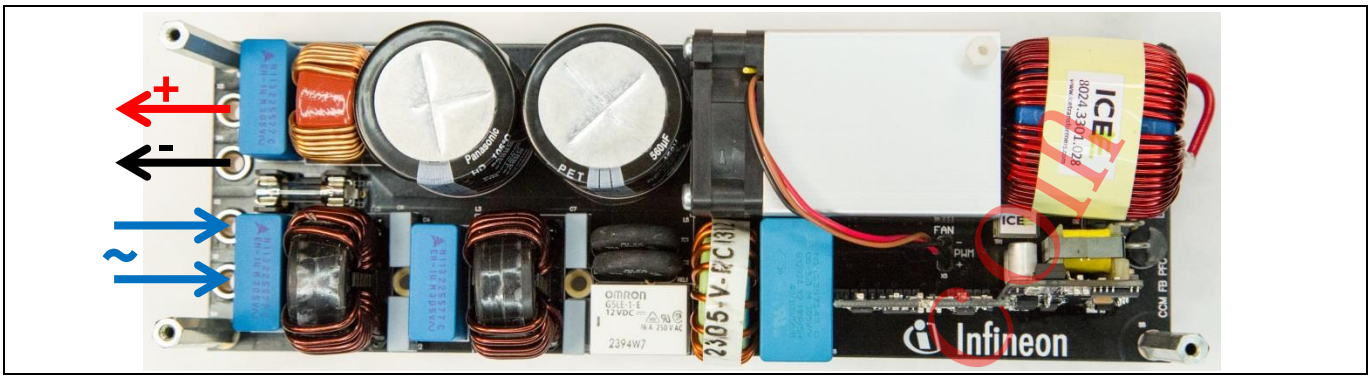

Figure 17 Top view of PCB with power input and output signals

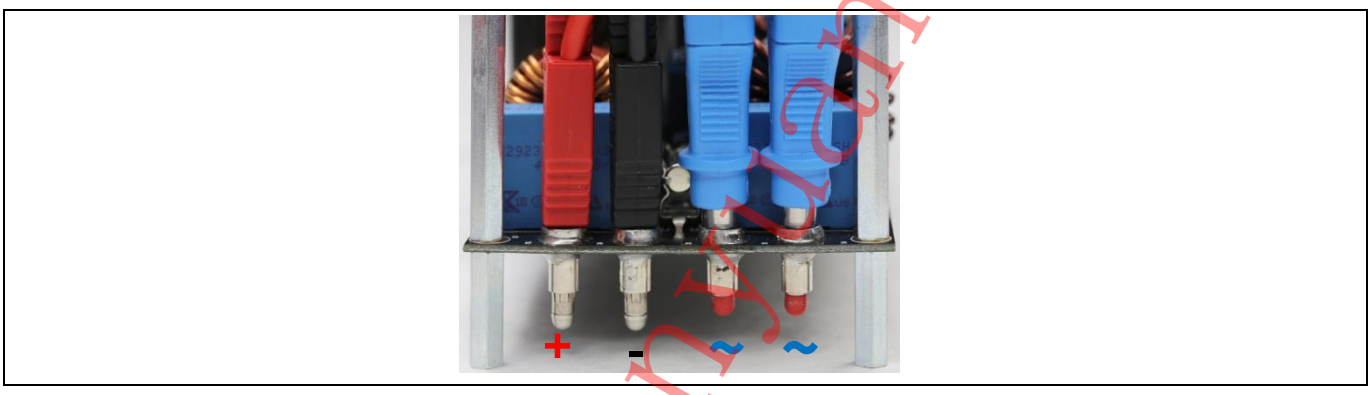

Figure 18 Laboratory wiring of the power signals

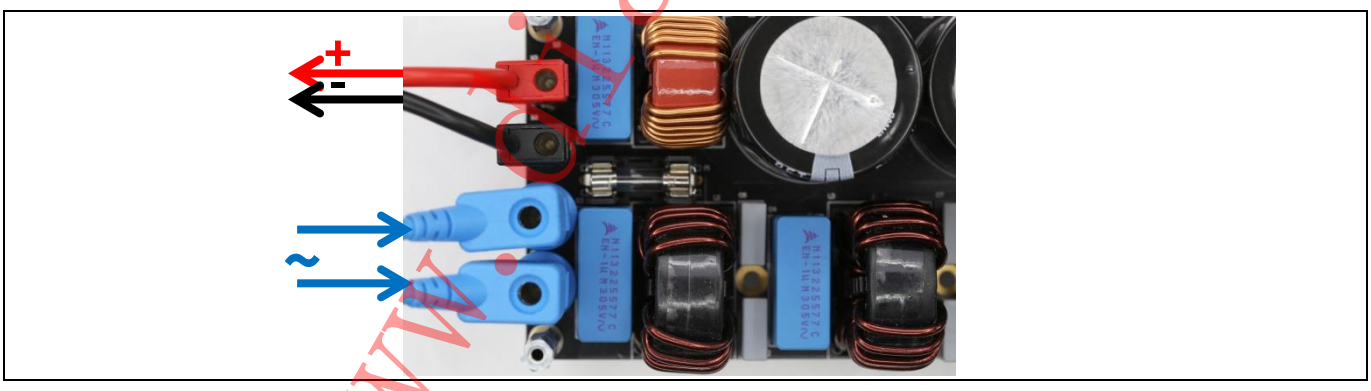

Figure 19 Laboratory wiring of the power signals – top view

Figure 20 Wiring with force and sense wires for accurate efficiency measurements

The input current (I_L) can be measured with a standard current probe. It is recommended to use the wire of the current inductor to perform this task. Figure 21 shows a photograph of this measurement set-up. A current probe that is able to handle the currents up to 40 A is recommended.

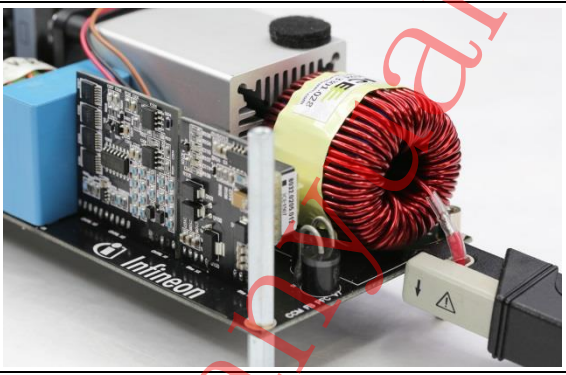

Figure 21 Probing of the inductor current with current probe

Figure 22 shows the recommended way of probing a voltage signal. In this example the V_{DS} voltage across the GaN switch is measured on the low-side of the high frequency half-bridge. The same technique could be applied to measure other signals such as the gate-source voltage provided that the same reference ground is used. If additional measurements are required that cannot be referred to the common ground, it is recommended to use differential voltage probes (for example, to measure the AC input voltage). Probes that meet the required voltage specifications (1000 V) are recommended.

For passive, ground-related probing it is recommended to connect the probe holder as close as possible to the leads of the package and to connect the ground of each probe. It is advantageous to use the central ground connection of the oscilloscope to obtain best results. Figure 22 shows the use of probe holders to measure V_{DS} on the low-side CoolGaN™ switch.

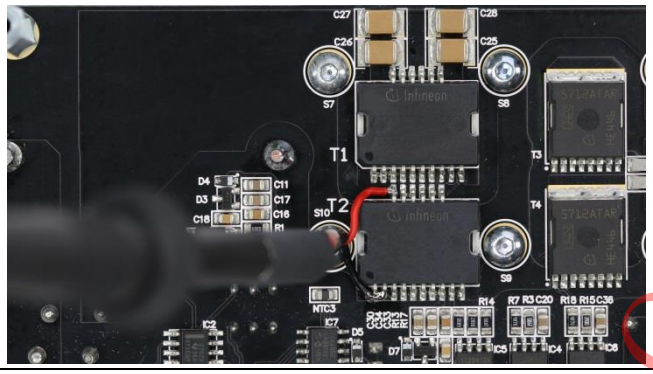

Figure 22 Probing of the V_{DS} signal on the low-side GaN switch with a passive probe and a probe holder directly soldered to the PCB

The demo board is equipped with a regulated fan on the heatsink. The fan is supplied with 12 V DC. The fan speed is controlled via a PWM signal generated by the on-board logic and a temperature sensor that is placed close to the CoolGaN™ switch. The fan could also be supplied externally if closed-loop operation is not required. Figure 23 shows how the fan could be supplied via an external power supply. The cables supplying the fan are simply unplugged from the main board and connected to an external supply. The red cable indicates the positive polarity, whereas the black color marks the negative polarity. The yellow cable (PWM input) is intentionally not connected. Thus, the fan is controlled by the externally supplied voltage only. 12 V DC translates to full fan speed.

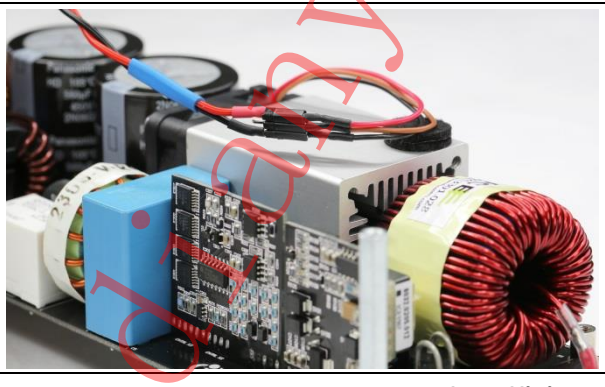

Figure 23 Fan supply with external laboratory voltage source for efficiency measurements. The supply voltage of the fan is set to 12 V DC.

2.2 Start-up procedure

Each board has been tested for full functionality after production (see attached test report).

The recommended way of starting up is to connect all of the necessary cables, as well as the external laboratory-grade source and electronic load. Set the electronic load to constant current mode and program a sink current of 100 mA. Set the AC source to an input voltage of 10 V_{rms} and increase the AC voltage slightly. The PFC will start operating at an input voltage of approximately 85 V_{rms}. The output voltage will become 390 V DC (nominal) once the PFC is in operation. Additionally, a current measurement can be performed. The current will change to a sinusoidal envelope when once the switches start operating. If this state is reached, the output power can be varied by setting the load point on the electronic load (any load jump is allowed within the specified output power range). Refer to Figure 24 to determine the maximum permissable output power as a function of the input voltage. The absolute maximum power is 2500 W at a minimum input voltage of 180 V_{rms}.

For the minimum input voltage (85 V_{rms}) do not exceed 1000 W (40 percent derating of the maximum output power as shown in Figure 24).

It is recommended to connect the fan to an external 12 V laboratory-grade power supply and to monitor the temperature of the power devices during efficiency tests or long-term operation (longer than 1 hour).

Start-up at full-load conditions is not recommended.

2.2.1 AC input voltage requirements

The evaluation board is able to operate at input voltages from 85 to 265 V_{rms}. All tests were performed with a dedicated laboratory-grade AC voltage source on the input. The PFC stage supports AC mains frequencies of 50 and 60 Hz.

Although the hardware is built as close as possible to real application conditions, direct connection to the AC mains is not recommended. Use dedicated laboratory voltage sources instead.

Note: The start-up threshold of the PFC board is 85 V nominal. If the input voltage is below this, the boost operation will not begin and the DC link voltage will not be 390 V. Nevertheless, the basic functionality of the gate drivers and the controller can be debugged with only 35 V DC on the input.

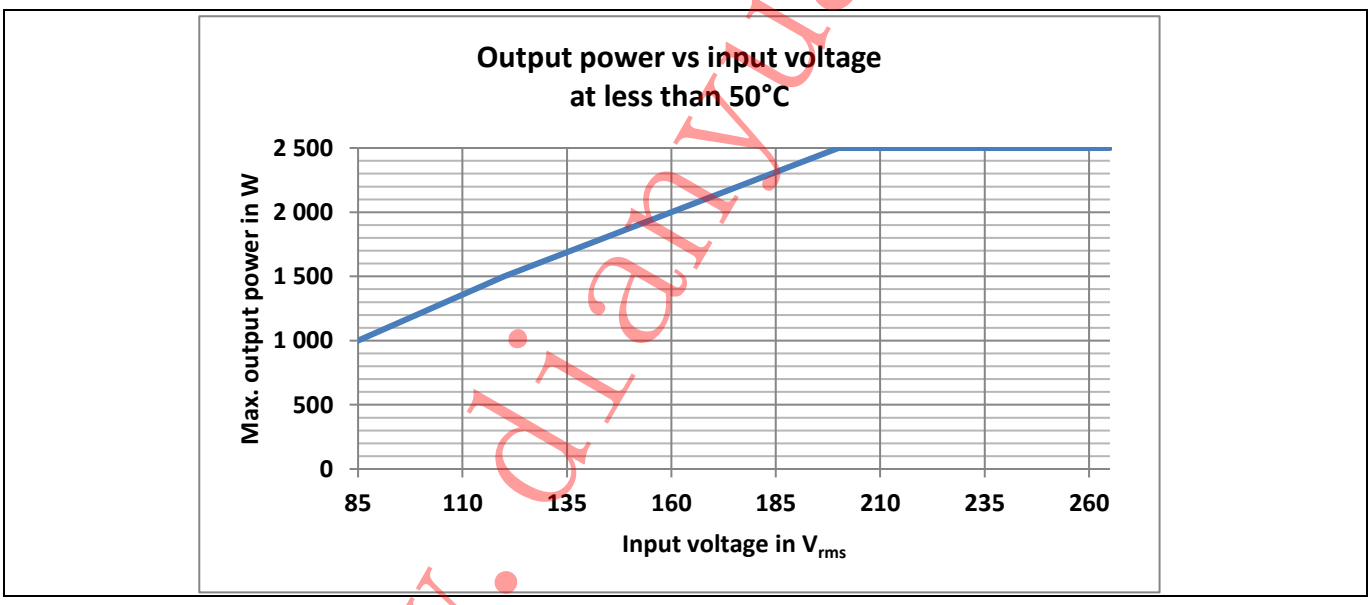

Figure 24 Recommended derating of output power vs input voltage at 50°C

2.2.2 DC output voltage

The nominal output voltage of the converter is set to 390 V. This voltage is achieved throughout the wide range input and over all load conditions. The power stage controller will adapt the PWM signal accordingly if a line jump on the input or a load jump on the output occurs within the specified operating points (see Figure 34).

It is recommended to use electronic loads at the output. The load must be capable of handling the voltages present and the maximum output power of 2500 W. All tests were performed with the load operating in either constant current or constant power mode as the PFC controller is able to maintain the output voltage at the nominal output voltage of 390 V.

As mentioned in Chapter 2.2, start-up has to be performed at no-load conditions, meaning that the electronic load at the output has to sink a small current of 100 mA or be off when the input voltage is applied to the PFC.

3 Measurement results

This section provides an overview of typical measurement results. All results were measured in laboratory conditions at an ambient temperature of 25°C.

3.1 Efficiency measurement

The concept of this demo board is to show that Infineon's GaN in combination with the best-in-class 650 V CoolMOS™ C7 Gold can push the efficiency above 99 percent. Figure 25 shows the measured efficiency curve. The red line shows the complete system efficiency, measured at the AC input and the DC output of the converter. All power losses present in the application (the auxiliary supply, the cooling fan, the control logic, the fuse, the cable contact resistances and the losses of the EMI filters) are included in the efficiency graph in Figure 25.

The efficiency curve in Figure 25 was obtained at an input voltage of 230 V_{rms} and at an ambient temperature of 25°C by using sense contacts connected to the equipment (four-wire measurement). The proposed cabling set-up is shown in Figure 17. The evaluation of the efficiency was performed with a Yokogawa WT3000 precision power analyzer as shown in Figure 25.

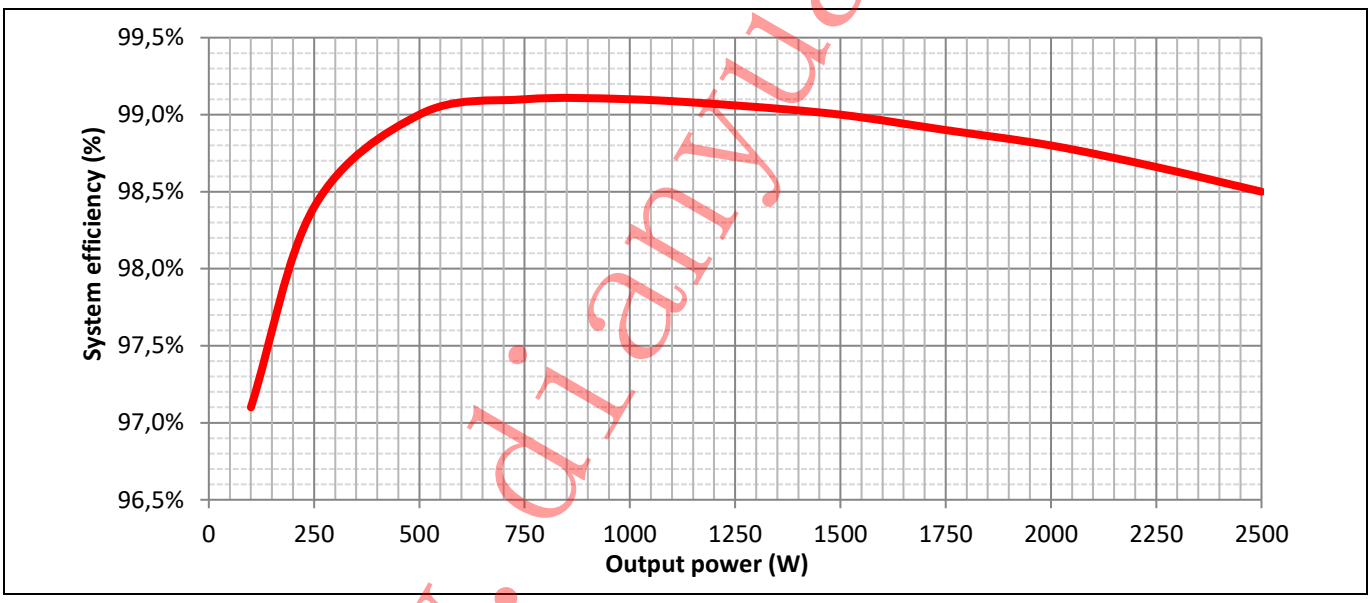

Figure 25 PFC efficiency vs output power at V_{in} = 230 V_{rms}. The measured peak efficiency is 99.2 percent at 1 kW output power.

3.2 Gate signal measurements

Figure 30 shows a typical V_{GS} while operating in high-load CCM operation. In the off-state V_{GS} is approximately -6 V, whereas the voltage in the on-state reaches approximately 3.2 V. Further details are given in Figure 27, where a turn-off event of the HEMT is shown. This figure shows a remarkable linear V_{DS} slope, rising in about 10 ns from the on-state to the DC link voltage – caused by the almost linear C_{oss} behavior of the GaN. The maximum voltage peak is 480 V, which is within the recommended derating target of 80 percent of $V_{DS,max}$.

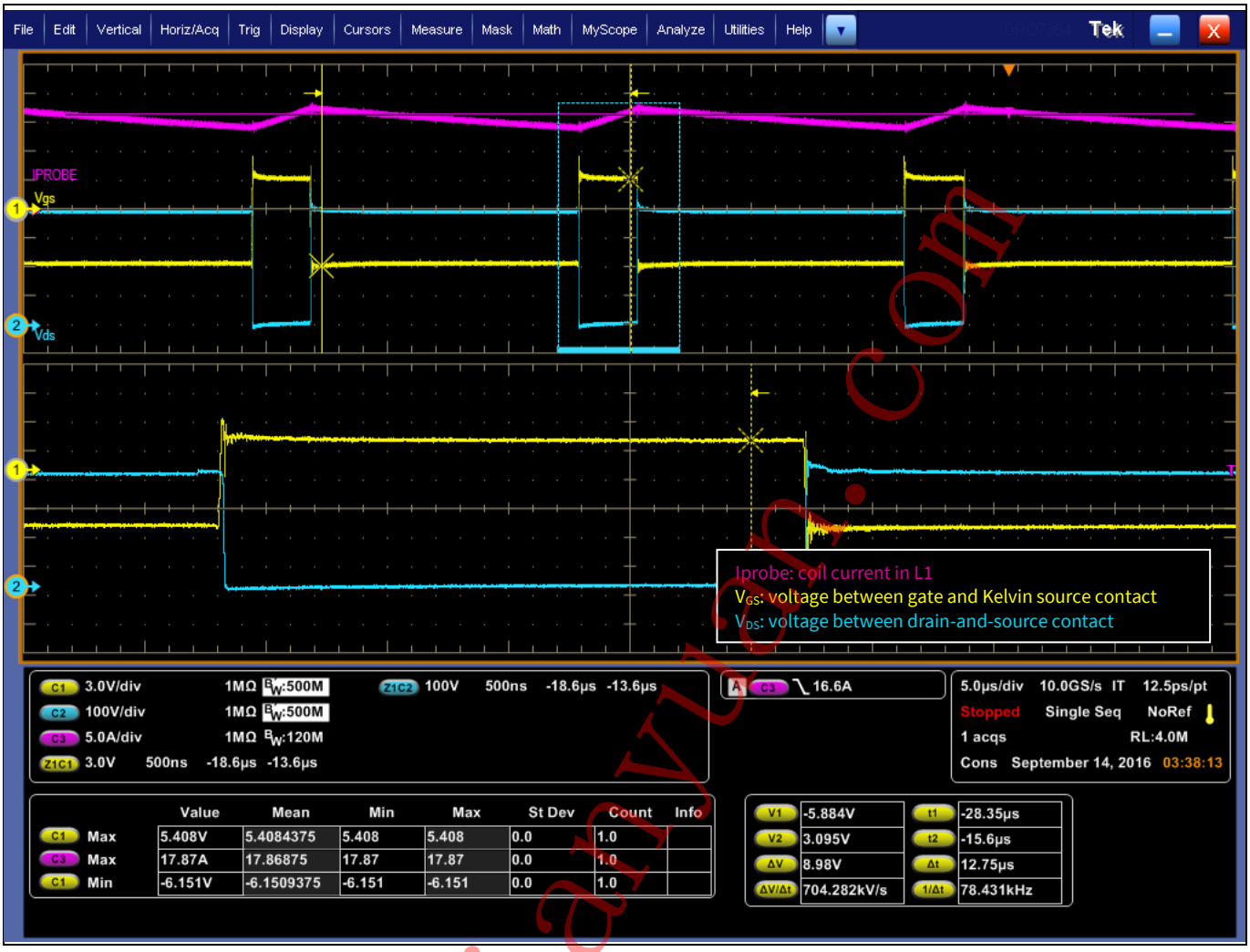

Figure 26 PFC operating in CCM mode at an average current of 17.86 A. The yellow curve shows the V_{GS} signal. The cursor position measures the steady-state V_{GS} in the on- and off-states. The blue curve shows V_{DS} measured on the low-side CoolGaN™ switch. The magenta curve is the current measured in the main PFC inductor.

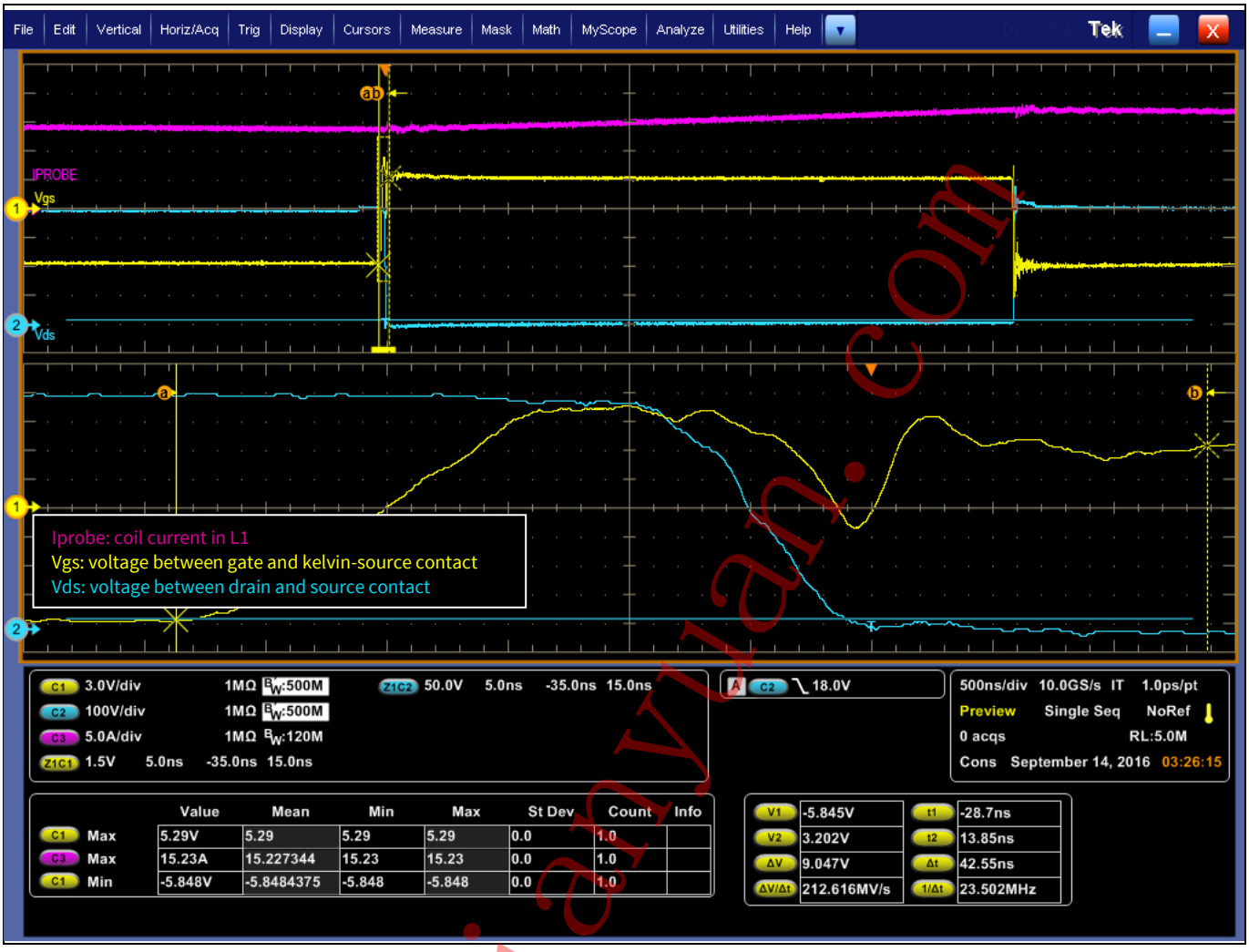

Figure 27 Typical PFC waveforms in CCM mode operation at turn-on of the low-side GaN HEMT. The magenta line represents the inductor current, the blue curve V_{DS} and the yellow curve shows the V_{GS} signal. The dip on the V_{GS} signal is caused by the fast dv/dt of V_{DS} and the finite CMRR of the voltage probe. This presents no risk to operation.

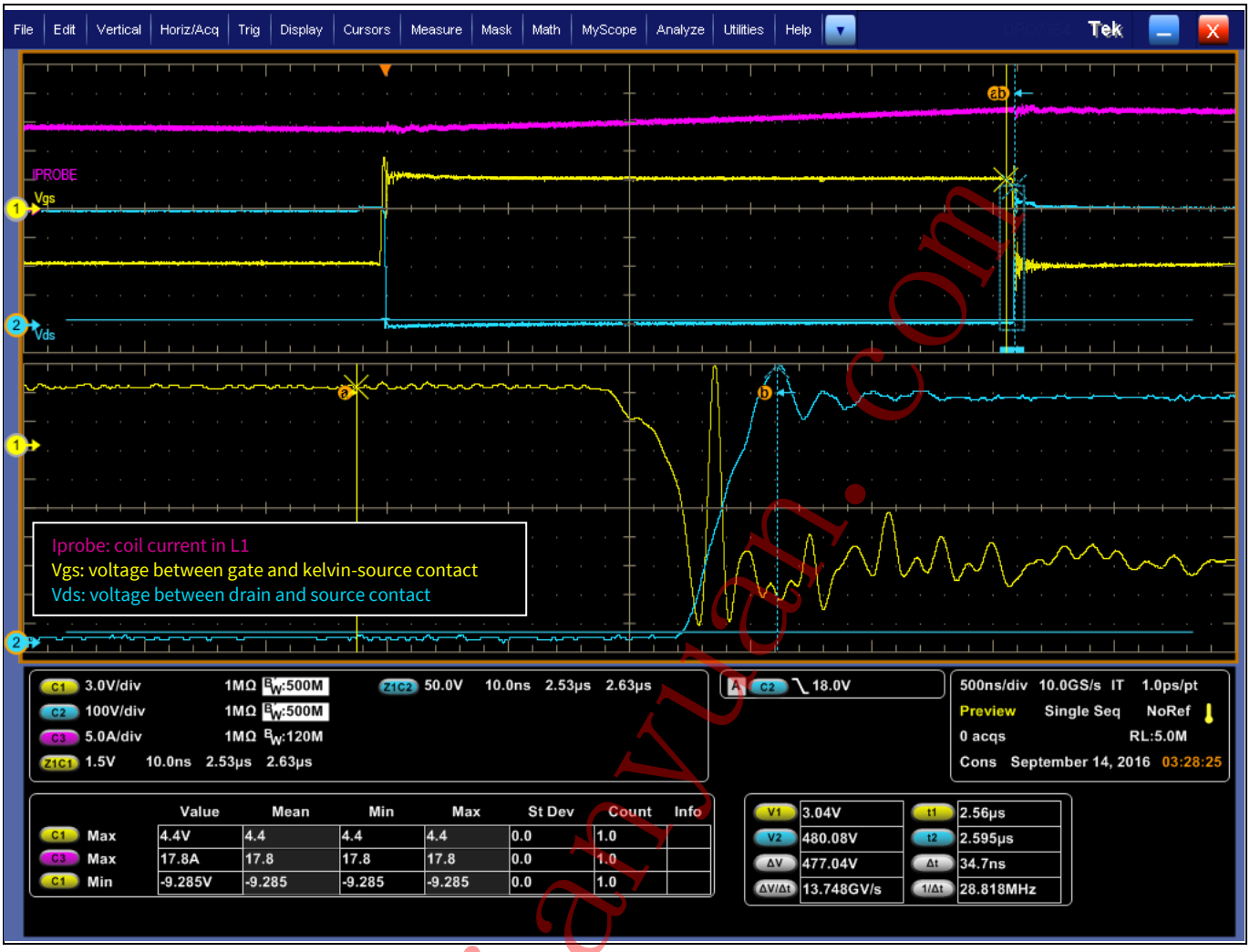

Figure 28 **Typical PFC waveforms in CCM mode operation. The magenta line represents the inductor current, the blue curve V_{DS} and the yellow curve shows the V_{GS} signal. The spike of the V_{GS} signal is a measurement artifact caused by the fast transition of V_{DS} and the limited CMRR of the voltage probe.**

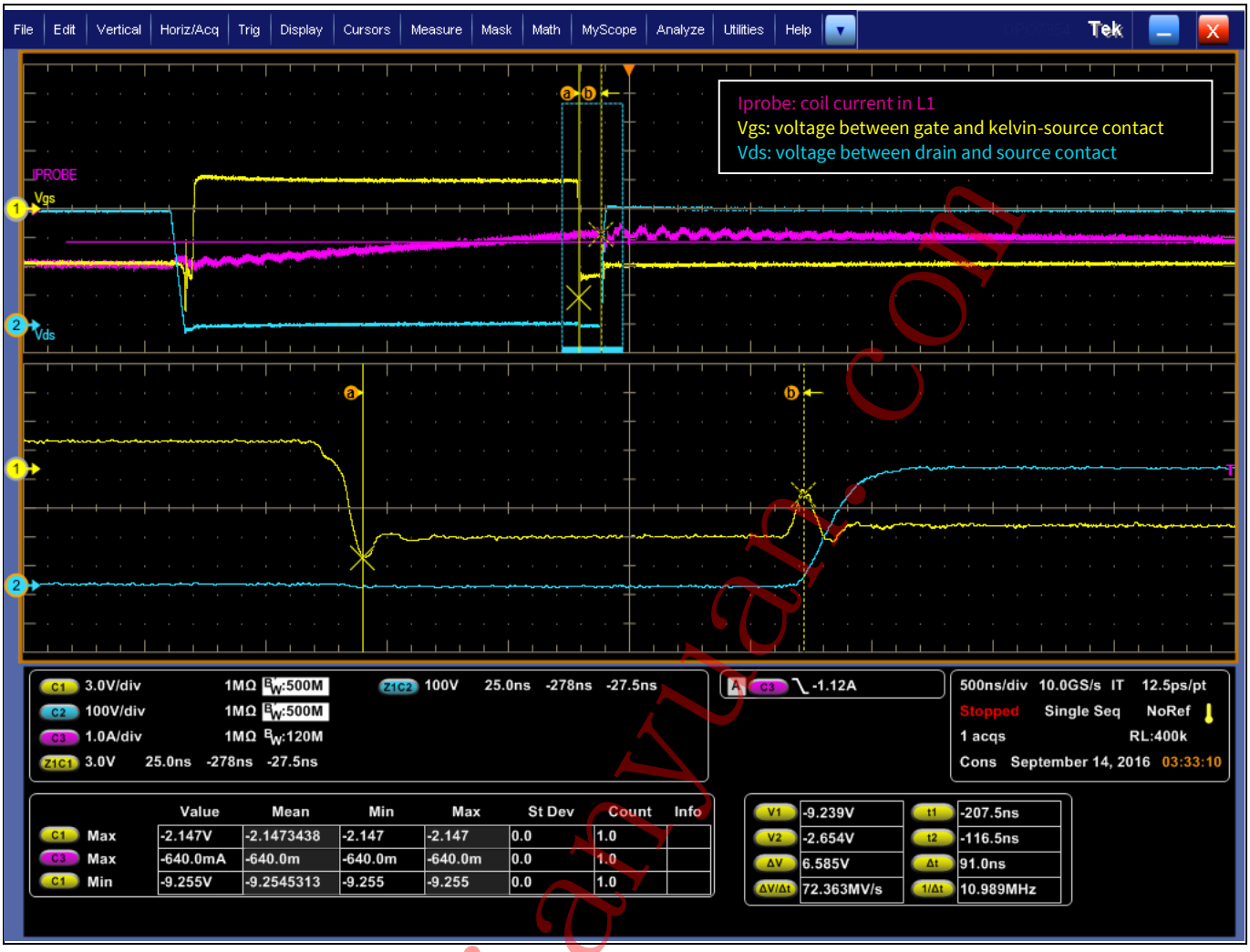

Figure 29 The zoom on the yellow waveform (V_{GS}) reveals the dead-time settings (approximately 90 ns). This value was chosen to minimize the time when the CoolGaN™ HEMT is inactively conducting (V_{GS} is below the threshold, but the channel conducts in reverse similar to a body-diode) and to maximize the active freewheeling time (V_{GS} is greater than V_{TH} and the channel is actively driven on).

3.3 Start-up

Figure 30 shows start-up of the PFC with a minimum load of 300 mA. The blue curve shows the DC link voltage on the output whereas the orange curve represents the input current. As shown, the maximum inrush current is 8 A at 230 V_{rms} and 35.4 A at 90 V_{rms}. The complete start-up procedure takes less than 500 ms.

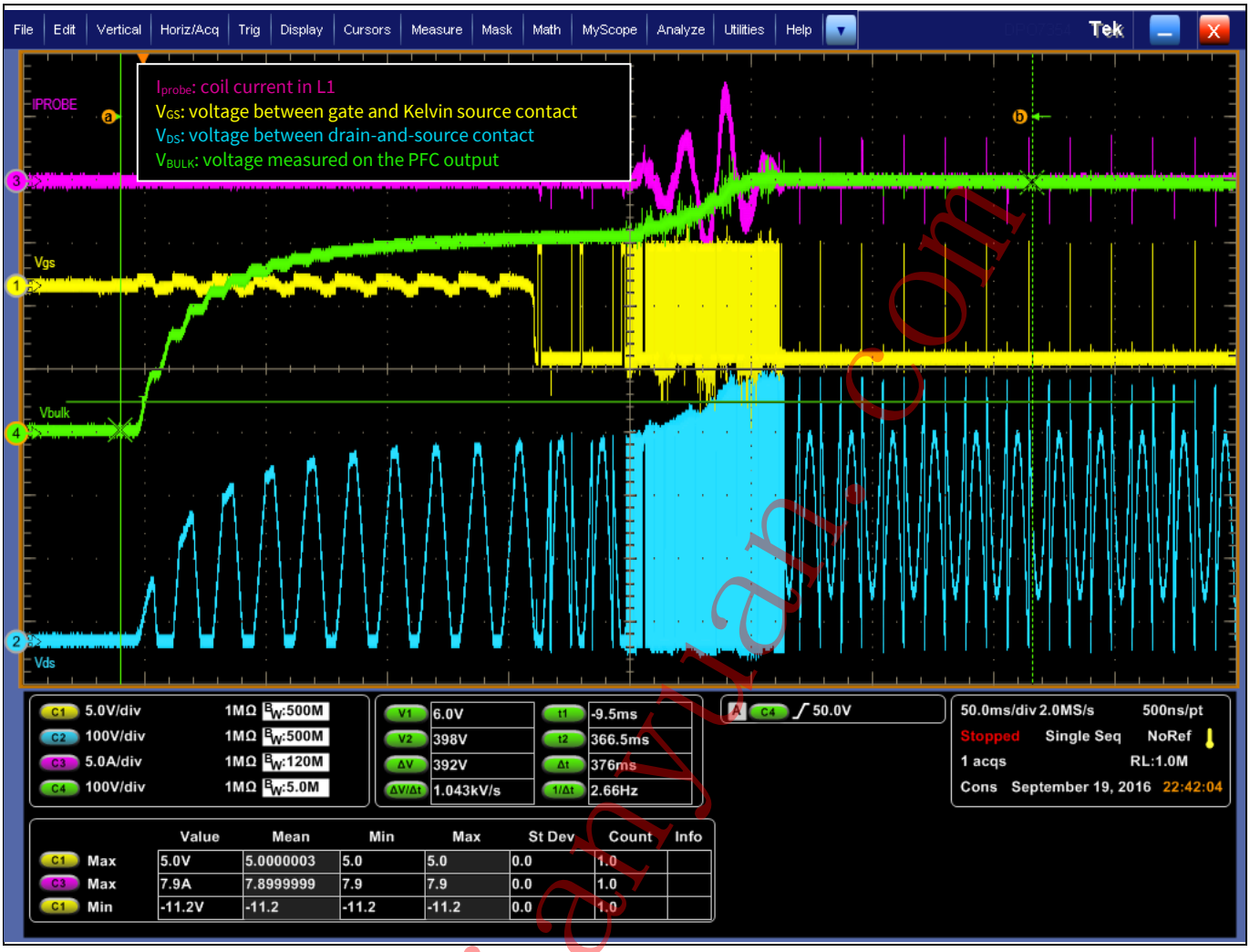

Figure 30 Start-up of PFC at 230 V_{rms} without load current. The blue curve represents V_{DS} voltage, the magenta curve shows the input current, the green curve shows the DC link voltage and the yellow curve shows V_{GS} voltage of the GaN HEMT. The measured peak input current is 7.9 A.

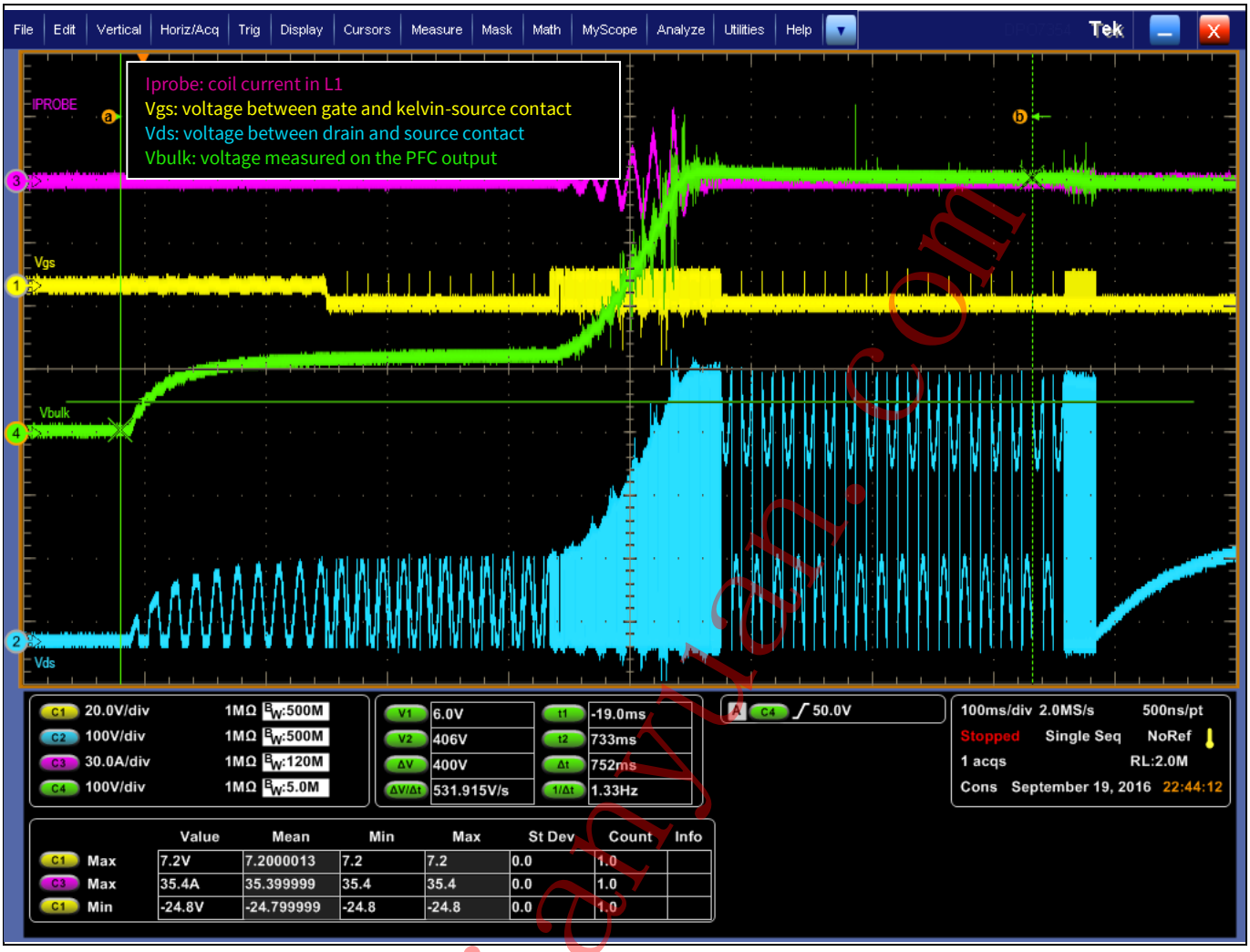

Figure 31 Start-up of PFC at 90 V_{rms} without load current. The blue curve represents the V_{DS} voltage, the magenta curve shows the input current, the green curve shows the DC-link voltage and the yellow curve shows the V_{GS} voltage of the GaN HEMT. The measured peak input current is 35.4 A.

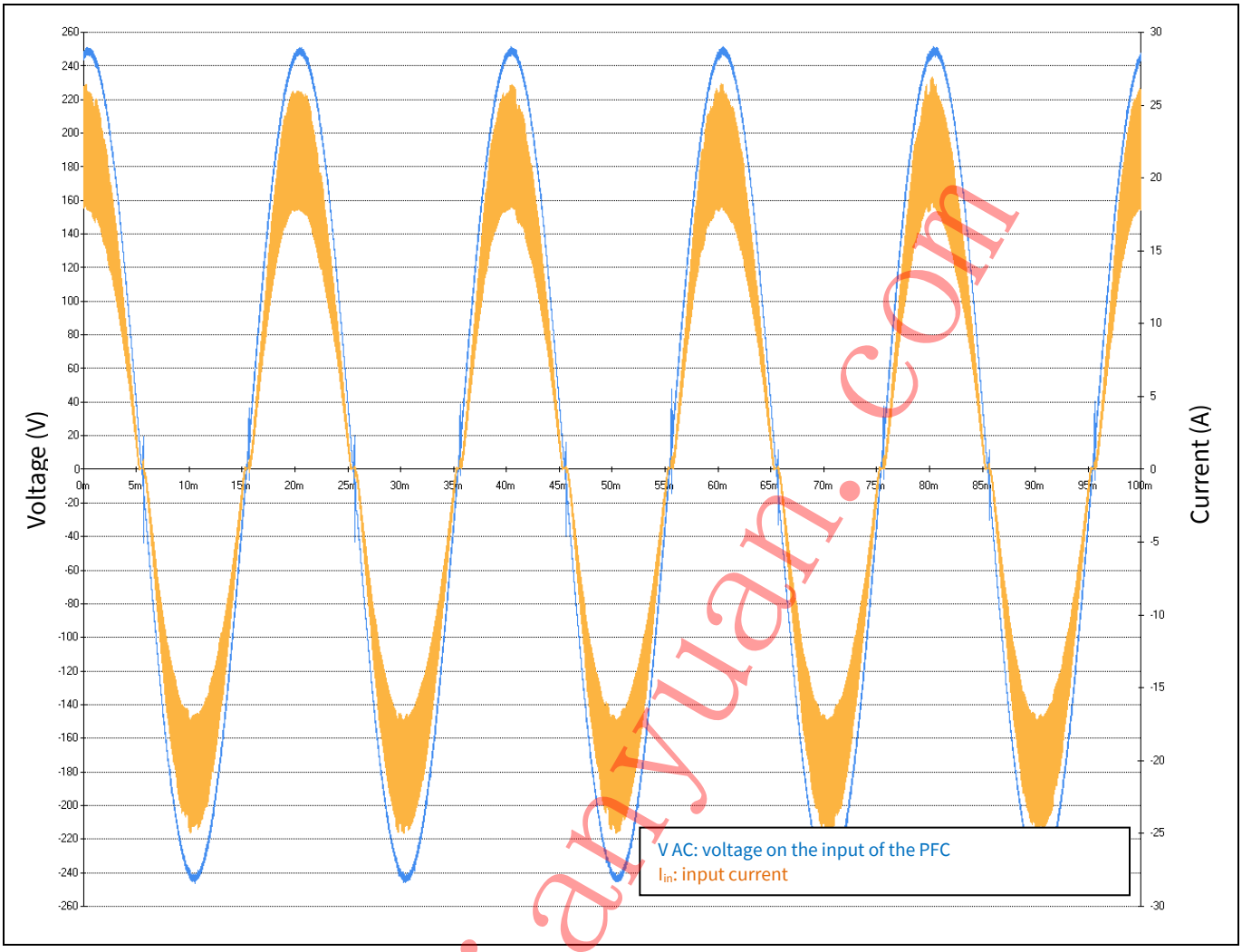

Figure 32 Continuous operation within tolerance conditions (V_{in} = 176 V_{rms}, blue curve); orange curve shows the input current; output power is 2500 W.

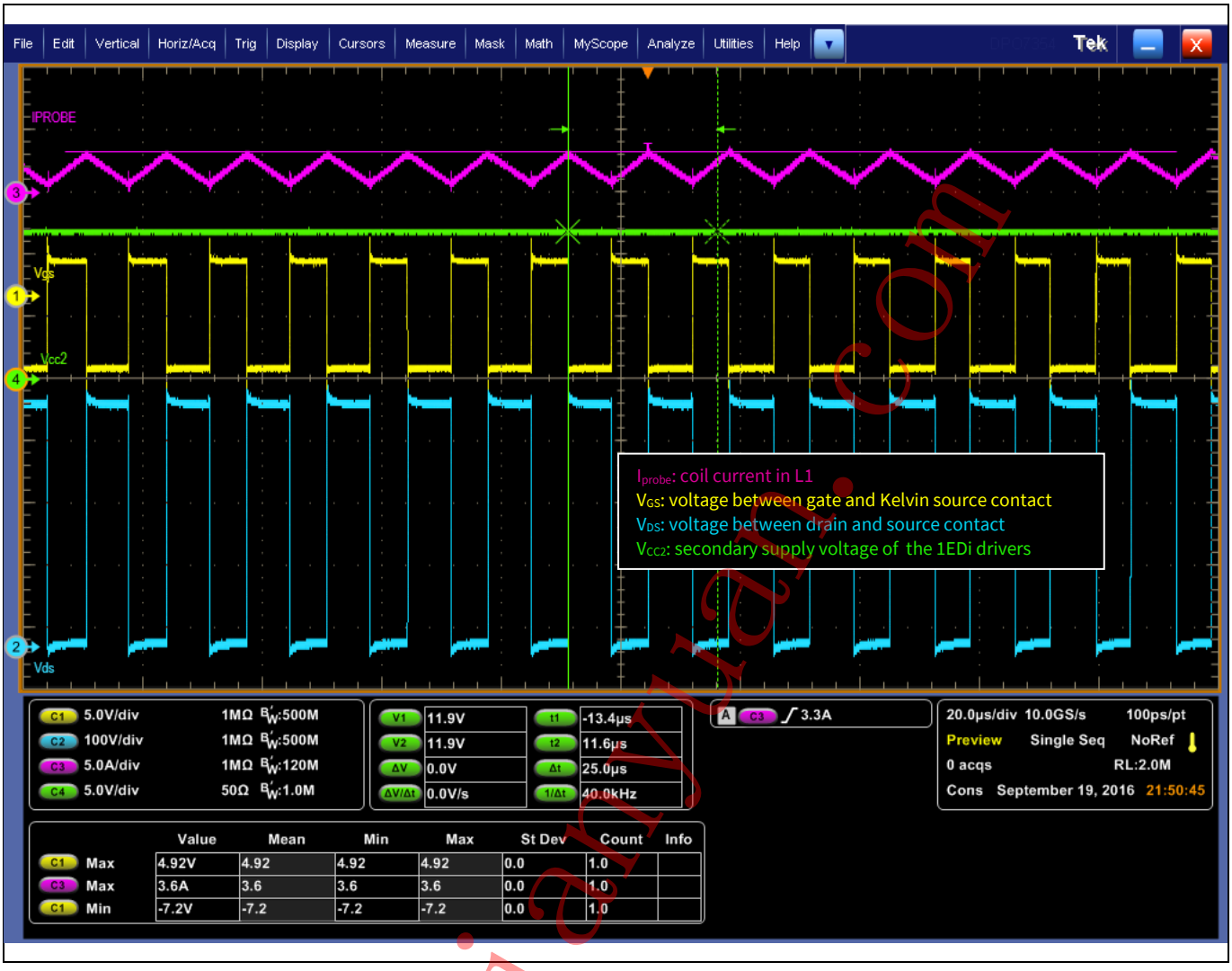

Figure 33 Continuous operation at nominal conditions (V_{in} = 230 V_{rms}); the output power is 500 W. The blue curve represents V_{DS}, the magenta curve shows the input current, the green curve shows the supply voltage of the 1EDi drivers on the secondary side and the yellow curve shows V_{GS} voltage of the GaN HEMT.

3.4 AC-line cycle drop-out test

Several drop-out tests of the AC input show the robustness of the demo board against power line disturbances. Figure 34 shows a severe loss of the AC input voltage for 20 ms and the subsequent recovery of the DC link voltage.

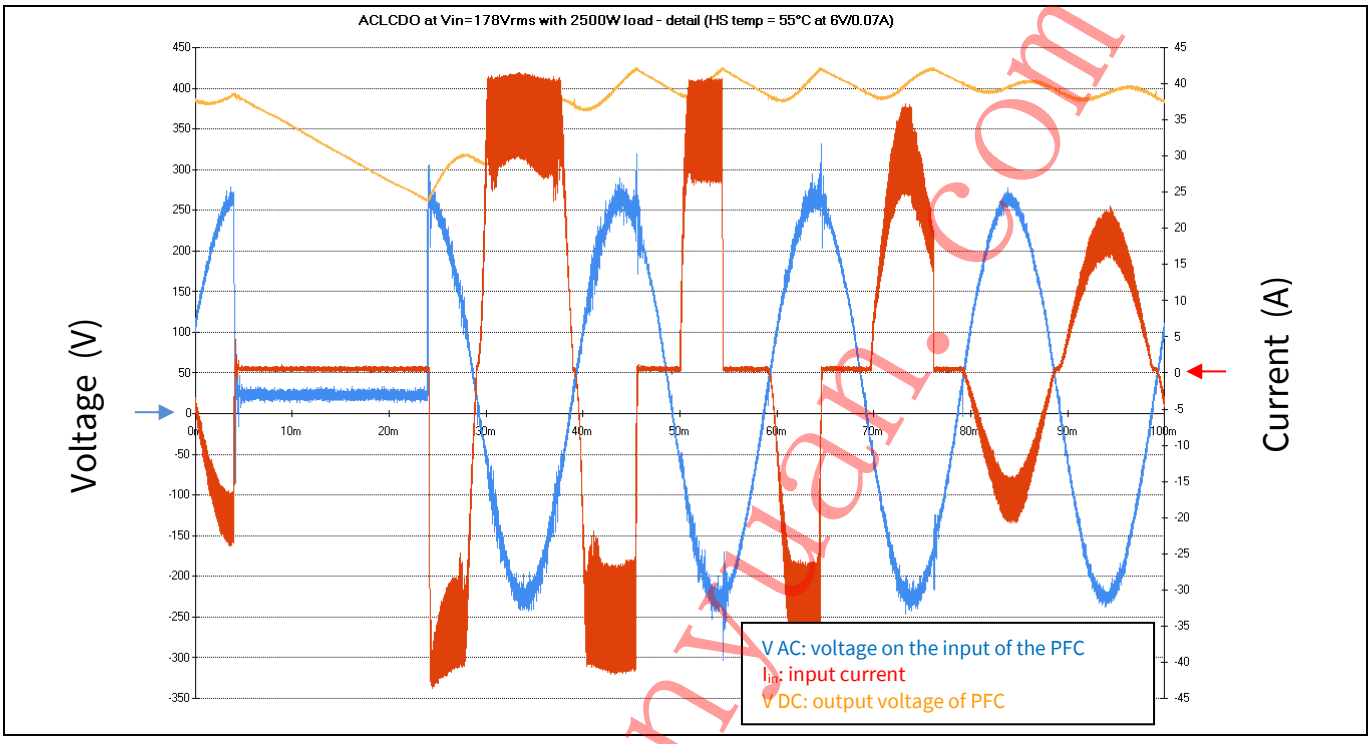

Figure 34 Measurement result of a 20 ms AC-line cycle drop-out test. The result shows that the demo board can handle this severe line disturbance and recover to full operation in less than 65 ms.

3.5 Load steps

The PFC demo board can handle load transients from 0 to 100 percent, as shown in Figure 34.

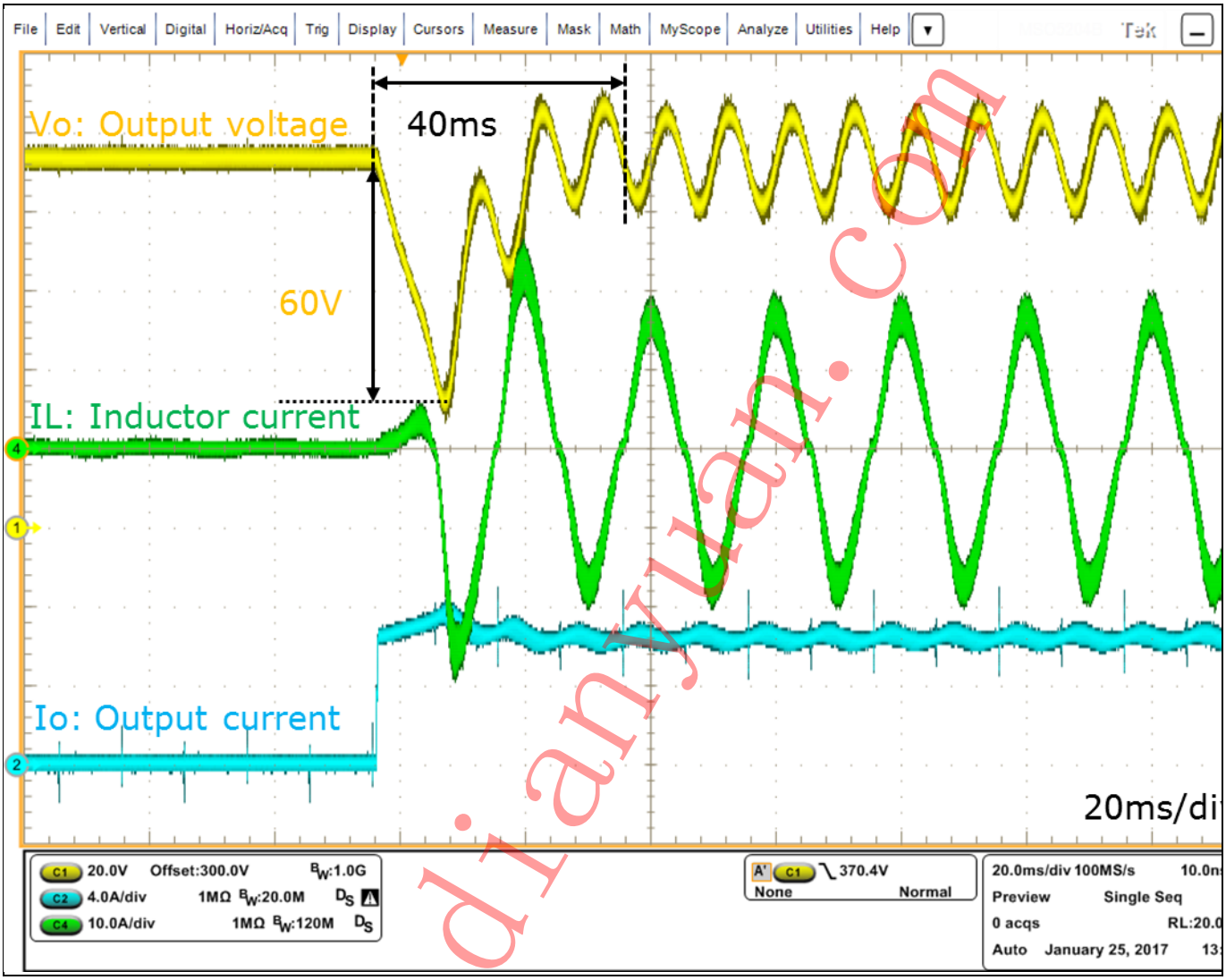

Figure 35 Measurement result of load step from 0 to 100 percent load. The inductor current peaks at approximately 28 A, and the output voltage recovers in about 40 ms. Maximum bus voltage deviation is -60 V.

3.6 EMI measurement result

An EMI test has been performed as well as the efficiency and PLC tests. The results in Figure 36 show the conducted EMI at full load and nominal input voltage. The test was performed in a certified Infineon EMI laboratory.

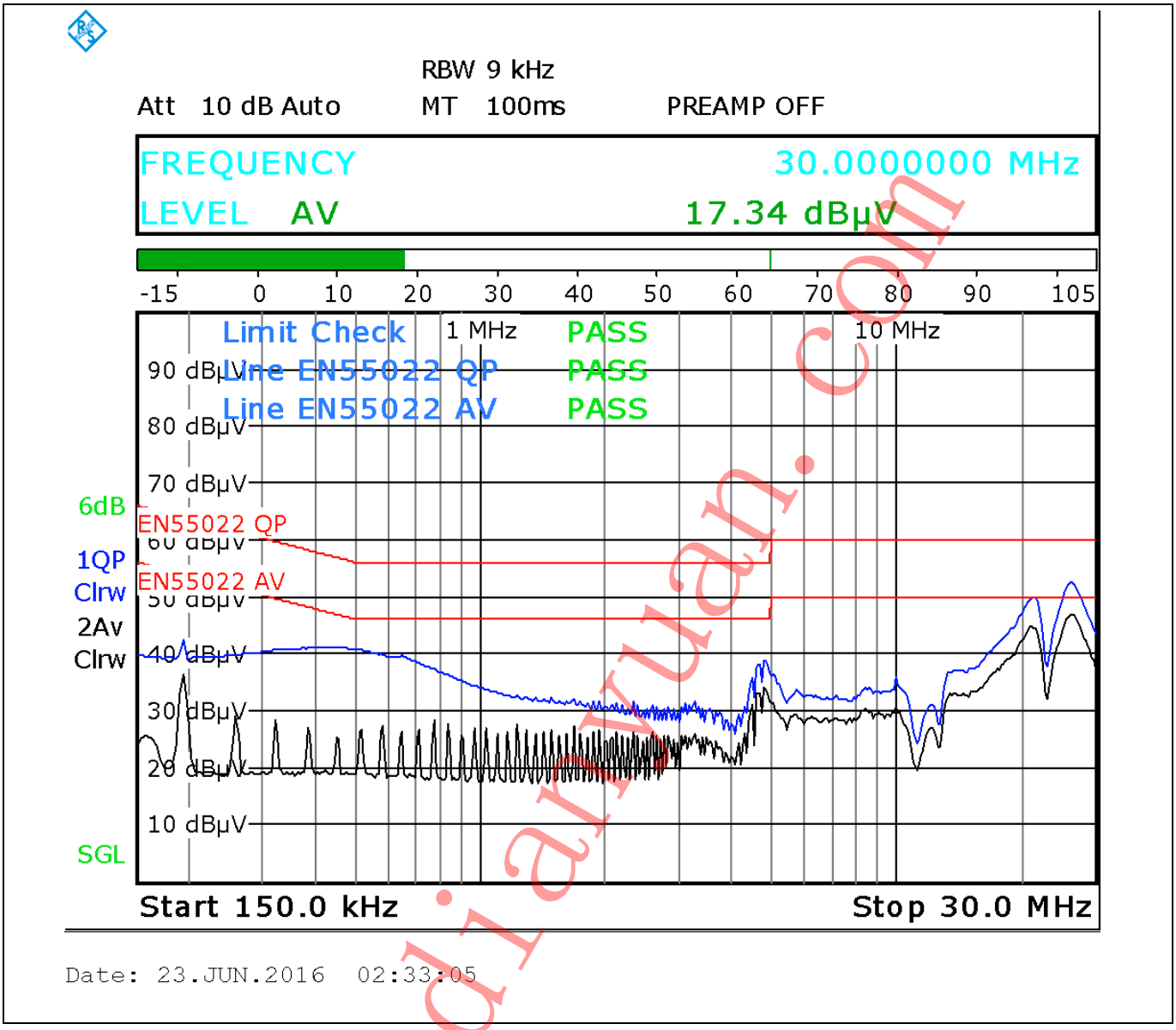

Figure 36 Conducted EMI measurement result showing a pass of the EN 55022 standard

4 Specifications

Note: All ratings are specified for lab conditions and an ambient temperature of 25°C.

- V_{in} = 85 V_{rms} to 265 V_{rms}
- P_{out} = 0 W to 2500 W
- f_{sw} = 65 kHz
- $t_{ambient}$ = 25°C
- $V_{out,nom}$ = 390 V DC
- $V_{out,\ min}$ = 340 V DC
- $V_{out,max}$ = 440 V DC

Note: Derate output power for lower input voltage according to Figure 24.

5 Addendum

5.1 Schematics of the main board

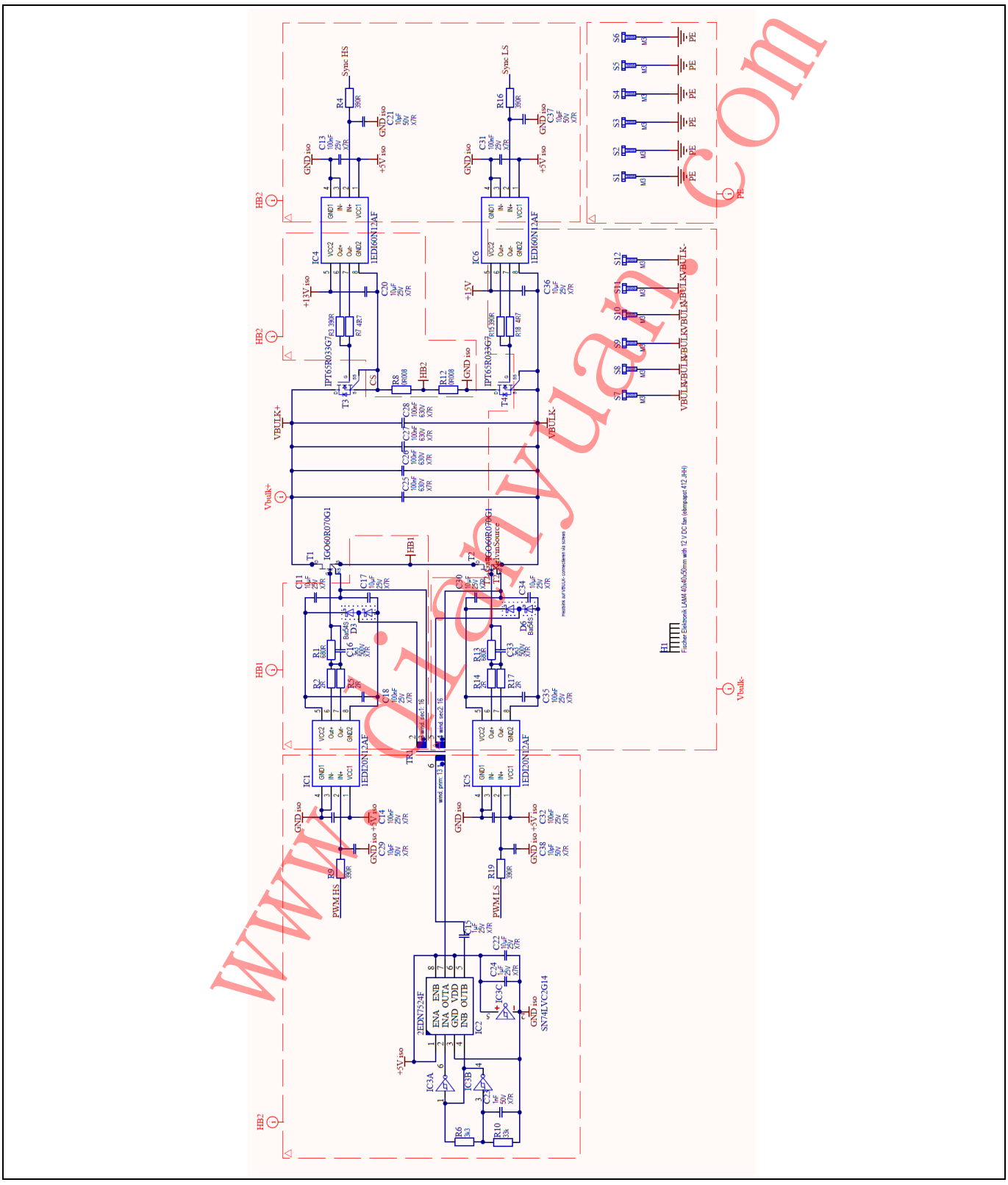

Figure 37 CCM totem pole PFC topology power section

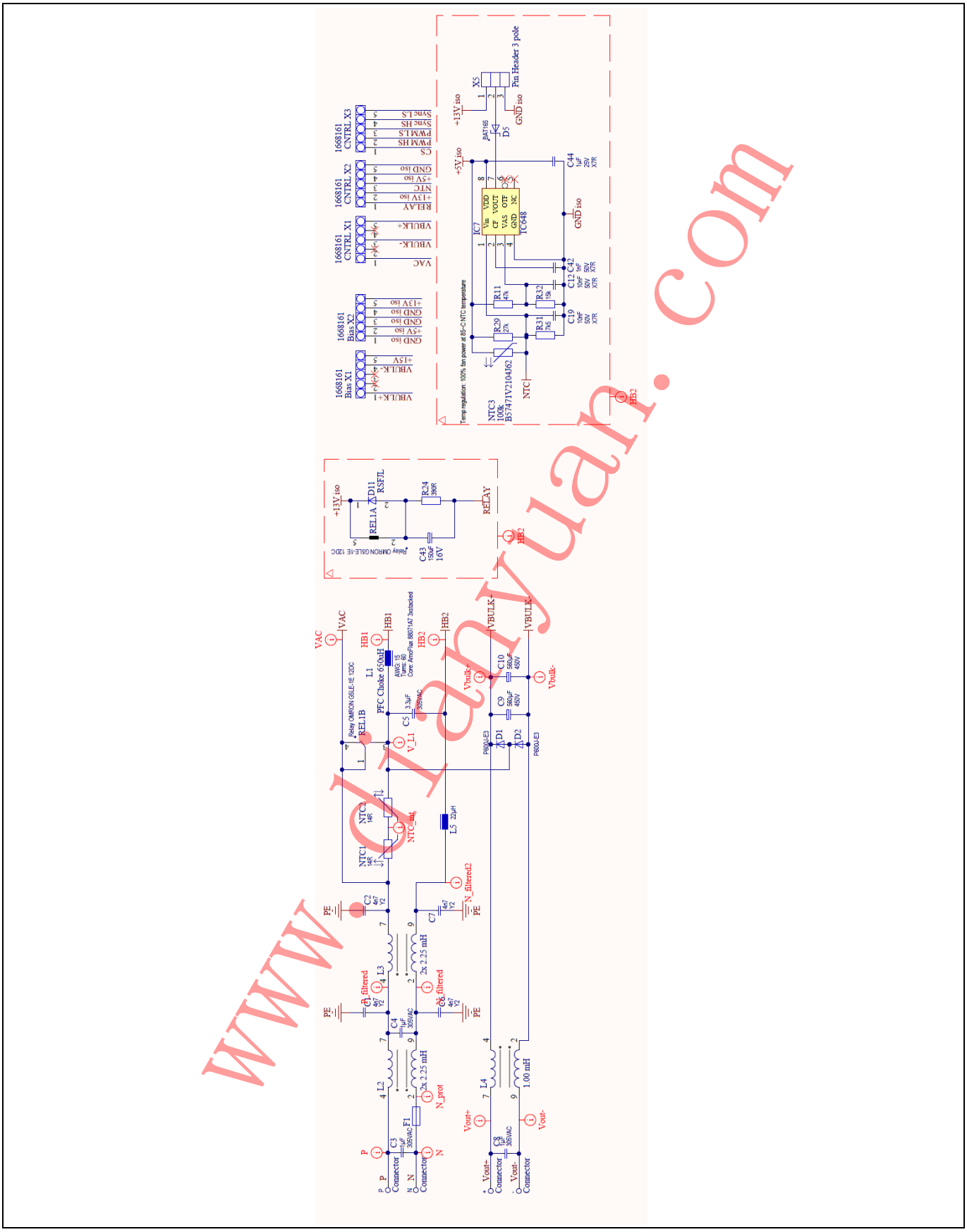

Figure 38 EMI filter and protections as well as heat sink temperature control

5.1 Schematics of the auxiliary supply daughter board

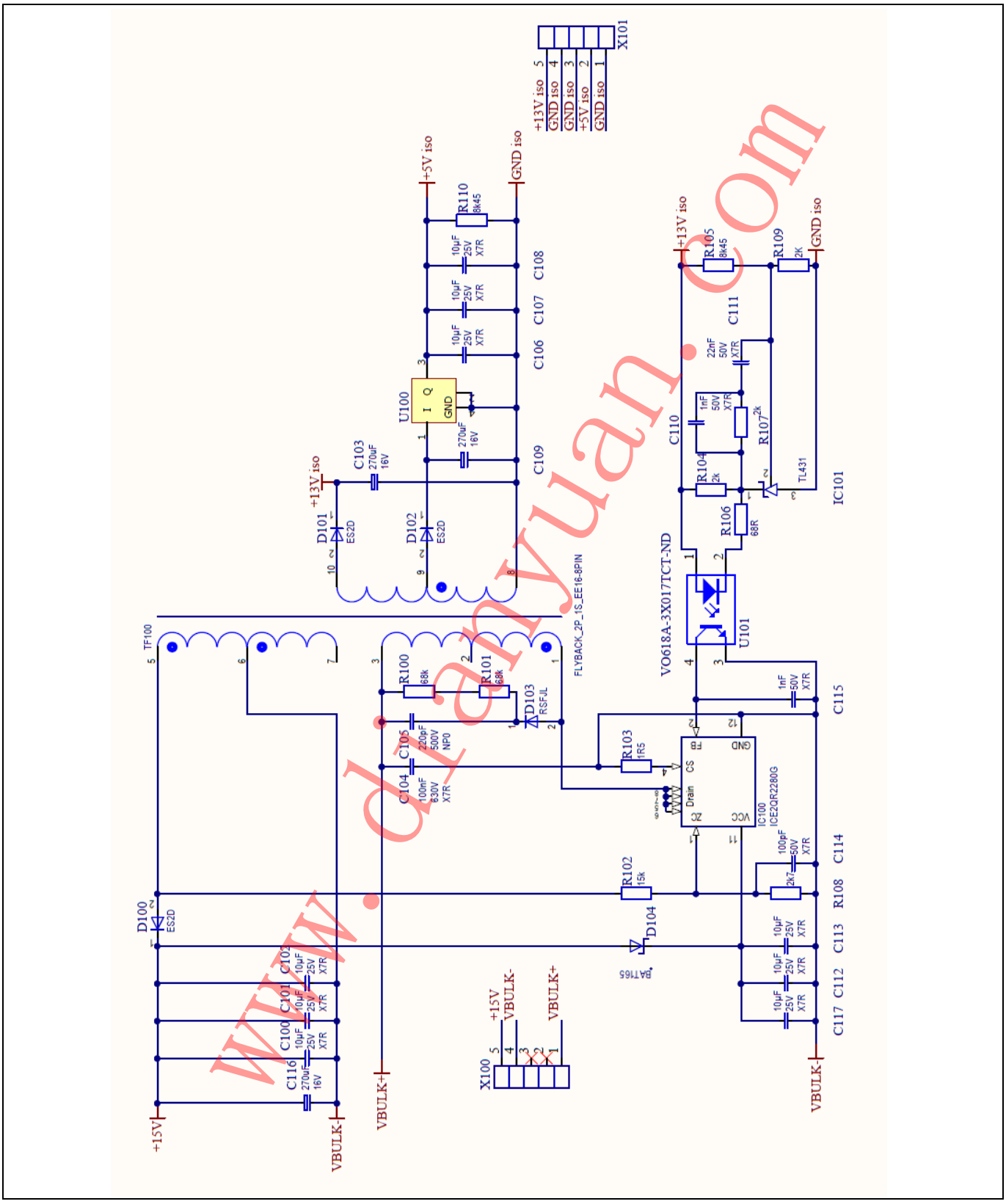

Figure 39 Auxiliary suppy

5.2 Schematics of the control board

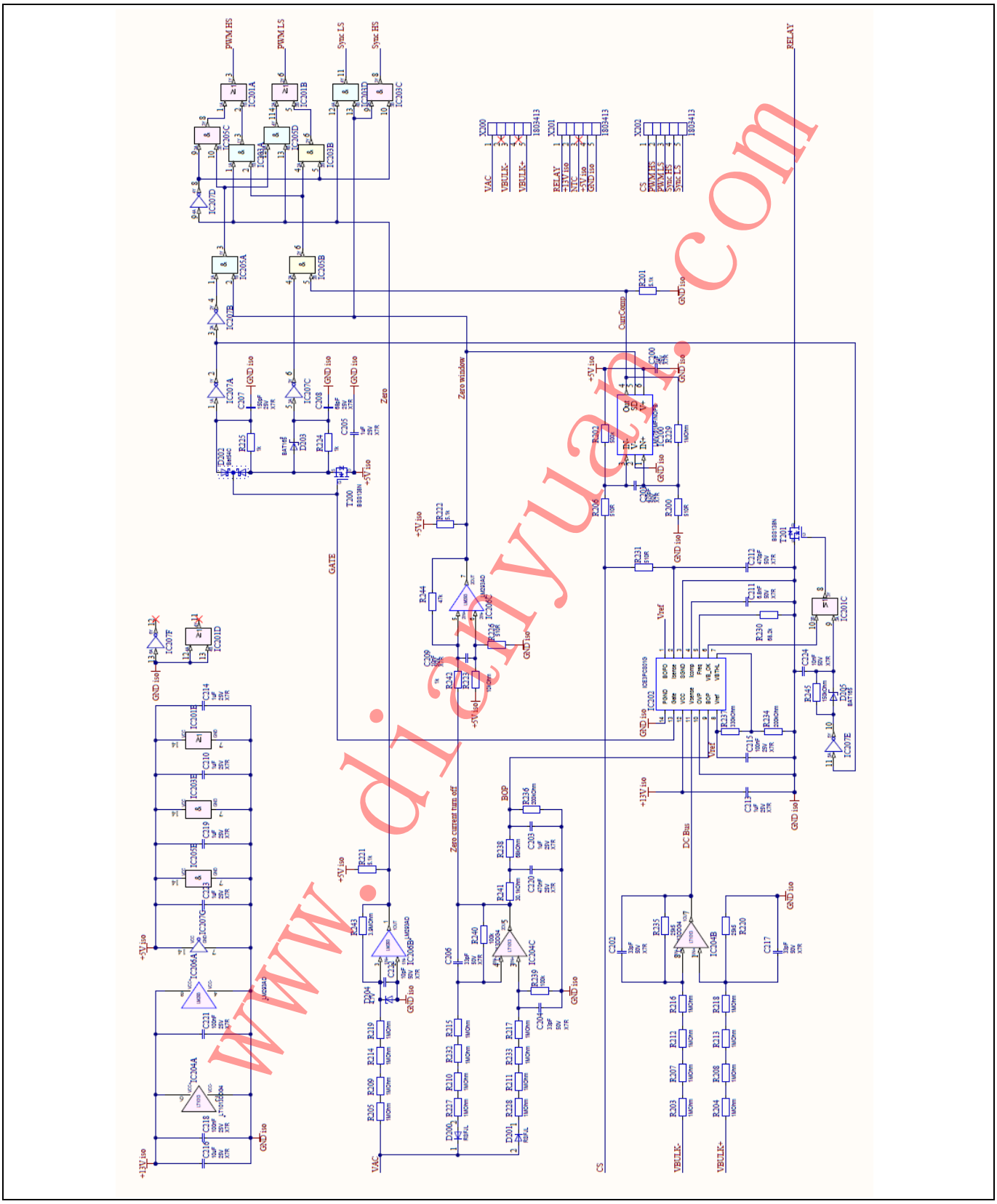

Figure 40 Control circuitry

5.3 Bill of Materials (BOM)

5.3.1 Main board

Part	Value	QTY	Voltage	Package	Description	Manufacturer	Supplier	Part number
C25, C26	100 nF	2	630 V	CAP1808R	Ceramic capacitor		Mouser	80-C1808C104KBRACTU
C27, C28	100 nF	2	630 V	CAP1812R	Ceramic capacitor		Farnell	1838753
C1, C2, C6	4n7	3	300 V	C foil capacitor 10 mm grid	Foil capacitor		Farnell	1166531
C12, C19	10 nF	2	50 V	CAP0805-IFX	Ceramic capacitor	AVX	Farnell	1740669
C16, C33	3n3	2	500 V	CAP0805-IFX	Ceramic capacitor	KEMET	Farnell	1702127
C9, C10	560 µF	2	450 V	C aluminum electrolytic 10 mm	Electrolytic capacitor	Panasonic Electronic Components	Digi-Key	P14904-ND
D1, D2	D_P600	2		D_P600	Diode	Vishay General Semiconductor	Farnell	1702801
NTC1, NTC2	14 R	2		R_SL22	NTC resistor	Ametherm	Digi-Key	570-1039-ND
R8, R12	0R008	2		RES1206R	Resistor	Welwyn	Farnell	1621974RL
C43	150 µF	1	16 V	CAP Panasonic SP-Cap	Ceramic capacitor		Farnell	2354978
C7	4n7	1	300 V	C foil capacitor 10 mm grid	Foil capacitor		Farnell	1166531
D11	RSFJL	1		SMA_SUB	Diode		Farnell	1559145RL
D5	BAT165	1		SOD323	Schottky diode	Infineon Technologies	Farnell	1056502
IC3	SN74LVC2G14	1		SOT23-6	Dual Schmitt trigger inverter	Texas Instruments	Digi-Key	296-13010-2-ND
IC7	TC648	1		SOIC8	TC648 fan controller IC	Microchip	Digi-Key	TC648BEUA-ND
REL1	Relay OMRON G5LE-1E 12DC	1		REL_G5LE-1E 12DC	Relay OMRON G5LE-1E 12DC		Farnell	1333642
C11, C20, C22, C30, C34, C36	10 µF	6	25 V	CAP0805-IFX	Ceramic capacitor			
C13, C14, C18, C31, C32, C35	100 nF	6	25 V	CAP0805-IFX	Ceramic capacitor			
C15, C24	1 µF	2	25 V	CAP0805-IFX	Ceramic capacitor			
C17	10 uF	1	25 V	CAP0805-IFX	Ceramic capacitor			
C21, C29, C37, C38	10 pF	4	50 V	CAP0805-IFX	Ceramic capacitor			
C23, C42	1 nF	2	50 V	CAP0805-IFX	Ceramic capacitor			
C3, C8	1 µF	2	305 V AC	C foil 22.5 mm	Foil capacitor		Mouser	871-B32923C3105M
C4	1 µF	1	305 V AC	C foil 22.5 mm	Foil capacitor		Mouser	871-B32923C3105M
C44	1 µF	1	25 V	CAP0805-IFX	Ceramic capacitor			
C5	3.3 µF	1	305 V AC	C foil 27.5 mm	Foil capacitor		Mouser	871-B32924E3335M
D3, D6	BAT54-04	2		SOT23R	Dual small-signal Schottky diodes	Infineon Technologies	Mouser	771-BAT54S-T/R
F1	Fuse holder	1	250 V AC	Fuse holder 5 x 20	Fuse holder – 22 mm x 9 mm for a 5 mm x 20 mm fuse		Mouser	693-0031.8201
IC1, IC5	1EDI20N12AF	2		SO8	2 A single-channel MOSFET gate-driver IC	Infineon Technologies	Infineon Technologies	1EDI20N12AF

IC2	2EDN7524F	1		SOIC127P600X175-8N-2	5 A dual-channel low-side HV MOSFET driver	Infineon Technologies	Infineon Technologies	2EDN7524F
IC4, IC6	1EDI60N12AF	2		SO8	6 A single-channel MOSFET gate-driver IC	Infineon Technologies	Infineon Technologies	1EDI60N12AF
NTC3	100 k	1		PTC 0805	NTC resistor	EPCOS	Mouser	871-B57471V2104J62
R1, R13	680 R	2		RES0805-IFX	Resistor			
R10	33 k	1		RES0805-IFX	Resistor			
R11	47 k	1		RES0805-IFX	Resistor			
R2, R5, R14, R17	2 R	4		RES0805-IFX	Resistor			
R29	27 k	1		RES0805-IFX	Resistor			
R3, R4, R9, R15, R16, R19, R24	390 R	7		RES0805-IFX	Resistor			
R31	7k5	1		RES0805-IFX	Resistor			
R32	15 k	1		RES0805-IFX	Resistor			
R6	3k3	1		RES0805-IFX	Resistor			
R7, R18	4R7	2		RES0805-IFX	Resistor			
T1, T2	IGO60R070D1	2		P/PG-DSO-20	600 V GaN power transistor 70 mΩ	Infineon Technologies	Infineon Technologies	
T3, T4	IPT65R033G7	2		HSOF-8-2	n-MOSFET with source sense	Infineon Technologies	Infineon Technologies	IPT65R033C7
Fuse	15 A 250 V T	1	250 V AC	5 mm x 20 mm	Anti-surge T LBC min fuse, 15 A 5 x 20 mm		RS Components	541-4599
Magnetics:								
L1	650 µH	1		Inductor AmoFlux – V2	Inductor	ICE Transformers	ICE Transformers	8024.3301.028
TR1		1		Transformer Ferroxcube	Pulse transformer	ICE Transformers	ICE Transformers	8034.0103.014
L2, L3	1 mH	2		Inductor WE-CMBNC	THT CM power line choke, WE-CMB, L = 1.00 mH	Würth Elektronik eiSos GmbH	Farnell	1636292
L4	1 mH	1		Inductor WE-CMB L	THT CM power line choke, WE-CMB, L = 1.00 mH	Würth Elektronik eiSos GmbH	Farnell	1636292
L5	22 µH	1		Inductor Bourns 2305-V-RC	Inductor	Bourns Inc.	Digi-Key	M8881-ND
Mechanical:								
H1	Fischer Elektronik LAM4 40mm x 40 mm x 50 mm with 12 V DC fan (ebmpapst 412 JHH)	1		Heatsink Fischer Elektronik	Heatsink with integrated 12 V fan		Fischer Elektronik	
X5		1		Pin header 3c single – vertical	Pin header, three contacts, 2.54 mm			
S1, S2	M3	2			Do not assemble!			

S7, S8, S9, S10, S11, S12	M3 screws	6		M3	Hex socket button steel-bright zinc-plated socket screw, M3 x 10 mm for heatsink mounting, add M3 metal washers between screws and PCB		RS Components	483-9559
S3, S4, S5	M3 spacers	3		M3	Spacer bottom: HTSN-M3-15-6-1, 15 mm high nylon-threaded hex spacer 6 mm wide for M3 thread spacers top: two pieces of "HTSN-M3-25-6-2, 25 mm high nylon-threaded hex spacer 6 mm wide with 8 mm bolt length for M3 thread" connected to achieve an overall stand-off of 50 mm		RS Components	102-6378 102-6542
S6	M3 spacers	2		M3	Spacer bottom: HTSN-M3-15-6-1, 15 mm high nylon-threaded hex spacer 6 mm wide for M3 thread spacer top: 2x "HTSN-M3-10-6-2, 10 mm high nylon-threaded hex spacer 6 mm wide with 8 mm bolt length for M3 thread"		RS Components	102-6378 102-6508
Insulation material	Sil-PAD 1500ST	1		Foil	Self-adhesive fiberglass thermal gap pad, 1.8 W/m·K, 10 x 12 in	Bergquist	RS Components	127-063

5.3.1 Auxillary supply daughter board

Designator	value	QTY	Tolerance	Voltage	Footprint	Description	Manufacturer	Supplier 1	Supplier Part Number 1
C100, C101, C102, C106, C107, C108, C112, C113, C117	10µF	9	±1%	25V	CAP0805-IFX	Capacitor Ceramic			
C103, C109	270uF	2	±1%	16V	C_POL_SMD_6.3	Capacitor Electrolyt	Panasonic, Panasonic Electronic Components	Mouser, Digi-Key	667-16SVPG270M, PCE5081CT-ND
C104	100nF	1	±1%	630V	CAP1812R	Capacitor Ceramic	AVX	Farnell	1838753
C105	220pF	1	±1%	500V	CAP1206R	Capacitor Ceramic	AVX	Farnell	1216450
C110, C115	1nF	2	±1%	50V	CAP0805-IFX	Capacitor Ceramic			
C111	22nF	1	±1%	50V	CAP0805-IFX	Capacitor Ceramic			
C114	100pF	1	±1%	50V	CAP0805-IFX	Capacitor Ceramic			
D100, D101, D102		3			SMB / DO-214AA	Diode	FAIRCHILD SEMICONDUCTOR	Farnell	1467491
D103		1			SMA_SUB	Diode	TAIWAN SEMICONDUCTOR	Farnell	1559145RL
D104	BAT165	1			SOD323	Schottky-Diode	Infineon Technologies	Mouser	726-BAT165E6327
IC100	ICE2QR2280G	1			PG-DSO-12	CoolSET® - Q1	Infineon Technologies	Mouser	726-ICE2QR2280GXUMA1
IC101	TL431	1			SOT23R	TL431- Adjustable Precision Shunt Regulator	Texas Instruments	Digi-Key	296-17328-2-ND
R100, R101	68k	2	±1%		RES1206R	Resistor			
R102	15k	1	±1%		RES0805-IFX	Resistor			

R103	1R5	1	±1%		RES1206R	Resistor			
R104, R107, R109	2k	3	±1%		RES0805-IFX	Resistor			
R105, R110	8k45	2	±1%		RES0805-IFX	Resistor			
R106	68R	1	±1%		RES0805-IFX	Resistor			
R108	2k7	1	±1%		RES0805-IFX	Resistor			
TF100	FLYBACK_2P_1S_EE16-8PIN	1			EE16 THT Bobbin	Magentic	ICEtransformers	ICEtransformers	8032.0205.012
U100	TLE4264-2G	1			SOT-223-4	5 V Low Drop Fixed Voltage Regulator, 5.5 to 45 V Supply, -40 to 150 degC, PG-SOT223 (SC-73), Reel, Green	Infineon Technologies	Mouser	726-TLE42642GHTSA2
U101	Optocoupler	1			DIL-4-SMD	Optocoupler	Vishay Semiconductor Opto Division	Digi-Key	VO618A-3X017TCT-ND
X100, X101	Pin Header 5 contacts	2			PIN Header 5C Single-2mm - THT	SAMTEC TMM-105-01-L-S-RA Board-To-Board Connector, Right Angle (abgewinkelt), TMM Series, Through Hole, Header, 5, 2 mm	SAMTEC	Farnell	1803413

5.3.2 Controller daughter board

Designator	value	QTY	Tolerance	Voltage	Footprint	Description	Manufacturer	Supplier 1	Supplier Part Number 1
C200, C203, C205, C210, C213, C214, C219, C223	1uF	8	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C201, C212	470pF	2	±1%	50V	CAP0805-IFX	Capacitor ceramic			
C202, C204, C206, C217	33pF	4	±1%	50V	CAP0805-IFX	Capacitor ceramic			
C207	150pF	1	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C208	68pF	1	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C209, C224	10nF	2	±1%	50V	CAP0805-IFX	Capacitor ceramic			
C211	6.8nF	1	±1%	50V	CAP0805-IFX	Capacitor ceramic			
C215, C218, C221	100nF	3	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C216	10uF	1	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C220	470nF	1	±1%	25V	CAP0805-IFX	Capacitor ceramic			
C222	10pF	1	±1%	50V	CAP0805-	Capacitor ceramic			

					IFX				
D200, D201		2			SMA_SUB	Diode	TAIWAN SEMICONDUCTOR	Farnell	1559145RL
D202	Bat54C	1			SOT23_N		Infineon Technologies	Mouser	726-BAT54E6327
D203, D205	BAT165	2			SOD323	Schottky diode	Infineon Technologies	Mouser	726-BAT165E6327
D204		1		4.7V	SOD323	Zener diode	ROHM	Farnell	1680099RL
IC200		1			SOT23-6	Low voltage, precision comparator with push-pull output	TEXAS INSTRUMENTS	Farnell	2147763
IC201	SN74AC32PW	1			SO14 - wide	TEXAS INSTRUMENTS - SN74AC32PW - LOGIK QUAD 2IN POS-ODER GATE 14TSSOP	Texas Instruments	Digi-Key	296-33645-5-ND
IC202	ICE3PCS01G	1			PG-DSO-14	CCM_PFC_Controller_Standalone	Infineon Technologies	Mouser	ICE3PCS01GXUMA1
IC203, IC205	SN74AC08PW	2			SO14 - wide	TEXAS INSTRUMENTS - SN74AC08PW - LOGIK,QUAD 2IN POS-UND GATE,14TSSOP	Texas Instruments	Mouser	595-SN74AC08PW
IC204	LT1013DDG4	1			SO8	TEXAS INSTRUMENTS - LT1013DDG4 - OP AMP,DUAL PRAEZISION, 1013, SOIC8	TEXAS INSTRUMENTS	Farnell	9589759
IC206	LM293AD	1			SO8	TEXAS INSTRUMENTS - LM293AD - KOMPARATOR DUAL,SMD SOIC8, 293	Texas Instruments	Digi-Key	296-26090-1-ND
IC207		1			SO14 - wide	TEXAS INSTRUMENTS - SN74AC04PW - LOGIK, HEX INVERTER, 14TSSOP	TEXAS INSTRUMENTS	Farnell	1741166
R200	510R	1	±1%		RES0805-IFX	Resistor			
R201, R221, R222	5.1k	3	±1%		RES0805-IFX	Resistor			
R202	500k	1	±1%		RES0805-IFX	Resistor			
R203, R204, R205, R209, R210, R211, R212, R213, R214, R216, R218, R227, R228, R229, R232, R233	1MOhm	16	±1%		RES0805-IFX	Resistor			

R206, R226, R231	510R	3	±1%		RES0805-IFX	Resistor			
R207, R208, R215, R217, R219	1MOhm	5	±1%		RES0805-IFX	Resistor			
R220, R235	25k5	2	±1%		RES0805-IFX	Resistor	Vishay / Dale	Mouser	71-CRCW0805-25.5K-E3
R223	10kOhm	1	±1%		RES0805-IFX	Resistor			
R224, R225, R242	1k	3	±1%		RES0805-IFX	Resistor			
R230	68.2k	1	±1%		RES0805-IFX	Resistor			
R234, R236	200kOhm	2	±1%		RES0805-IFX	Resistor			
R237	330kOhm	1	±1%		RES0805-IFX	Resistor			
R238	68kOhm	1	±1%		RES0805-IFX	Resistor			
R239, R240	100k	2	±1%		RES0805-IFX	Resistor			
R241	30.1kOhm	1	±1%		RES0805-IFX	Resistor	VISHAY DRALORIC	Farnell	1652981
R243	3.9MOhm	1	±1%		RES0805-IFX	Resistor			
R244	47k	1	±1%		RES0805-IFX	Resistor			
R245	150kOhm	1	±1%		RES0805-IFX	Resistor			
T200, T201	BSS138N	2			SOT-23-3	NMOS FET	Infineon Technologies	Mouser	726-BSS138NH6327
X200, X201, X202		3			PIN Header 5C Single-2mm - THT	SAMTEC TMM-105-01-L-S-RA Board-To-Board Connector, Right Angle (abgewinkelt), TMM Series, Through Hole, Header, 5, 2 mm	SAMTEC	Farnell	1803413

5.4 Abbreviations

SMPS	Switched Mode Power Supply
PFC	Power Factor Correction

HV	High Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GaN	Gallium nitride
CCM PFC	Continuous Current Mode Power Factor Correction
$R_{DS(ON)}$	Drain source on-state resistance
V_{in}	Input voltage
V_{out}	Output voltage
P_{out}	Output power
f_{sw}	Switching frequency
$t_{ambient}$	Ambient temperature
EMI	Electro-Magnetic Interference
CS	Current Sense
HB1	Half-Bridge point 1 (boost stage)
HB2	Half-Bridge point 2 (synchronous grid rectification)
V_{BULK+}	Bulk voltage positive rail
V_{BULK-}	Bulk voltage negative rail
PTC	Positive Temperature Coefficient
ISO	Isolated
GND	Ground
LS	Low-Side
HS	High-Side
n.c.	Not Connected
V_{CS}	Voltage on current sense
R_{shunt}	Resistive shunt for current sensing
DSP	Digital Signal Processor
PWM	Pulse Width Modulated
QR flyback	Quasi Resonant flyback
DCM	Discontinuous Current Mode
R_{th}	Thermal resistance
SMD	Surface Mount Device
PCB	Printed Circuit Board
TIM	Thermal Interface Material/Thermal Insulation Material
CMRR	Common Mode Rejection Ratio
ACLCDO	AC-Line Cycle Drop-Out

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7 Revision history

Major changes since the last revision

Page or reference	Description of change
Rev 1.1	Modified first page, corrected product name of GaN HEMT in BOM, added more information about current sensing concept, added BOM of daughter cards, added more description about control daughter card

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