Application Report
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350-W, Two-Phase Interleaved PFC Pre-Regulator Design Review

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1 Abstract

In higher power applications to utilize the full line power and reduce line current harmonics PFC pre-regulators are generally required. In these high power applications interleaving PFC stages can reduce inductor area and reduce output capacitor ripple current. This is made possible through the inductor ripple current cancellation that occurs with interleaving. This application note reviews the design of a 350-W two phase interleaved power factor corrected (PFC) pre-regulator. This power converter achieves PFC with the use of the UCC28528 PFC/PWM controller along with the UCC28220 interleaved PWM controller that is used to interleave the two power stages. The converter also has a 2-W auxiliary bias supply that supplies power to the converters gate drive and PWM/PFC circuitry. The complete schematic of the working design is shown in Figure 7 and Figure 8.

2 Review the Benefits of Interleaving PFC Boost Pre-Regulators

Figure 1 shows the functional diagram of a two phase interleaved boost converter. The interleaved boost converter is simply two boost converters operating 180 degrees out of phase. The input current is the sum of the two inductor currents IL1 and IL2. Because the inductor's ripple currents are out of phase, they cancel each other out and reduce the input ripple current caused by the boost inductors. The best input inductor ripple current cancellation occurs at 50% duty cycle. The output capacitor current is the sum of the two diode currents (I1 + I2) less the dc output current. This reduces the output capacitor ripple current (I_{OUT}) as a function of duty cycle. As the duty cycle approaches 0%, 50% and 100% duty cycle, the sum of the two diode currents approaches dc. At any of these optimum operating points, the output capacitor only has to filter the inductor ripple currents.

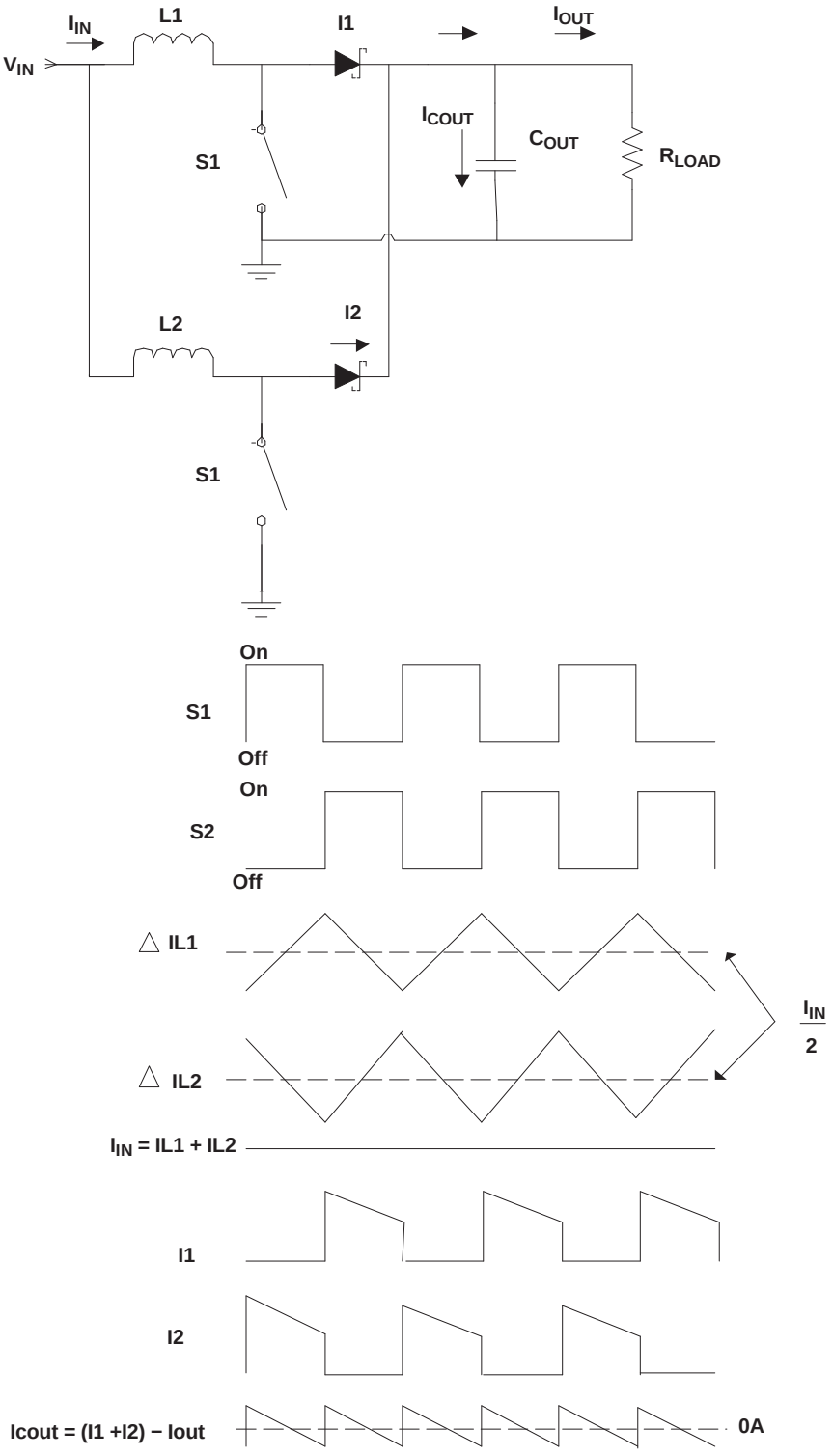

Figure 1. Interleaved Boost Stage

2.1 Input Ripple Current Reduction as a Function of Duty Cycle

The following equations show how the ratio of input ripple current to inductor ripple current (K(D)) vary with changes in duty cycle. Figure 2 shows how K(D) varies with changes in duty cycle. It's important to remember these variations in input ripple current, when selecting inductors for the interleaved boost converters. This is because the duty cycle in PFC pre-regulator is not fixed and changes with line voltage.

$$K(D) = \frac{\Delta I_{IN}}{\Delta IL1} \quad (1)$$

$$K(D) = \frac{1 - 2D}{1 - D} \text{ if } D \leq 0.5 \quad (2)$$

$$K(D) = \frac{2D - 1}{D} \text{ if } D > 0.5 \quad (3)$$

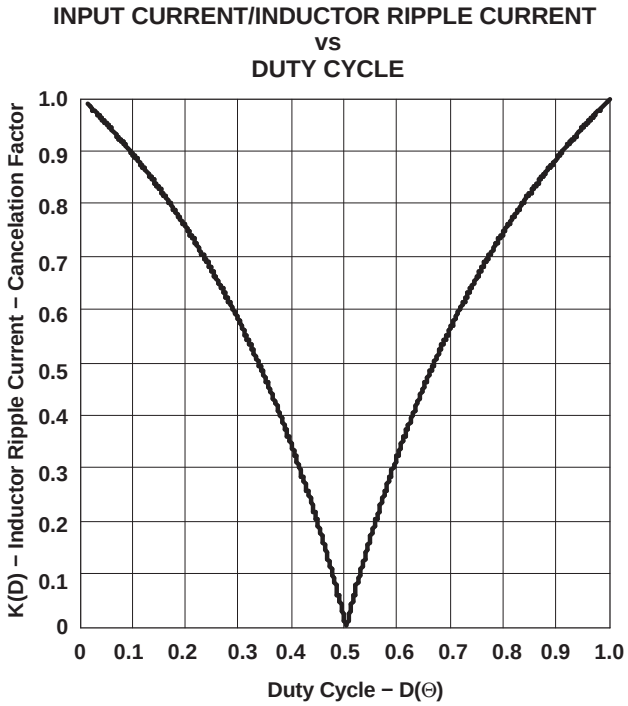

Figure 2. Input Ripple Current Reduction

In PFC pre-regulators the duty cycle (D(θ)) is not constant and varies with changes in line voltage (Vin(θ)). The amount of duty cycle variation for universal applications can be quite large. This variation in duty cycle can be observed by evaluating a converter that was designed for a universal input of 85 V to 265 V with a regulated 385 V dc output. At low line the duty cycle (D1(θ)) varies from 100% to 68% and at high line the duty cycle (D2(θ)) varies from 100% down to 2%. The inductor ripple current cancellation will not be 100% throughout the line cycle. However, it is good enough to drastically reduce the input ripple current for a given inductance. The highest ripple current in this example would occur at the peak of low line with a duty cycle of 68%. The amount of inductor ripple current seen at the input for this duty cycle would be 55%.

$V_{IN}(\Theta) = V_{IN(rms)} \times \sqrt{2}\sin(\Theta)$ line voltage as a function of phase angle. (4)

$$D(\Theta) = \frac{V_{OUT} - V_{IN}(\Theta)}{V_{OUT}}$$ duty cycle as function of phase angle (5)

where $\omega = 2\ \pi\ f_{LINE}$

and $\theta = \omega\tau$

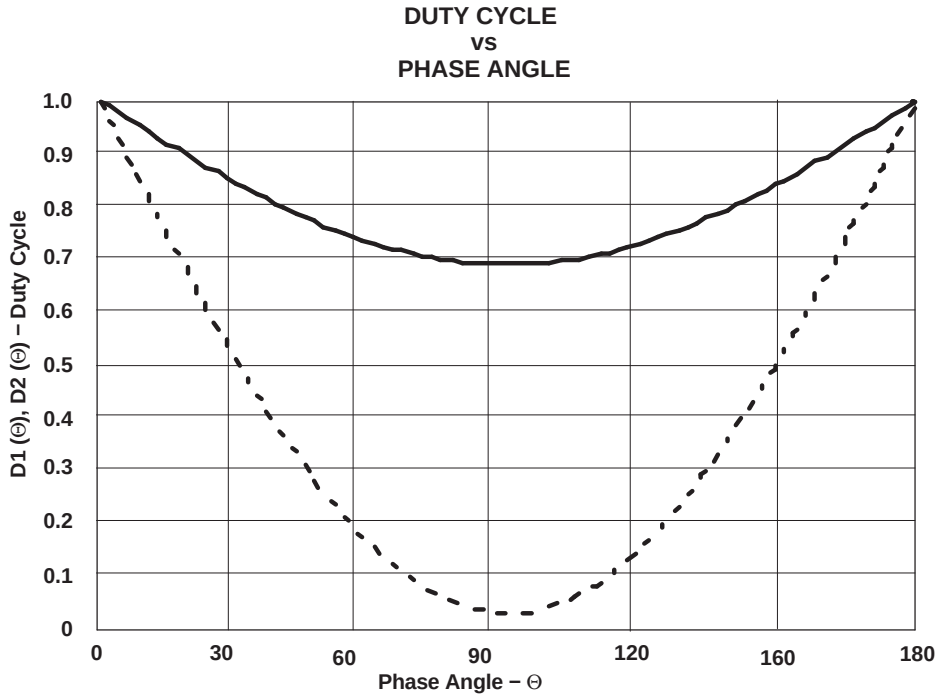

Figure 3. Duty Cycle Variation in Universal PFC Pre-Regulator

2.2 Evaluate Magnetic Volume Reduction

The inductor ripple current cancellation allows the designer to reduce boost inductor magnetic volume. This is due to the energy storage requirement of the two interleaved inductors being half that of single stage pre-regulator designed for the same power level, switching frequency and inductance.

$$E_{SINGLE} = \frac{1}{2}LI^2 \text{ single stage inductor energy.} \quad (6)$$

$$E_{INTERLEAVED} = \frac{1}{2}L\left(\frac{I}{2}\right)^2 + \frac{1}{2}L\left(\frac{I}{2}\right)^2 = \frac{1}{4}LI^2 \text{ two phase total inductor energy.} \quad (7)$$

The amount of reduction in boost inductor volume can be seen mathematically by comparing the required inductor area products of single stage PFC pre-regulator ($WaAc_{SINGLE}$) with that of a two phase interleaved pre-regulator inductor ($WaAc_{INTERLEAVED}$) for a given inductance. The exact values for the inductor (L), inductor RMS current (I_{RMS}), current density (C_D) and flux density (B) are not required to show the reduction in area product.

$$I_{PEAK} = \frac{P_{OUT(max)} \times \sqrt{2}}{V_{IN(min)}} \quad (8)$$

$$WaAc_{SINGLE} = \frac{L \times I_{PEAK}}{B} \times \frac{I_{RMS}}{C_D} = \frac{L \times I_{PEAK}}{B} \times \frac{\frac{I_{PEAK}}{\sqrt{2}}}{C_D} \quad (9)$$

$$WaAc_{INTERLEAVED} = \frac{L \times \frac{I_{PEAK}}{2}}{B} \times \frac{\frac{I_{PEAK}}{2 \times \sqrt{2}}}{C_D} \quad (10)$$

The ratio of the total interleaved area product (2 X $WaAc_{INTERLEAVED}$) to the area product of a single stage pre-regulator is 0.5. This results in a 50% reduction in area product just by interleaving, which will result in a substantial reduction in boost magnetic volume.

$$\frac{2 \times WaAc_{INTERLEAVED}}{WaAc_{SINGLE}} = \frac{1}{2} \tag{11}$$

Interleaving PFC pre-regulators if done in this fashion will not increase the size of the EMI filter. A common design practice is to select the switching frequency of the power converter below the EMI band of 150 kHz. The second harmonic of switching frequency would be twice the fundamental and will most likely be in the EMI band and would need to be filtered to meet specifications. Interleaving two pre-regulators causes the input to see a switching frequency that is twice the switching frequency of a single phase. This means the fundamental switching frequency of the converter will most likely be pushed into the EMI band and be at the second harmonic of an individual stage's switching frequency. However, the input ripple current is reduced by a factor of two. This should not put any additional constraints on the EMI filter.

2.3 Output Capacitor Ripple Current Reductions as a Function of Duty Cycle

Figure 4 shows the normalized output capacitor RMS current in a single stage boost ($I_{COUT(single)}(D)$) and the normalized capacitor RMS current in a two phase interleaved boost converter ($I_{COUT}(D)$) as a function of duty cycle. Figure 4 illustrates that the output capacitor ripple current in a two phase interleaved is half that in a traditional single stage boost converter for the same power levels. The reduction in RMS current reduces heating caused by the capacitor's ESR losses, reducing electrical stress.

$$I_{COUT(single)}(D) = \sqrt{(1 - D) \times [1 - (1 - D)]} \tag{12}$$

$$I_{COUT}(D) = \frac{1}{2}\sqrt{(1 - 2D) - (1 - 2D)^2} \text{ if } D < 0.5 \tag{13}$$

$$I_{COUT}(D) = \frac{1}{2}\sqrt{(2 - 2D) - (2 - 2D)^2} \text{ if } D \geq 0.5 \tag{14}$$

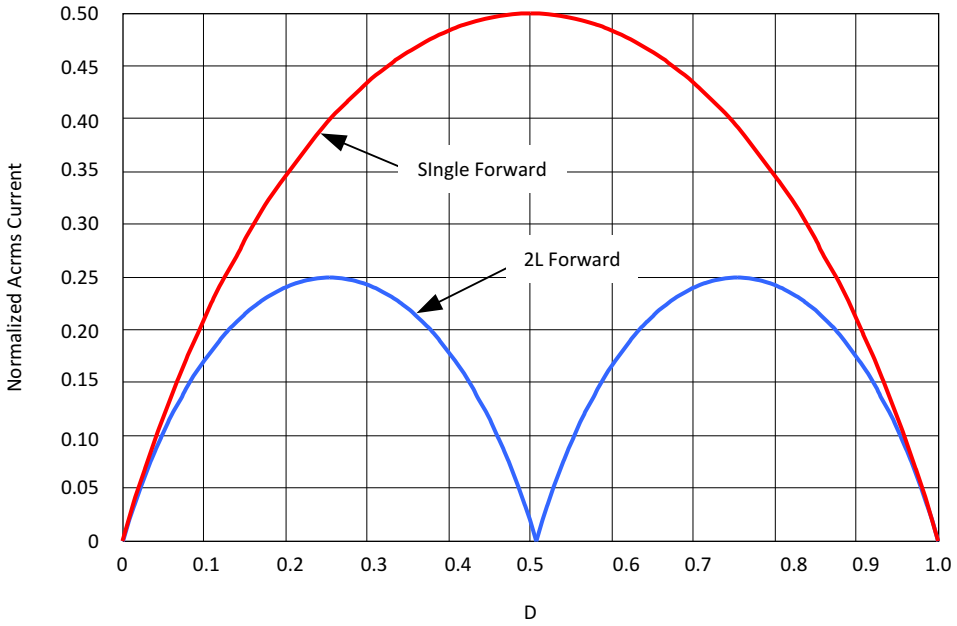

Figure 4. Normalized Output Capacitor Ripple Currents

3 Design Review

The power supply design requirements are presented in Table 1. Please note this 350-W PFC pre-regulator design is based on a TI evaluation module HPA117, TI User's Guide Literature number SLUU228, which is orderable through TI. Please visit www.ti.com for details. Also note that the design presented in this application note is based on typical values. In a production environment a worst case analysis would have to be conducted.

Table 1. Design Requirements

PARAMETER	MIN	TYP	MAX
V_{IN}	85 V RMS	110 V or 230 V RMS	265 V RMS
V_{OUT}	374 V	390 V	425 V
V_{RIPPLE}			30 V
Current THD at 350 W			10%
PF at 350 W	0.95		
Full load efficiency	90%		
f_S		100 kHz	
Holdup requirements (t_{HOLD})			20 ms
f_{LINE}	47 Hz	50 Hz	60 Hz

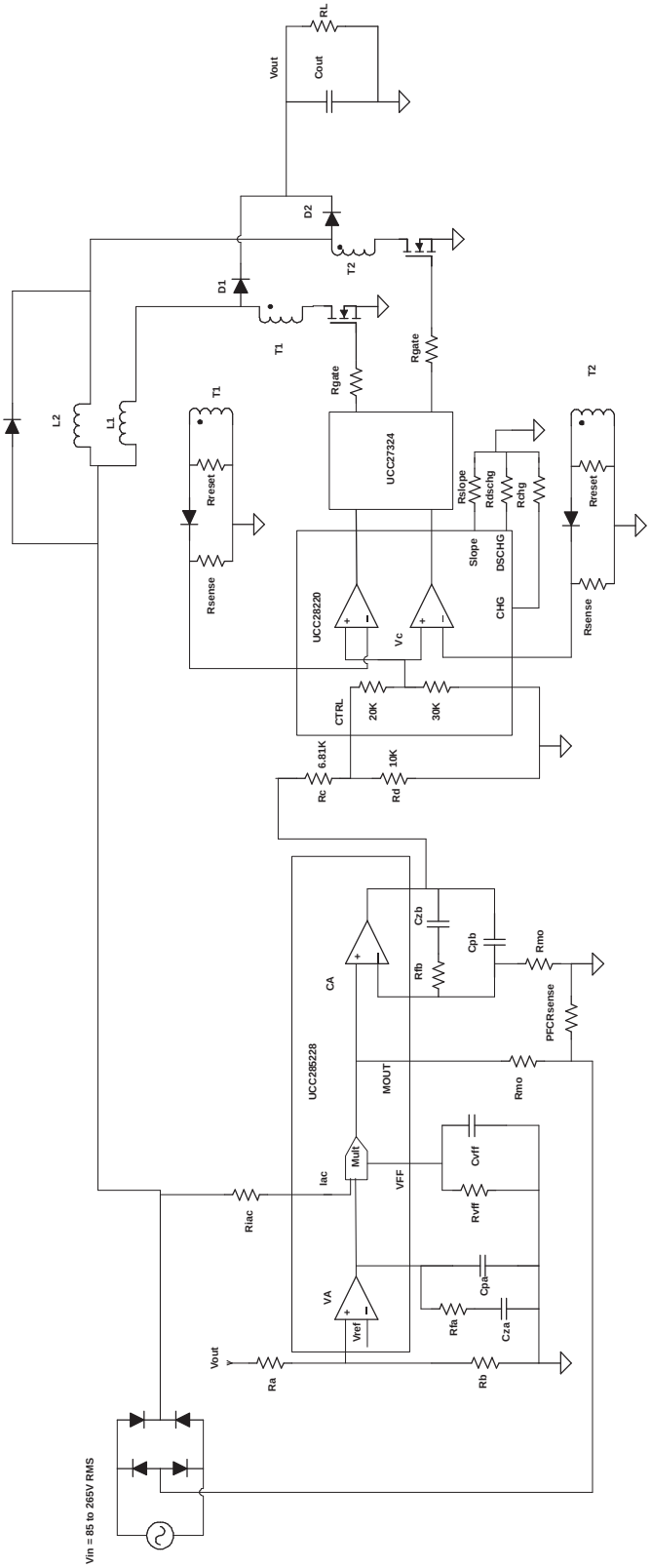

Figure 5. Functional Schematic

3.1 Boost Inductor Selection

Cooper Electronics designed the 200 µH, CTX16-17309, boost Inductors for our design.

$$L1 = L2 = \frac{V_{IN(min)} \times \sqrt{2} \times D_{MIN(LL)}}{\Delta IL \times f_S} = \frac{85\ V \times \sqrt{2} \times 0.69}{4.1\ A \times 100\ kHz} \approx 200\ \mu H \quad (15)$$

3.2 Output Capacitor Selection (C_{OUT})

There are three determining criteria for selecting the output capacitor. They are holdup energy, output ripple voltage and lastly RMS ripple current. Equation 16 and Equation 17 are used to select the output capacitor. Equation 16 selects the output capacitor based on holdup requirements, while Equation 17 sizes capacitance base on output voltage (V_{RIPPLE}) requirements. The designer should select the largest result of Equation 16 and Equation 17 for the design.

$$C_{OUT} \geq \frac{2 \times P_{OUT} \times \frac{1}{f_{LINE}}}{V_{OUT}^2 - \left(\frac{V_{OUT}}{2}\right)^2} \approx 123\ \mu F \quad (16)$$

$$C_{OUT} \geq \frac{1}{4} \times \frac{\frac{P_{OUT}}{V_{OUT} \times \eta \times 0.637}}{V_{RIPPLE} \times 0.8 \times \pi \times f_{LINE}} \approx 104\ \mu F \quad (17)$$

$$ESR_{MAX} = \frac{V_{RIPPLE} \times 0.2}{\frac{P_{OUT} \times \sqrt{2}}{V_{IN(min)} \times \eta}} \approx 1.3\ \Omega \quad (18)$$

The capacitor should also be de-rated based on capacitor tolerances. The following equation de-rates the output capacitor based on 20% error in capacitance tolerance and a 20% variation over the life of the capacitor.

$$C_{OUT} \geq \frac{C_{OUT}}{(1 - 0.2)(1 - 0.2)} \approx 220\ \mu H \quad (19)$$

The RMS ripple current for the boost capacitor can be calculated with the following equations. To use these equations it is a good idea to use MathCAD or MATLAB design tools.

$$Iterations = \frac{f_S}{2 \times f_{LINE}} \approx 1 \times 10^3 \quad (20)$$

$$Step = \frac{\left[\frac{1}{f_{LINE}}\right]}{Iterations} \quad (21)$$

$$I_{IN(t)} = \frac{P_{OUT} \times \sqrt{2}}{V_{IN(min)}} \times \sin(\omega \times t) \quad (22)$$

$$I_{COUT(rms)} = \sqrt{\frac{\sum_{n=1}^{Iterations}\left[I_{IN}(n \times Step)^2\left[\frac{1}{2}\sqrt{(2 - 2 \times D1(n \times Step)) - (2 - 2 \times D1(n \times Step))^2}\right]^2\right]}{Iterations}} \approx 1\ A \quad (23)$$

3.3 FET and Diode Selection

To meet the efficiency requirements (η) of the design a power budget (P_{SEMI}) of 19 W was set. Selecting these semiconductor devices are always trial an error. It may take several tries before the appropriate semi conductor devices can be chosen for the design.

$$P_{SEMI} = \left(\frac{P_{OUT}}{\eta} - P_{OUT}\right) \times 0.5 \approx 19\ W \tag{24}$$

3.4 Diode Selection

To reduce switching losses CREE CSD10060 SiC rectifiers were used. These diodes have close to zero reverse recovery current. The following equation is used to estimate the diode loss (P_{DIODE}) and diode peak ($I_{DIODE(peak)}$) and average current (I_{DIODE}), where V_f is the forward voltage drop of the boost diode. These diodes in our design will dissipate around 0.6 W (P_{DIODE}) per diode dissipating a total of 1.2 W for both diodes in the design. This leaves 17.8 W of losses for the boost FETs and the auxiliary bias supply.

$$I_{DIODE} = \frac{P_{OUT}}{2 \times V_{OUT} \times \eta} \approx 2.3\ A \tag{25}$$

$$I_{DIODE(peak)} = \left(\frac{P_{OUT}\sqrt{2}}{2 \times V_{IN(min)} \times \eta} + \frac{\Delta IL1}{2}\right) \approx 5.3\ A \tag{26}$$

$$P_{DIODE} = \frac{P_{OUT} \times V_F}{2 \times V_{OUT} \times \eta} \approx 0.6\ W \tag{27}$$

3.5 FET Selection Based on RMS and Peak Currents and Estimated FET Losses

$$I_{PEAK} = \left(\frac{P_{OUT}\sqrt{2}}{2 \times V_{IN(min)} \times \eta} + \frac{\Delta IL1}{2}\right) \approx 5.3\ A$$, peak FET current. (28)

The following equation estimates FET RMS current ($I_{FET(rms)}$) which is needed to estimate boost FET (P_{FET}) losses.

$$I_{FET(rms)} = \sqrt{f_{LINE} \times \sum_{n=1}^{Iterations} \int_{O}^{\left[\frac{D1(n \times Step)}{f_S}\right]} \left(\frac{I_{IN}(n \times Step)}{2}\right)^2 dt} \tag{29}$$

$$I_{IN_{ton}}(t) = \left(\frac{P_{OUT} \times \sqrt{2}}{2 \times V_{IN(min)} \times \eta} - \frac{\Delta IL1}{2}\right) \sin(\omega \times t)$$, peak FET line currents ($I_{IN\ ton}$ (t)) at switch turn off. (30)

$$I_{IN_{toff}}(t) = \left(\frac{P_{OUT} \times \sqrt{2}}{2 \times V_{IN(min)} \times \eta} + \frac{\Delta IL1}{2}\right) \sin(\omega \times t)$$, peak FET line currents ($I_{IN\ toff}$ (t)) at switch turn off. (31)

Part of the total FET losses are contributed Coss ($C_{OSS(avg)}$) charging and discharging during a PWM switching cycle. C_{OSS} varies with line voltage and is not a linear function. The following equation and information from the FETs data sheet can be used to calculate $C_{OSS(avg)}$. $C_{OSS(spec)}$ is the typical C_{OSS} measured at a specified V_{DS} voltage ($V_{DS(spec)}$). A IRF840, 8 A 500 V FET was selected for the design. The estimated $C_{OSS(avg)}$ was roughly 160 pF.

$$C_{OSS(avg)} \approx 2 \times C_{OSS(spec)} \times \sqrt{\frac{V_{DS(spec)}}{V_{OUT}}} = 2 \times 310\ pF \times \sqrt{\frac{25\ V}{385\ V}} = 160\ pF \tag{32}$$

To estimate FET turn-on ($t_{ON(delay)}$) and turn off ($t_{OFF(delay)}$) delays requires studying the FETs V_{GS} versus Q_G characteristics of Figure 6 along with the following equations.

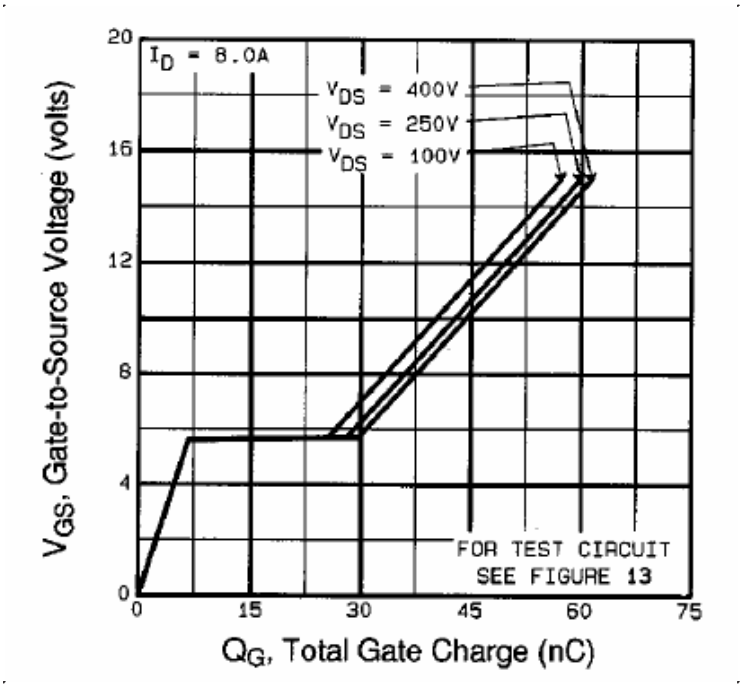

Figure 6.

$Q_{GS(miller)} = 30\ nC$, the typical maximum miller plateau gate charge for V_{DS} equal to 400 V. (33)

$Q_{GS(max)} = 52\ nC$

, is the amount of gate charge when the FET V_{GS} is at its maximum $V_{GS(max)}$. (34)

$$I_{GATE} = \frac{V_{GS(max)}}{2 \times R_{GATE}}$$, is average FET gate drive current. (35)

$$t_{ON(delay)} = t_{OFF(delay)} = \frac{Q_{GS(miller)}}{I_{GATE}}$$ (36)

$$P_{SWITCH(toff)} = f_{LINE} \sum_{n=1}^{Iterations} \left[I_{IN_{toff}}(n \times Step) \times V_{OUT} \times t_{OFF(delay)} \right]$$, switching losses at FET turnoff. (37)

$$P_{SWITCH(ton)} = f_{LINE} \sum_{n=1}^{Iterations} \left[I_{IN_{ton}}(n \times Step) \times V_{OUT} \times t_{ON(delay)} \right]$$, switching losses at FET turn-on. (38)

$$P_{COSS} = \frac{1}{2} \times C_{OSS} \times V_{OUT}^{2} \times f_S$$, C_{OSS} loss. (39)

$P_{GATE} = Q_{OFF} \times V_{GS(max)} \times f_S$, FET gate loss. (40)

$P_{RDS(on)} = I_{FET(rms)} \times R_{DS(on)}$, FET $R_{DS(on)}$ loss (41)

$P_{FET} = P_{SWITCH(toff)} + P_{SWITCH(ton)} + P_{COSS} + P_{GATE} + P_{RDS(on)} \approx 5\ W$ (42)

The estimated FET loss (P_{FET}) for this design was 5 W. The total FET loss would be 10 W and with the 1.2 W total diode loss comes to a total semiconductor loss of 11.2 W, which is below the 19 W power budget (P_{SEMI}) that was initially set.

3.6 Selecting Heat Sinks for the FETs

Because the diodes only dissipated 0.6 W heat sinks were not required for the boost diodes. However, the FETs required heat sinks and the following equation was used to calculate the thermal impedance ($R\theta_{SA}$) of the required heat sink. This equation is based on a maximum allowable ambient temperature (T_{AMB}) of 40°C, and the thermal impedance from junction to case $R\theta_{jc}$ of the IR840 and the case to sink thermal impedance of a TO220 ($R\theta_{CS}$) which all can be found in the IRF840's data sheet. For this design we chose an AAVID 531202 heat sink to meet the $R\theta_{SA}$ requirements.

$$R\theta_{SA} \leq \frac{T_{J(max)} \times \frac{3}{4} - T_{AMB} - P_{FET}\left(R\theta_{JC} + R\theta_{CS}\right)}{P_{FET}} \approx \frac{16.6^{o}C}{W} \tag{43}$$

3.7 Over Voltage Protection and Under Voltage Lockout

The OVP function and under voltage lockout (UVLO) were handled by the UCC28220. It is a simple comparator that monitors the boost voltage. Information on setting up these thresholds can be found in the UCC28220's data sheet. The OVP for this design was set to 425 V and UVLO was set to 108 V. The pre-regulator will not start switching until V_{OUT} reaches 108 V.

3.8 Peak Current Limit

Peek current limit is set by the maximum control voltage (V_C) at the input of the UCC28220's PWM comparator. Where "a" is the current sense transformer turns ratio of T1 and T2. The peak current limit trip point was set for 130% of the nominal peak current to protect the boost FETs.

$$a = \frac{N_P}{N_S} = \frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{1}{50} \tag{44}$$

$$I_{PEAK} = \left(\frac{P_{OUT} \times \sqrt{2}}{2 \times V_{in(min)} \times \eta} + \frac{\Delta IL1}{2}\right) \times 1.3 \tag{45}$$

V_C = 1.8, V_{CTRL} was set to a maximum of 3.0 V to protect the UCC28220 CTRL pin. (46)

$$R_{SENSE} = \frac{\frac{V_C - 0.5\ V}{2}}{I_{PEAK} \times a}$$, this equation takes into account slope compensation that is added later. (47)

The peak current of the FET during power up is 2 times I_{PEAK} under normal operation. This is due the excessive slope compensation that is needed for stability.

$$I_{PEAK(startup)} = 2 \times I_{PEAK} \tag{48}$$

3.9 Current Sense Transformer Reset Resistor (T1 and T2)

$$R_{RESET} = \frac{\frac{V_C - 0.5\ V}{2}}{I_{PEAK} \times \left(1 - D_{MIN(LL)}\right) \times a} \tag{49}$$

3.10 Oscillator and Maximum Duty Cycle Clamp

The UCC28220's oscillator and maximum duty cycle clamp are setup through resistor R_{CHG} and discharge. The desired duty cycle clamp (D_{MAX}) was set at 0.9 to stop the current sense transformers from saturating.

$$K_{OSC} = \left(2.04 \times 10^{10}\right)\frac{\Omega}{s}$$, UCC28220 oscillator constant. (50)

$$F_{OSC} = 2 \times f_S$$, UCC28220 internal oscillator frequency. (51)

$$F_{OSC} = 2 \times f_S$$, internal duty cycle clamp. (52)

$$D_{MAX(osc)} = 1 - 2\left(1 - D_{MAX}\right) \tag{53}$$

$$R_{DISCHG} = K_{OSC}\frac{\left(1 - D_{MAX(osc)}\right)}{F_{OSC}} \quad (54)$$

3.11 Control Loop Compensation

All the control equations for the voltage loop and current loop are estimates. The control equations in this paper gives starting points for feedback compensation. In most control loops it is required to adjust the loop compensation as necessary with a network analyzer.

3.12 Current Loop

The first step in setting up the current loop is setting up the multiplier components. The R_{IAC} resistor is tied to the rectified line voltage and is what forces the current amplifier output to track changes in the line voltage. This resistance typically is a group of series resistors needed to meet the high voltage requirements.

$$R_{IAC} = \frac{V_{IN(max)} \times \sqrt{2}}{500\ \mu A} \quad (55)$$

The multiplier internal to the UCC28528 has a voltage feed forward (VFF) function that keeps the power stage gain constant and provides soft power limiting when the line drops keeping the line current from increasing excessively. A detailed explanation can be found in TI/Unitrode application note SLUA196A. The VFF signal is produced through an internal current mirror within the PFC controller. The maximum current leaving the VFF pin is equal to one half the I_{AC} current. The following equations are used to select a VFF resistor (R_{VFF}) and a filter capacitor (C_{VFF}) to remove ac components from the VFF signal.

$$R_{VFF} = \frac{1.5\ V}{\frac{V_{in(min)}}{2 \times R_{IAC}} \times 0.9} \quad (56)$$

The VFF signals ac portion has an affect on total current harmonic distortion (THD). The filter's pole (fp1) is set at a frequency to limit the VFF contribution to 1.5% in order to meet the power supplies current THD design requirements.

$$f_{P1} = f_{LINE} \times \frac{1.5\%}{66\%} \quad (57)$$

$$C_{VFF} = \frac{1}{2 \times \pi \times R_{VFF} \times f_{P1}} \quad (58)$$

This control methodology is based on average and peak current mode control and the following formulas to compensate the current loop. These calculations get the design close to the correct compensation and will have to be fine tuned with a network analyzer. In this design example to compensate the current loop ($T_{C(s)}$) we set a design goal of 45 degrees of phase margin and a crossover frequency of one tenth the switching frequency.

$T_{C(s)} = G_{ID(s)} \times G_{CA(s)}$, current loop transfer function. (59)

$G_{ID(s)} = \frac{\Delta IL1}{\Delta I_C} = \frac{V_{OUT} \times R_{SENSE} \times a}{s \times L1 \times V_{C1}}$, control to output current transfer function. (60)

$V_{C1} = V_C$ - 0.5 V, V_{C1} is the maximum control voltage at the input of the PWM comparator of the UCC28220. Note Equation V_{C1} takes into account the 500 mV offset that is present in the UCC28220 PWM controller. (61)

The current amplifier compensation transfer function $G_{CA(s)}$ is as follows

$$G_{CA(s)} = \frac{\Delta I_C}{\Delta IL1} = \frac{\left(s \times R_{ZB} \times C_{ZA} + 1\right)}{s \times R_{MO} \times \left(C_{ZB} + C_{PB}\right) \times \left(s \times \frac{C_{ZB} \times C_{PB}}{C_{ZB} + C_{PB}} \times R_{ZB} + 1\right)} \times H_{CNTRL} \times H_{CA} \quad (62)$$

$$H_{CNTRL} = \frac{\Delta V_C}{\Delta V_{CTRL}} = 0.6$$, internal divider of the UCC28220 CTRL pin. (63)

The voltage divider H_{CA} was required to divide down the CA output of the UCC28528, to protect the CTRL pin of the UCC28220. This divider should work fine for any power requirement and should be considered a fixed variable.

$$H_{CA} = \frac{\Delta V_{CTRL}}{\Delta V_{CA(out)}} = \frac{R_D}{R_C + R_D} \approx 0.594 \tag{64}$$

For stability the current sense signal needs slope compensation. It is required to add at least half of the inductor current down slope to the current sense signal. The UCC28220 has internal slope compensation that is setup by resistor R_{SLOPE}.

$$R_{SLOPE} = 0.1\ V \times \frac{\left(1 - D_{MIN(LL)}\right)}{10\ pF \times \frac{\Delta IL \times a \times R_{SENSE}}{2}} \tag{65}$$

The UCC28528 needed a current sense resistor ($PFCR_{SENSE}$) to monitor the input current. Calculating this resistor value is based on allocating a maximum allowable current sense voltage (V_{SENSE}).

$$PFCR_{SENSE} = \frac{V_{SENSE}}{\frac{P_{OUT} \times \sqrt{2}}{V_{IN(min)} \times \eta}} \tag{66}$$

The UCC28528 also uses the current sense signal to trigger power limiting. The power limit can be setup by properly selecting the multiplier resistor R_{MO}. The power limit was set to 110% of full load power. Please refer to the UCC28528s data sheet for details on how this power limiting function works. The power limit was set at 110% as not to interfere with the UCC28220's peak current limit function which was set at 130%.

$$R_{MO} = \frac{\frac{P_{OUT} \times \sqrt{2} \times 1.1 \times PFCR_{SENSE}}{V_{IN(min)} \times \eta}}{\frac{2 \times V_{IN(min)} \times \sqrt{2}}{R_{IAC}}} = \frac{V_{R(sense)}}{2 \times I_{AC}} \tag{67}$$

$$R_{ZB} = \frac{\frac{1}{\left|G_{ID}\left(2 \times \pi \times j \times \frac{f_S}{10}\right)\right|} \times R_{MO}}{H_{CA} \times H_{CNTRL}}$$, resistor R_{ZA} is set to force $T_{C(s)}$ to cross over at (f_S/10). (68)

Putting a zero at loop crossover adds an additional 45 degrees of phase at crossover to ensure control loop stability.

$$C_{ZB} = \frac{1}{2 \times \pi \times R_{ZB} \times \left(\frac{f_S}{10}\right)}$$, capacitor C_{ZB} is adjusted to put a zero at frequency crossover. (69)

$$C_{PB} = \frac{1}{2 \times \pi \times R_{ZB} \times \left(\frac{f_S}{2}\right)}$$, capacitor C_{PB} is used to attenuate high frequency noise. (70)

3.13 Voltage Loop ($T_{V(s)}$)

Compensating the voltage loop has two major constraints. First is attenuating the 2 x f_{LINE} output capacitor voltage ripple, this is required to reduce input current harmonic distortion. Second is control loop stability. If either of these criteria is compromised PF and THD will be affected greatly.

$$T_{V(s)} = G_{VD(s)} \times G_{VA(s)} \tag{71}$$

V_{C2} = 5.5 V, maximum voltage amplifier (VA) output. (72)

$$G_{VD(s)} = \frac{\Delta V_{OUT}}{\Delta V_C} \times \frac{\frac{P_{OUT}}{\eta}}{V_{C2} \times s \times C_{OUT} \times V_{OUT}}$$, voltage control to output transfer function. (73)

gm = 100 umho, trans-conductance voltage amplifier (VA) gain. (74)

$$H1 = \frac{R_B}{R_B + R_A} = \frac{V_{REF}}{V_{OUT}} = \frac{7.5\ V}{V_{OUT}}$$, this divider can also be used to set up the R_A and R_B voltage divider. (75)

$$G_{VA(s)} = H1 \times gm \times \frac{s \times R_{ZA} \times C_{ZA} + 1}{s \times R_{MO} \times \left(C_{ZA} + C_{PA}\right) \times \left(s \times \frac{C_{ZA} \times C_{PA}}{C_{ZA} + C_{PA}} \times R_{ZA} + 1\right)}$$ (76)

To ensure that this loop would have low harmonic distortion the loop was designed to crossover (f_C) at 10 Hz.

$$R_{ZA} = \frac{\frac{1}{\left|G_V\left(2 \times \pi \times j \times f_C\right)\right|}}{H1 \times gm}$$ (77)

$$C_{ZA} = \frac{1}{2 \times \pi \times f_C \times R_{ZA}}$$, C_{ZA} is set at f_C to give the voltage loop 45 degrees of added phase at crossover. (78)

$$C_{PA} = \frac{1}{2 \times \pi \times \left(2 \times f_{LINE}\right) \times \left(\frac{V_C \times 0.015}{V_{RIPPLE}} \times \frac{1}{H1 \times gm}\right)}$$, is sized to attenuate the output ripple voltage. (79)

After the critical parameters were calculated the power supply was constructed and evaluated. The final design of the 350-W two phase interleaved PFC is shown in the schematics of Figure 7 and Figure 8. This power supply also has a 2-W auxiliary power supply that is based on a discontinues current mode (DCM) flyback topology.

4 Schematic

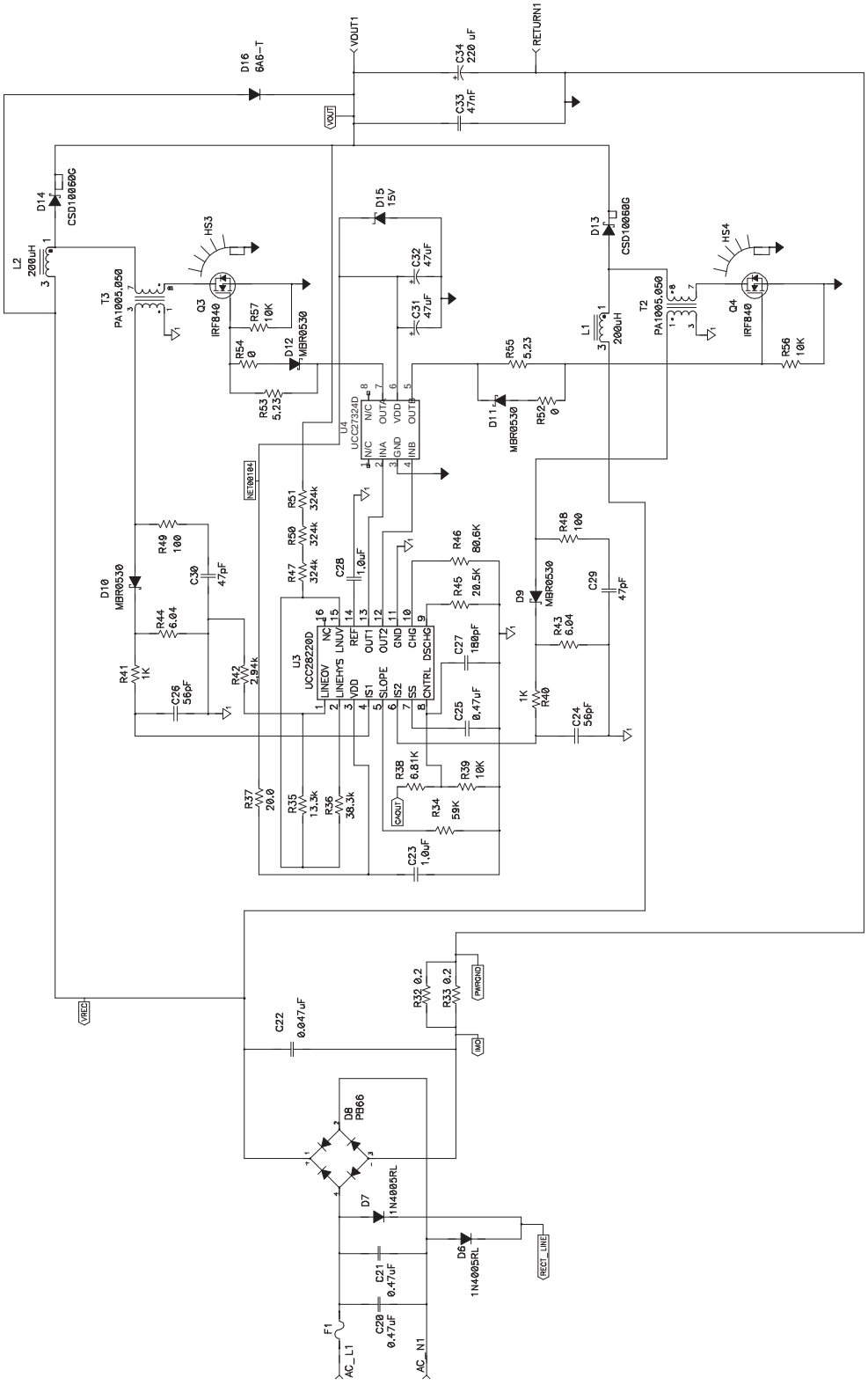

Figure 7. 350-W Interleaved PFC Boost Pre-Regulator Schematic

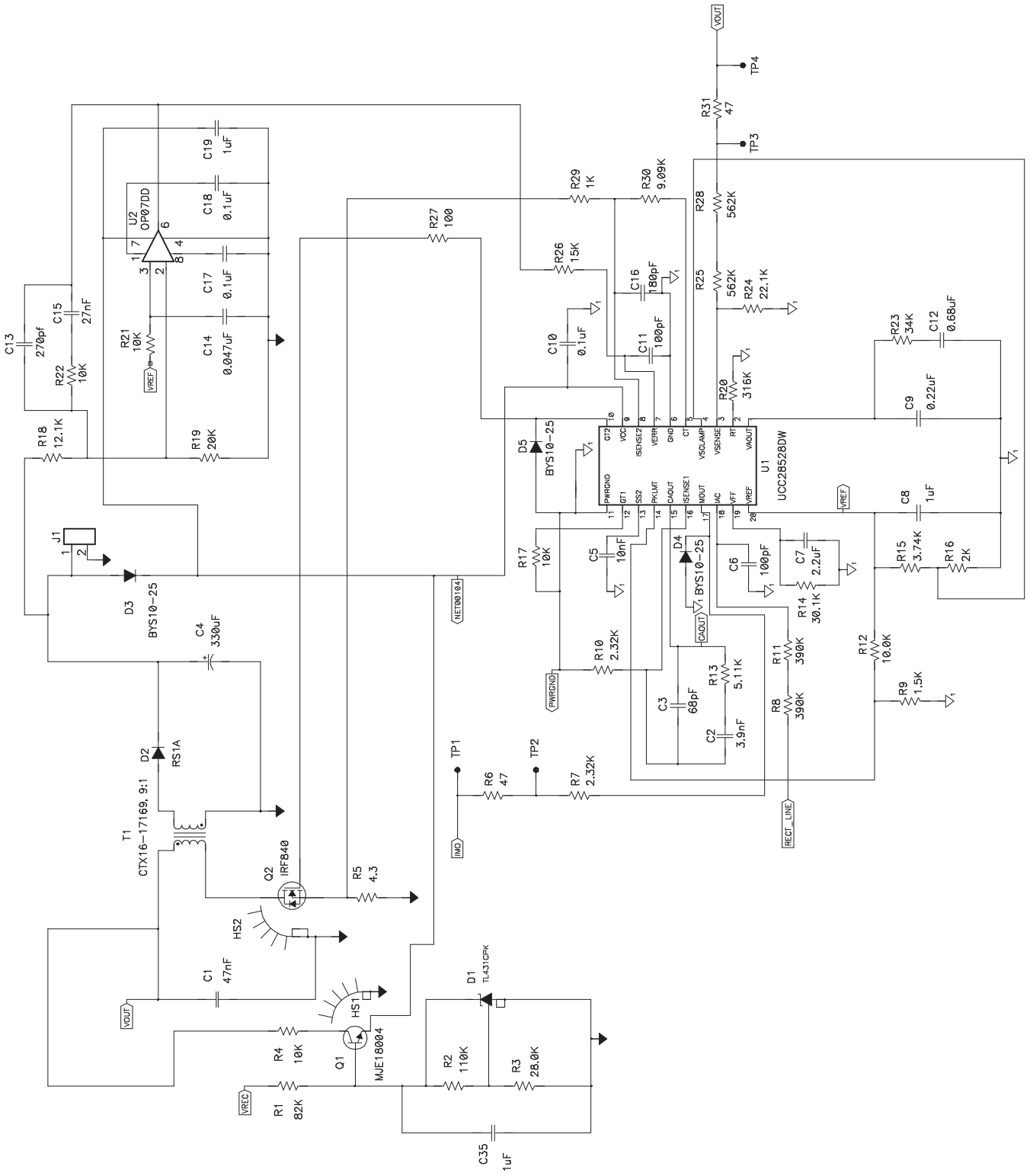

Figure 8. 2-W, Flyback and PFC/PWM Controller Schematic

5 Design Performance

The current loop $T_{C(s)}$ was measured with a network analyzer and did not exactly track the model presented above. The $T_{C(s)}$ gain moved with input voltage and appeared to have a double pole around 30 kHz. This is probably due to the excessive slope compensation that this topology requires. However, the current loop was stable and did not have to be adjusted. Note to measure the current loop or voltage loop requires a dc input voltage, otherwise the line current and voltage affects the loop measurements. A network analyzer with a low enough frequency range was not available to measure the voltage loop.

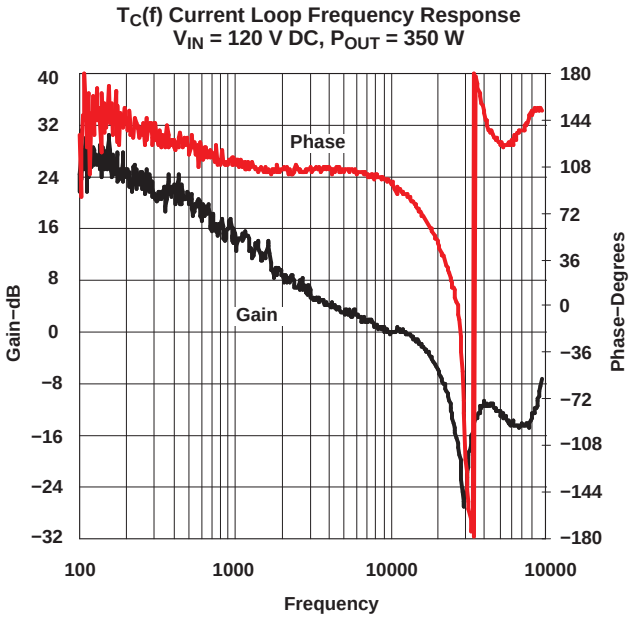

Figure 9.

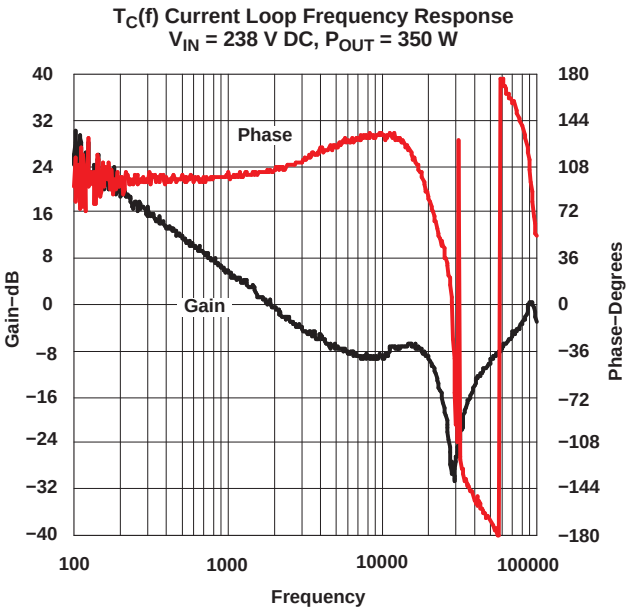

Figure 10.

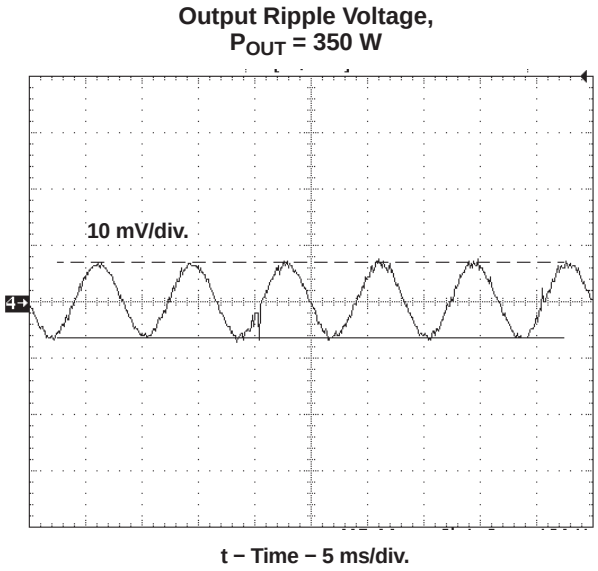

Figure 11.

5.1 Input Inductor Ripple Current Cancellation

Figure 12 shows the inductor ripple current cancellation at the peak of line with a minimum input of 85 V RMS. From this graph it can be observed that the input current (CH4) is 1/2 the individual inductor ripple currents of L1 (CH2) and L2 (CH3). The ratio of input ripple current to inductor ripple current agrees with graph in Figure 2. Note that the current ratio is 0.225 A/mV in the following graphs.

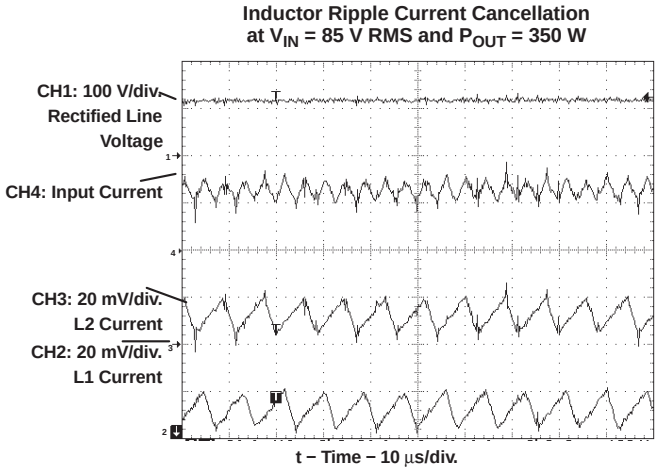

Figure 12.

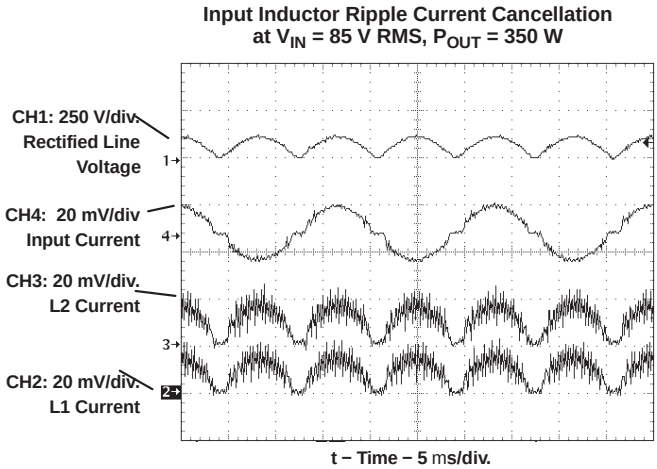

Figure 13.

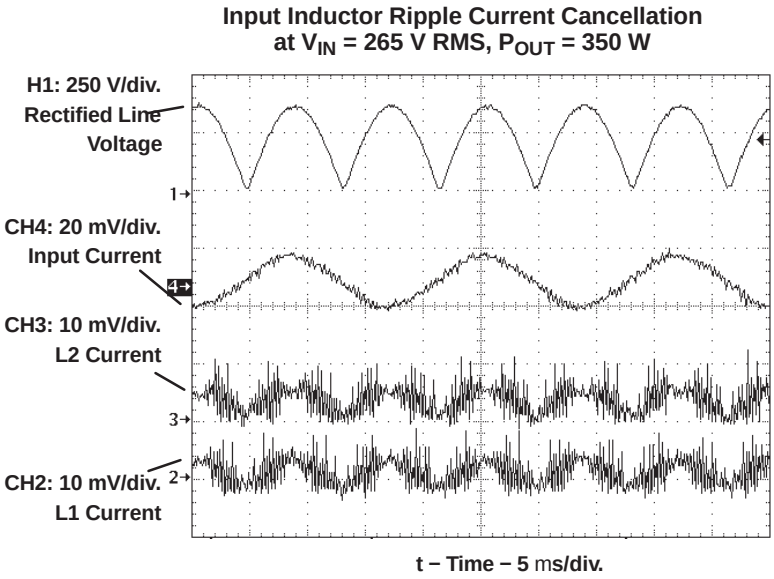

Figure 14.

5.2 Transient Response

The voltage loop of a PFC pre-regulator is generally below 10 Hz, which means the fastest the voltage loop can respond to a small transient is roughly 100 ms. In typical applications a PFC pre-regulator takes 5 to 10 times as long to recover from a transient response. However, a large signal comparator built into the UCC28528 control device allowed the design to recover from large signal transient responses in less than 200 ms.

Startup No Load and V_{IN} = 85 V

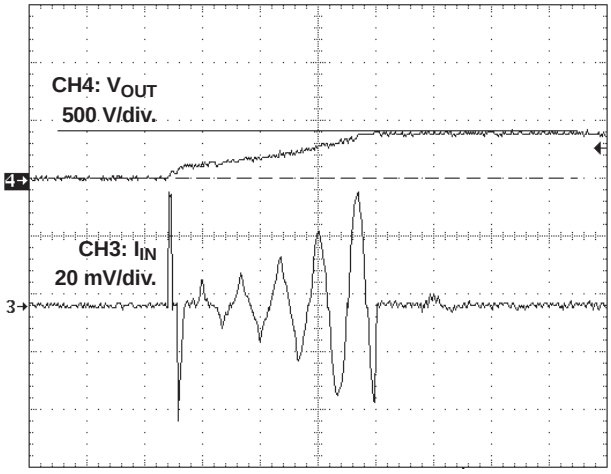

Figure 15.

Startup at V_{IN} = 85 V, P_{OUT} = 350 W

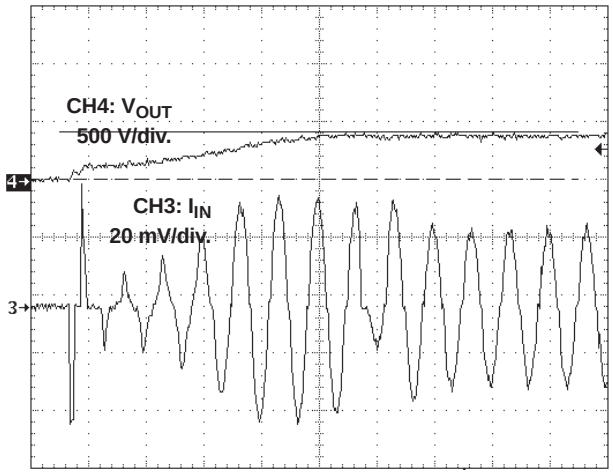

Figure 16.

Line Transients at 350-W Load, V_{IN} Stepped from 240 V to 120 V to 240 V

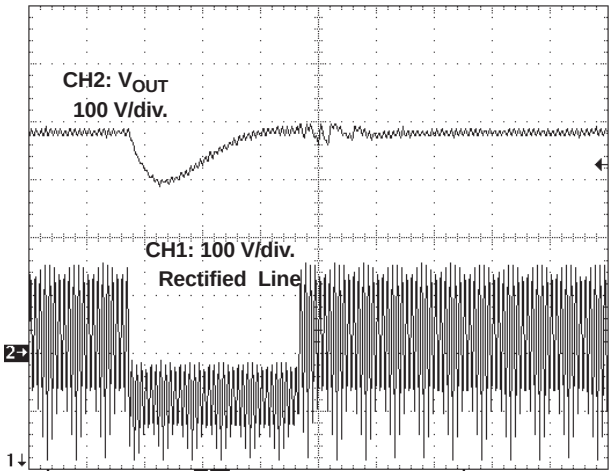

Figure 17.

Line Dropout at Full Load

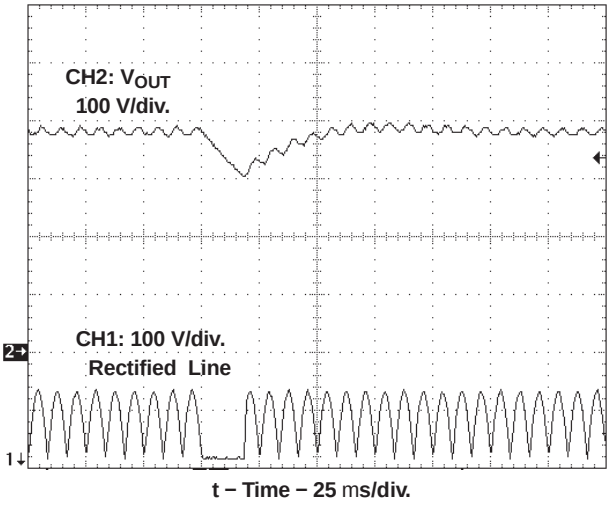

Figure 18.

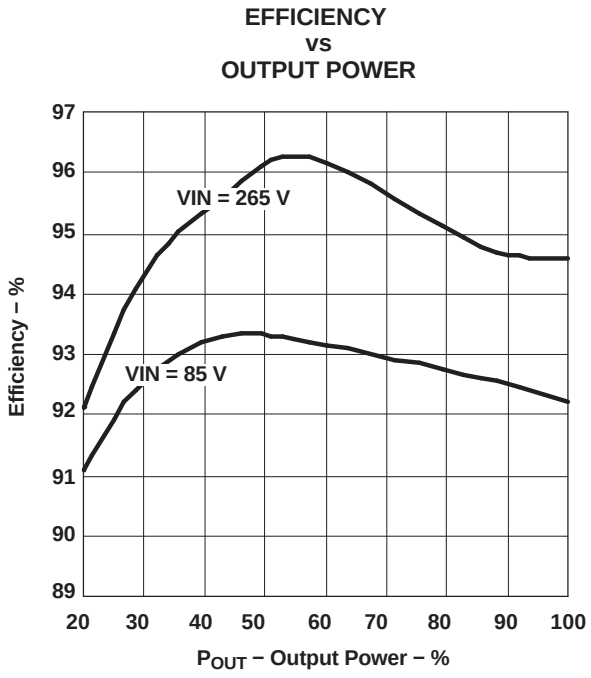

Figure 19.

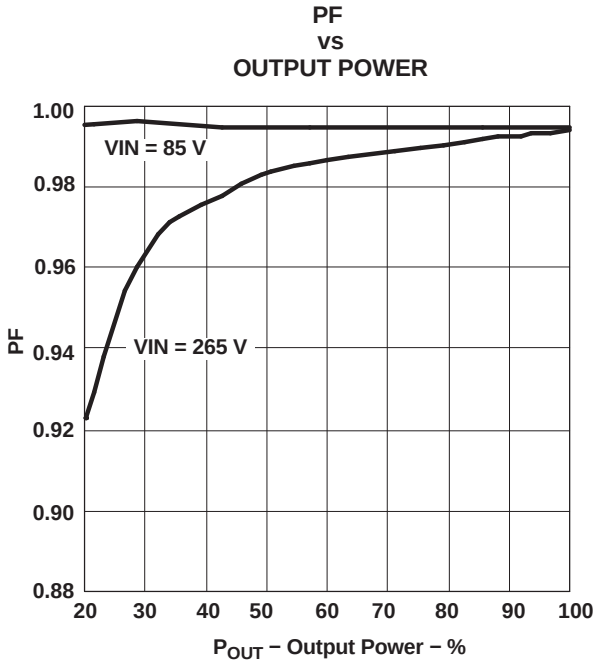

Figure 20.

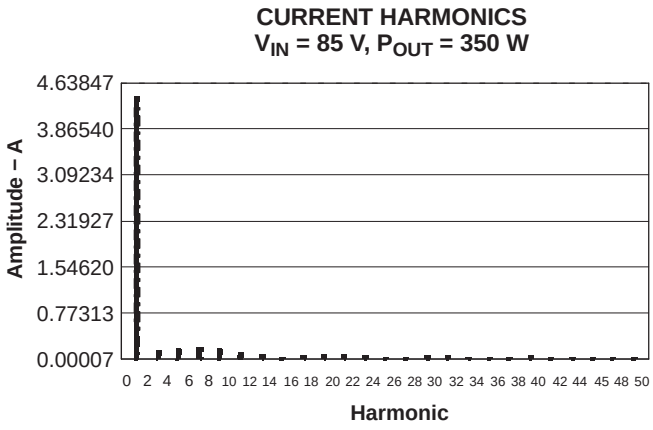

Figure 21.

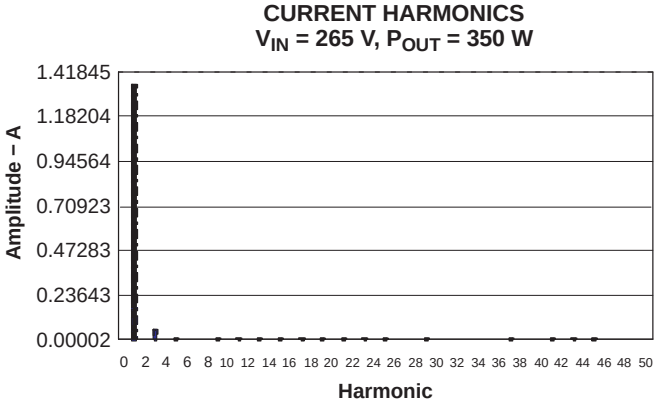

Figure 22.

6 Conclusion:

By interleaving boost pre-regulator stages enables the power supply designer to reduce boost inductor area product by 50% and reduce boost capacitance RMS current. This allows the designer to reduce the size of the PFC pre-regulator; as well as, use output filter capacitors with lower RMS ratings.

In high power applications interleaving PFC pre-regulators would be a good choice, where many boost FETs and boost diodes would be required for the design. In these applications the only added cost would be adding the additional control circuitry that is needed to accomplish interleaving.

Revision History

Changes from B Revision (February 2007) to C Revision	Page
• Deleted incorrect image title.	5

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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