

Features

- Wide Input Voltage Range: 3V~36V
- Adjustable 0.8V~20V Output Range
- $\pm 1\%$ Output Voltage Accuracy over Line and Load
- Wide output load range: 0 to 10A
- Constant-on-time control scheme for fast transient and high Efficiency
- Programmable Operation Frequency from 100kHz to 600kHz
- Selectable Forced PWM or automatic PFM/PWM mode
- 45% Under-Voltage Protection
- 125% Over-Voltage Protection
- FB Short Protection
- Internal 5V Pre-regulator
- External Adjustable Soft-Start and Soft-Stop
- Internal Over Temperature Protection
- Programmable Over Current Protection
- TQFN20-5x5 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Notebook computers
- CPU core/IO Supplies
- Chip/RAM Supplies

General Description

The GS92B3 is small size chip with a relative constant on-time synchronous buck switching converter suitable for applications in notebook computers and other battery operated portable devices. Features include very wide input voltage range, high efficiency and a fast dynamic response with internal fast response scheme.

The GS92B3 have a unique power save mode, which can save battery power supply by decreasing frequency when load current falls down below preset critical current point.

The fast dynamic transient response means that buck converter applications based on GS92B3 will provide about 100ns-order response to load when output voltage falls down or rises up. The frequency will increase or decrease to meet the change in output load. Moreover, the GS92B3 will take the same method to regulate the output voltage when input voltage changes. When transient response regulated, the converter will maintains a new steady-state operation. Both the transient response state and the new state, the GS92B3 always has the same on-time.

The GS92B3 is suitable for the solutions which have the output voltage between 0.8V and 20V. An external setting resistor and output voltage can set the on-time, duty-cycle and frequency for the converter. The integrated gate drivers feature adaptive shoot-through protection, fast signal transmission. Additional features include current limit, soft-start, over-voltage and under-voltage protection, a Power Good flag and soft discharge upon shutdown. The GS92B3 is available in package TQFN20-5x5.

Typical Application

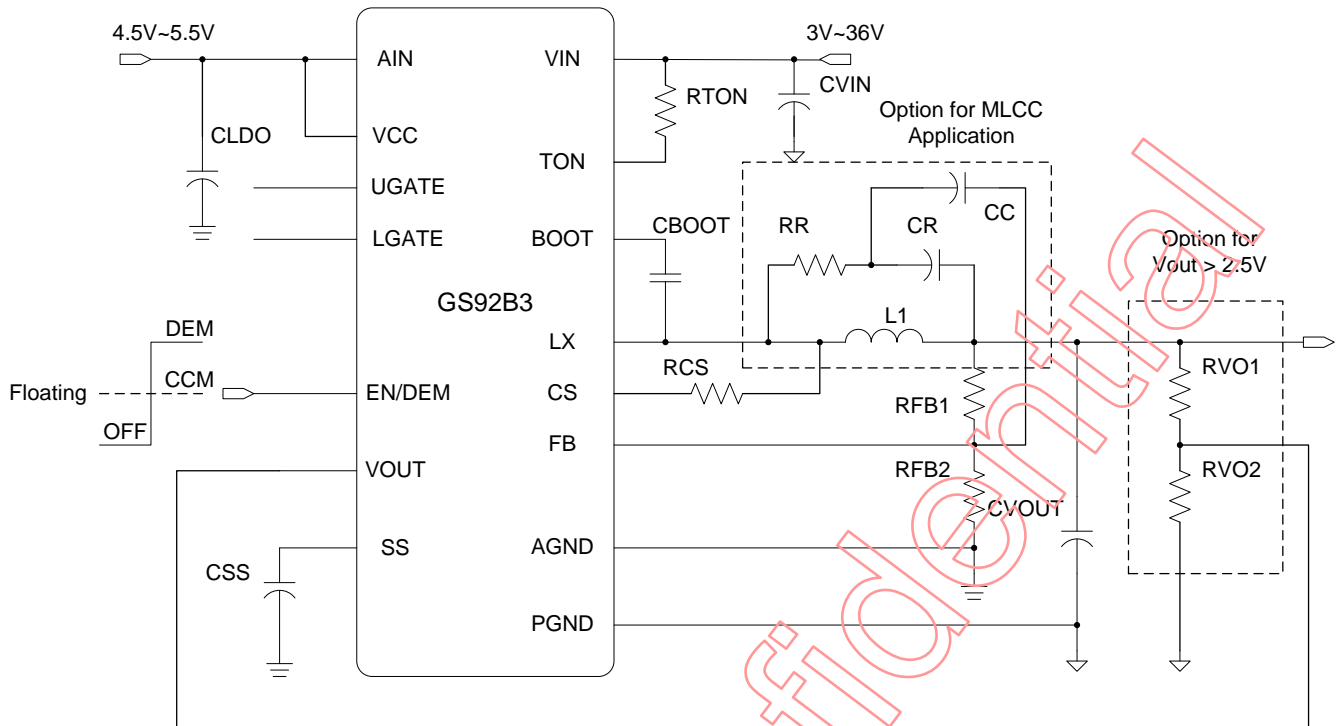


Figure 1a Typical Application of GS92B3

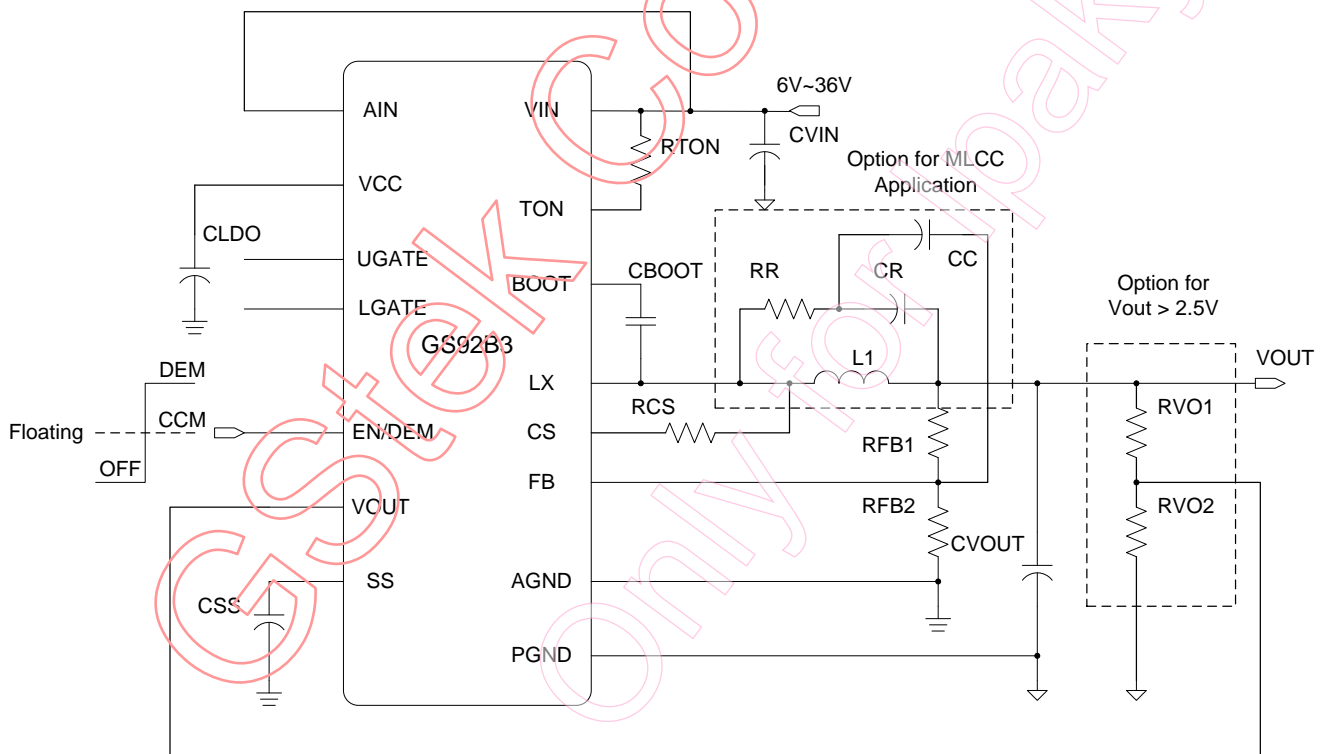


Figure 1b Typical Application of GS92B3

Function Block Diagram

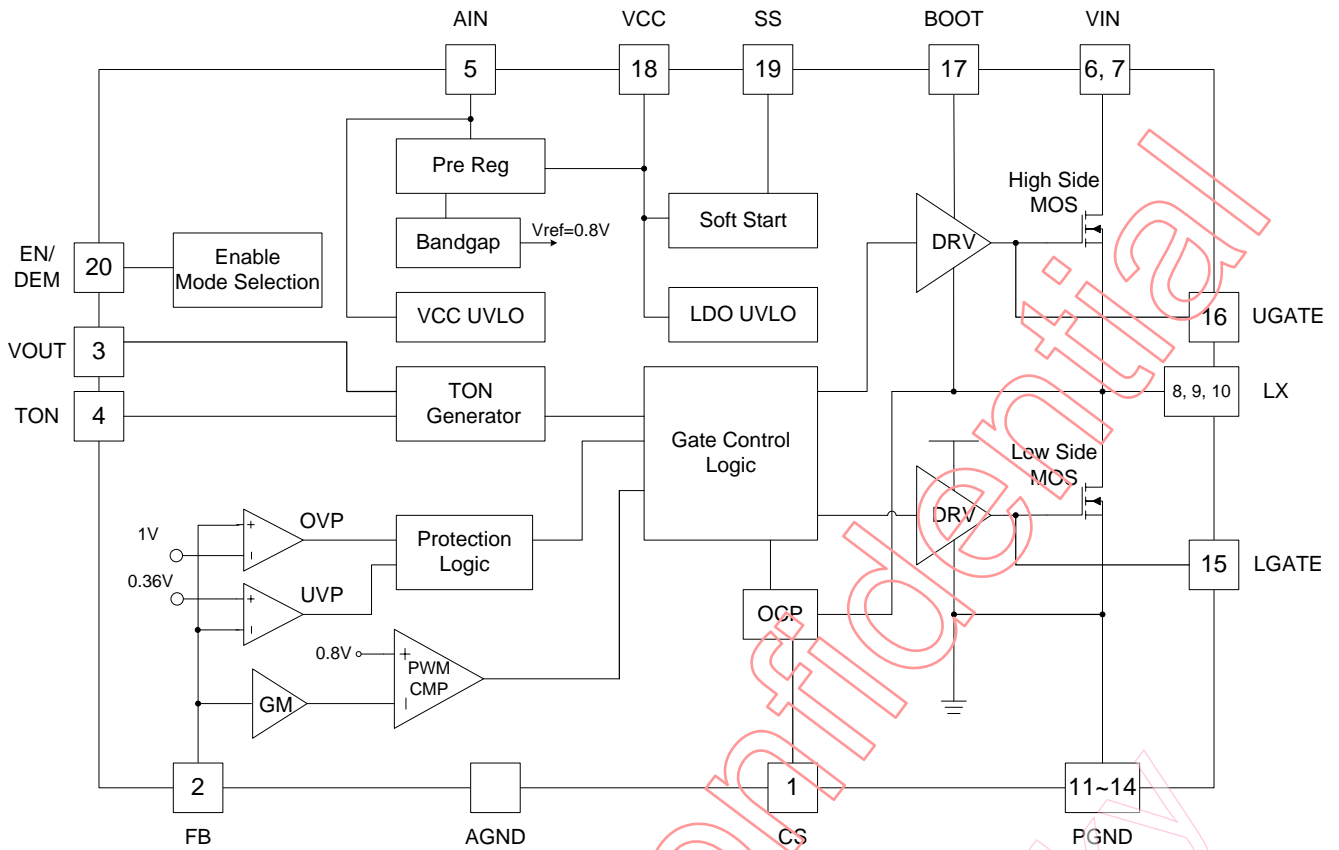
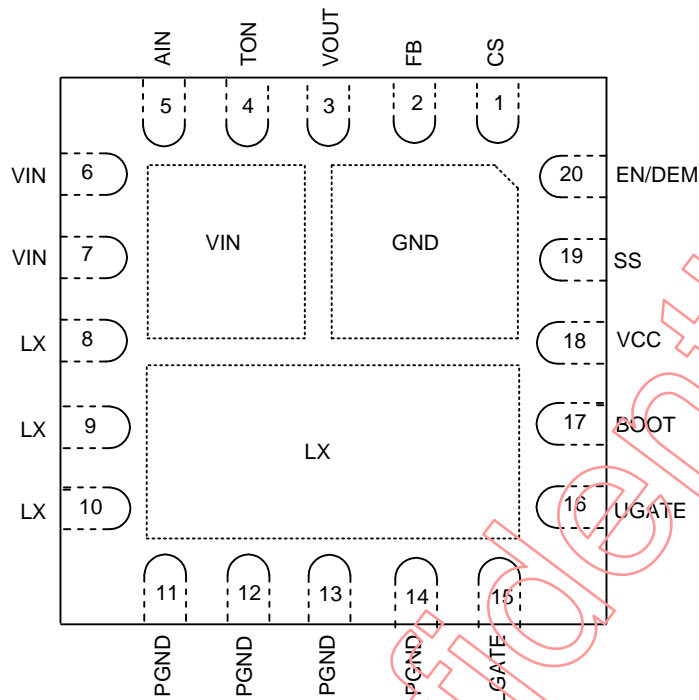


Figure 2 Function Block Diagram

Pin Configuration



(Top view)

Figure 3 TQFN20-5x5 Package

Pin Descriptions

| No. | Name | I/O | Description |
|----------|------|-----|---|
| 1 | CS | I/O | Current Limit Detecting Input Pin. Connect LX Pin through an external resistor to set the current limit threshold. |
| 2 | FB | I | Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND. |
| 3 | VOUT | I | VOUT Pin offers the output information to the chip, in order to make the frequency setting more accuracy. When OVP condition occurs, through this pin discharge the energy of vout capacitor. |
| 4 | TON | I/O | On-Time Setting Input. Connect a resistor between VIN and TON to set the on time width. |
| 5 | AIN | I/O | Supply Input for analog functions. |
| 6, 7 | VIN | I | Supply Input. VIN is the regulator input. All VIN pins must be connected together. |
| 8, 9, 10 | LX | I/O | Upper Driver Floating Ground for Buck Controller. Connect to an external inductor. |

| | | | |
|-------|--------|-----|--|
| 11~14 | PGND | O | Power Ground. |
| 15 | LGATE | O | Lower gate drive output. Connect to gate of low-side power MOSFET. |
| 16 | UGATE | O | Upper gate drive output for Buck Converter. Connect to gate of high-side power MOSFET. |
| 17 | BOOT | I | Bootstrap Capacitor Connection. Connect an external capacitor between BOOT and VSWH Pin. |
| 18 | VCC | I/O | Internal Linear Regulator Output. |
| 19 | SS | I/O | Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time. |
| 20 | EN/DEM | I | Buck Enable Control Pin. EN=Low, Shutdown; EN=High, Auto-DEM Mode; EN=Floating, Forced CCM |

Ordering Information

GS92B3PP-R

1. Package ← → 2. Shipping

| No | Item | Contents |
|----|----------|----------------|
| 1 | Package | TQ:TQFN20-5x5 |
| 2 | Shipping | R: Tape & Reel |

Example: GS92B3 TQFN20-5x5 Tape & Reel ordering information is "GS92B3TQ-R"

Absolute Maximum Rating (Note 1)

| Parameter | Symbol | Limits | Units |
|--|---------------------|----------------------|------------------|
| VAIN to GND | V_{AIN} | -0.3 ~ 40 | V |
| TON to GND | V_{TON} | -0.3 ~ 40 | V |
| CS to GND | V_{CS} | -0.3 ~ 40 | V |
| VCC to GND | V_{CC} | -0.3 ~ 6 | V |
| EN to GND | V_{EN} | -0.3 ~ 40 | V |
| FB, VOUT to GND | V_{FB}, V_{OUT} | -0.3 ~ 6 | V |
| BOOT Voltage | $V_{BOOT-GND}$ | -0.3 ~ 46 | V |
| BOOT to LX Voltage | $V_{BOOT-V_{VLX}}$ | -0.3 ~ 6 | V |
| LGATE to GND | V_{GL} | -0.3 ~ 6 | V |
| VLX to GND DC <200ns | V_{VLX} | -0.7V~40V -8V~40V | V |
| Package Power Dissipation at $T_A \leq 25^\circ\text{C}$ | $P_{D_TQFN20-5x5}$ | 4228 | mW |
| Junction Temperature | T_J | - 45 ~ 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | - 55 ~ 150 | $^\circ\text{C}$ |
| Lead Temperature (Soldering) 10S | T_{LEAD} | 260 | $^\circ\text{C}$ |
| ESD (Human Body Mode) (Note 2) | V_{ESD_HBM} | 2K | V |
| ESD (Machine Mode) (Note 2) | V_{ESD_MM} | 200 | V |

Thermal Information (Note 3)

| Parameter | Symbol | Limits | Units |
|--|---------------------------|--------|--------------------|
| Thermal Resistance Junction to Ambient | $\theta_{JA_TQFN20-5x5}$ | 23.65 | $^\circ\text{C/W}$ |

Recommend Operating Condition (Note 4)

| Parameter | Symbol | Limits | Units |
|----------------------|--------------|------------------------|------------------|
| VIN to GND (Note 5) | V_{IN} | 3~36 | V |
| VAIN to GND (Note 5) | V_{AIN} | 6~36 | V |
| VCC to GND | V_{CC} | 4.5~5.5 | V |
| EN/DEM to GND | $V_{EN/DEM}$ | $V_{EN/DEM} = V_{AIN}$ | V |
| Junction Temperature | T_J | -40 ~125 | $^\circ\text{C}$ |
| Ambient Temperature | T_A | -40 ~ 85 | $^\circ\text{C}$ |

Electrical Characteristics

($R_{TON}=300K\Omega$, $V_{IN}=12V$, $V_{OUT}=1.2V$, $EN/DEM=V_{IN}$, $T_A =25^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---------------------------------------|--|-----|-------------|------|---------|
| Supply Voltage (VAIN) | | | | | | |
| Under voltage lock out (Rising) | V_{AIN_UVLO} | | | 5.5 | | V |
| UVLO Hysteresis | $V_{AIN_UVLOHYS}$ | | | 0.2 | | V |
| 5V Pre-regulator (V_{VCC}) | | | | | | |
| Output Voltage | V_{VCC} | | | 5.15 | | V |
| Under voltage lock out (Rising) UVLO Hysteresis | V_{VCC_UVLO} $V_{VCC_UVLOHYS}$ | | | 4.15 0.3 | | V V |
| Reference Voltage | | | | | | |
| FB Reference Voltage | V_{FB} | $V_{VCC}=5V$ | | 0.8 | | V |
| Enable Logic | | | | | | |
| EN Logic Low Voltage | V_{EN_L} | EN Falling | | | 0.6 | V |
| EN Floating Voltage | V_{EN_F} | V_{IN} Power On, Stable State(Forced CCM) | | 2.2 | | V |
| EN Logic High Voltage | V_{EN_H} | EN Rising(DEM) | 3.1 | | | V |
| Current Parameters | | | | | | |
| Quiescent | I_Q | $FB=0.85V$, $V_{IN}=12V$ | | 830 | | μA |
| Soft start current | I_{SS} | $V_{SS}=0$ | | 10 | | μA |
| Shutdown Current | I_{SHTDN} | $EN=0$, $I(V_{IN})$ | | 4 | | μA |
| | | $EN=0$, $I(TON)$ | | | 0.01 | μA |
| | | $EN=0$, $I(EN)$ | -2 | -1 | | μA |
| Logic Input Current | I_{EN} | $EN=12V$ | | 13 | | μA |
| | | $EN=0V$ | -2 | -1 | | μA |
| System Time & Driver On-Resistance | | | | | | |
| On-Time | T_{ON} | $V_{IN}=12V$, $V_{FB}=0.79V$, $R_{TON}=300K$, $V_{OUT}=1.2V$ | | 300 | | ns |
| Minimum On-Time | T_{ON_Min} | $V_{IN}=12V$, $V_{FB}=0.79V$, $R_{TON}=1K$, $V_{OUT}=1.2V$ | | 100 | | ns |
| Minimum Off-Time | T_{OFFMIN} | $V_{IN}=12V$, $V_{FB}=0.79V$, $R_{TON}=300K$ | | 440 | | ns |
| High Side MOS RDSON | R_{DSH} | BOOT-LX=5V | | 15 | | mohms |
| High Side Leakage | I_{LEAKH} | | | 10 | | μA |
| Low Side MOS RDSON | R_{DSL} | VCC-GND=5V | | 6 | | mohms |

| | | | | | | |
|--|-----------------|--|-----|---------------------------------|-----|------------|
| Low Side Leakage | I_{LEAKL} | | | 10 | | uA |
| Current Sensing | | | | | | |
| CS Set Source Current | I_{CS} | $V_{CS}=1V$ | | 20 | | uA |
| ICS current temperature coefficient | TCS | On the bias of $T_A=25^{\circ}C$ | | 4900 | | ppm/ °C |
| Current Limit 1 (Rising) | I_{LIM1} | GND-LX, RCS=18K | 324 | 360 | 396 | mV |
| Current Limit 2 (Rising) | I_{LIM2} | GND-LX, RCS=10K | 180 | 200 | 220 | mV |
| Current Limit 3 (Rising) | I_{LIM3} | GND-LX, RCS=2.5K | 35 | 50 | 65 | mV |
| Zero Crossing Threshold | V_{T_0} | GND-LX | -10 | | 10 | mV |
| Voltage Fault Protection | | | | | | |
| UVP Threshold | V_{UV_TH} | Measure at V_{FB} , with respect to reference voltage | | 45 | | % |
| UVP Blank Time | T_{UV_B} | From Enable to UVP $80mV < V_{FB} < UVP$ Threshold | | $1.6 \times 10^8 \times C_{SS}$ | | ms |
| UVP Fault Delay | T_{UV_D} | Force V_{FB} below UVP threshold | | 20 | | us |
| OVP Threshold | V_{OV_TH} | Measure at V_{FB} , with respect to reference voltage | | 125 | | % |
| OVP Fault Delay | T_{OV_D} | Force V_{FB} above OVP Threshold | | 20 | | us |
| Over Temperature Shutdown | | | | | | |
| Thermal Shutdown Threshold | T_{TSDN} | | | 150 | | °C |
| Thermal Shutdown Hysteresis | T_{HYS_TSDN} | | | 20 | | °C |
| Bootstrap Diode | | | | | | |
| Internal Boost Charging Switch On-Resistance | R_{BT_D} | VCC to BOOT, 10mA | | | 120 | ohms |

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5 Recommend the Pulse time < 100ns when V_{IN} over than 40V.

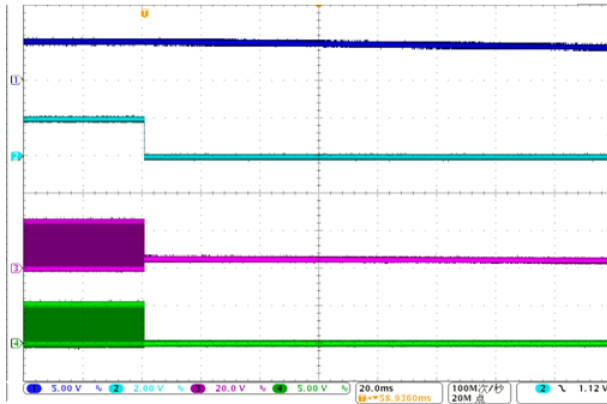
Note 6 If $V(\text{BOOT})-V(\text{VLX}) < 4\text{V}$, a boot diode is recommended.

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Typical Characteristics

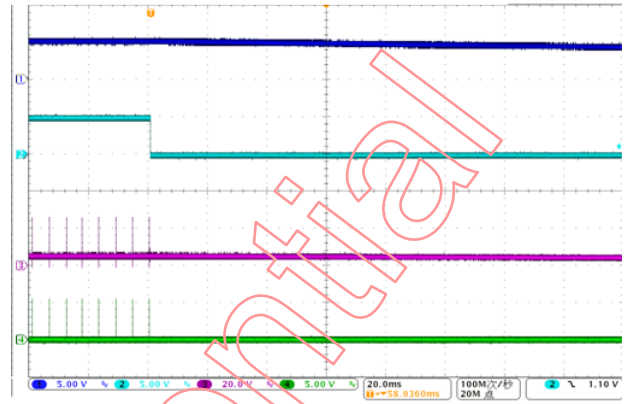
Power Off From EN(CCM Mode)

CH1: VOUT CH2: EN CH3: UGATE CH4: LGATE



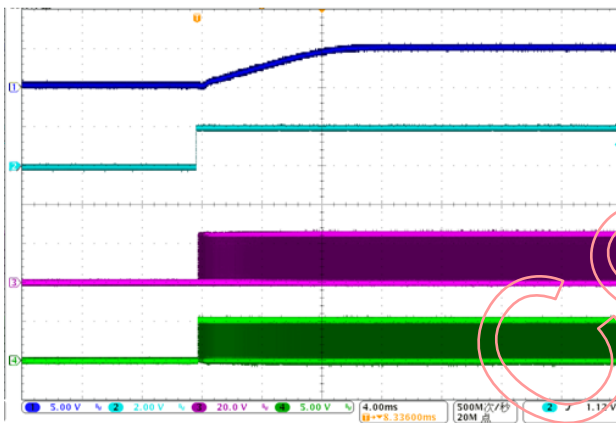
Power Off From EN(DEM Mode)

CH1: VOUT CH2: EN CH3: UGATE CH4: LGATE



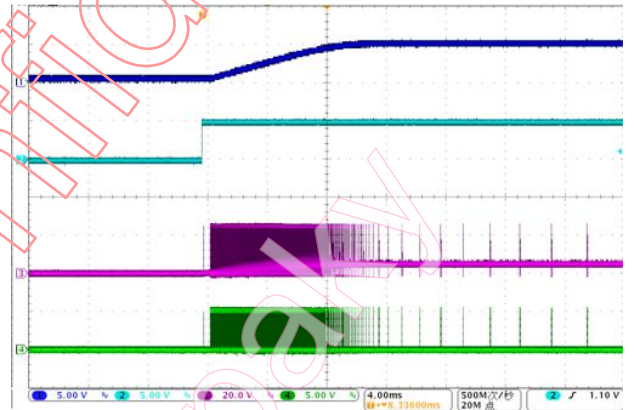
Power on from EN (CCM No Load)

CH1: VOUT CH2: EN CH3: UGATE CH4: LGATE



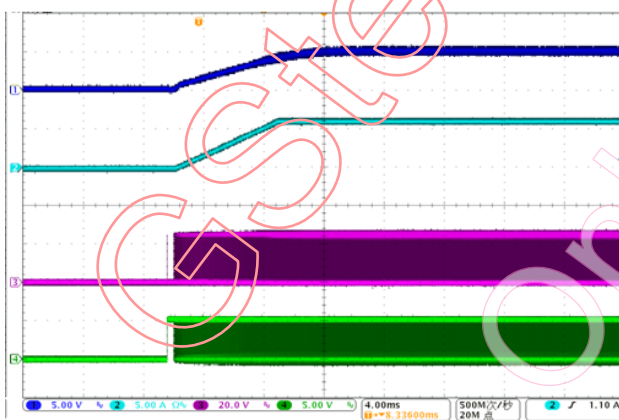
Power on from EN (DEM No Load)

CH1: VOUT CH2: EN CH3: UGATE CH4: LGATE



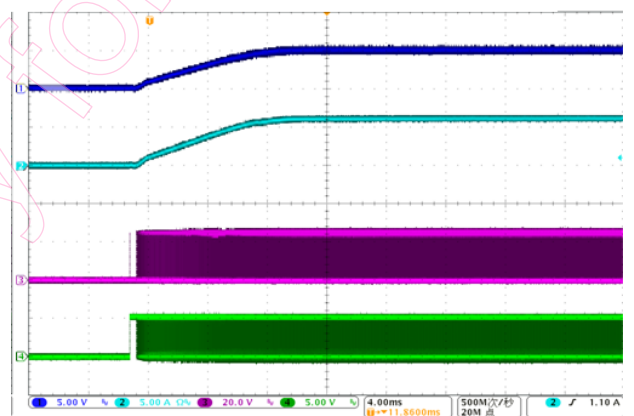
Power on from EN (6A Load)

CH1: VOUT CH2: IOUT CH3: UGATE CH4: LGATE



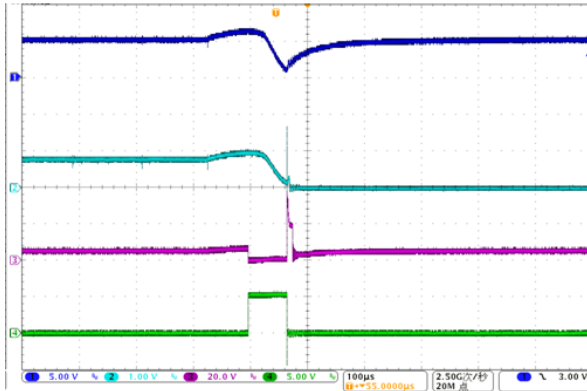
Power on from EN (833mΩ Load)

CH1: VOUT CH2: IOUT CH3: UGATE CH4: LGATE



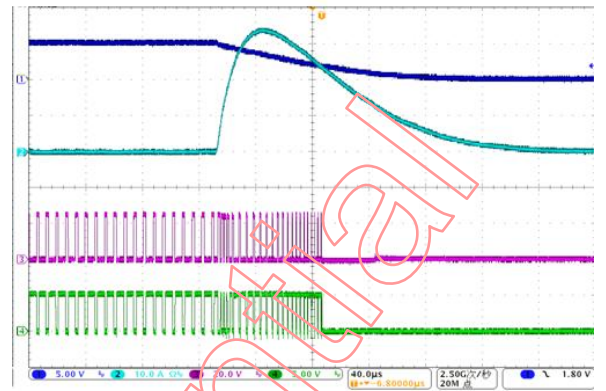
OVP

CH1: VOUT CH2: FB CH3: UGATE CH4: LGATE



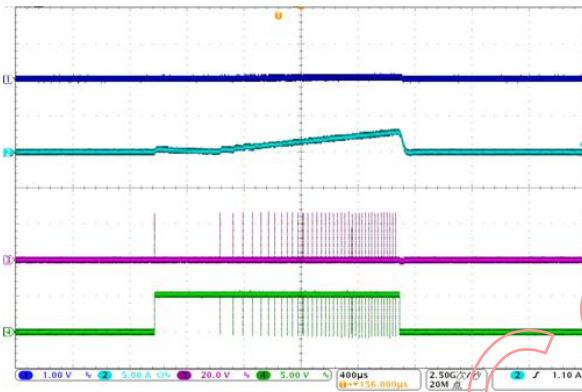
UVP

CH1:VOUT CH2:IOUT CH3: UGATE CH4: LGATE



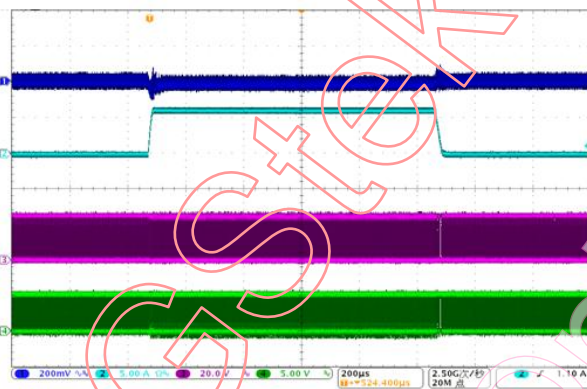
Power ON in Short Condition

CH1:VOUT CH2:IOUT CH3: UGATE CH4: LGATE



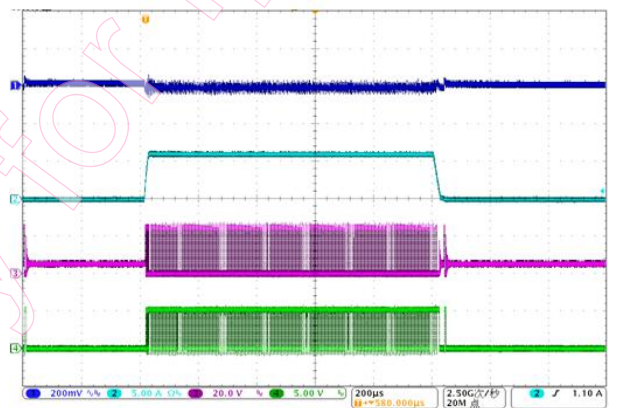
Load Transient CCM Mode(0A to 6A)

CH1:VOUT CH2:IOUT CH3: UGATE CH4: LGATE



Load Transient DEM Mode(0A to 6A)

CH1:VOUT CH2:IOUT CH3: UGATE CH4: LGATE



Application Information

The GS92B3 is small size chip with a relative constant on-time synchronous buck switching converter suitable for applications in notebook computers and other battery operated portable devices. Features include wide input voltage range, high efficiency and fast dynamic response.

System Clock Generator and PWM Control

The on-time of GS92B3 can be set by an external setting resistor from input voltage to TON Pin. The converter maintains the on-time width as loop feedback path exists between the GS92B3 converter, low pass filter and voltage divider. For a given input voltage buck application, the feedback maintains the constant on-time width. Due to the constant resistor and input voltage, the GS92B3 based buck converter has the relative constant frequency. Moreover, the GS92B3 can increase the duty-cycle automatically as input voltage falls down. Because of the constant on-time in each switching period, the converter maintains the relative frequency when the input voltage changes

At the beginning of each switching cycle, upper power MOSFET is turned on, after typical fixed on-time, the upper MOSFET is turned off, and then lower power MOSFET is turned on after internal dead time. The upper MOSFET will not be turned on at the beginning of next cycle until output voltage falls down below the preset voltage and the dead time passes. The same events repeat the following switching cycles. To avoid the surge inductor current during large load transient, a minimum Off-time is added. Typical minimum off-time is around 440ns. The too small on-time can affect soft-start and anti-noise ability, so in order to avoid the on-time too small to be eliminated; a minimum on-time is set to around 110ns. This should be noted in the small duty applications.

High Side Switch On-Time Count

The on-time is decided by the external setting resistor, and the input voltage. Looking at the TON pin, the input voltage is converted to current which is inversely proportional to itself by dividing the external setting resistor. The input voltage-proportional current is used to charge an internal capacitor from zero volts. When the voltage between two terminals of the capacitor reaches to the internal setting voltage, on-time one-shot pulse is generated, and then upper power MOSFET is turned off and lower power MOSFET is turned on.

We can count the on-time and switching frequency according to the equation below:

$$T_{ON} = (V_{OUT} \times R_{TON} \times 8p) / (V_{IN} - 0.8) \quad \text{for } V_{OUT} \leq 2.5V$$

If VOUT is higher than 2.5V, please set VOUT PIN voltage equal to 2.5V by divider resistors. And, the frequency can be calculated as equation below:

$$T_{ON} = (R_{TON} \times 20p) / (V_{IN} - 0.8) \quad \text{for } V_{OUT} > 2.5V$$

Then, the switching frequency is:

$$F_{SW} = V_{OUT} / (V_{IN} \times T_{ON})$$

R_{TON} is a resistor connected from the input supply (VIN) to the TON pin.

For heavy load (more than 8A) application, due to ground bounced and the high impedance of R_{TON}, the TON pin should always be bypassed to GND using a several nF-order ceramic capacitor for reliable system operation.

EN, PFM/PWM Mode and Shutdown Soft-Discharge

The EN/DEM pin enables the power supply. When EN/DEM is tied to high voltage (over V_{EN,H}) the GS92B3 is enabled and diode-emulated mode (DEM, which is power save mode) will be also enabled. When the EN/DEM is floating or tri-stated, an internal tri-stated judged logic module will activate the controller and the DEM Mode will be disabled.

In DEM mode, when the loads goes low, GS92B3 starts power save mode in order to maintain the on-time and

decrease the system clock frequency to skip PWM pulses for better efficiency. If DEM Mode is enabled, the GS92B3 zero crossing comparator will sense the inductor current and judge its value by comparing the LX node (LX) to PGND. Once the LX node voltage is equal to the PGND node voltage, the converter will enter the DEM Mode and turn off the low side power MOSFET. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than required the next switching cycle. The on-time is kept the same as that in the heavy-load condition.

If the EN/DEM pin is pulled low, the GS92B3 internal logic will shutdown the switching clock and stop the buck converter, and Discharge Module works to discharge the related output voltage through the VOUT pin. This will ensure that the output is in a defined state next time when it is enabled. Since this is a soft discharge, that there are no dangerous negative voltage excursions to be concerned about. In order to maintain the correct function of the soft-discharge module, the chip power supply must be online.

Output Voltage Selection

The output voltage is set by the feedback resistors R_{FB1} and R_{FB2} of Figure1a and Figure1b. The internal reference is 0.8V, so the voltage at the feedback pin is also 0.8V. Therefore the output can be set by the equation below:

$$V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times 0.8V$$

Current Limit

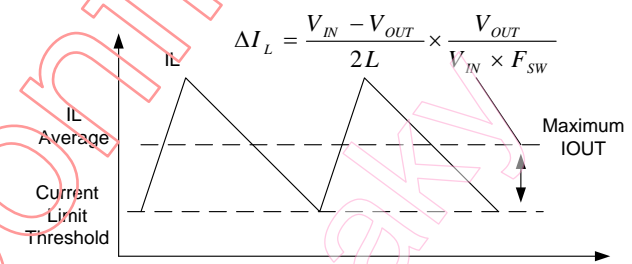
The GS92B3 uses the on-state resistance of the low-side power MOSFET as a current-sense resistor. In this case, the R_{CS} resistor between the LX pin and CS pin sets the over current threshold. This resistor R_{CS} is connected to a 20uA current source within the GS92B3 which is turned on when the low side power MOSFET turns on. When the voltage drop across the

low side power MOSFET equals the voltage crossing the current limit resistor R_{CS}, positive current limit will activate. The high side Power MOSFET will not be turned on until both the voltage drop across the sense element (low side power MOSFET) falls below the voltage across the R_{CS} resistor and the output voltage falls to pre-set value. The current sensing circuit actually regulates the inductor valley current. This means that if the magnitude of the current-sense signal at CS pin is above the current-limit threshold, the PWM is not allowed to initiate a new switching cycle. The equation for the current limit threshold is as follows:

$$I_{L_LIMIT} = 20\mu A \times R_{CS} / R_{DSL}$$

Where, R_{DSL} is the resistance of low side power MOSFET.

It is diagramed by the graph below:



Ensure that noise and DC errors do not corrupt the current-sense signal seen by CS and PGND. Mount the IC close t the low side power MOSFET and sense resistor with short, direct traces, making a Kelvin sense connection to the sense resistor.

Output Over-Voltage Protection

When the output voltage rises up to 125% of the preset voltage, the internal fault-logic module delays about 20us and turns on the low side Power MOSFET. It stays latched on and the GS92B3 is latched off until Power Reset or EN Reset.

Output Under-Voltage Protection

When the output voltage falls down to 45% of the preset voltage, the internal fault-logic module will delay about 20us and turns off both the high side and low side Power MOSFETs. Both switches stay latched off and

the GS92B3 is latched off until Power Reset or EN Reset. During soft-start, the UVP will be blanked, until soft-start procedure finished. The blank time depended on the value of the capacitor connected to SS Pin. But if the output voltage rises up above the UVP threshold tolerance during the counter period, the UVP counter is released immediately.

UVLO and Soft-Start

An internal under voltage lockout (UVLO) module is used to sense the VCC power supply. The PWM converter is forbidden by the under voltage lockout module. When VCC rises about 4.15V, the GS92B3 will initial the control logic circuitries and soft-start ramping generator, and then allows switching to occur. When VCC falls down to about 3.85V, the PWM converter is forbidden again.

When VAIN rises about 5.5V, the LDO output voltage (VCC) of GS92B3 enables and regulates a 5.15V voltage. After VAIN falls down to 5.3V the LDO (VCC) will turn off.

After soft-start module starting, the GS92B3 converter will release the current limit threshold followed the soft-start ramp. After UVP blanking time, the output under voltage protection and power good indicator is enabled.

FB Short Protection

Because the UVP protection is blanked during the soft-start period, if FB pin short to GND, the output voltage will increase continuously without OVP protection. It is a very dangerous condition. The GS92B3 build in a safety protection scheme to avoid this situation. When soft-start procedure begins, the GS92B3 monitors the output situations, if FB Pin short condition happens, the device will stop the switching cycle and latch on. Only Power on Reset and EN Reset can release this latch condition.

VOUT Pin

The Vout Pin offers feedback information of output

voltage. This information makes the ton more accurate, so the switching frequency variation is very small even when the GS92B3 operates on very wide input voltage range. When any fault condition occurs, the Vout Pin provides a discharge path from output to gnd.

External Devices Selection

For loop stability, the 0 dB frequency (f0), defined in the follow equation:

$$f_0 = \frac{1}{2\pi \times RESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

The loop stability is determined by the output capacitor. Specialty polymer capacitors have COUT in the order of several 100uF and RESR in range of 10mohm is recommended. However, ceramic capacitors have f0 at more than 700 KHz, which is not recommended.

In order for the right regulate manner, the ripple voltage at the feedback pin (FB), should be approximately 15mV. This generates Vripple= (VOUT/0.8) x15mV at the output node. The output capacitor RESR should meet this equation.

The external device selection is list below:

Choose Feedback Voltage Divider Resistor

Set RFB2=1K~20K ohm

$$R_{FB1} = \frac{(V_{OUT} - 0.8)}{0.8} \times R_{FB2}$$

Choose RTON

$$T_{ON(Max)} = \frac{1}{f_{SW}} \times \frac{V_{OUT}}{V_{IN(Min)}}$$

$$R_{TON(MAX)} = (V_{IN} - 0.8) \times 375K$$

Choose Inductor

Set the ripple current approximately 1/4 to 1/2 of the maximum output current. 1/3 is recommended. The recommended inductor can be calculated from the output current, indicated by formula below

$$L_{IND} = \frac{3}{I_{IOUT(max)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}}$$

For applications that require fast transient response with minimum VOUT overshoot, consider a smaller inductance than above. The cost of a small inductance value is higher steady state ripple, larger line regulation, and higher switching loss.

Choose Output Capacitors

$$RESR = \frac{1}{I_{ripple}} \times \frac{V_{OUT}}{0.8} \times 0.015$$

$$\approx \frac{3}{I_{OUT(max)}} \times \frac{V_{OUT}}{0.8} \times 0.015$$

$$RESR \approx \frac{V_{OUT}}{I_{OUT(max)}} \times 75(\text{mohm})$$

Organic semiconductor capacitors are recommended.

Choose Soft-Start Capacitor

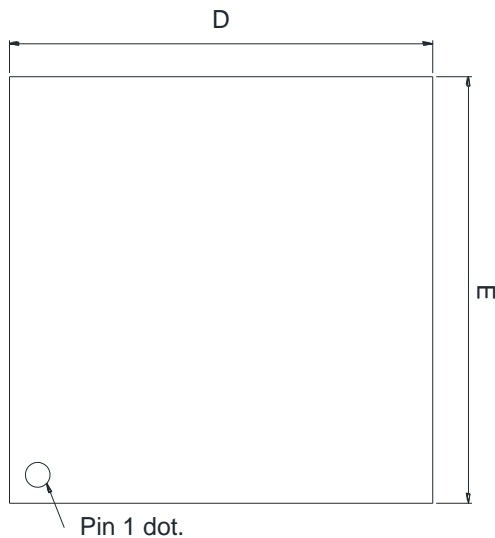
When SS ramp rise up to about 1.6V, the chip thinks the soft-start procedure is over, and then, release the UVP protection function. At the same time, the VOUT voltage will reach the target set by the FB resistor divider. So, the total soft-start time is defined by the formula below:

$$T_{SS} = \frac{1.6 \times C_{SS}}{I_{SS}} = 1.6 \times 10^8 \times C_{SS}(\text{ms})$$

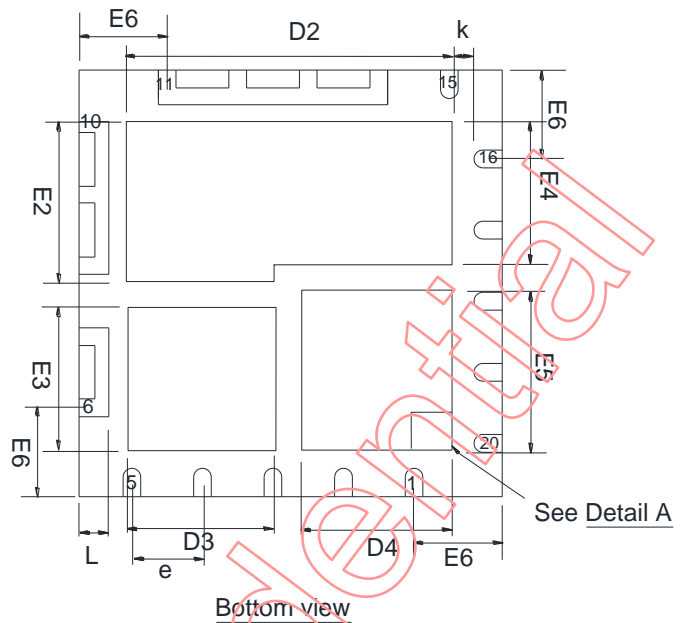
Where, the unit of Tss is mS.

For example, the typical Tss is equal to 1.6mS with 10nF C_{SS}.

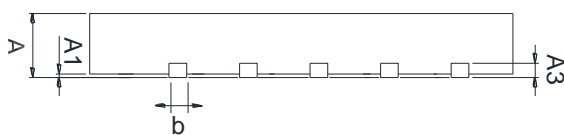
Package Dimensions, TQFN20-5x5



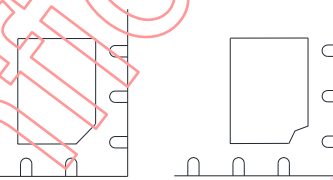
Top view



Bottom view



Side view



Detail A

Pin #1 ID Options
 Note: The configuration of the Pin#1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions in Millimeters | |
|--------|---------------------------|------|
| | Min | Max |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.203 REF. | |
| b | 0.25 | 0.35 |
| D | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 |
| D3 | 1.67 | 1.88 |
| D4 | 1.72 | 1.93 |
| E | 4.90 | 5.10 |
| E2 | 1.80 | 2.00 |
| E3 | 1.60 | 1.80 |
| E4 | 1.80 | 2.00 |
| E5 | 1.60 | 1.80 |
| E6 | 1.10 REF. | |
| e | 0.80 REF. | |
| k | 0.20 REF. | |
| L | 0.30 | 0.40 |

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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