# LT1008P

## USB TypeC PD2.0/PD3.0,QC3.0/QC2.0, FCP,SCP, AFC, Apple 2.4A,BC1.2 ,MTK PE+ High Voltage Charger Protocol

## FEATURES

- USB Power Delivery (PD) Rev.3.0 Certified Provider
- Provides USB PD 5V, 9V,12V Source Power Output
- USB Type-CTM Rev.1.2 Compliant Source
- Supports Qualcomm® Quick Charging 3.0/2.0(QC3.0/QC2.0)™ Protocol
- Supports HiSilicon® Fast Charge Protocol(FCP/SCP)
- Supports Samsung® Adaptive Fast Charging(AFC)
- Supports MediaTek® Pump Express Plus(PE+)
- Meets Battery Charging Specification BC 1.2 for DCP
- Supports USB DCP applying 2.7V on DP and DM line, output Current up to 2.4A for Apple® Device
- High Voltage and Safety Integration
- Overvoltage, Under-voltage, Overcurrent, Over-temperature Protection and VBUS Discharge
- Input Pin for Fast Shutdown Under Fault
- Internal N-channel HV MOSFET integration for best cost
- Overvoltage Protection on CC1, CC2, DP and DM
- Wide VIN Supply (4.25-16V)
- Supports NTC
- Low Quiescent Current when Unattached (Typical 20uA)
- Package: SSOP-16

## APPLICATIONS

- Car charger
- USB Power Output Ports
- AC power Adapter for cellphone, notebook, tablet, VR box, UAV, robot Adapte

## DESCRIPTION

The LT1008P is a low-cost USB Power Delivery Port Controller which is fully compliant to USB Power Delivery 3.0 version and Type-C revision 1.2 and BC 1.2 and other non BC1.2 standards like YD/T 1591-2009 Apple® & Samsung® Charging Spec, HiSilicon® Fast Charge Protocol, Qualcomm® Quick Charging™ 3.0/2.0.

The LT1008P monitors the CC pin to detect when a USB Type-C sink is attached, then it turn on VBUS and automatically detect whether a connected Device is USB PD 3.0 or Quick Charge 2.0/3.0 or FCP/SCP or AFC or PE+ Capable before enabling output voltage adjustment. If the Device not compliant to which description , it disables output voltage adjustment to ensure safe operation with legacy 5V.Protection features include overvoltage protection, undervoltage protection, overcurrent protection, over-temperature, overvoltage protection on CC1, CC2, DP and DM, and except overvoltage protection on CC1, CC2, DP, DM, system override to turn off VBUS and restart to detecting.

The LT1008P typically draws 20uA when no device is attached. Additional system power saving is achievable by using the Port Attachment Indicator (UFP) output to disable the power source when no device is attached.

The LT1008P is available in SSOP16 package.

## Ordering Information

| Part Number | Marking | Functional Specifications | Package |
|---|---|---|---|
| LT1008P2 | LINTOP<br>LT1008P2 | 5V/9V ( MAX:18W ) | SSOP16 |
| LT1008P3 | LINTOP<br>LT1008P | 5V/9V/12V ( MAX:18W ) | SSOP16 |

Marking：
1:LINTOP
2:LT1008P (Part Number)
3:XXXXXX(Lot Number)

## Typical Application Schematic

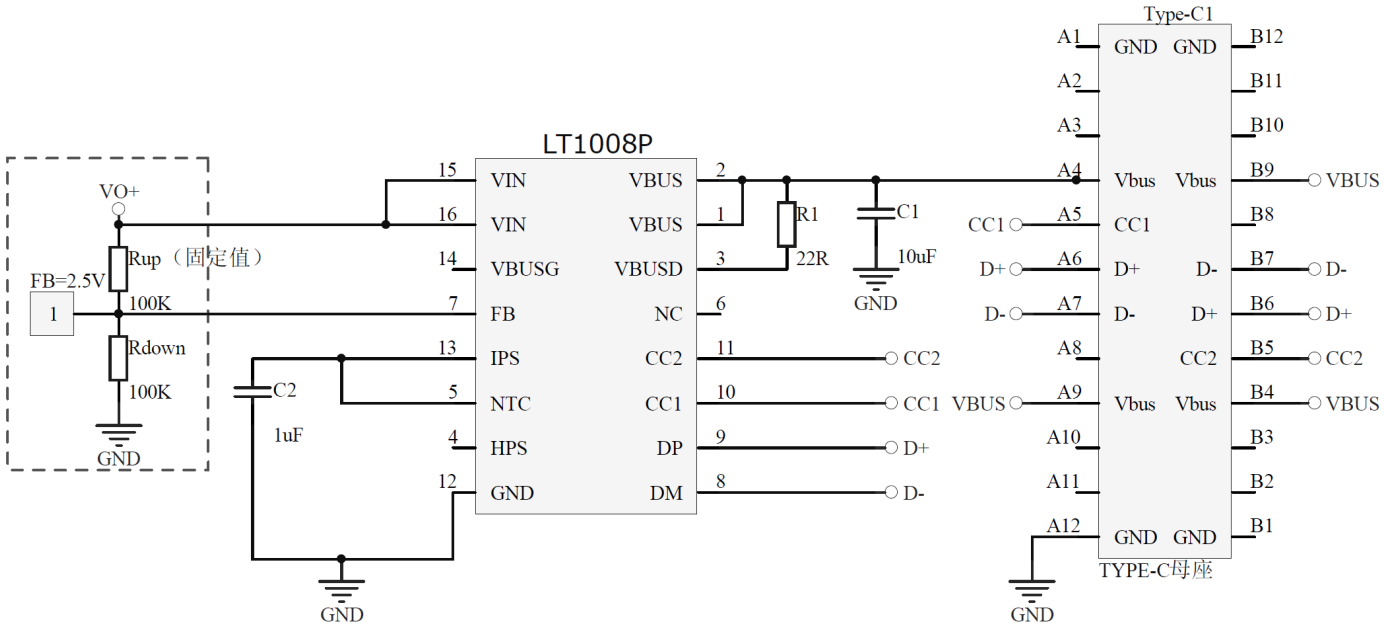



**Figure 1.**

## PACKAGE REFERENCE

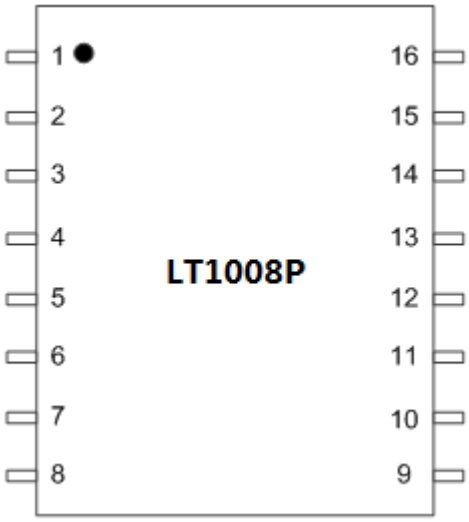



**Figure 2.**

## PIN DESCRIPTION

| NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | VBUS | The voltage monitor for VBUS line, which is the high-side power conductor |
| 2 | VBUS | The voltage monitor for VBUS line, which is the high-side power conductor |
| 3 | VBUSD | Open-drain output to discharge the system VBUS line through an external resistor |
| 4 | HPS | A five-state input used for selecting the maximum power that can be provided. |
| 5 | NTC | External shutdown control, can be configured for OTP by connecting an NTC resistor to GND |
| 6 | NC | --- |
| 7 | FB | Current source/sink output for output voltage adjustment |
| 8 | DM | USB negative data line |
| 9 | DP | USB positive data line |
| 10 | CC1 | Configuration channel interface pin to USB Type-C |
| 11 | CC2 | Configuration channel interface pin to USB Type-C |
| 12 | GND | Power ground |
| 13 | IPS | Internal regulated power supply for PMU, need a bypass capacitor |
| 14 | VBUSG | High voltage open drain gate driver used to drive NMOS power switch, connected to the gate terminal |
| 15 | VIN | External voltage source |
| 16 | VIN | External voltage source |

## ABSOLUTE MAXIMUM RATINGS (1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage Range（To PGND） | $V_{BUSG}$,$V_{BUS}$, VIN, $V_{BUSD}$ | -0.3 | 16 | V |
| | $V_{(VBUSG)–V(VBUS)}$ | -0.3 | 7 | V |
| | Others | -0.3 | 6 | V |
| Operating Junction Temperature | $T_J$ | -40 | 150 | ℃ |
| Storage Temperature Range | $T_{STG}$ | -65 | 150 | ℃ |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**ESD RATING**

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $V_{ESD}$ | CC1/CC2/DP/DM | ±8000 | V |
| | Others | ±2000 | V |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 100 | ℃/W |
| $R_{\theta JCtop}$ | Junction-to-case(top) thermal resistance | 36 | ℃/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45 | ℃/W |

**RECOMMENDED OPERATING CONDICTIONS**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VIN}$ | Input Supply Voltage | 4.5 | | 15 | V |
| $R_{VBUSD}$ | Series Resistance | | 22 | 100 | Ω |
| $C_{IPS}$ | IPS Bypass Capacitance | 0.1 | | 2.2 | μF |
| $C_{VBUS}$ | Output Capacitance | 2.2 | | 10 | μF |
| $R_{FBUP}$ | Feedback Pull-up Resistor | | 100 | | KΩ |
| $T_A$ | Operation Temperature Range | -40 | | 85 | ℃ |

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated in a specific test condition the following Conditions apply: TJ =25℃, 5V≤VVIN≤15V, CIPS=1Uf

| PARAMETER | | TEST CONDICTIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Supply (VBUS, VIN) | | | | | | |
| $V_{VIN\_TH}$ | VIN UVLO threshold | Rising edge | | 3.7 | | V |
| | | Falling edge | | 3.4 | | |
| | | Hysteresis | | 0.3 | | |
| $V_{VBUS\_TH}$ | $V_{BUS}$ UVLO threshold | Rising edge | | 4.45 | | V |
| | | Falling edge | | 3.9 | | |
| | | Hysteresis | | 0.55 | | |
| $I_{VIN}$ | Quiescent Current | VIN=5V，CCx open | | 20 | | uA |
| $I_{SUPP}$ | Operating current while sink attached | VIN=5V，VBUS=5V | | 2 | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| Voltage Protection (VBUS) | | | | | | |
| $V_{FOVP}$ | Fast OVP threshold, always enabled | Ref to target voltage | | +20% | | V |
| $V_{SOVP}$ | Slow OVP threshold | Ref to target voltage | | +15% | | V |
| $V_{SUVP}$ | VBUS UVP threshold | Ref to target voltage | | -22% | | V |
| IPS | | | | | | |
| $V_{IPS}$ | Output voltage | 0 ≤ $I_{IPS}$ ≤$I_{IPS\_EXT}$ | | 3.65 | | V |
| $I_{IPS\_EXT}$ | External load allowed | | | | 5 | mA |
| Discharge (VBUSD) | | | | | | |
| Fast discharge | ON state (linear) | Internal switch | | 6 | | Ω |
| Slow discharge | ON state (saturation) | Internal resistor | | 1000 | | Ω |
| Switch MOSFET | | | | | | |
| RDSON | | | | 12 | | mΩ |
| NMOS gate driver (VBUSG, GDNS) | | | | | | |
| IN VBUSG ON | Sourcing current | 0V ≤ VGDNS ≤ 25V, 0V ≤ V VBUSG - VGDNS ≤ 6V | | 10 | | uA |
| V VBUSG ON | Sourcing voltage (V VBUSG - VGDNS) | 0V ≤ VGDNS ≤ 25V, I VBUSG ON ≤4uA | 4 | | 6 | V |
| Transmitter (CC1, CC2) | | | | | | |
| RTX | Output resistance | During transmission | | 50 | | Ω |
| VTXHI | Transmit HIGH | | | 1.25 | | V |
| VTXLO | Transmit LOW | | -75 | | 75 | mV |
| tUI | Bit unit interval | | | 3.3 | | us |
| tBMC | Rise/fall time of BMC | Rload=5.1k,Cload=1nF | 300 | | 600 | ns |
| Receiver (CC1, CC2) | | | | | | |
| VRXHI | Receive HIGH | | 800 | 840 | 885 | mV |
| VRXLO | Receive LOW | | 485 | 525 | 570 | |
| IRP_SRC | CC1/CC2 Broadcasting current | 3A DFP mode, 0 ≤ $V_{CCX}$ ≤ 2.5V | 304 | 330 | 356 | uA |
| | | 1.5A DFP mode, 0 ≤ $V_{CCX}$ ≤ 1.5V | 166 | 180 | 194 | uA |
| VOVP_CC | CC1/CC2 OVP threshold | | | | 5.5 | V |
| OCP (ISEN, VBUS) | | | | | | |
| VITRIP | Shunt voltage when OCP tripped | Ref to Power Capability(pd) | | +30% | | A |
| OTP (internal) | | | | | | |
| TJ1 | Die temperature | Temperature rising edge | 125 | 135 | 145 | ℃ |
| | | Hysteresis | | 20 | | ℃ |
| NTC | | | | | | |
| VOTPDET | External OTP based on NTC | Temperature rising edge | | 0.3 | | VIPS |
| | | Hysteresis | | 0.1 | | VIPS |

| | | | | | | |
|---|---|---|---|---|---|---|
| HVDCP interface (DP, DM) | | | | | | |
| VDAT(REF) | Date Detect Voltage | | 0.25 | 0.325 | 0.4 | V |
| VSEL(REF) | Output voltage selection reference | | 1.8 | 2 | 2.2 | V |
| TGLITCH(DP)HIGH | DP High Glitch Filter Time | | 1 | 1.25 | 1.5 | s |
| TGLITCH(DM)LOW | DM Low Glitch Filter Time | | | 1 | | ms |
| TGLITCH(V)CHANGE | Output Voltage Glitch Filter Time | | 20 | 40 | 60 | ms |
| TGLITCH(CONT)CHANGE | Continuous Mode Glitch Filter Time | | 100 | 150 | 200 | us |
| RDAT(LKG) | DP | | 300 | 500 | 800 | KΩ |
| RDM(DWN) | D- Pull-Down Resistance | | 14.25 | 19.53 | 24.5 | KΩ |
| RON(N1) | SwitchSW1 on-resistance | | | 40 | 100 | Ω |
| VTH(PD) | Data Line Capacitance | | 0.25 | 0.325 | 0.4 | V |
| TDPD | Output Device Connection Detection threshold | | 120 | 160 | 200 | ms |
| ΔIT(UP) | Output Device connection Detection Glitch Filter Time | RIREF=100KΩ | | 2 | | uA |
| ΔIT(DO) | Up Current Step | RIREF=100KΩ | | 2 | | uA |
| VOVP_DPDM | Down Current Step | | | | 5.5 | V |
| Apple 2.4A Mode | | | | | | |
| VDAT(2.7V) | D+/D- line output voltage | | 2.57 | 2.7 | 2.84 | V |
| RDAT(2.7V) | D+/D- line output Impedance | | | 15 | | KΩ |
| FCP Mode | | | | | | |
| VTX-VOH | D- FCP TX Valid High | | | 2.7 | | V |
| VTX-VOL | D- FCP TX Valid Low | | | | 0.3 | V |
| VRX-VIH | D- FCP RX Valid High | | | 1.2 | | V |
| VRX-VIL | D- FCP RX Valid High | | | 0.9 | | V |
| Trise | FCP Pulse Rise Time | 10% - 90% | | | 2.5 | us |
| Tfall | FCP Pulse Fall Time | 90% - 10% | | | 2.5 | us |

## Function Description

**Power Data Object Advertise**

The power advertised to PD Sinks is always 18 W. The LT1008P advertises 5V/3A, 9V/2A, 12V/1.5A&5V/3A, 9V/2A.

**Discharge Function**

In order to ensure the voltage change or abnormal protection VBUS voltage satisfies the requirement of PD in the prescriptive time，LT1008P supports Discharge Function.The external series resistor between VBUSD and VBUS is need if enabled this function,which recommended value for 22Ω (VBUS 10uf capacitance in parallel case, it is recommended to use 1/4 W or higher power encapsulated resistance)。

**FB**

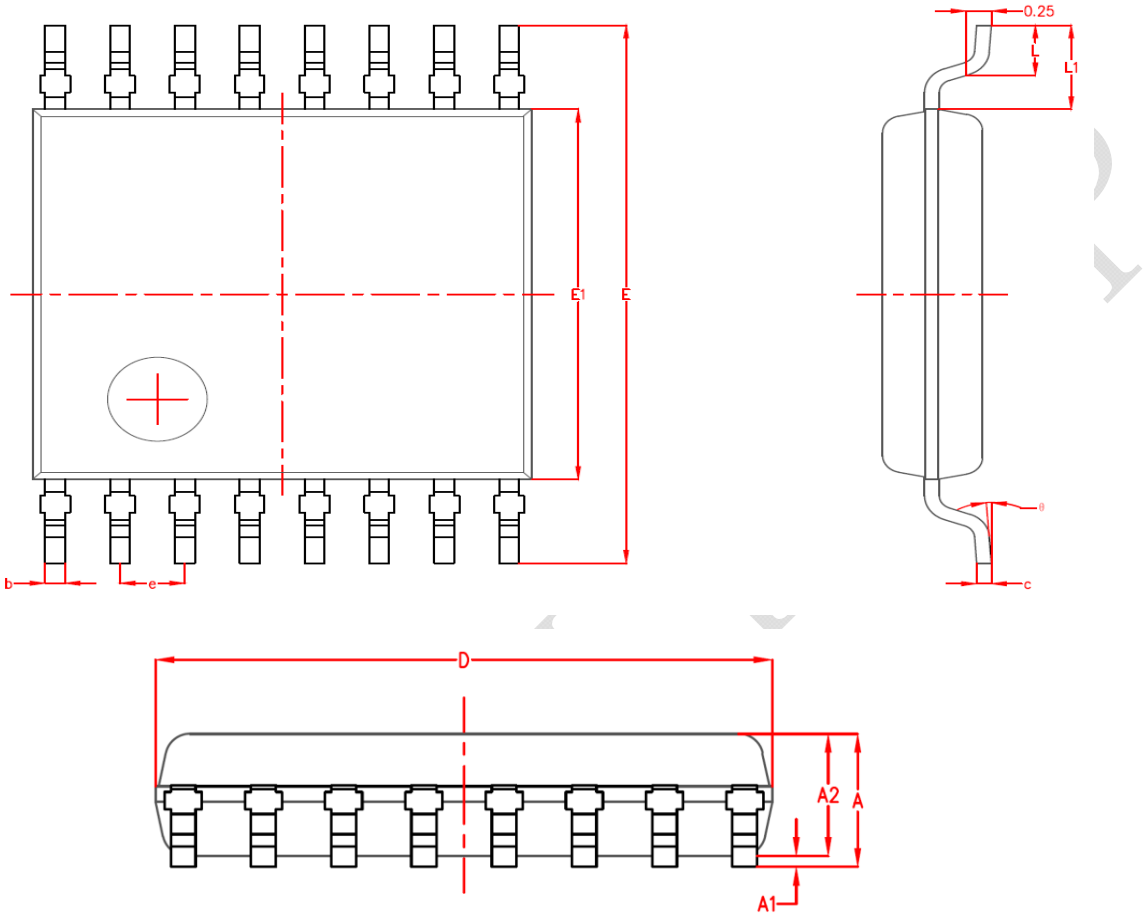
LT1008P through FB Source or Sink current to achieve voltage regulation for 2uA steps, thus FB need access to the system voltage feedback point and the pull up resistance value must be 100KΩ.

**NTC**

NTC can be used to closed the fast charge when pull it GND or when which voltage is lowed to 0.3 IPS can be used for NTC to closed Fast charge

# PACKAGING INFORMATION

## SSOP-16 PACKAGE OUTLINE DIMENSION




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.09 | 1.19 |
| A1 | 0.02 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.14 | 0.22 | 0.30 |
| c | 0.08 | 0.13 | 0.18 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65BSC | | |
| L | 0.5 | 0.60 | 0.70 |
| L1 | 1.05BSC | | |
| θ | 0° | 4° | 8° |