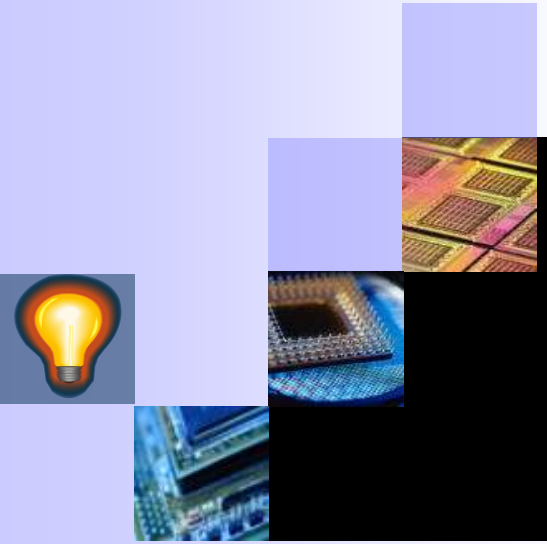


Sigrity 电源完整性（PI）信号完整性（SI）解决方案

2010-10-19

SIGRITY

Agenda

- 1: Sigrity公司简介
- 2: 直流电分析 PowerDC-E
- 3: 电热混合分析 PowerDC-T
- 4: 交流分析 PowerSI(3DFEM)
- 5: 电容优化 OptimizePI
- 6: 提取电路模型BroadBand SPICE
- 7: 时域分析 SPEED2000
- 8: 高速串行互连分析：Channel Designer
- 9: BUS DESIGNER
- 10: 封装模型提取与分析：XtractIM功能介绍

Sigrity公司简介

Sigrity 概况

- 混合仿真引擎的专利技术和电磁场算法的突破
- 业界的强烈需求和广泛采用
- 美国国家自然科学基金的支持

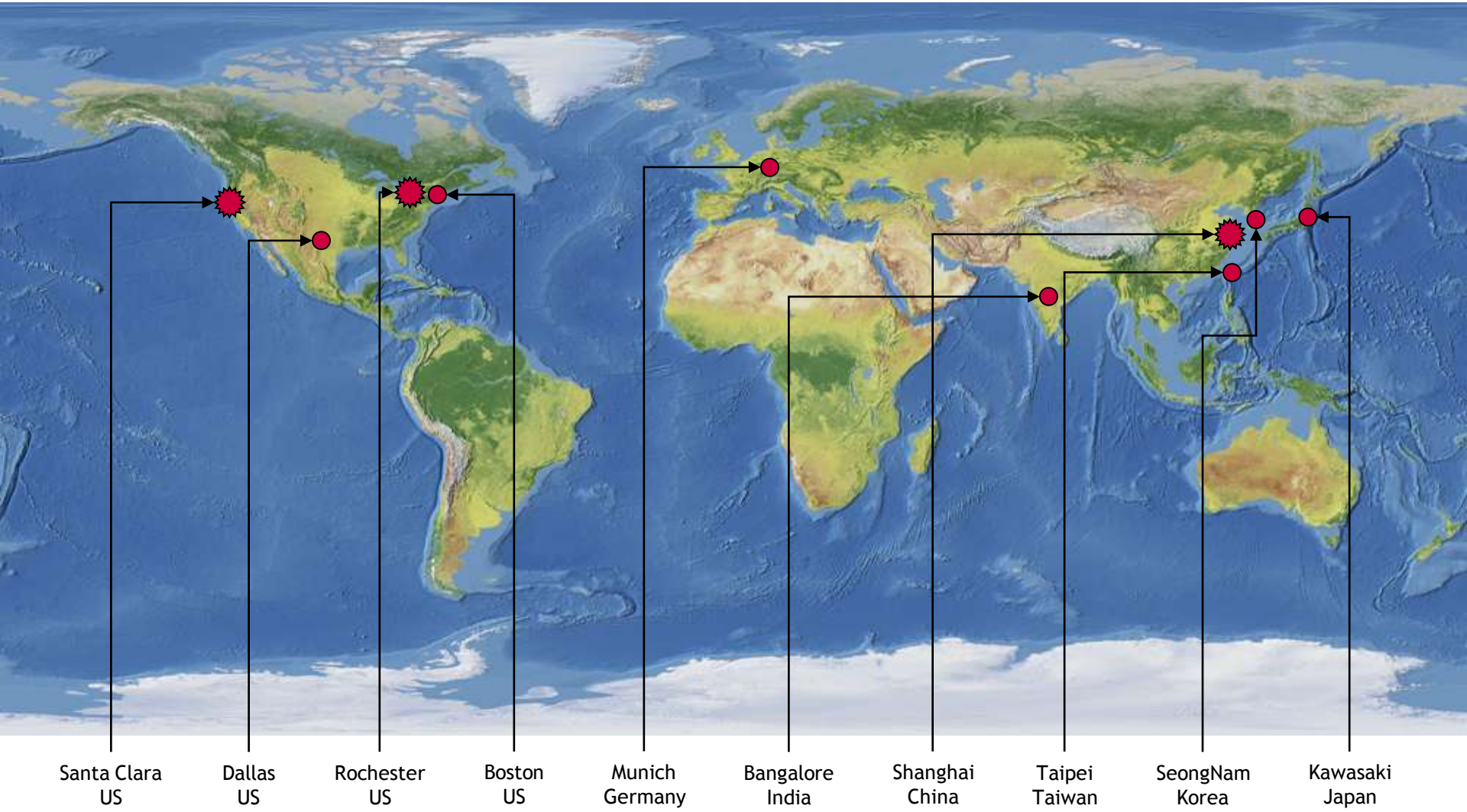
  Small Business Innovation Award (SBIR)

Sigrity 的团队

Development and Support Center

Support Center

www.sigrity.com

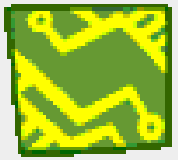


Sigrity的客户（200+）

半导体和封装厂商

IDM Semiconductor
8 of the top 10

Freescale
IBM Microelectronics
Intel
Infineon
Micron
NEC Electronics
NXP
Samsung
STMicroelectronics



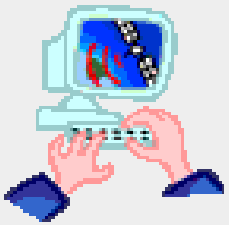
Fabless Semiconductor
8 of the top 10

Actel
Altera
Broadcom
IDT
LSI
Marvell
Micronas
nVidia
Xilinx

IC Packaging

Amkor
ASAT
ASE
GAPT
Kyocera
Shinko
Signetics
STATS ChipPAC
UTAC

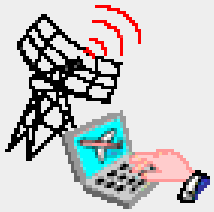
系统厂商



Computer

Apple
DELL
IBM
HP
SUN
EMC
NEC

Virtually all use Sigrity



Communications

2 Wire
Cisco
Extreme Networks
Juniper Networks
Qualcomm
Siemens
Tellabs

Consumer Digital

AVID
Canon
Eastman Kodak
LG Electronics
Matsushita
Philips
Samsung
Silicon Graphics
Sony

Aerospace & Defense

Draper Laboratory
Hughes Network Systems
NASA Goddard
Northrop Grumman
Raytheon

Sigrity的产品与服务

- *封装和板级的PI、SI分析*
  - *SPEED2000*
  - *PowerSI*
  - *PowerDC-E, PowerDC-T*
  - *OptimizePI*
  - *Channel Designer*
  - *Broadband SPICE*
  - *XtractIM*
- *芯片级的PI、SI分析*
  - *XcitePI*
- *封装的物理设计*
  - *UPD*
- *芯片、封装和板级的IO规划*
  - *OrbitIO*
- *软件与设计服务*
  - *Software Services – GES*
  - *Package Design and Training Service*

Sigrity客户成功案例

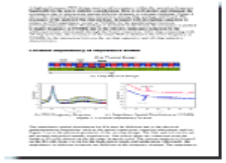
http://www.sigrity.com/success/cus_doc.htm

49. The Effects of Chip and Board Behavior on Package-Centric, System-Aware Power Delivery Design

-- Virendra Adsure, Long Wang, Jiang Li - Intel Corporation and Sigrity, Inc; DesignCon February 2009

A package Power Delivery System (PDS) is examined to determine the effects of both chip and board electrical behavior. Package performance is assessed assuming different levels of knowledge about related chip and board structures. Optimization of decoupling capacitor implementations for performance and cost addresses these situations. The increased accuracy of package analysis performed with both chip and board data is confirmed. Sigrity products referenced: OptimizePI.

Paper (PDF Format) Presentation (PDF Format)



48. Broadband Methodology for Power Distribution System Analysis of Chip, Package and Board for High-Speed IO Design

-- Hsing-Chou Hsu, Jack Lin - Via Technologies, AzureWave Technologies and Sigrity, Inc; DesignCon February 2009

This paper covers characterization utilizing frequency domain impedance information to assess power delivery system coupling and the impact this has on simultaneous switching effects for adjacent IO cells. A new method for integrated simulation is discussed along with key enabling technologies that enable the linking of broadband network parameter (BNP) information for chips, packages and boards. The resulting simulations identify frequency dependent issues and support what-if assessment of decoupling strategies. Sigrity products referenced: PowerSI and XcitePI.

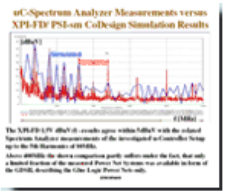
Paper (PDF Format) Presentation (PDF Format)

47. Switching voltage Regulator Noise Coupling Analysis for Printed Circuit Board Systems

-- Amy Luoh, Gene Garrison, John Powell - Intel Corporation; DesignCon February 2009

System reliability issues associated with switching voltage regulator noise are growing ... particularly for motherboard designers. This paper describes a simulation methodology developed to predict and prevent these problems. The simulation flow discussed identifies coupling between planes, shapes, transmission lines and vias for entire boards. Targeted design improvements were identified by the simulations and there was good agreement between these simulated results and measured values. Sigrity products referenced: SPEED2000.

Paper (PDF Format) Presentation (PDF Format)

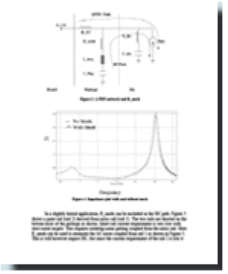


46. Time and Frequency Analysis of Signal Noise as a Function of Power Noise and Vice Versa of a Microcontroller Plus its Packaging

-- Ekkehard Miersch, Mehmet Goekcen, Thomas Steinecke - Infineon Technologies and EFM Consulting; DesignCon February 2009

The paper covers strategies for the assessment of signal and power integrity effects in complex systems that include chip and system level structures. Methods to determine current signatures are discussed along with frequency and time domain co-simulation techniques. Simulation results enable accurate assessment of distributed on-chip and package level decoupling capacitor implementations. Simulation results are correlated with measured data. Sigrity products referenced: XcitePI, SPEED2000 and PowerSI.

Paper (PDF Format) Presentation (PDF Format)



45. A novel methodology to handle the layout constraints for designing an optimal Power Delivery Network

-- Praveen Pai, Parthasarathy Ramaswamy, Julius Delino C Intel Corporation; DesignCon February 2009

Power Delivery Network (PDN) design flows focus on meeting in either the frequency domain or time domain targets to control issues such as noise or jitter margin. Successful design requires adapting to many constraints including keep out zones, narrow power shapes and mesh like structures on the power planes. The paper provides a new methodology to address these challenges. Simulation and lab data are provided for designing a good reference plane. Sigrity products referenced: PowerSI and SPEED2000.

Paper (PDF Format)

Sigrity产品一览表

- SPEED2000：第一个也是现今唯一一个可以进行 IC 封装或 PCB 整板时域电磁仿真的时域分析工具；
- PowerSI：先进的频域分析工具，可用于提取 IC 封装或 PCB 整板信号和电源的频域阻抗参数和 S 参数，及随频域变化的空间噪声分布；
- PowerDC：高效准确的直流分析工具，可用于 IC 封装或 PCB 整板的直流压降分析、电流密度分析和过孔电流的分析，感应线位置优化和直流 DRC 检查；
- OptimizePI：封装和 PCB 电源完整性分析及去耦电容优化设计工具，可用于给定目标阻抗情况下的最佳成本优化，给定电容类型情况下的最佳性能优化等；

- XtractIM：芯片封装的电性能提取工具，可提取 IBIS，SPICE 及宽带等效电路模型；
- Broadband Spice：宽频带高精度的模型转换工具，可以方便的将 N 端口的网络参数综合成 SPICE 等效电路模型；
- XcitePI：芯片级瞬态电源噪声分析工具，考虑了 IC 内部所有的容性和感性耦合；
- CoDesign Studio：芯片和封装的联合设计工具，可以在一个集成的设计环境中同时仿真芯片和封装结构；

- Unified Package Designer (UPD)：专业的IC封装设计工具，支持各种Wirebond、Flip-chip、Leadframe和SiP等封装类型，其独特的验证和优化布线方案可以确保封装的设计满足所有的加工和可靠性要求；
- OrbitIO Planner：芯片，封装及PCB系统IO互连的优化工具；
- Channel Designer：高速串行通道的专业分析工具，支持芯片的AMI模型和互连网络的S参数模型，能够仿真10Gbps以上系统的误码率（BER）指标

SpeedXP Suite简介

- **时域分析 - SPEED2000**
  - 信号网络的时域波形分析
  - 电源/地噪声的实时纹波分析和空间分布分析
  - 板级的EMI/EMC分析

- **频域分析 - PowerSI**
  - 电源与信号的网络参数（S/Y/Z）模型提取
  - 空间模式下的电容位置优化
  - 谐振模式分析

- **电路模型转换 - BroadBand SPICE**
  - 将网络参数（S/Y/Z）模型转换成高精度确保收敛性的SPICE 等效电路模型

- **直流分析，热分析 - PowerDC**
  - 直流压降，电流密度和过孔电流分析
  - VRM感应线的位置优化
  - 电热混合分析

- **串行通道分析 - Channel Designer**
  - 高速串行通道的眼图分析
  - 误码率分析
  - 支持器件的AMI模型

与其他布线工具的接口

Sigrity UPD

Cadence Allegro, APD, Specctra

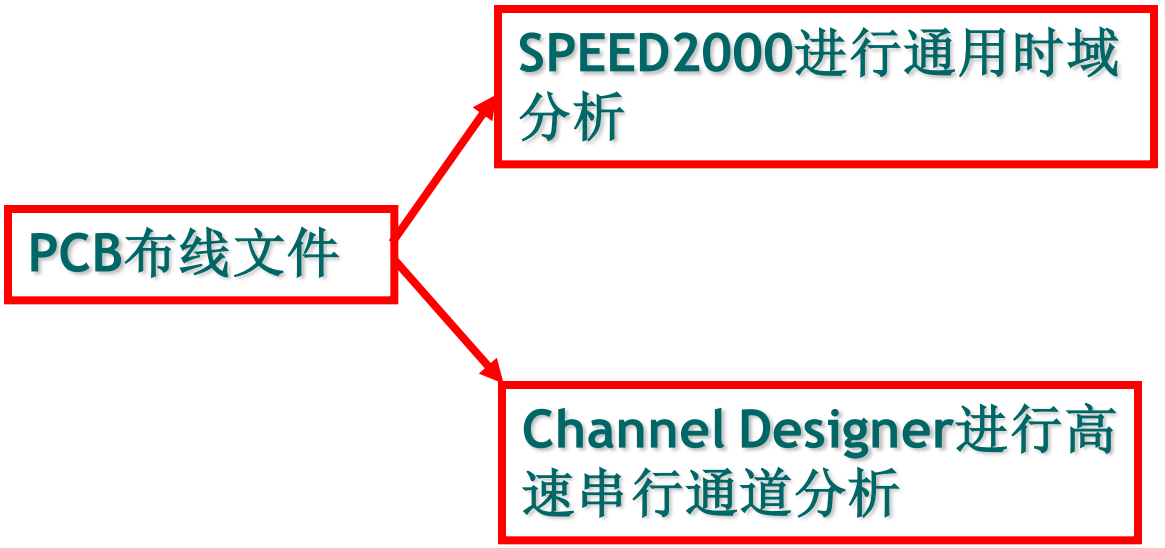
Mentor Graphics Boardstation, Expedition, PowerPCB, ICX

Zuken CR5000, Visula, CADstar

Altium Protel, P-CAD

Sigrity推荐的PI频域分析流程

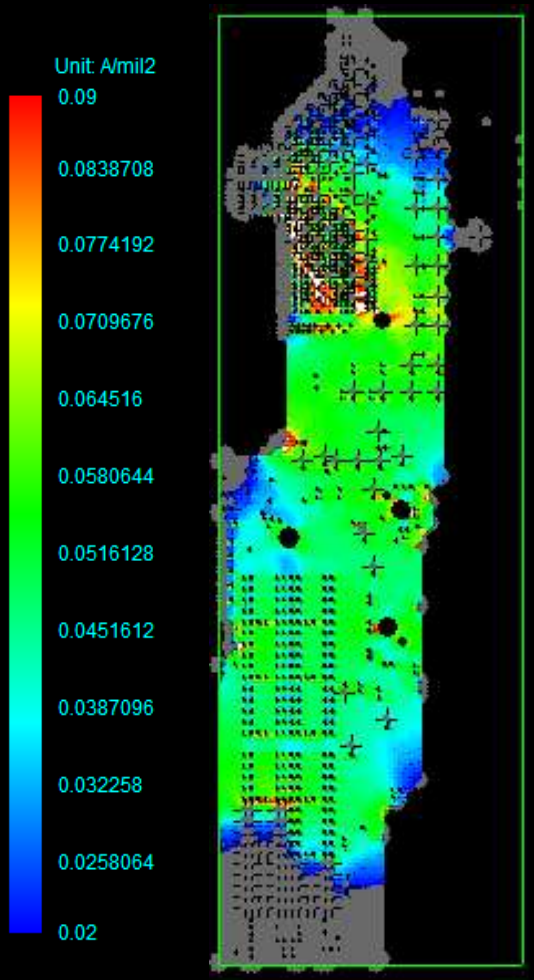
Sigrity推荐的SI时域分析流程



Sigrity PI/SI 仿真解决方案

直流电分析：PowerDC-E

不考虑直流问题 →冒烟 or 冒火?



常见DC问题1：直流压降（IR Drop）

- **IR Drop其含义为直流工作时由直流电阻造成的电压降，而此时的压降可直接由 I * R 的乘积得到因而得名**

- **ASIC芯片的正常工作需要持续稳定的电压源**
  - 芯片厂商一般允许电压可以在一定范围内波动；
  - 电源的波动实际是由 DC损耗和 AC噪声这两部分构成的；
  - **IR Drop**的容限通常为供电电压的 5%（或更低）；
  - 如果总的容限为常数，那么降低了 DC损耗将为 AC噪声留出更大的设计余量

- **各种设计中的不利因素使DC IR Drop问题加剧**
  - 核心供电电压持续减小：**1.2V**供电变得司空见惯；
  - 器件的工作电流持续增大，使 **IR Drop**也有不断增大的趋势；
  - 层数变少和高密度布线使电源网络的布线空间受到压缩和限制；
  - 过孔周围的反焊盘使原来完整的电源平面变得支离破碎；
  - 越来越复杂的PCB结构使非常有经验的工程师也难以靠手工完成 **IR Drop**的计算

- **IR Drop是一个系统级的问题**
  - 分析中有时需要考虑封装以及多个子板的整个系统级的PDN网络；
  - 需要优化系统中每个器件的电压容限，确保他们都能正常工作；
  - 有些高端系统的 **VRM**还带有电压反馈，反馈线的设计需要科学布局才能发挥最大效果

常见DC问题1：IR Drop分析的重要性

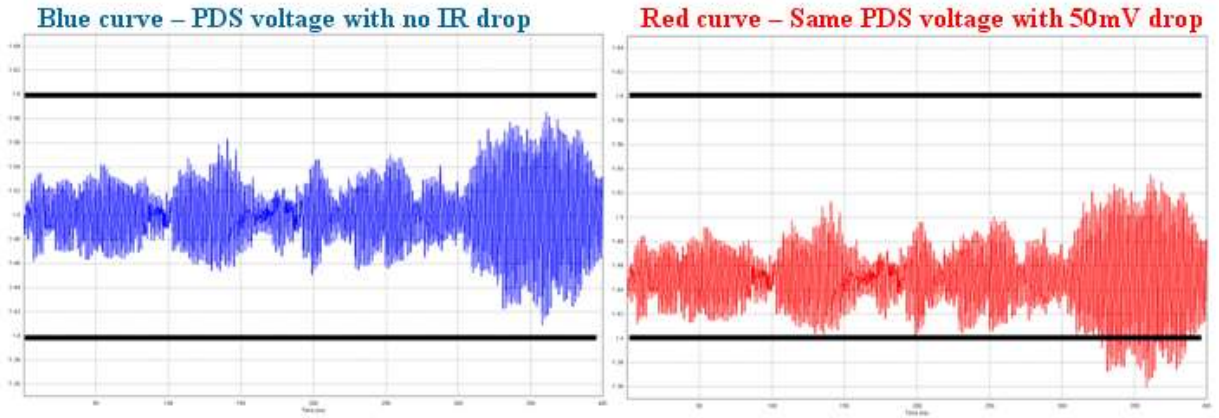


Fig1 IR Drop使系统的电压波动超标，系统不能正常工作

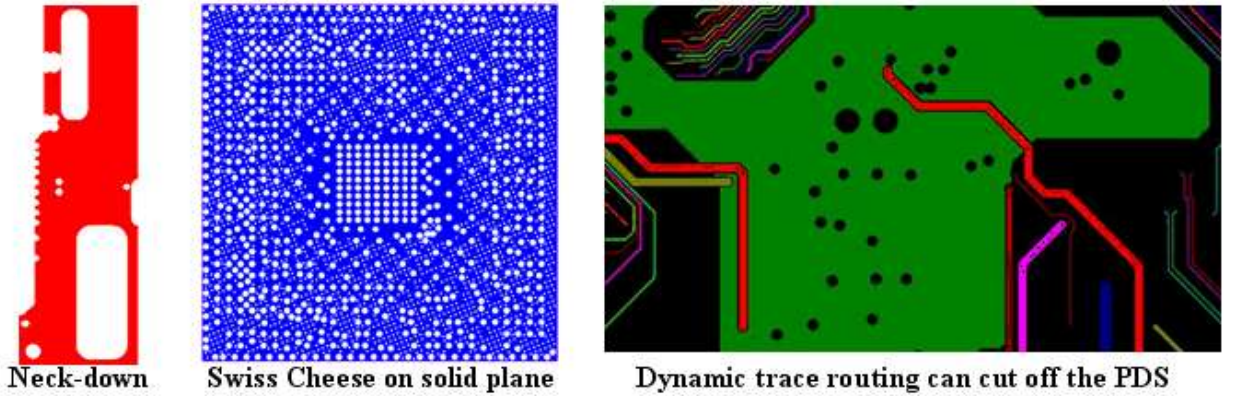


Fig2 各种设计中的不利因素使 IR Drop的问题加剧

常见DC问题2：电流密度

- 当电流通过一个狭窄区域的时候，通常会产生较大的电流密度，从而导致PCB板局部温度的升高。
- 电源平面上最大的电流密度区域通常称之为电流热点（Hot Spot），这些电流热点有可能导致严重的热可靠性问题。
- 设计人员应尽量使板上的电流密度分布均匀， 并且最大值尽量不要超过常用的经验门限100A/mm2。

PowerDC的算法及理论基础

- PowerDC基于电磁场理论求出电源/地平面上的电压分布、电流密度的矢量分布，过孔电流和电阻。

- 全新的FEM仿真引擎在仿真精度和效率上有了很大的提升。其精细的三角形网格剖分比其他工具采用的矩形网格在计算结果和显示精度上要先进很多，另外特有的快速算法使工具即使在仿真大型PCB时也仅需数分钟的时间。

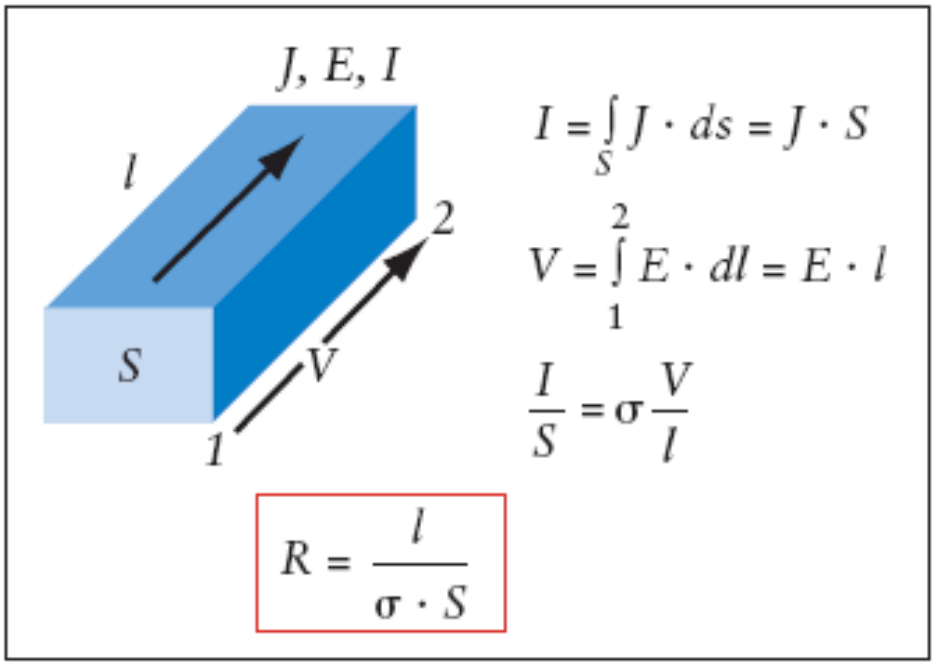
电路理论基础

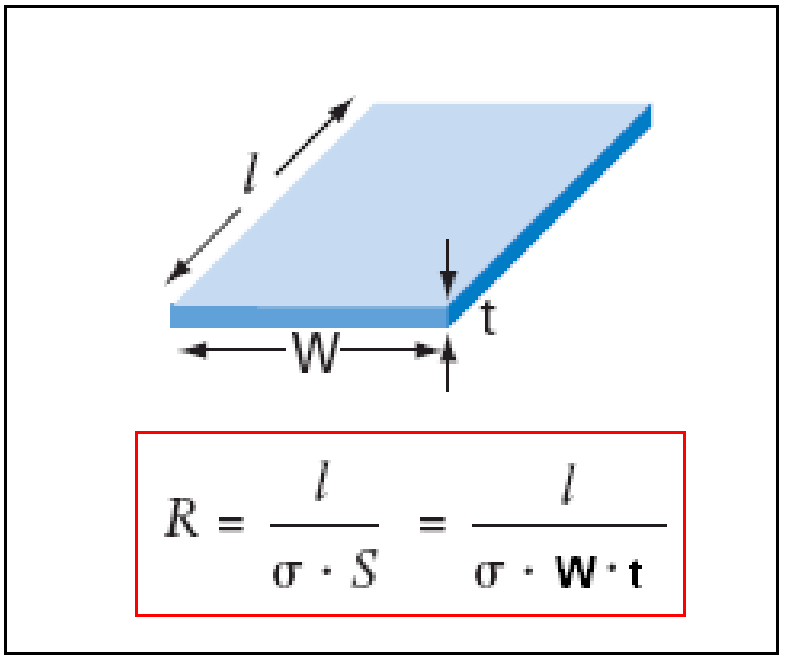
- 电路理论是电磁场理论在低频段的近似表达方式

- 将低频近似引入到Maxwell方程中，可以得到以下结论：
  - Kirchoff电压定律：环路中的电压代数和为0；
  - Kirchoff电流定律：流入一个电路节点的电流代数和为0

电阻

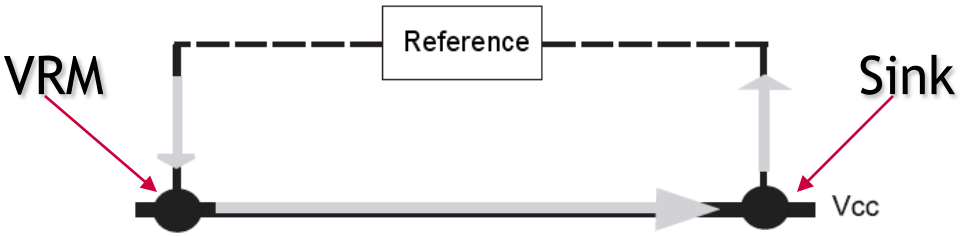
- 欧姆定律定义了电阻为穿过一个导体上的电压与电流的比值，即R=V/I。





σ 为材料的电导率，铜的电导率为 5.8×10^7 S/m

精度比对1（与理论计算相比）



- 200mm long (L)
- 10mm wide (W)
- 5um thick (T)
- conductivity is 5.8e7 S/m (σ).

➢ 上述案例为一个矩形的Vcc电源平面，VRM和Sink的电压观测点均参考同一个Reference节点。

➢ 分析：平板电阻，$R = L/(\sigma \times W \times T) = 0.06862 Ohms$

假设VRM的供电电压为1V，Sink的工作电流为1A，则 IR Drop＝1*0.06862＝0.06862 (V)，因此Sink Voltage＝1-0.06862≈0.9314 (V)

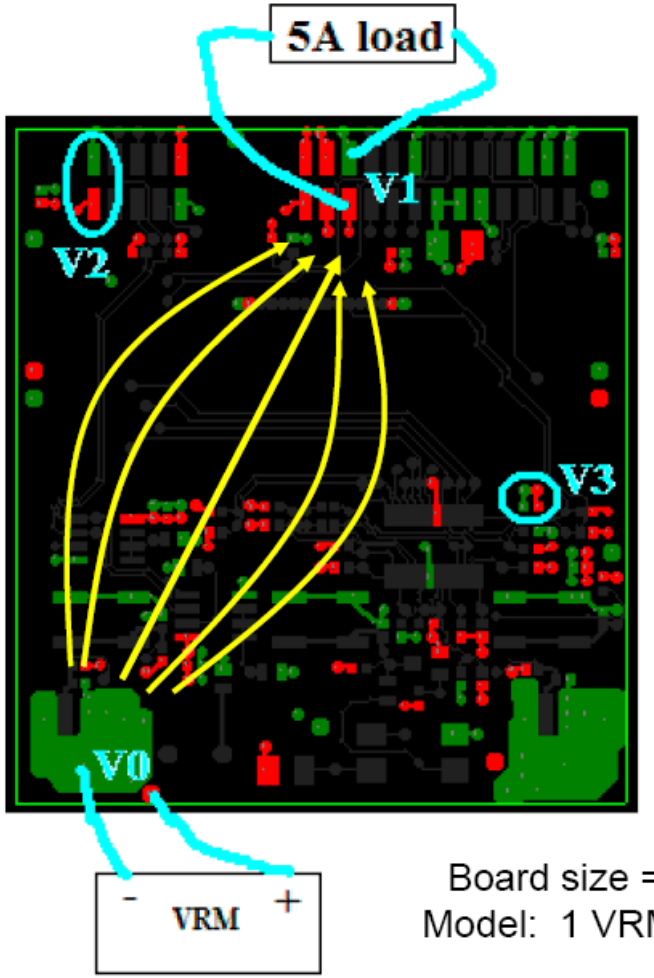
➢ 仿真结果如下，Sink端得到的实际电压也为0.9314V，与理论计算的结果吻合的非常好。

Show Results -> Sink Voltage (1 of 1 Failed)

VRM Voltage | **Sink Voltage** | Interconnect Current | Probes Measurements | Global Via Current | Global Via Current Density | Specific Via Curre

Sink Name	Model	Nominal Voltage (V)	Input Tolerance (%)	Actual Voltage (V)	Margin (V)
Sink	Equal Voltage	**1**	0	**0.931405** ✘	**-0.0685946**

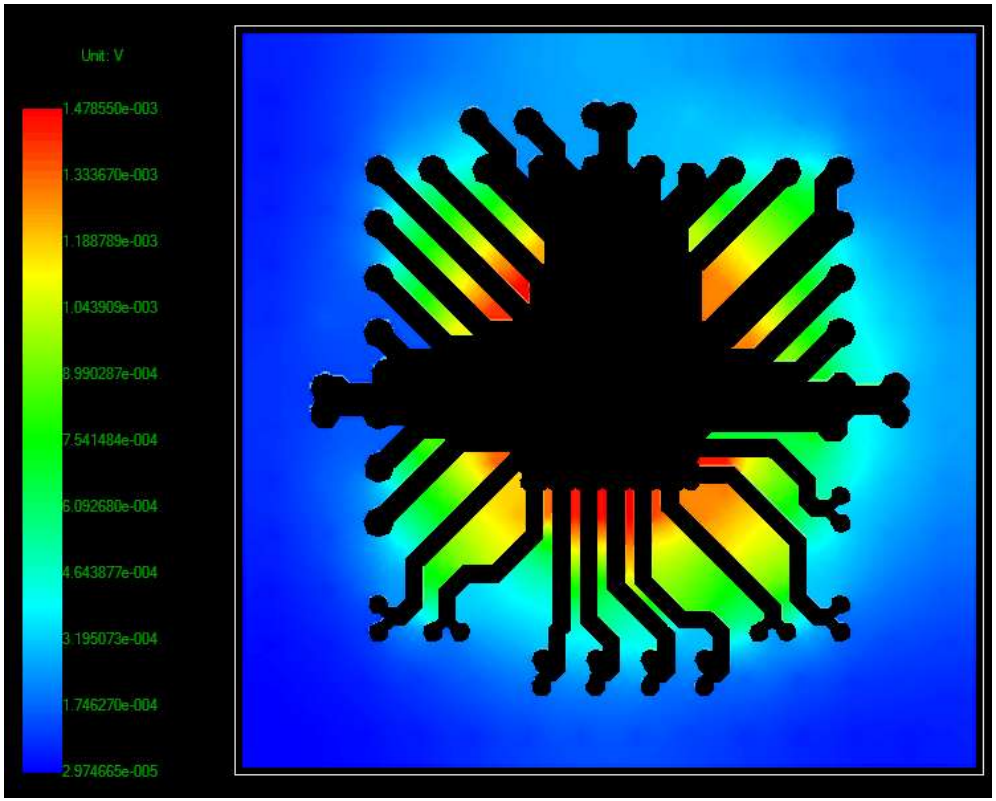
精度比对2（与Lab实测相比）

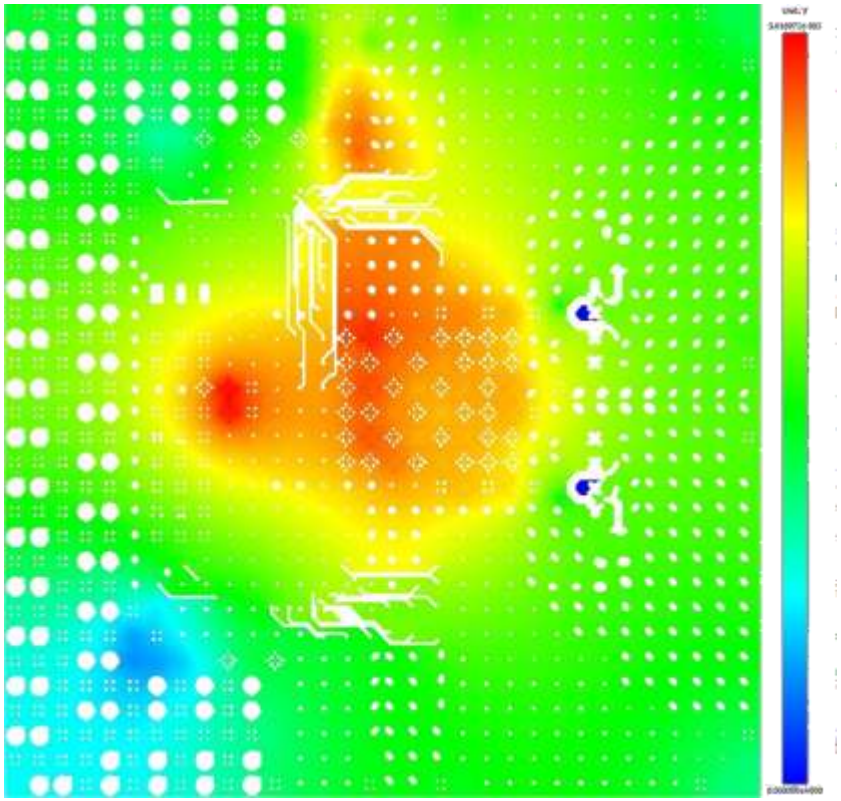


Location	Voltage drop (mV)	
	Measurement	**PowerDC**
V0-V1	35	36.1
V0-V2	12	11.0
V0-V3	9	9.3

Board size = 2.28” x 2.52” 4 layers board,
Model: 1 VRM, 1 load, 2 observation points

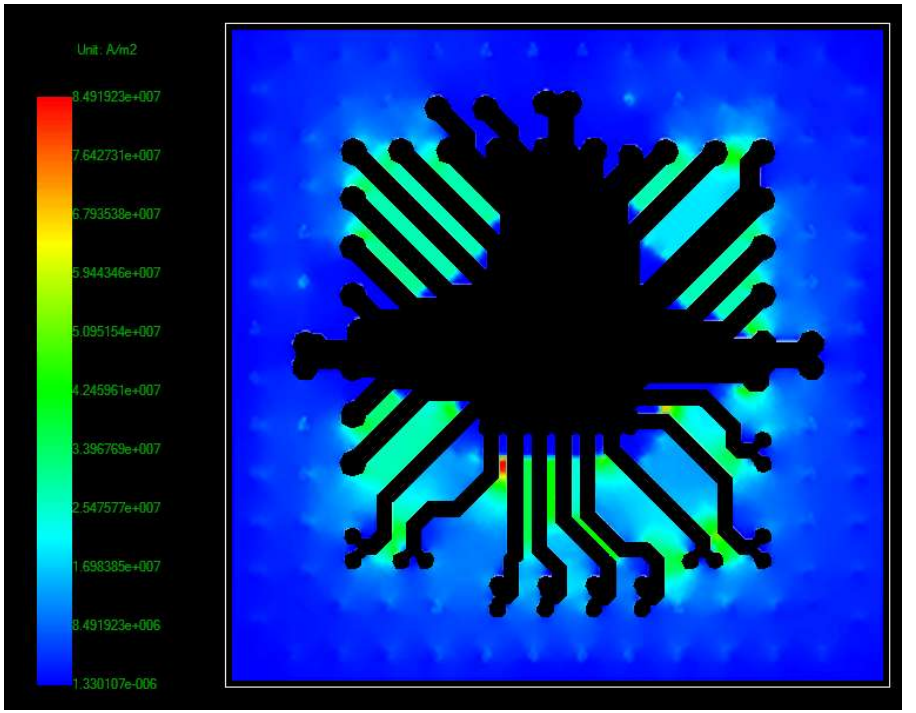
应用1：分析封装的电压分布





- 根据 IR Drop 的分析，可以决定电源/地网络所需要的 bump，pad 和 ball 的数量；
- 根据 ball 的数量可以进一步的确定 Package 的大小

应用2：分析封装的平面电流密度



找出平面上最大的电流密度“热点”区域

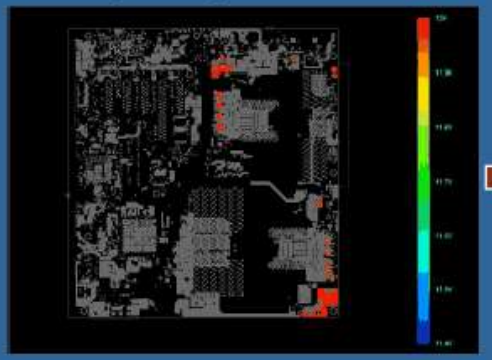
- 通常封装平面上的某些局部区域会出现相对于其他区域特别大的电流，这种功能有助于定位最大的电流密度区域，并放置相应的电源/地的过孔。

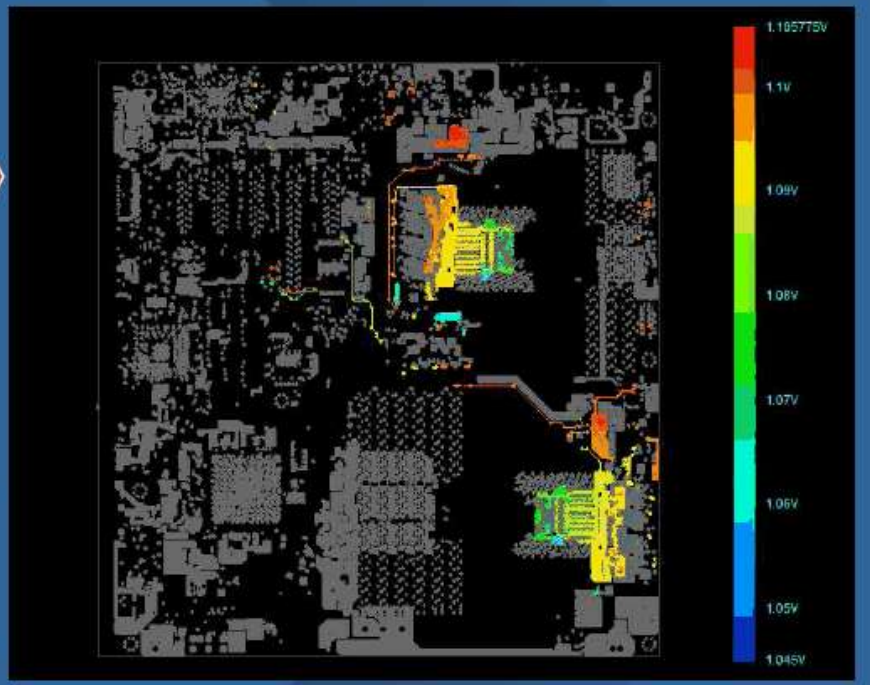
应用3：分析PCB的电压分布

（Flextronics应用实例）

DC Analysis for Power Integrity

Voltage Drop:





i. Power DC helps us to track down the voltage distribution along the Power Delivery Path.

ii. Power DC helps us to generate clear table to judge the simulation result Pass or Fail.

iii. The whole procedure is easy and fast.

Sink Name	Model	Nominal Voltage (V)	Input Tolerance (%)	Actual Voltage (V)	Margin (V)
SINK_U15_PV_VCCP_CPU0_GND	Equal Current	1.100000e+000	5.000000e+000	1.066218e+000 ✓	2.121827e-002
SINK_U16_PV_VCCP_CPU1_GND	Equal Current	1.100000e+000	5.000000e+000	1.068928e+000 ✓	2.392785e-002
SINK_U15_PV_VTT_CPU0_GND	Equal Current	1.100000e+000	5.000000e+000	1.049691e+000 ✓	4.660785e-003
SINK_U16_PV_VTT_CPU1_GND	Equal Current	1.100000e+000	5.000000e+000	1.047043e+000 ✓	2.042820e-003

FLEX Computing

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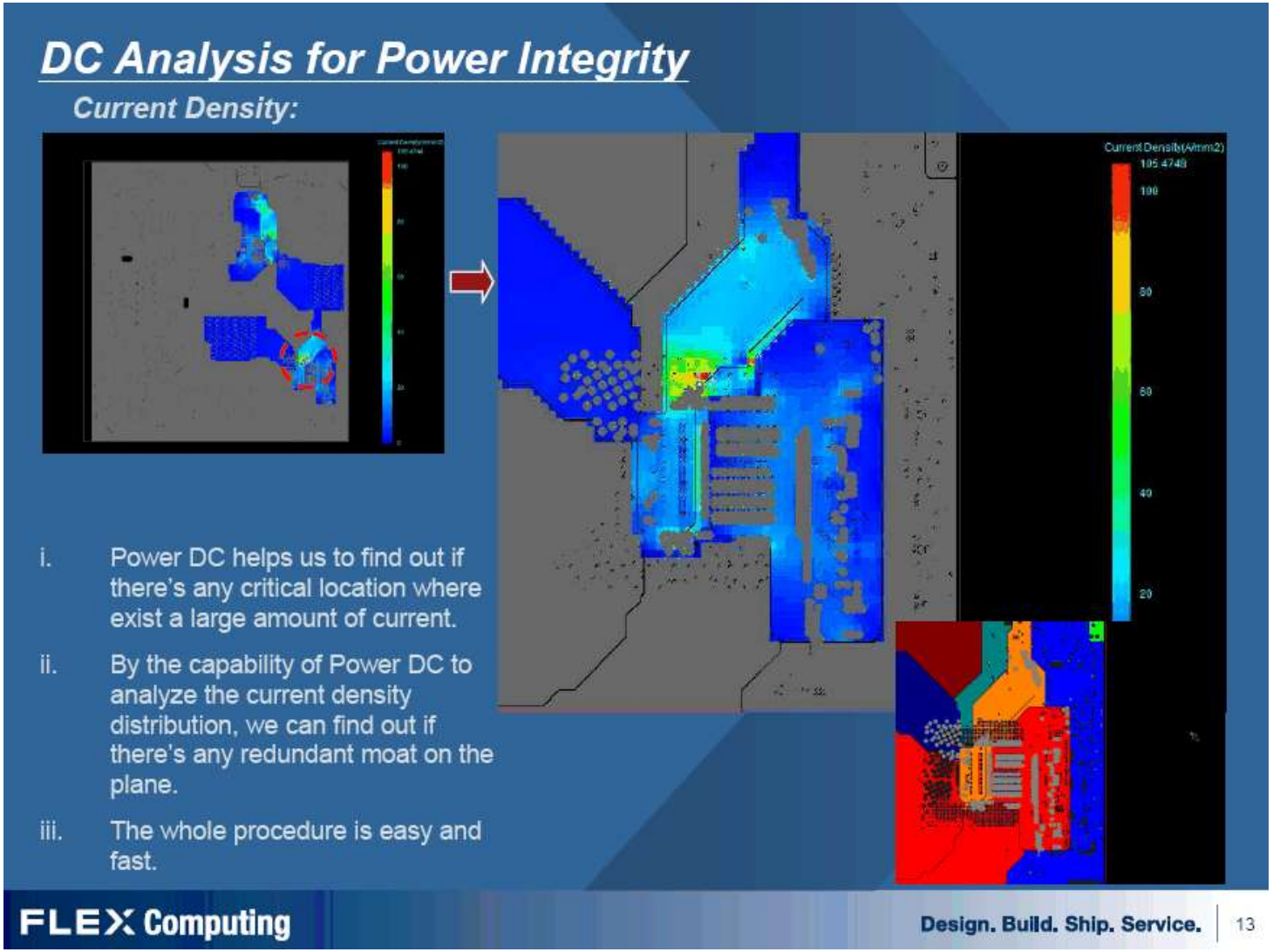
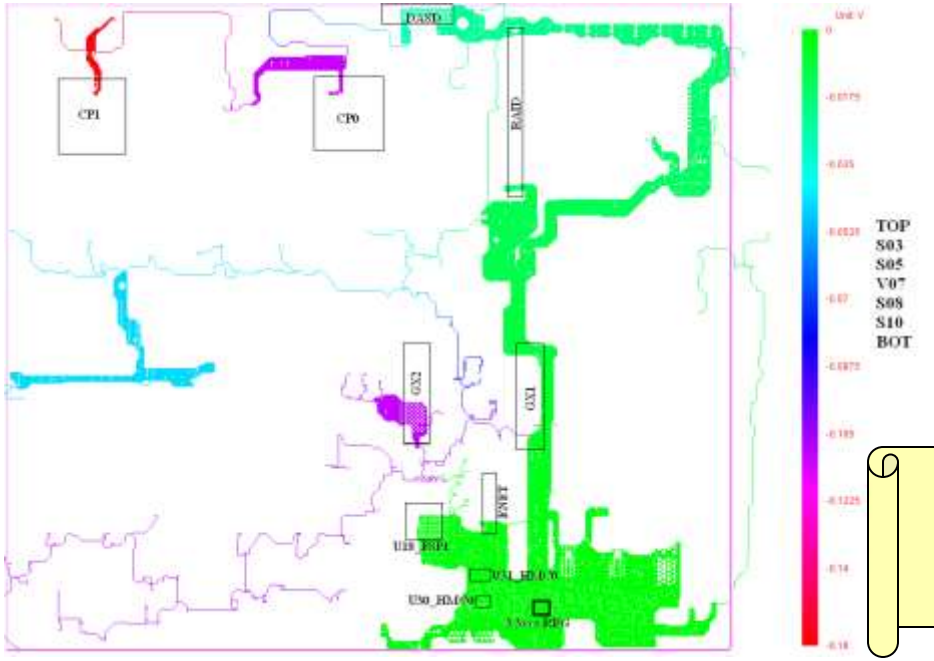
应用4：分析PCB的电流分布

（Flextronics应用实例）



应用5：PCB的IR Drop超标案例



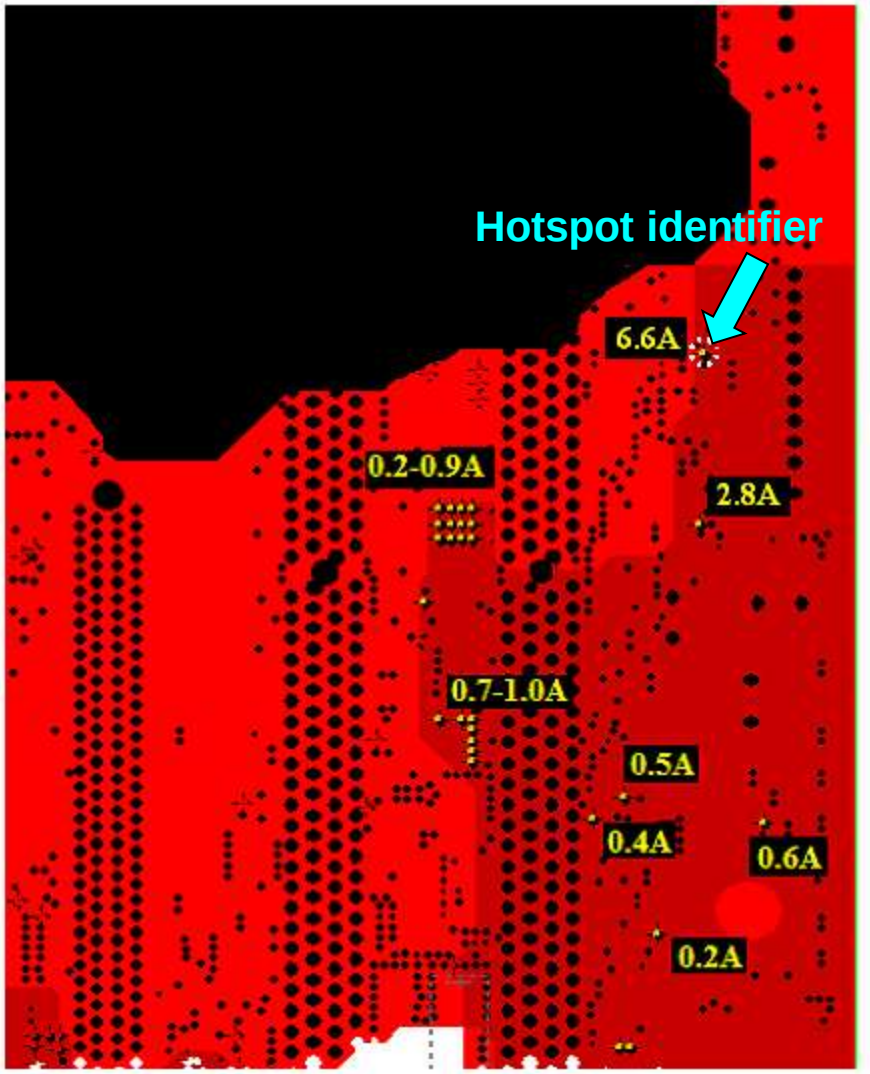
- 电源走线太细太长，导致直流压降过大，从而引起重要器件的供电不足！

IR drop target is 66mV

		criteria		66mV (2%)
Voltage	refdes	Breif description	Max current (A)	IR drop (mV)
+3.3VCS	U3_CP1	P6	0.250	-160
	U2_CP0	P6	0.250	-115
	J23_GX1	GX CARD	0.218	-113
	J24_GX2	GX CARD	0.218	-111
	J54_DASD	DASD backplane	0.006	-29
	J49_RAID	RAID card	0.006	-13
	U18_FSP1	FSP1 chip	0.51	-2.0
	J25_ENET0	ENET card	0.006	-1.4
	U31_HMC0	HMC chip	0.012	-1.2
	U30_HMC0	HMC chip	0.012	-1.0

← 超标159%

应用6：PCB的过孔电流超标案例

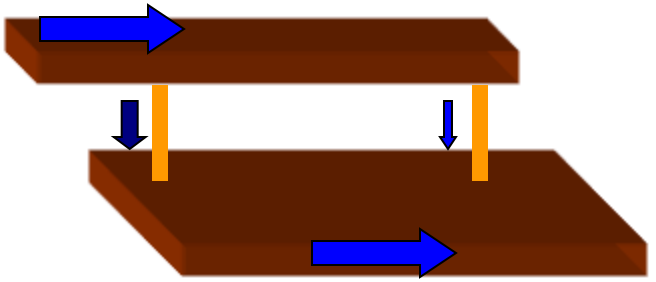


overlap shape

Non-overlap shape

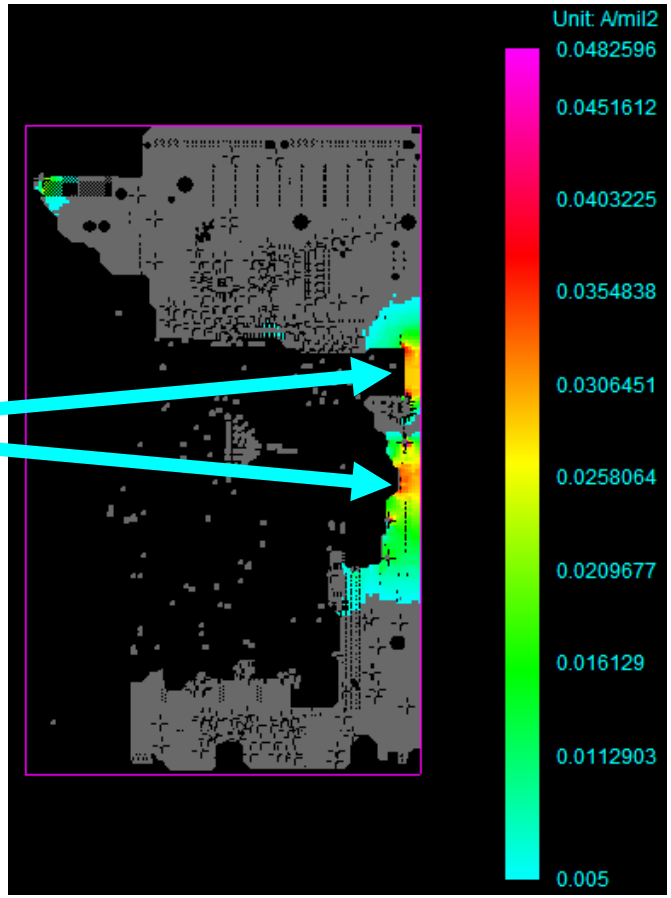
Layer V07 and V11

- 下图中的黄色过孔为2个电源重叠部分的汇流孔，因此电流显得特别大一些。



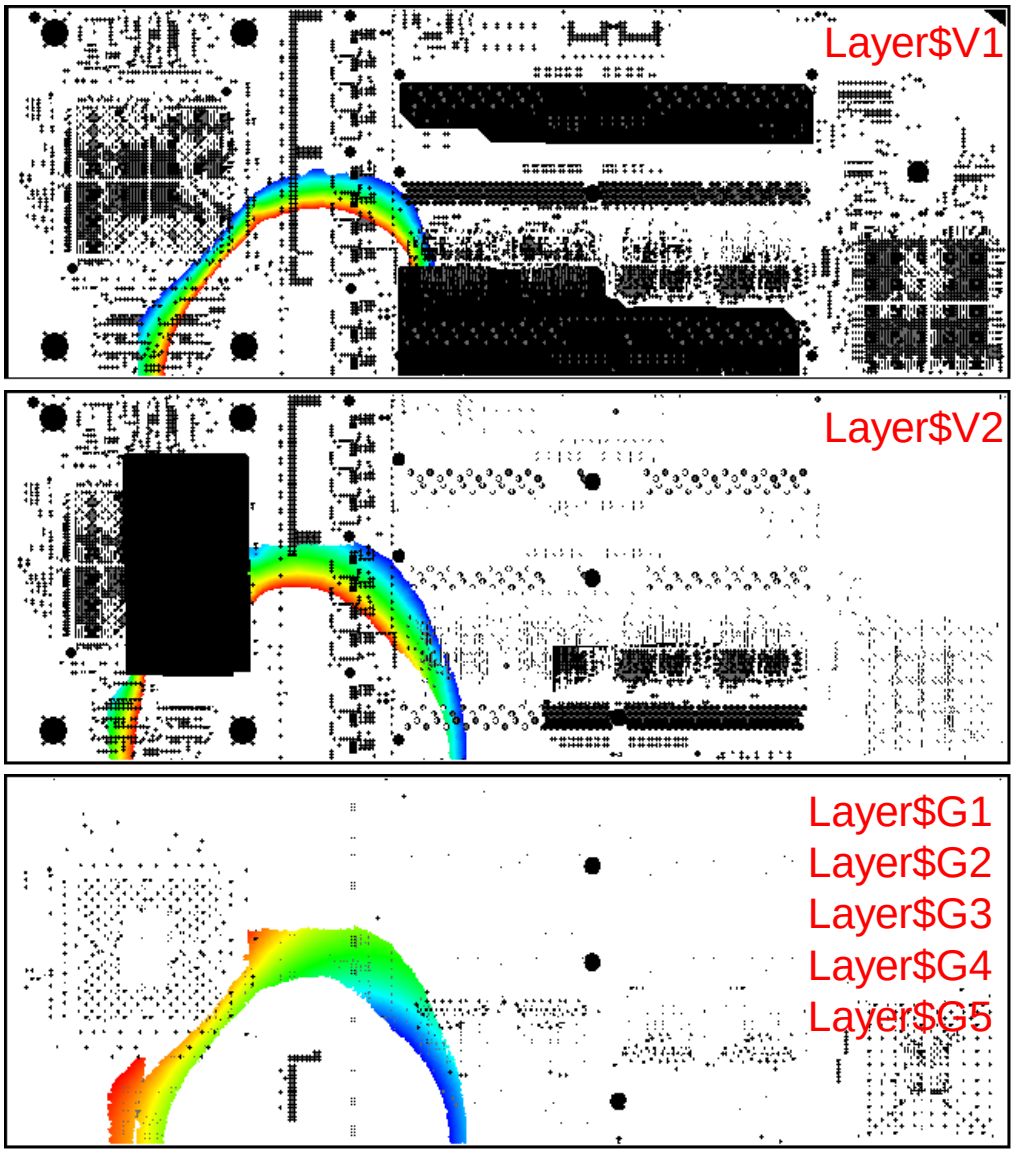
应用7：PCB的电流密度超标案例

大电流密度

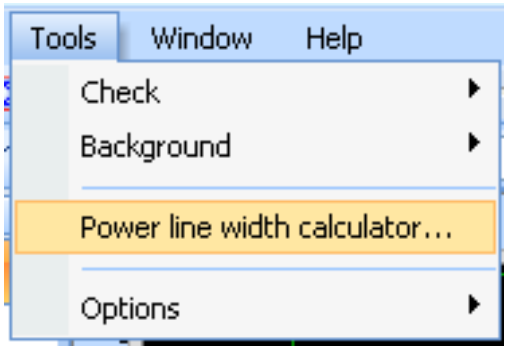


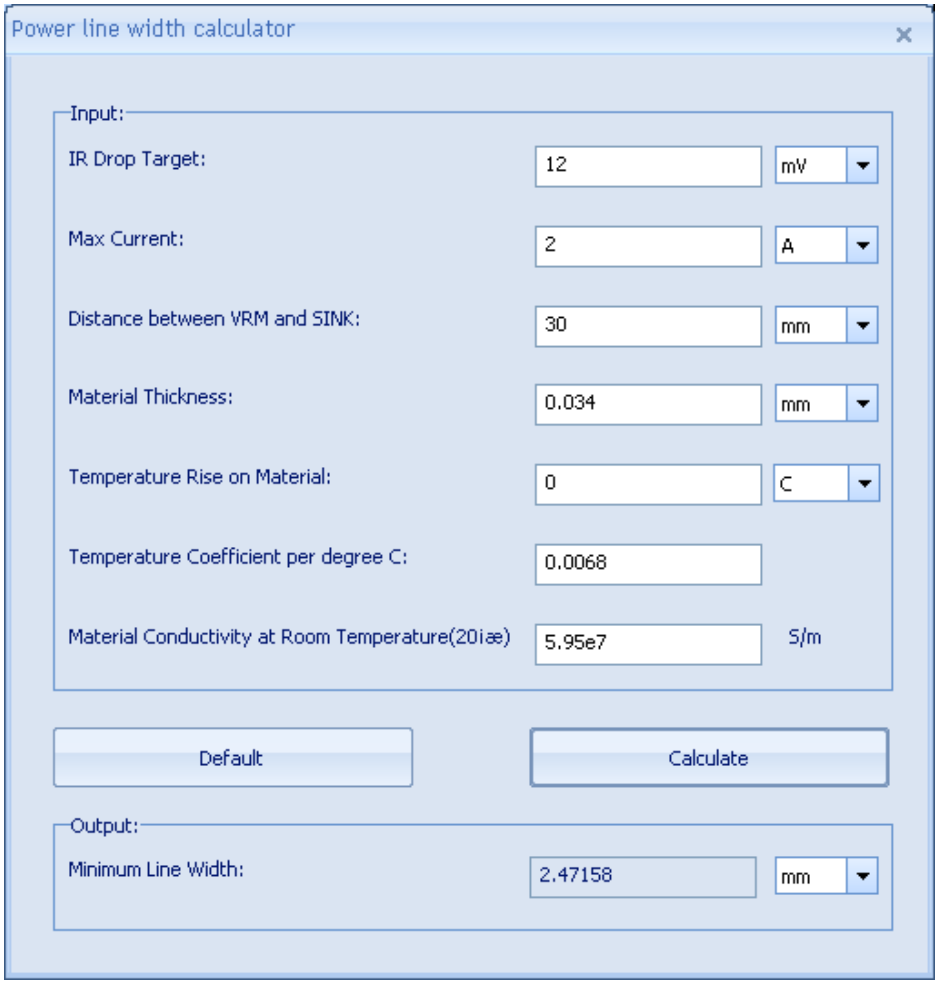
- 显示电流密度超过 5mA/mil^2的部分，小于该门限的将以灰色显示

应用8：最佳感应线



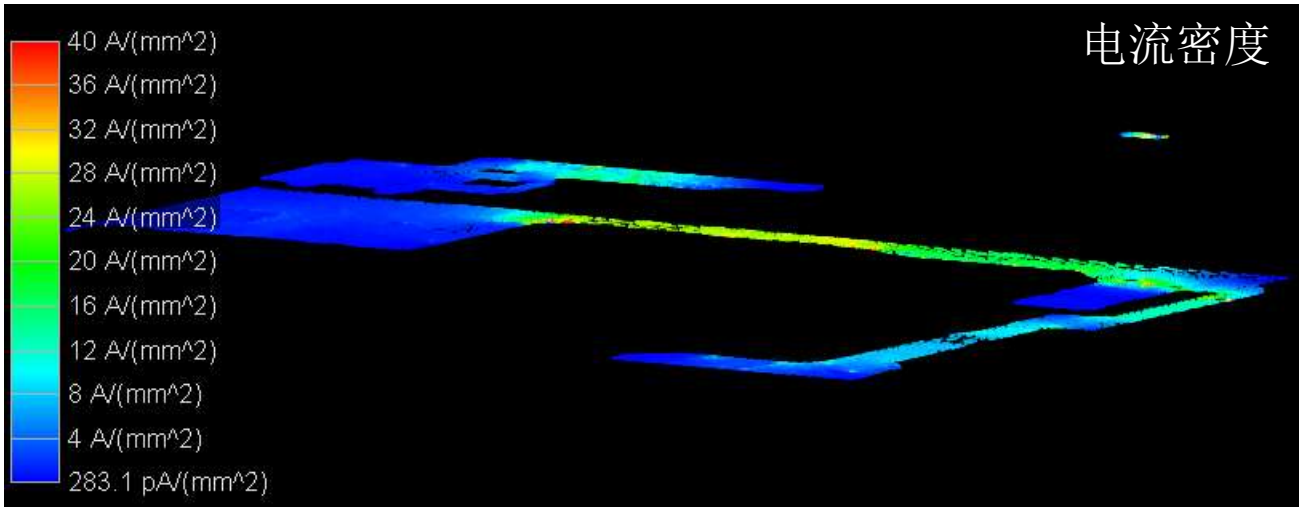
应用9：预估电源走线的最小宽度

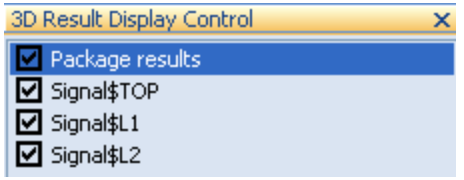


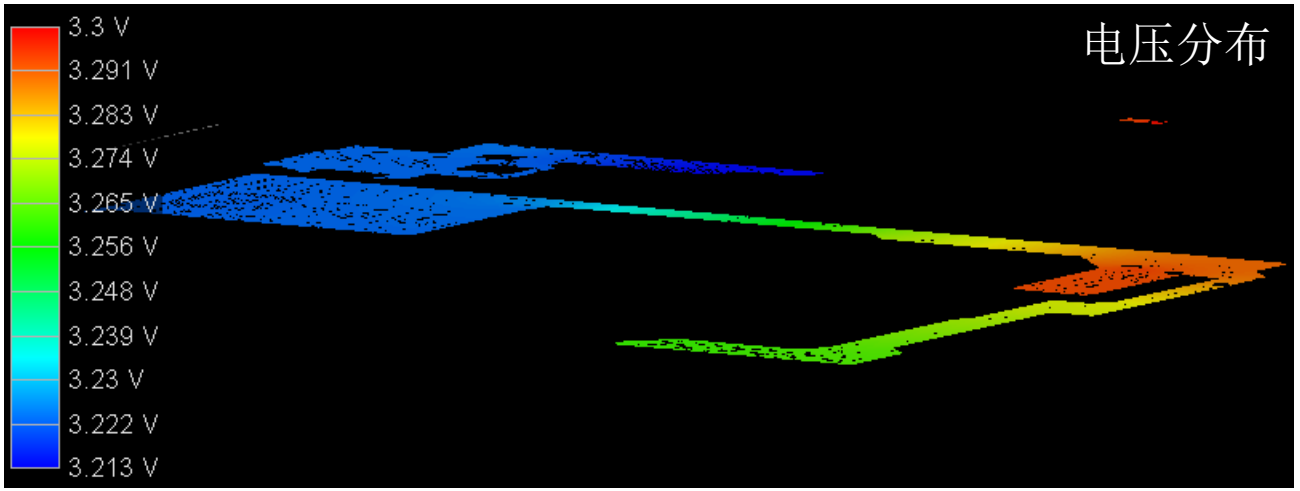


➢ 该选项用于布局布线前预估电源走线的最小宽度

应用10：3D立体显示电压和电流分布







PowerDC 总结

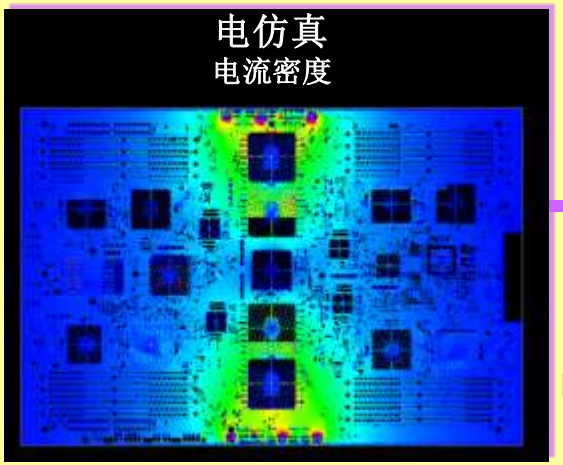
（主要功能列表）

- 布局布线前/后PCB或IC封装DC分析；
- 彩色显示PCB各层的电压分布、平面电流分布和过孔电流分布；
- 可仿真Lumped to Lumped，Lumped to Multiple，Multiple to Lumped以及Multiple to Multiple等各种形式的pin-to-pin电阻；
- 还可仿真多端口的阻抗网络，并生成DC情况下相应的S-param模型和SPICE等效模型；
- 多子板/多封装的IR Drop分析；
- 流程化仿真，指导用户快速准确的完成整个仿真，而且用户可以定制自己特定的Workflow；
- 高效的有限元（FEM）算法无需用户设定Mesh即可得到平面上精细而平滑的每一个位置上的电压、电流值；
- 内置的Constraint management使仿真支持复杂设计的DRC检查；
- 生成所有的电压、电流结果表格，并与预先设定的Constraints作比较；
- 将DRC Marker反标回Allegro Layout文件。

电热混合分析：PowerDC-T

电热混合仿真

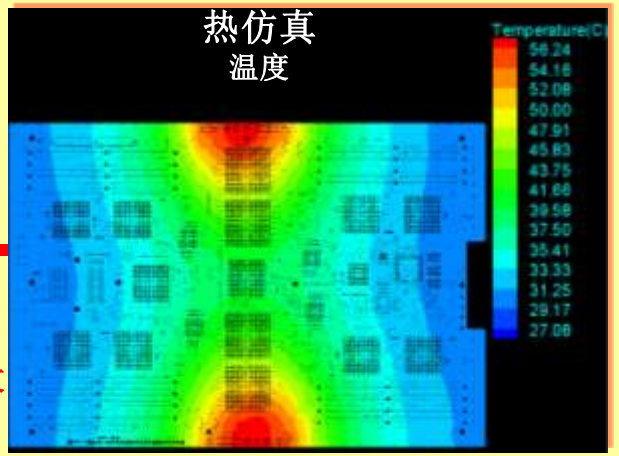
PowerDC Thermal



电流密度随温度变化

迭代直至收敛

由于焦耳热和器件发热导致温度升高

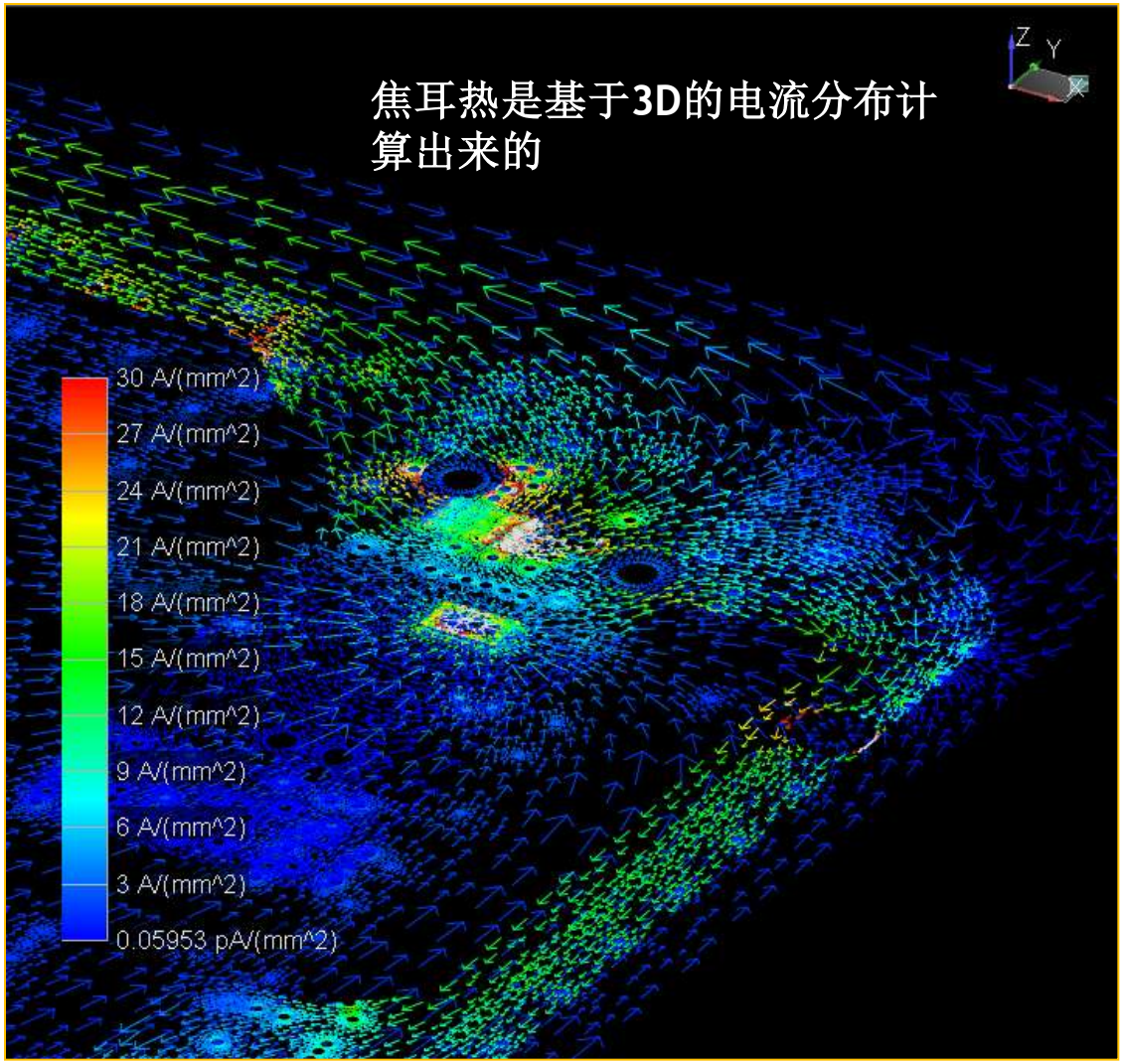


- 温度升高，电阻增加
- 高温下器件的泄漏功率也相应增加

覆铜上的焦耳热将影响温度的分布

➢ 集成的电热混合仿真引擎给设计人员提供了准确的设计指导，并降低了制造成本。

用于计算焦耳热的3D电流分布



用户定义的器件热

- 除了焦耳热之外，另一个热源是器件热，器件的发热是半导体Die内部由于电源和走线的漏电流引起的。

- PowerDC-Thermal允许用2种格式输入器件热

1. 简单功耗输入，温度是独立的，并且均匀分布于器件内部

2. 导入功耗文件，温度与AC电源的漏电和空间分布有关（见下页）

器件的功耗定义文件

```
LEAKAGE POWER
20
30.75     8.641237
34.80     9.019732
38.45     9.376941
42.35     9.787694
46.17     10.230422
49.98     10.729415
53.88     11.276497
57.73     11.841193
61.75     12.528715
65.85     13.243416
69.7      14.002816
73.55     14.812501
77.88     15.755441
81.7      16.813701
86.03     17.873299
90.2      19.087921
94.1      20.361731
98.42     21.740563
102.38    23.224039
106.35    24.840946
```

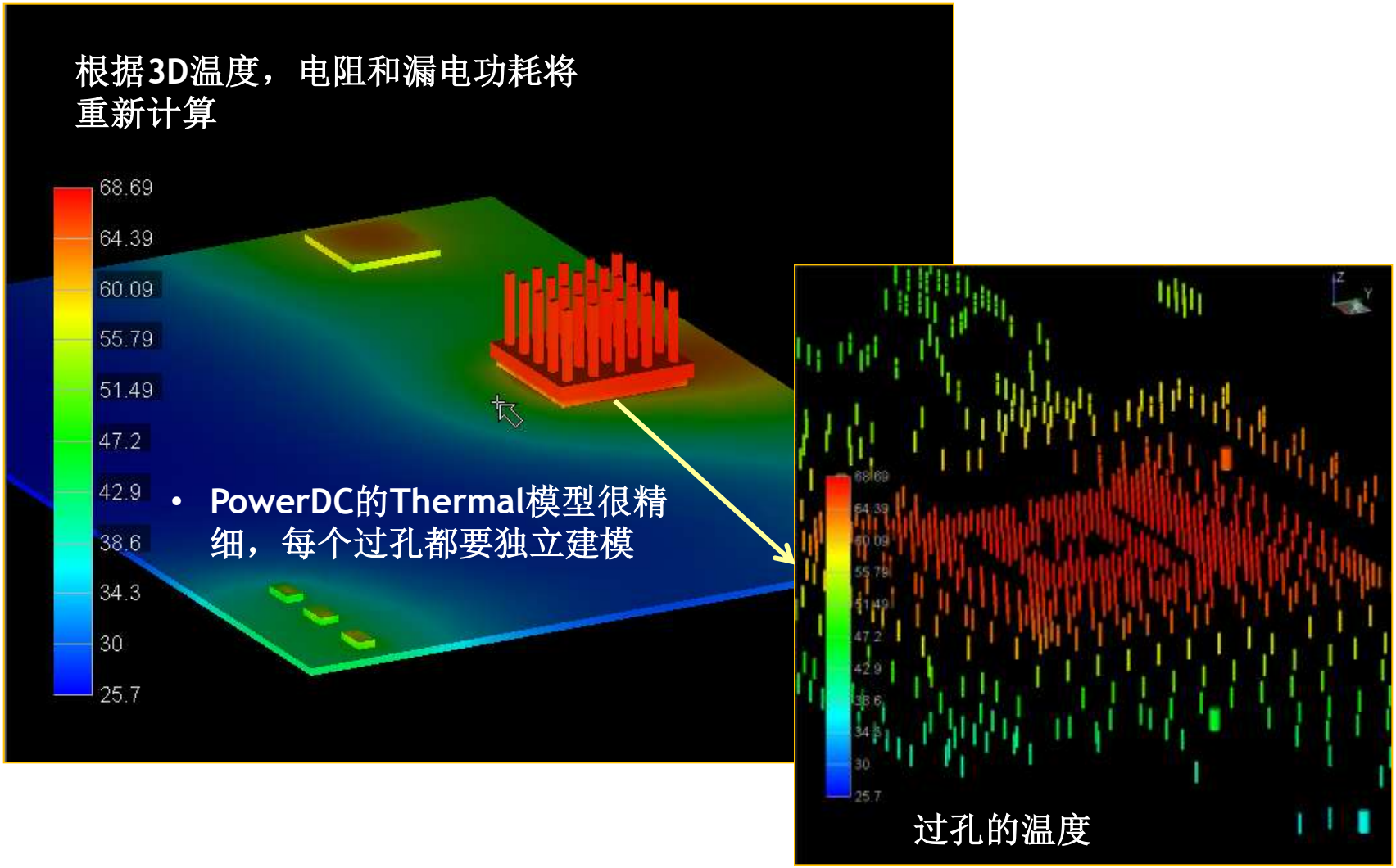
温度相关的功耗，由Die内部的漏电功耗引起的

位置相关的功耗，由Die内部的动态翻转引起的

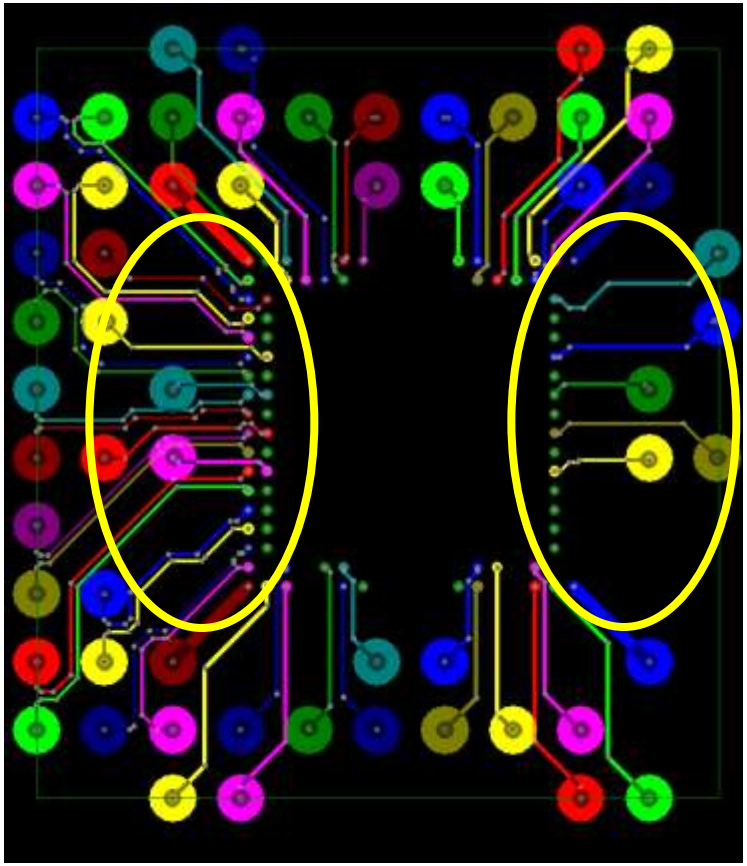
```
POWER MAP
22        24
0.07      0.07      0.07      0.043315217       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0.043315217       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0.043315217       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0.043315217       0.043315217       0.043315217
0.07      0.07      0.07      0.034118078       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0.043315217       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0.043315217       0.043315217       0.043315217       0.043315217
0.043315217       0.043315217       0         0         0.043315217
0.07      0.07      0.07      0.034118078       0.034118078       0.034118078       0.034118078
0.034118078       0.043980476       0.043980476       0.043980476       0.043980476       0.043980476
0.054770054       0.054770054       0.054770054       0.054770054       0.035191907       0.035191907
```

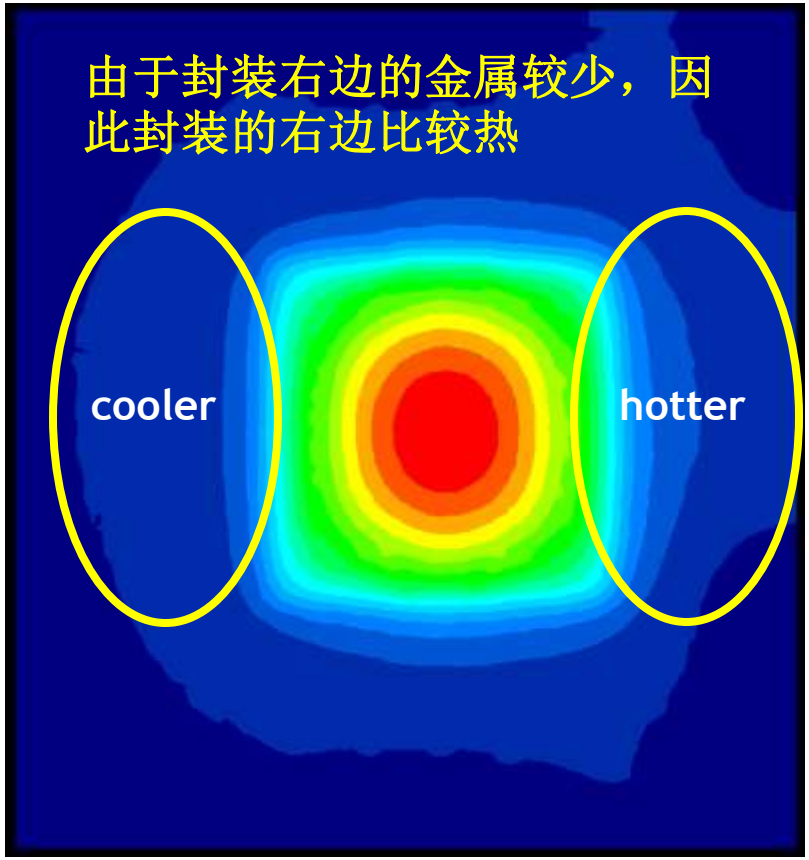
3D的温度显示

根据3D温度，电阻和漏电功耗将重新计算



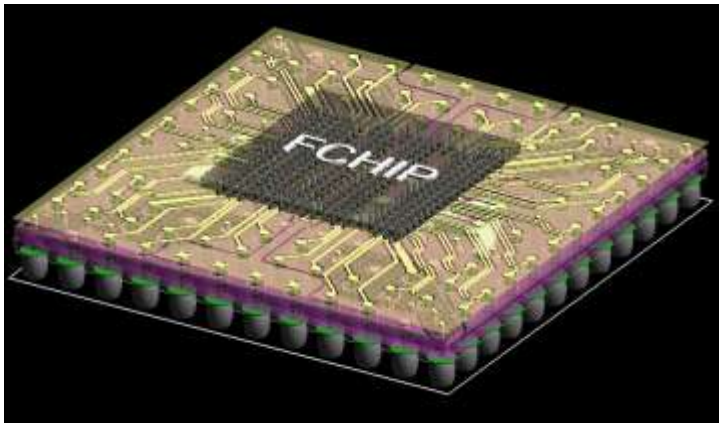
热传递反映了真实的Substrate布线





产品综述

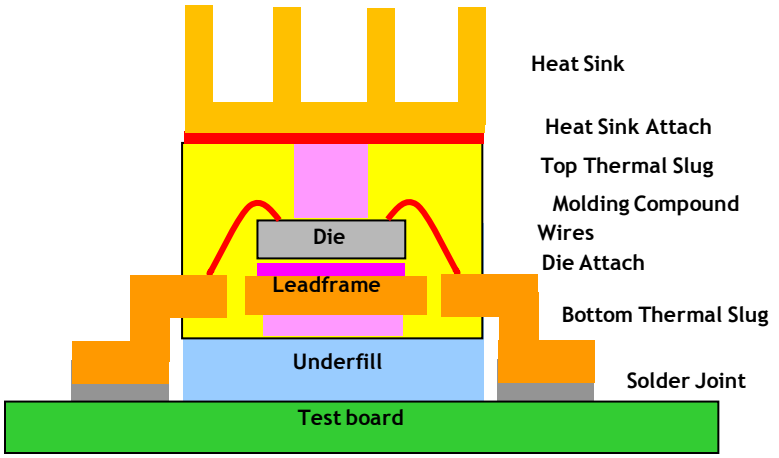
- 导入CAD设计文件
- 电/热混合仿真
- 封装/主板联合仿真
- JEDEC的标准热参数
- JEDEC的紧凑型热模型
- BGA, Leadframe, SiP & PoP
- 3D的有限元建模
- 3D的温度分布
- 3D的热通量分布

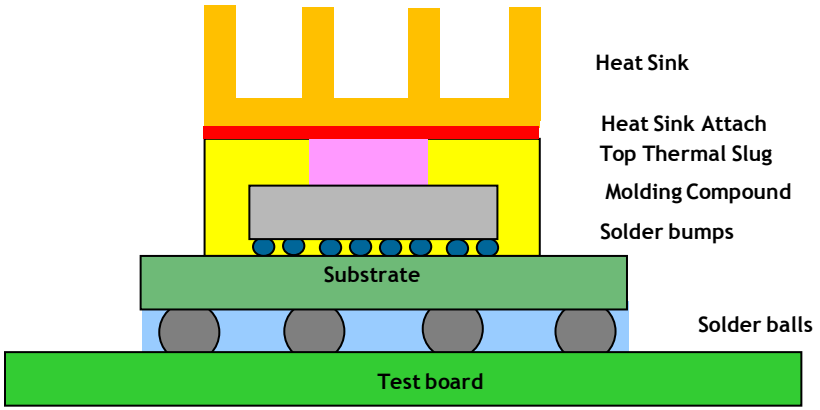


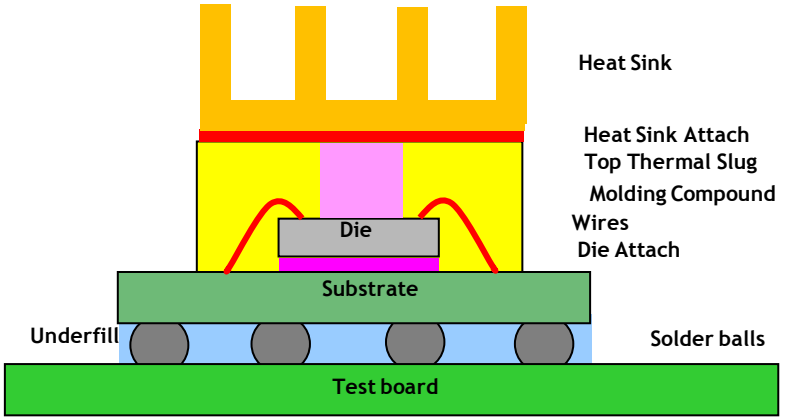
封装的标准热参数

1. 封装的标准热参数
   - 静态空气 θJA, ΨJT, ΨJB (JESD51-2A)
   - 强制对流 θJMA, ΨJT, ΨJB (JESD51-6)
   - θJB (JESD51-8)
   - θJCtop, θJCbottom (JESD51-12)

2. 封装的紧凑型热模型 (CTM)
   - 双电阻型紧凑模型 (JESD15-3)
   - DELPHI 紧凑模型 (JESD15-4)

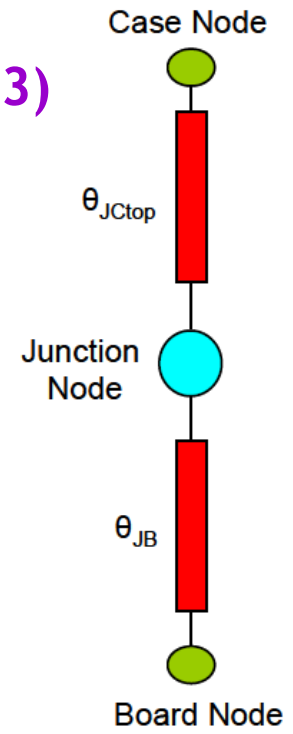




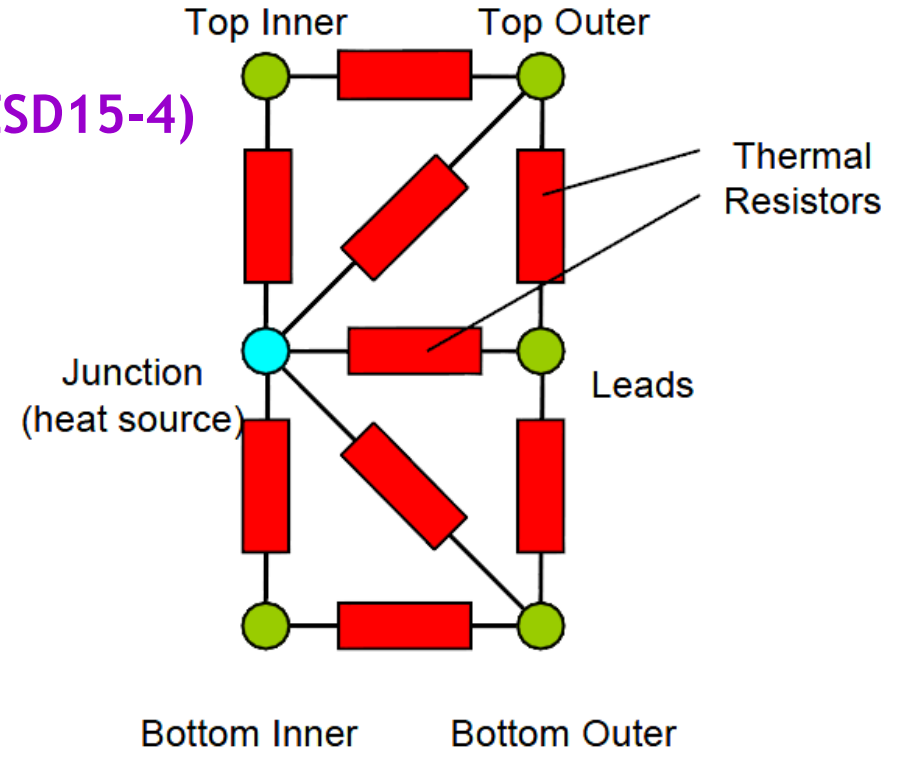


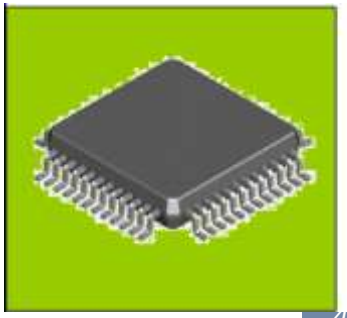
封装的紧凑型热模型

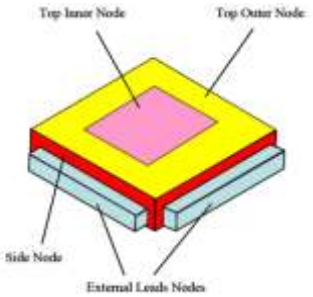
(JESD14-3)



(JESD15-4)







多Die的电阻矩阵

这里是一个 4-die的封装示例

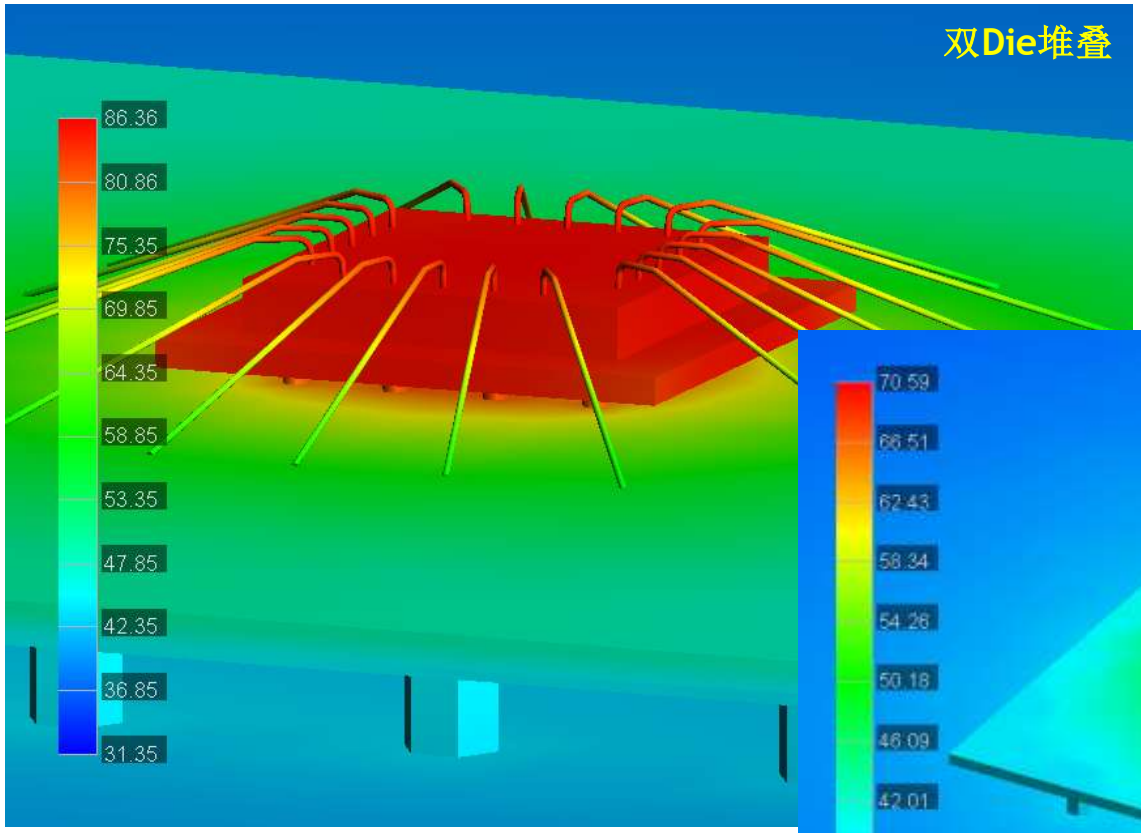
$$\begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{bmatrix} \begin{Bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{Bmatrix} = \begin{Bmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{Bmatrix}$$

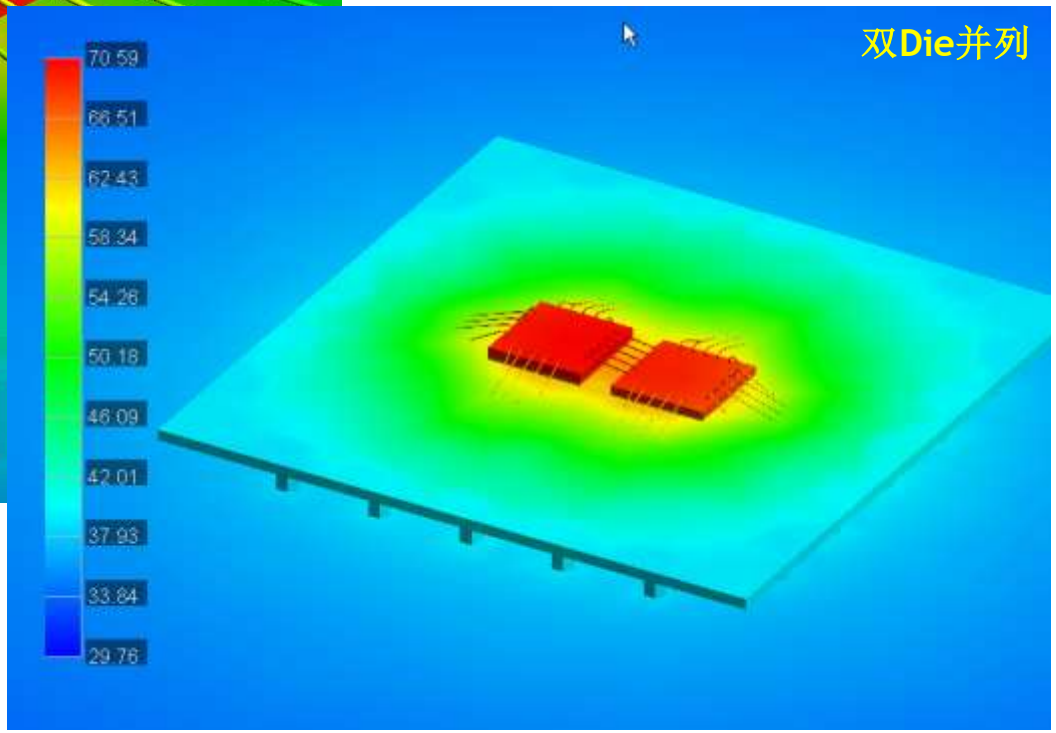
其中 $\Delta T = (T_i - T_{Amb})$

计算Rij 的方法：

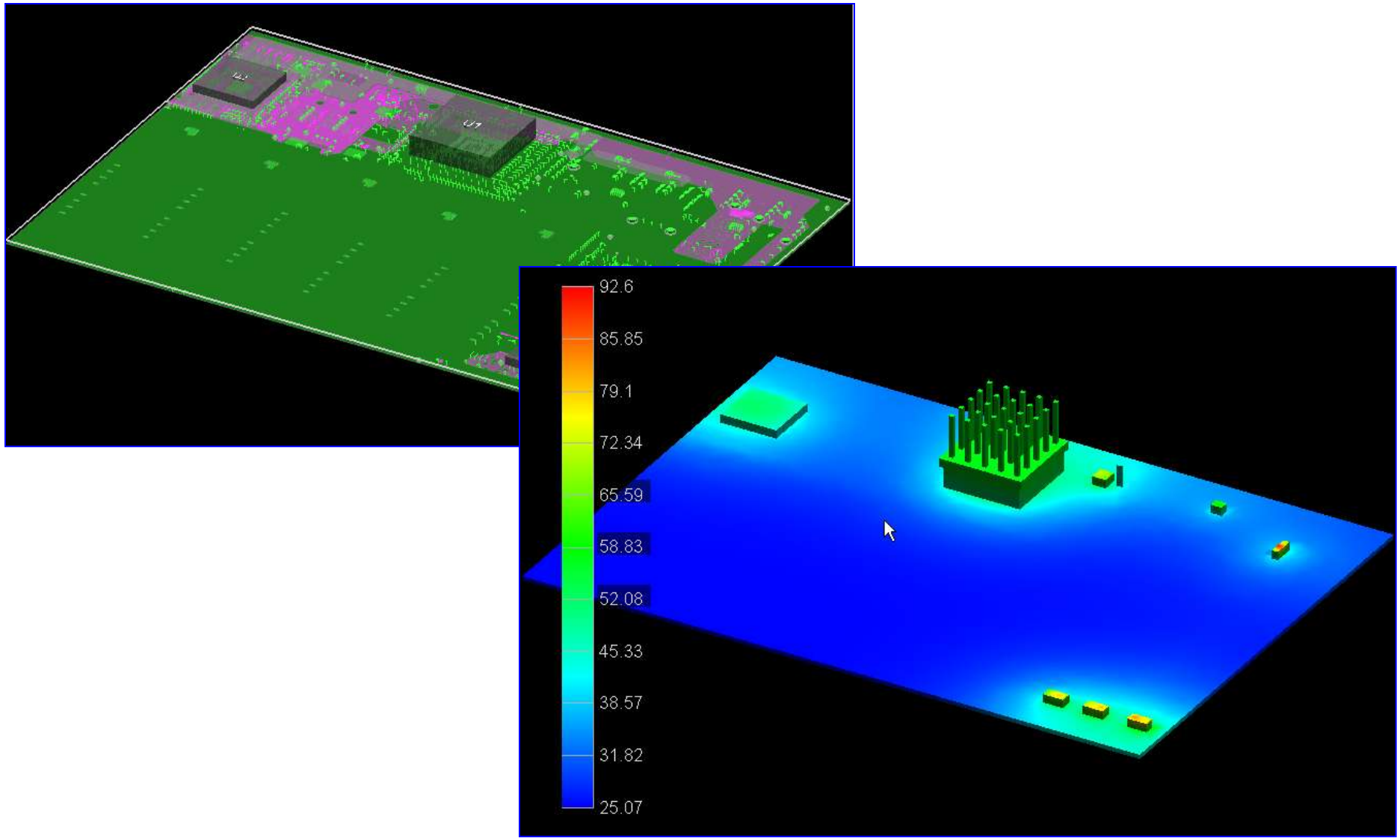
- 在 Die j上输入 nW的功率, 其他Die上输入的功率为 0；
- Rij=(Ti-Tamb)/nW

应用1：SiP封装的热分析案例



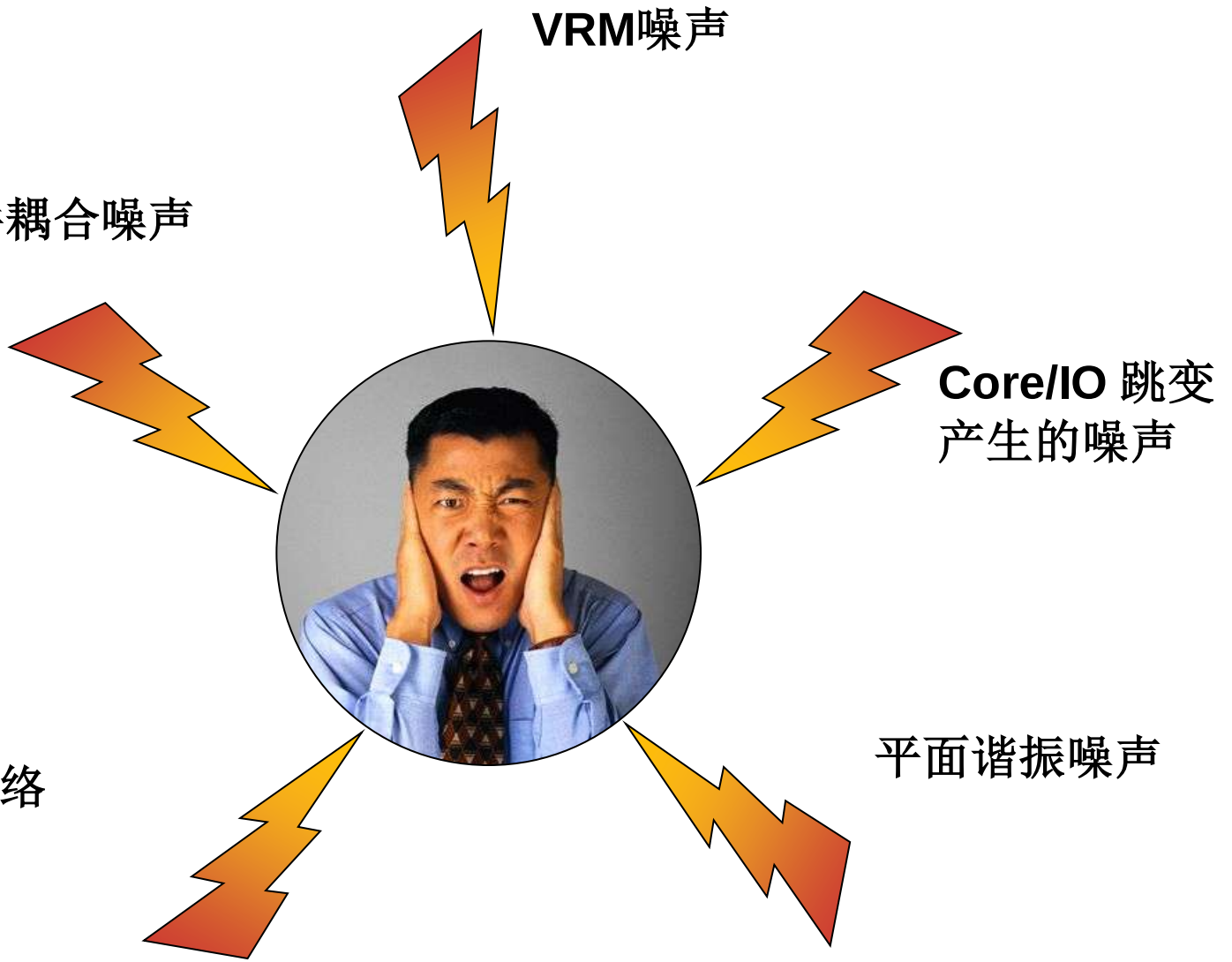


应用2：PCB的热分析案例

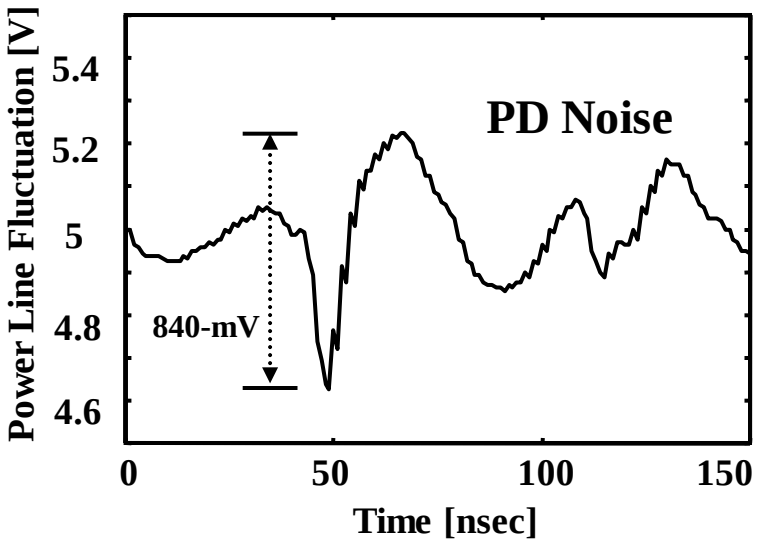


交流分析：PowerSI

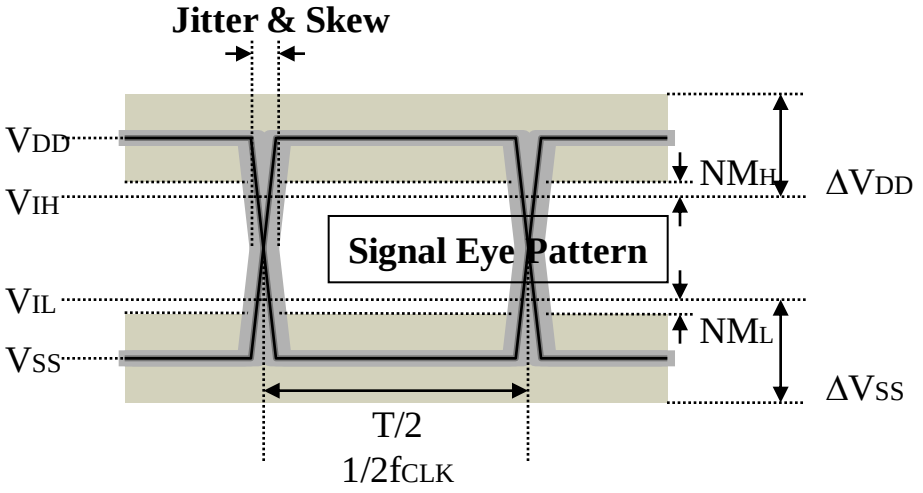
电源地平面噪声来源

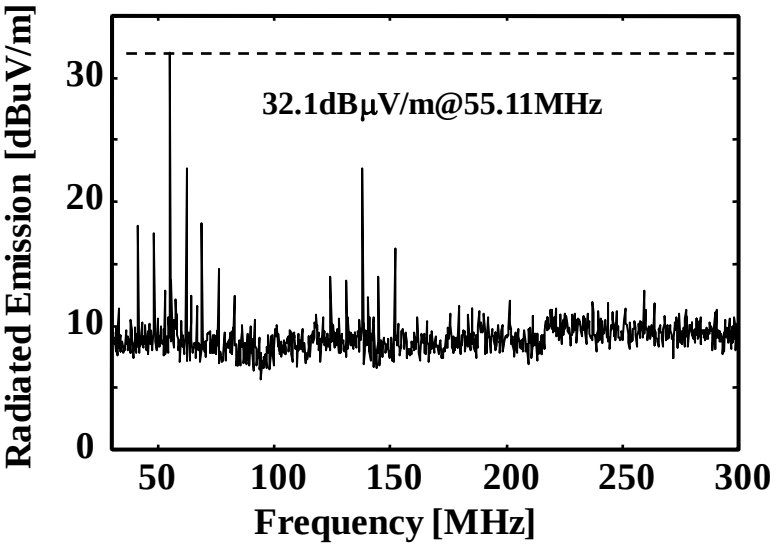


不好的PI性能将带来以下问题

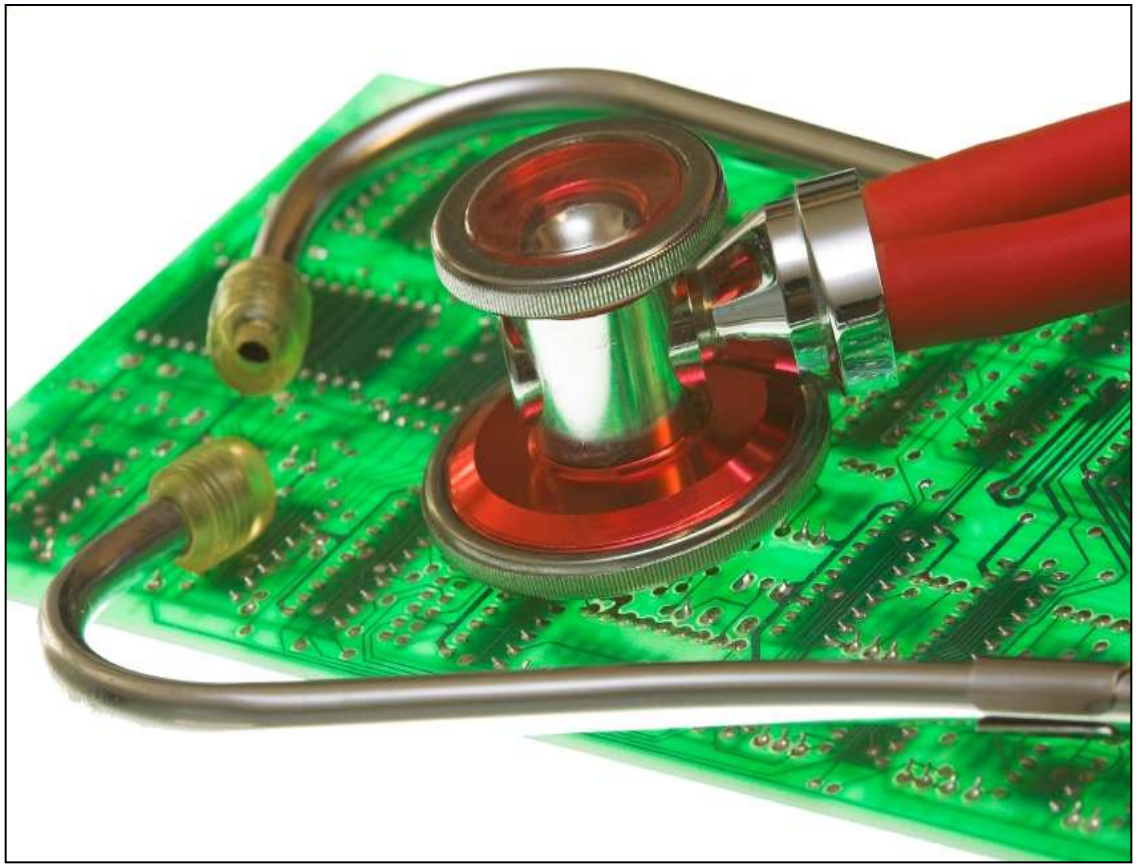


- 噪声容限变小
- 时序容限变小
  - 数据相移/抖动
- EMI增大



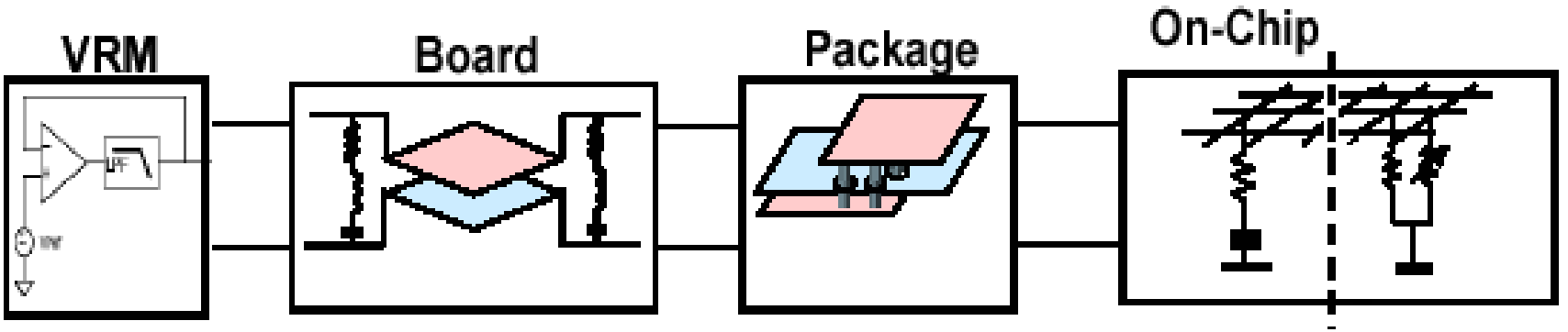


如何解决潜在的电源系统问题

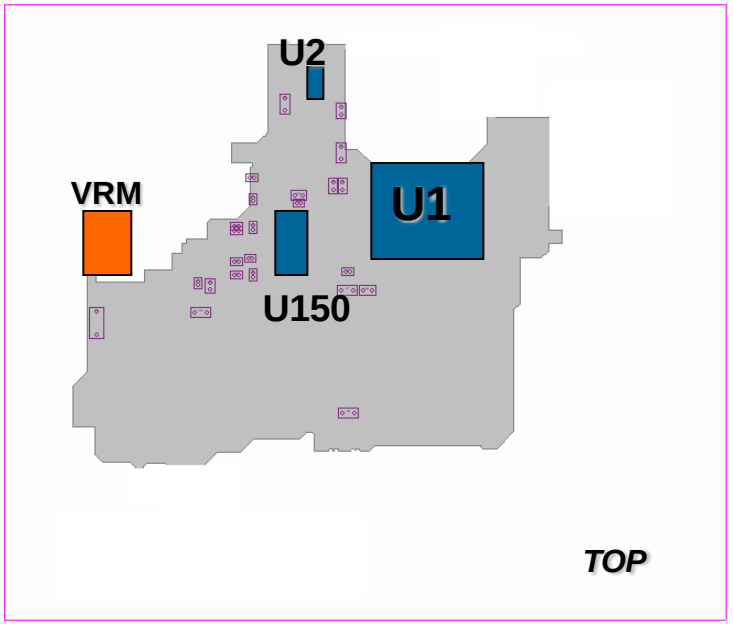


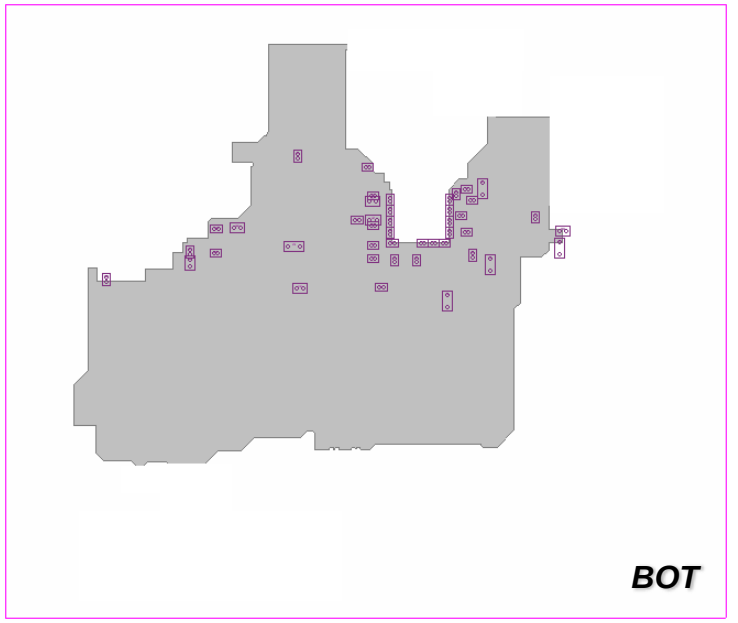
电源是如何传递的?

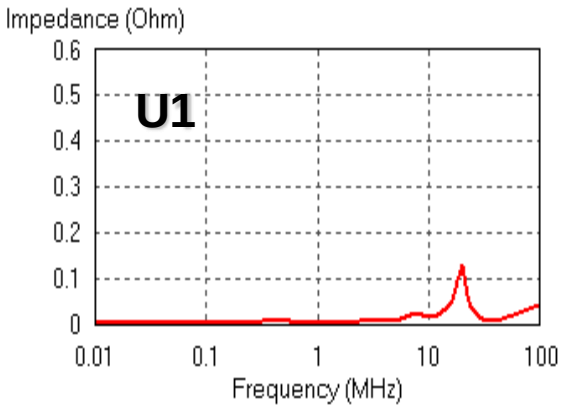
- 电源能量从电源模块（VRM）出发，经过电源分配网络（PDN），到达芯片内的电路

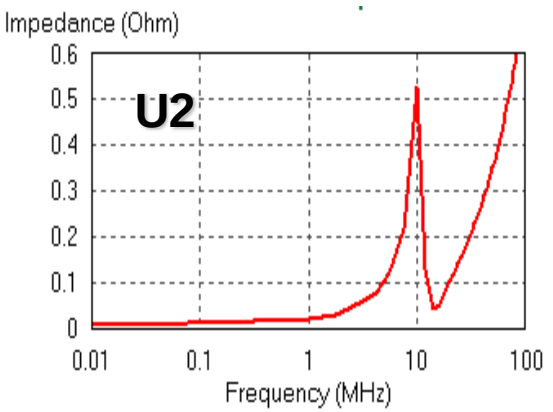


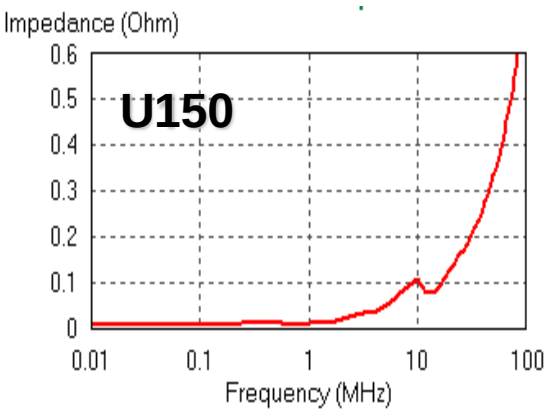
观察各个器件处的自阻抗



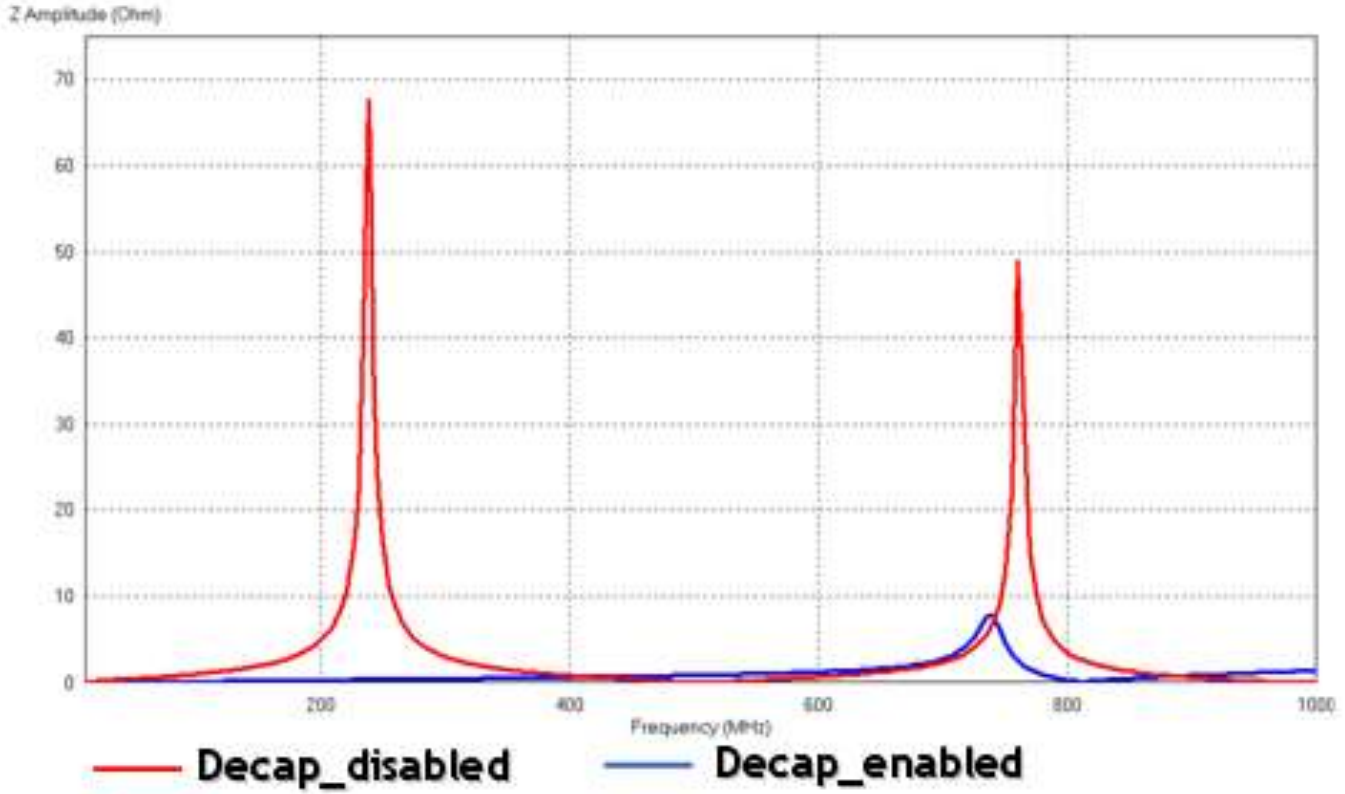






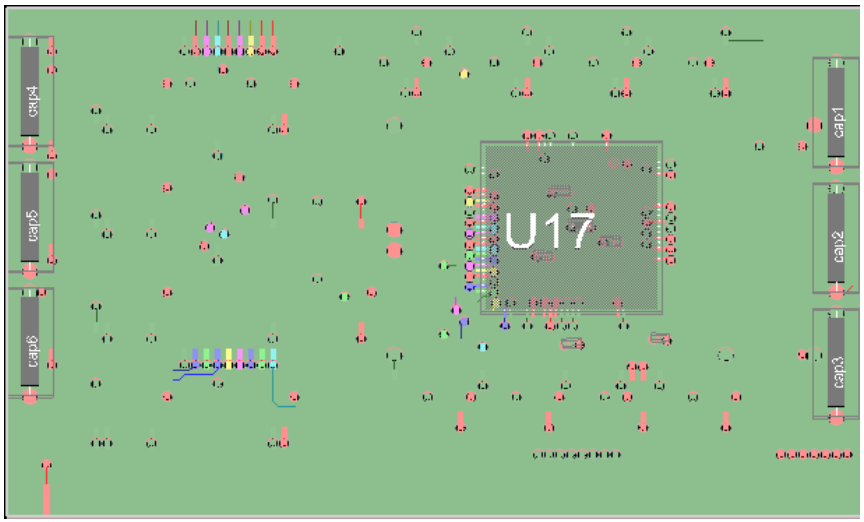


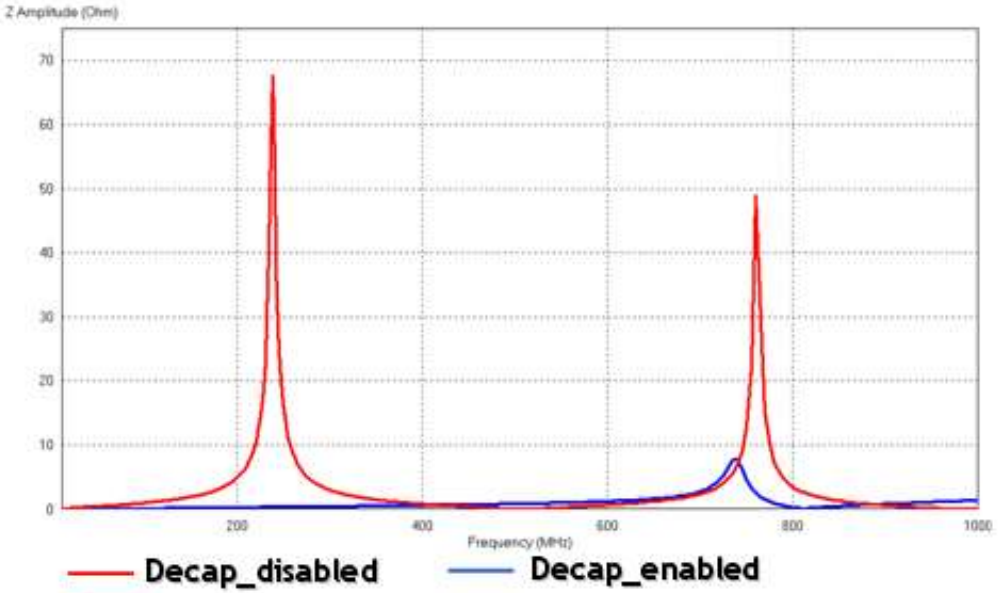
PI性能的好坏比较～频域



✓ 好的电源供电: 电源的输入阻抗较小;
✓ 差的电源供电: 电源的输入阻抗大， 有明显谐振！

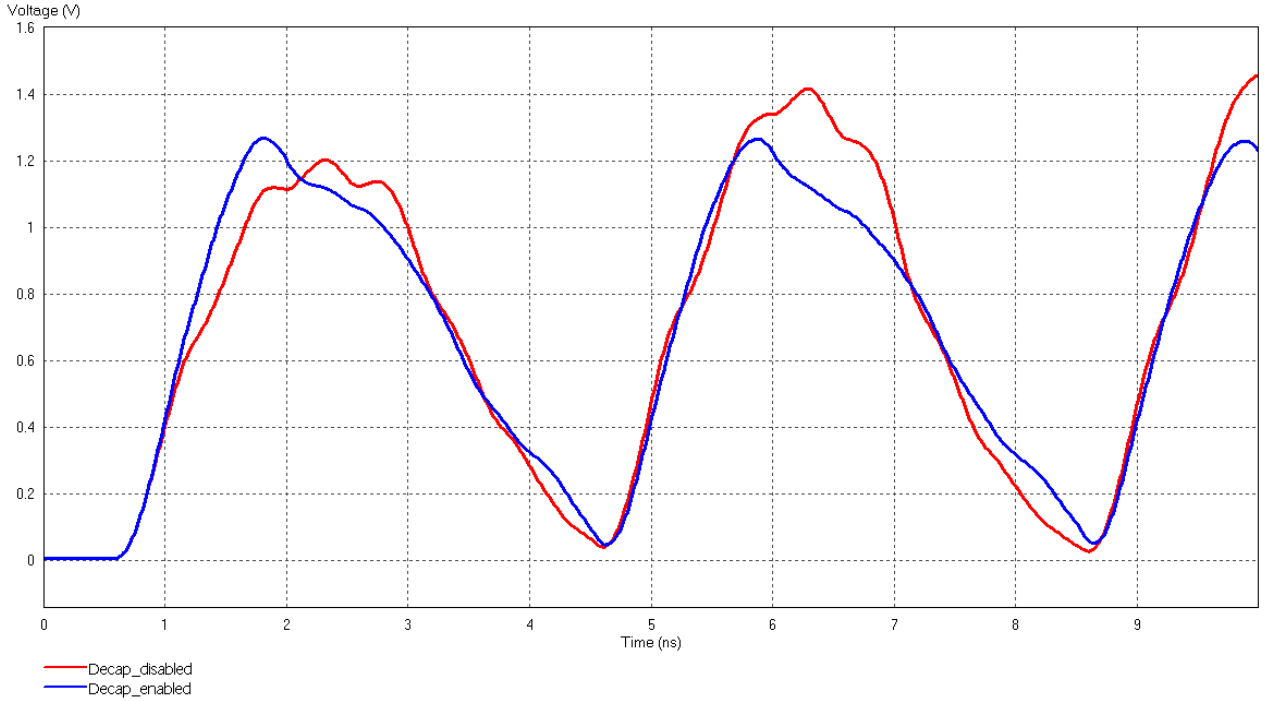
PDN的谐振





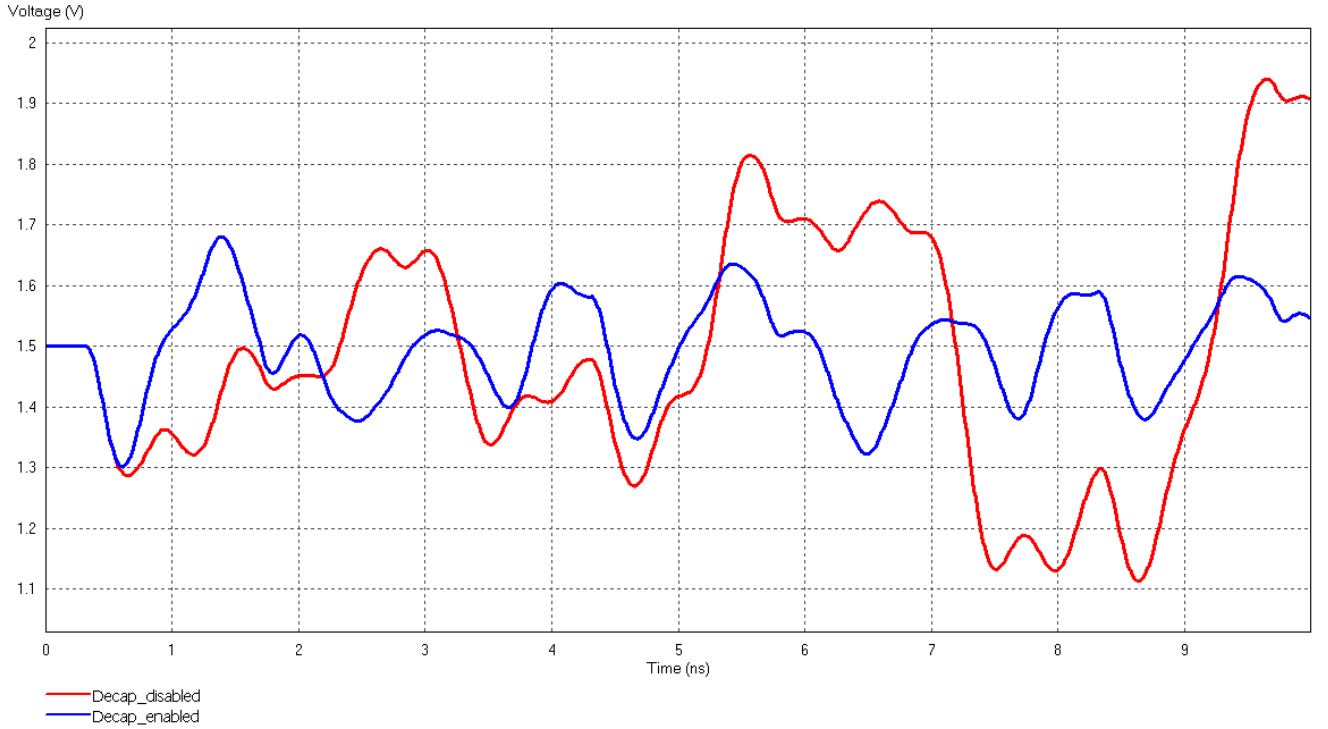
- PDN的阻抗是电源地平面设计中需要重点考虑的因素；
- PDN的谐振将使信号的SI性能变差；
- PDN的谐振将使电源地平面的PI噪声变大

PDN的谐振对SI的挑战



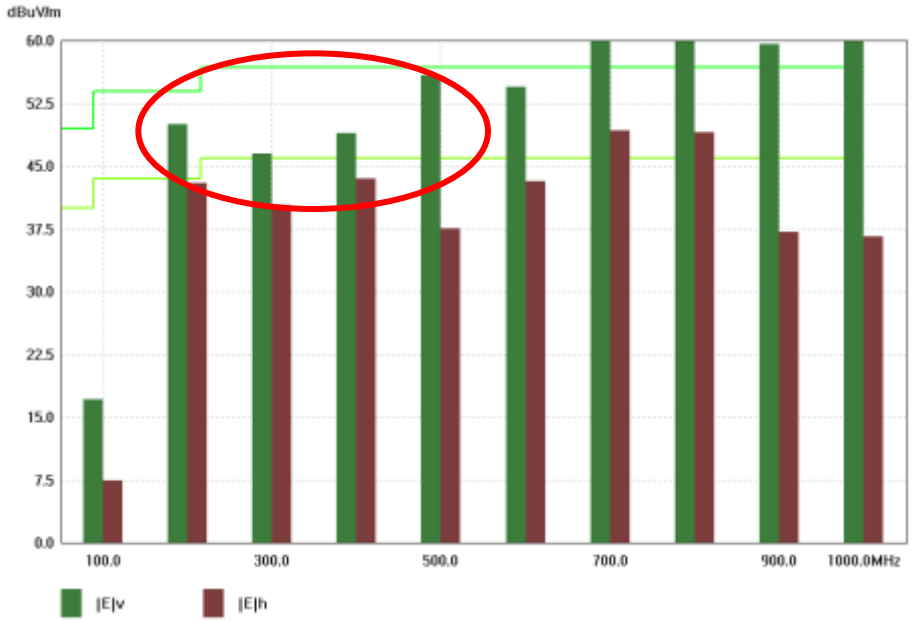
- 对于上述PCB Demo板，需要发送的信号为250MHz；
- 当把Decap全部去掉时，信号频率恰好与PDN的第一个谐振频率240MHz比较接近，此时信号波形较差；
- 当把Decap全部打开时，由于PDN在240MHz的谐振被消除，此时信号波形（蓝色线）得到了明显的改善

PDN的谐振对PI的挑战

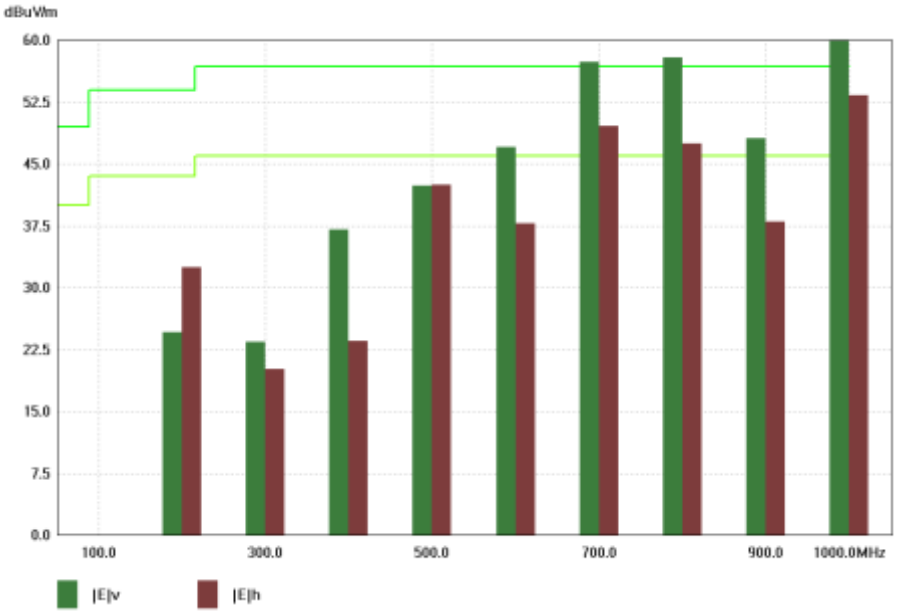


- 当把Decap全部去掉时，由于PDN谐振的影响，此时VCC电源波形（红色线）较差；
- 当把Decap全部打开时，由于PDN在240MHz的谐振被消除，此时VCC电源波形（蓝色线）得到了明显的改善

PDN的谐振对EMI的挑战



Decap_disabled



Decap_enabled

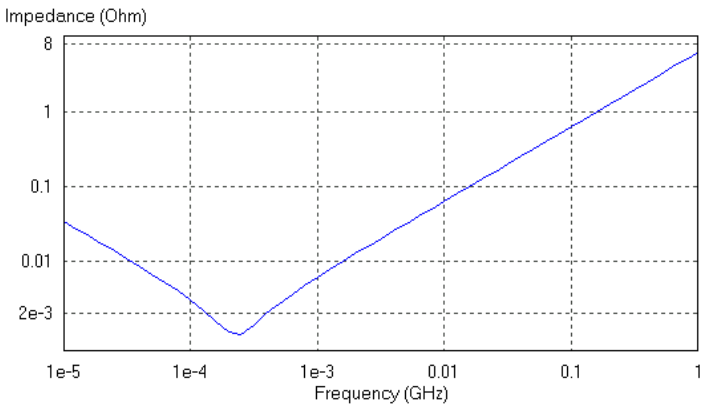
- 当把Decap全部去掉时，由于PDN谐振的影响，此时全板EMI的辐射在200MHz~500MHz全部超标；
- 当把Decap全部打开时，由于PDN在240MHz的谐振被消除，全板EMI的辐射在500MHz以下均满足了FCC CLASS B的标准

电容特性

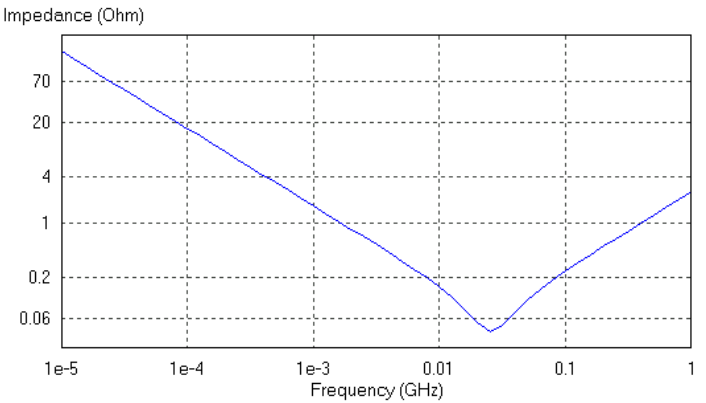
- 一个真实的电容包含一些重要的寄生参数，如串接电感（ESL）和串接电阻（ESR）

- ESL可能会引起电容在一定频率上的谐振

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$



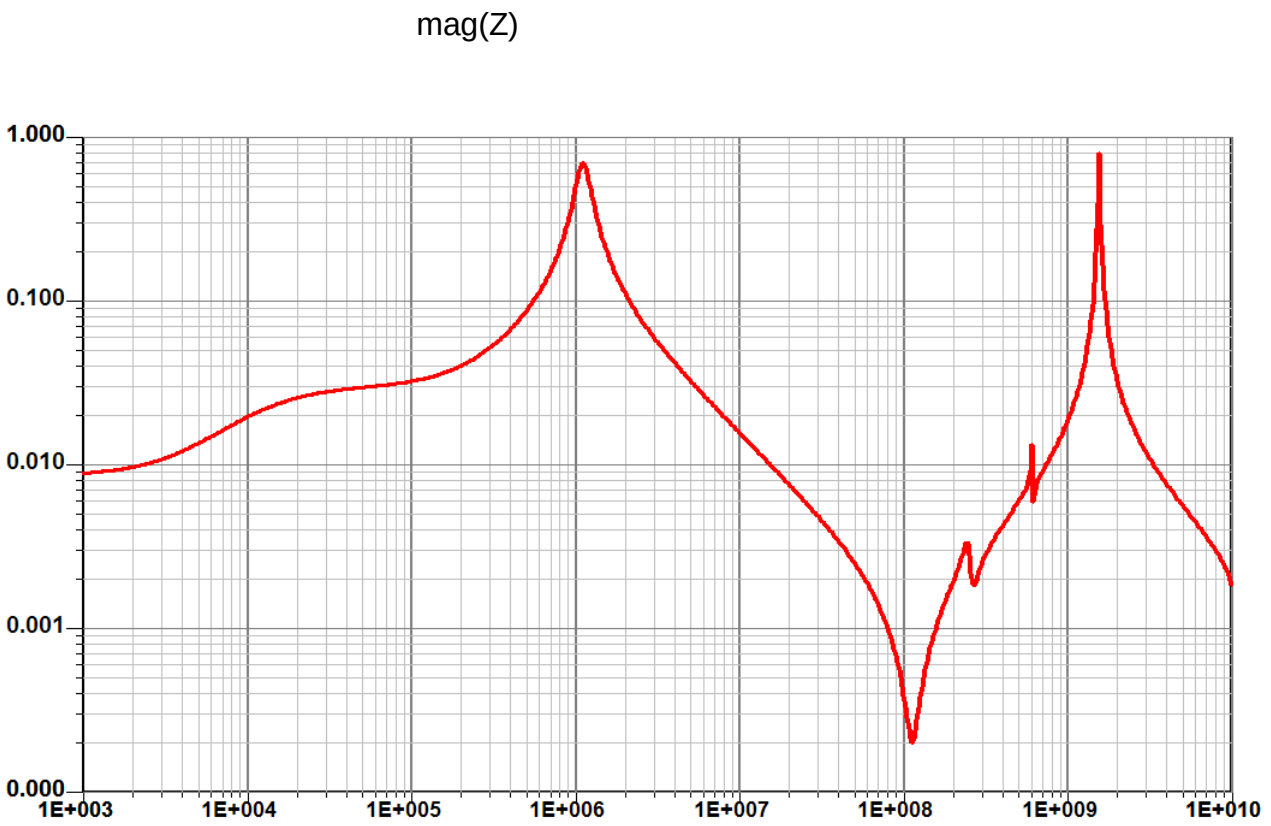
大电解电容：470uF (232KHz)



主板高频电容：100nF (26MHz)

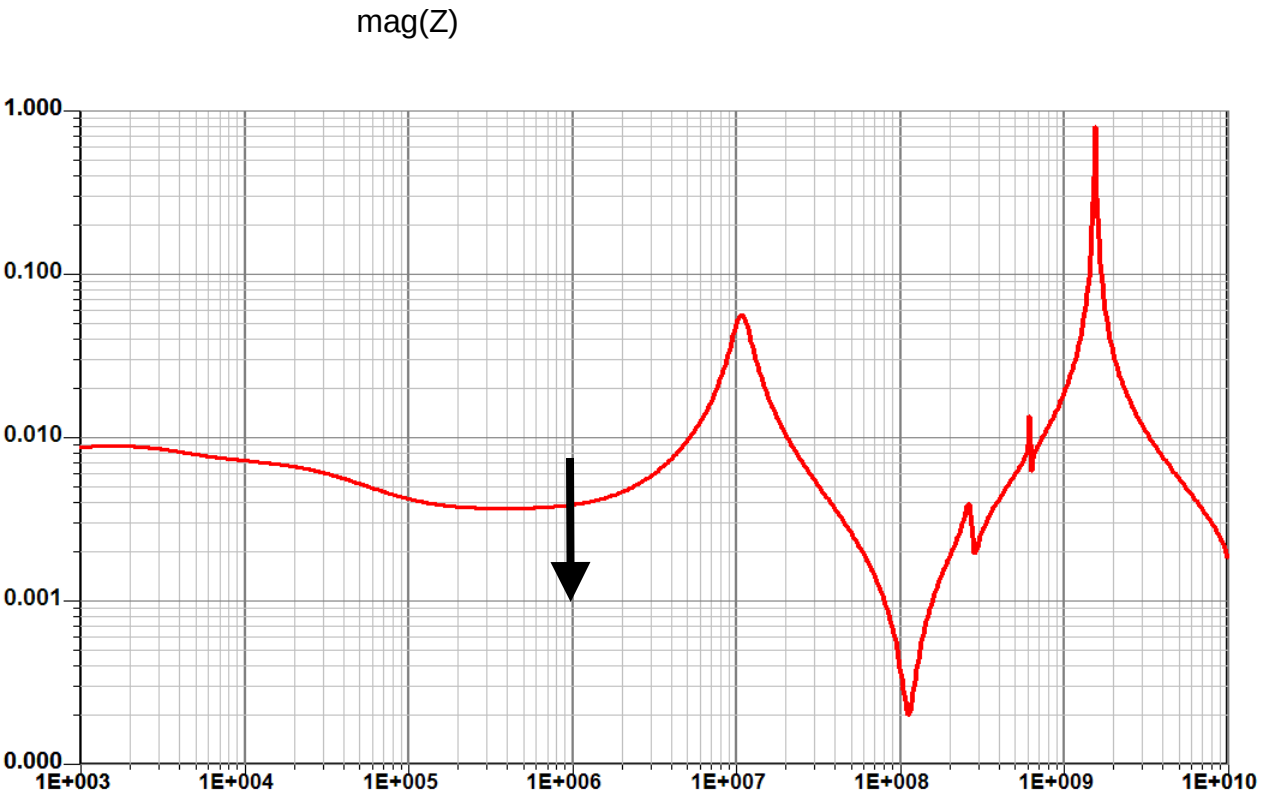
Example1：去耦电容效应

原始PDN网络的输入阻抗



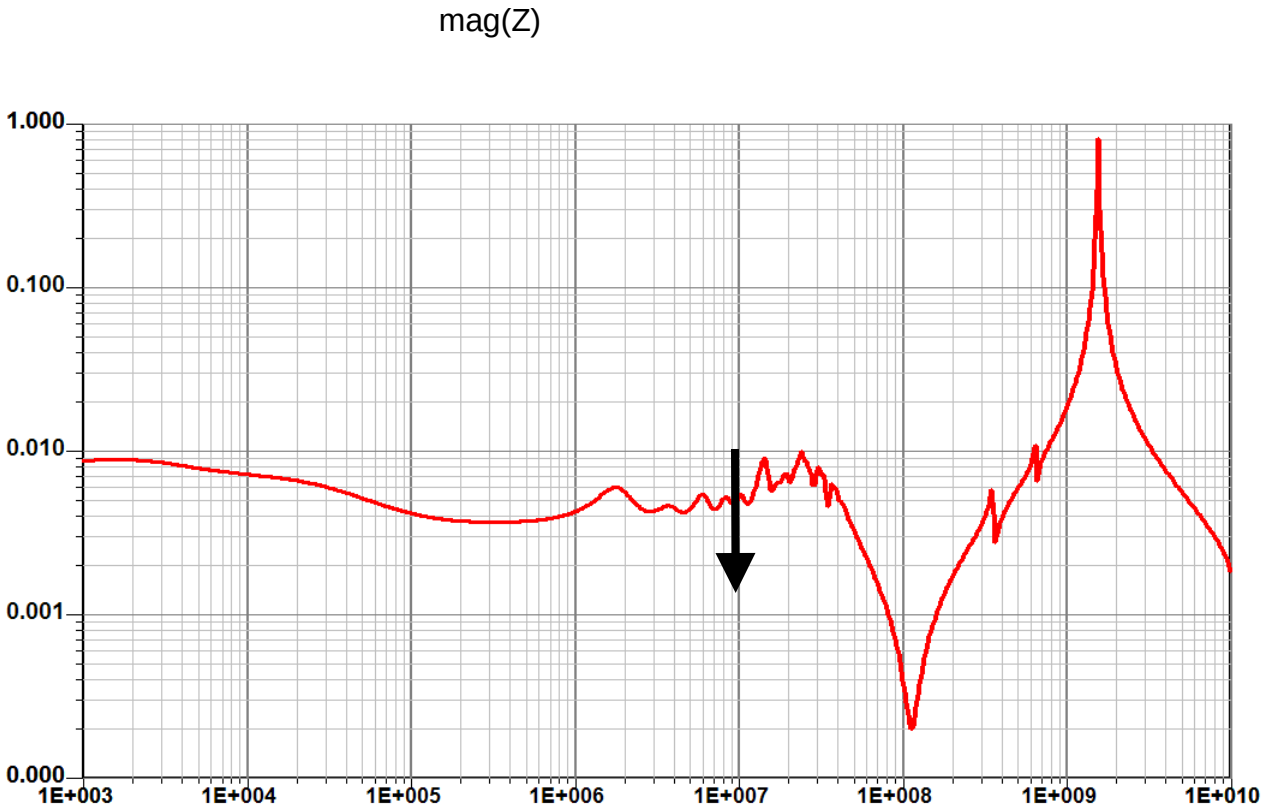
Example1：去耦电容效应

加Bulk低频电容

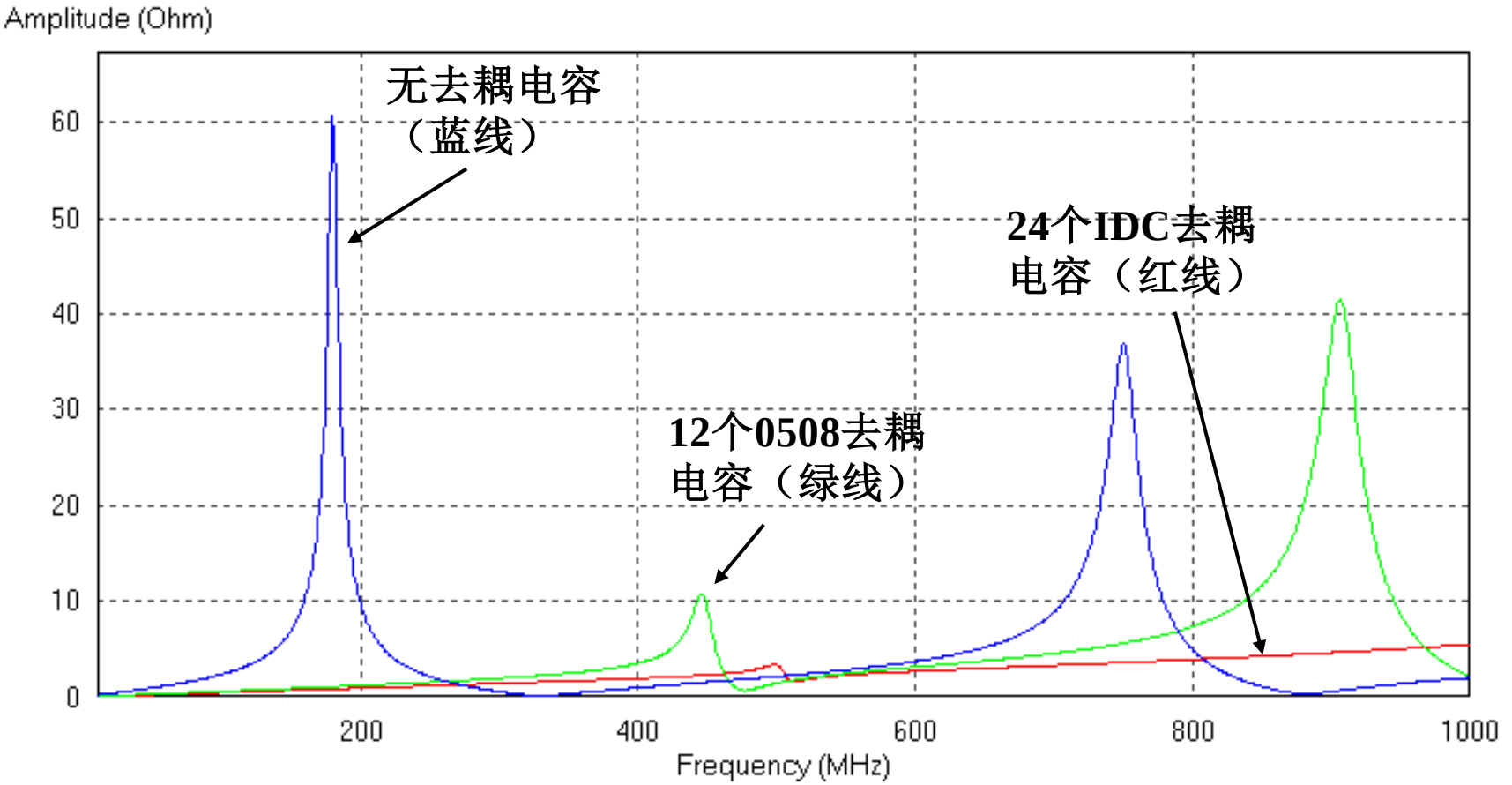


Example1：去耦电容效应

加高频电容

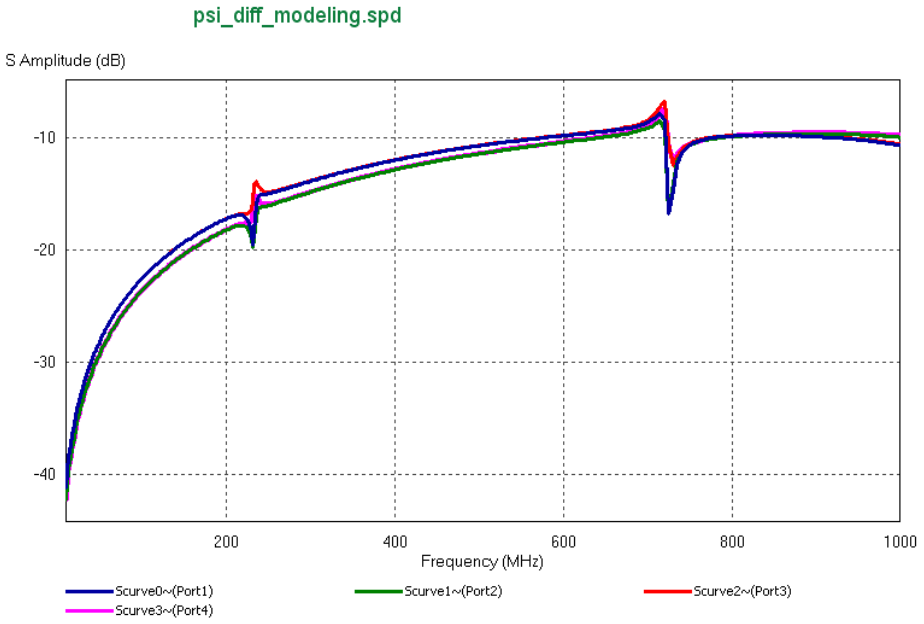


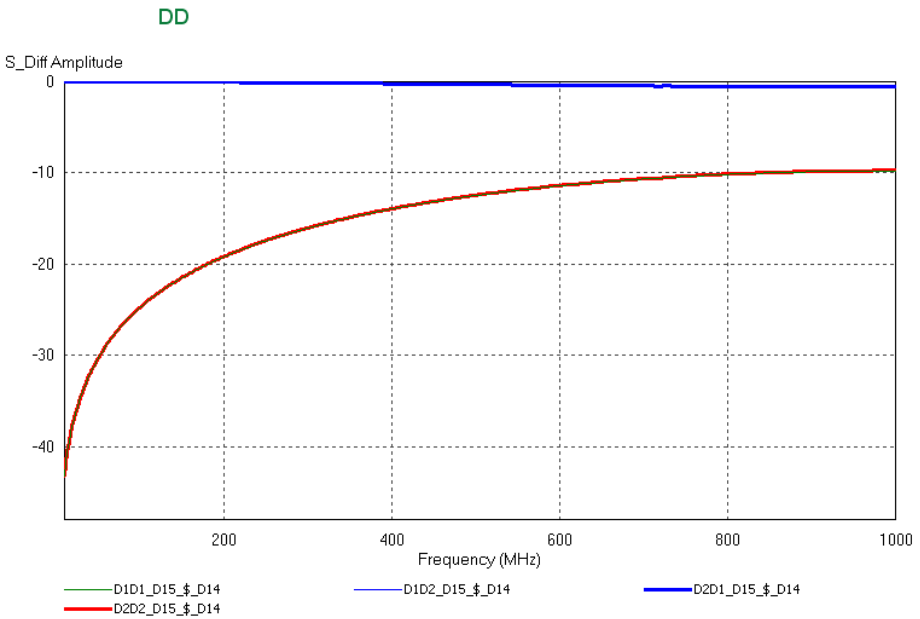
PowerSI典型应用1：电源网络的模型提取



- 电源/地网络的阻抗提取，研究其谐振频率以及输入阻抗
- 为电源/地网络的设计性能和去耦电容的放置提供依据

PowerSI典型应用2：信号网络的模型提取





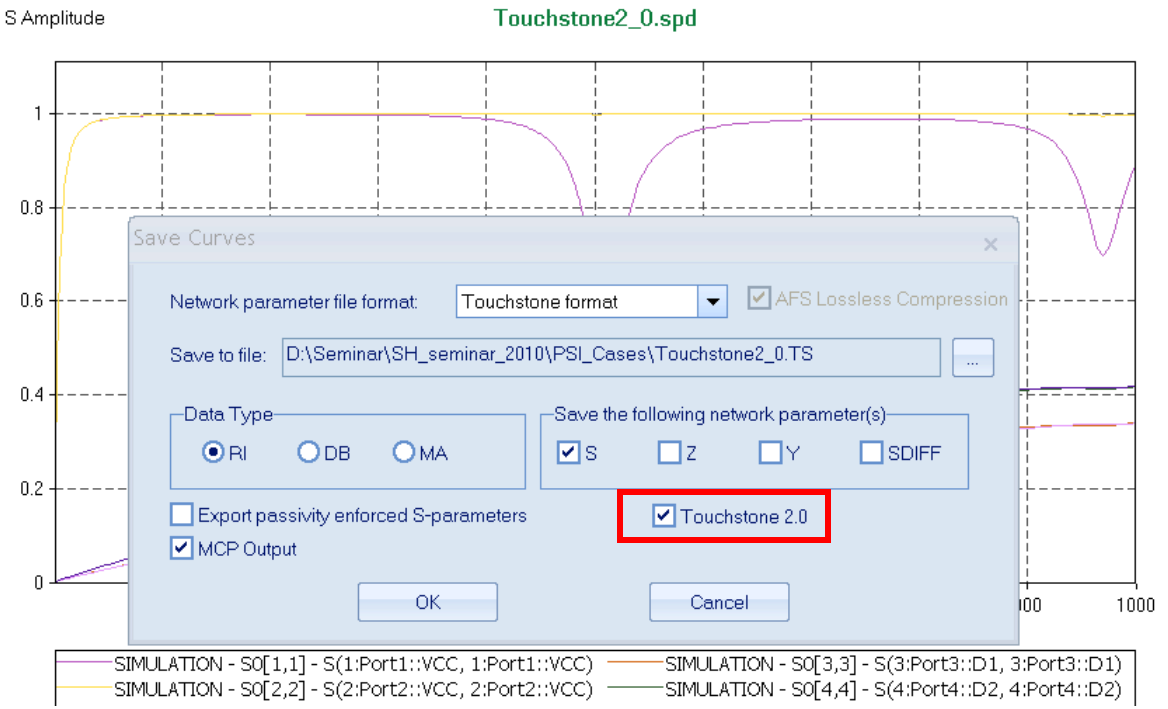
单端4端口网络
S11

差分信号线对
S11/S12

- 信号网络的S参数提取，研究信号的插入损耗及反射系数
- 为单端和差分信号对的设计性能及终端匹配提供依据

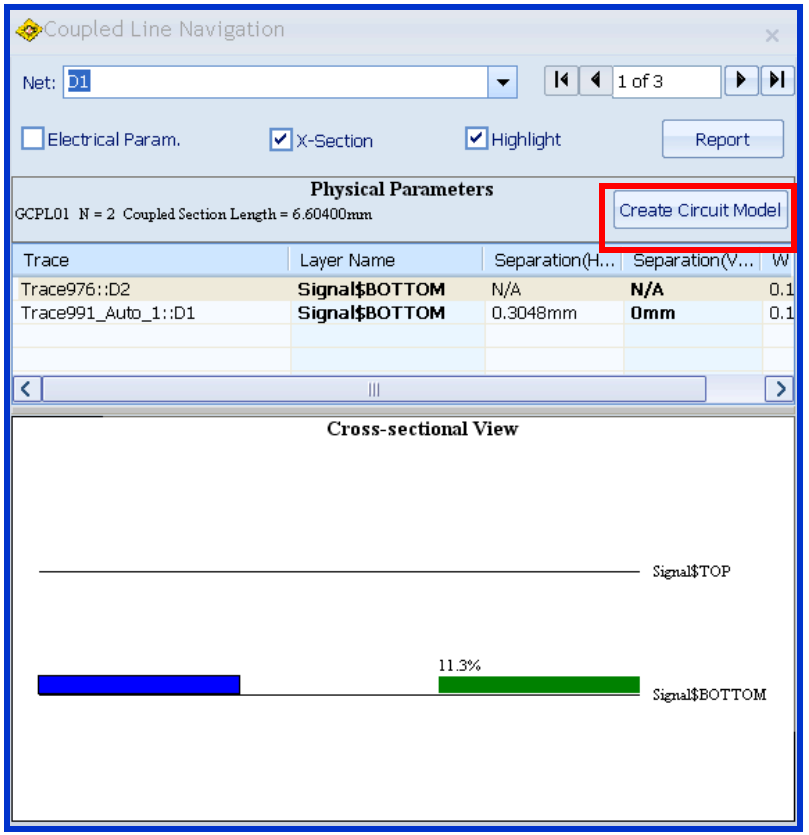
特色：支持TouchStone2.0

- Touchstone2.0的特点：与1.0兼容, 于2009年7月发布；支持混合模式（单端+差分），使SI仿真时可以更好的考虑 PDN对信号的影响；Per-port 阻抗参考，使频域建模时设置不同的Port阻抗成为可能；去除了数据点数和端口数的上限，方便了对大型IC的建模；Z和Y参数不再参照Z0进行归一化。
- PowerSI10.0是业界最早支持Touchstone 2.0模型的工具之一，可方便的导出和导入。



➢ PowerSI可直接导出Touchstone 2.0模型

特色：支持W-element




```
.SUBCKT GCPL01_ckt pos0 pos1 ref1 neg0 neg1 ref2
.Model GCPL01 W MODELTYPE=RLGC N=2
+ Lo=
+ 4.25240986e-007
+ 1.19147884e-007 4.25240986e-007
+ Co=
+ 8.05636637e-011
+ -1.36862092e-011 8.05636638e-011
+ Ro=
+ 3.61265663e+000
+ 0.00000000e+000 3.61265663e+000
+ Go=
+ 0.00000000e+000
+ -0.00000000e+000 0.00000000e+000
+ Rs=
+ 8.58920131e-004
+ 0.00000000e+000 8.58920131e-004
+ Gd=
+ 0.00000000e+000
+ -0.00000000e+000 0.00000000e+000

W1 pos0 pos1 ref1 neg0 neg1 ref2
+ N=2 L=6.60400000e-003 RLGCModel=GCPL01
FGD=5.00000000e+009
.ENDS
```

导出W-Element模型　　**生成的W-Element模型**

- 点击Net Manager>Coupled Lines>Coupled Lines Report，你可以看到耦合的详细信息，包括哪些线之间超过耦合门限，耦合长度，耦合百分比以及耦合的电参数
- 点击Create Circuit Model，则可生成2根临近传输线D1和D2的W-element子电路，从而对常见传输线模型的支持得到了增强

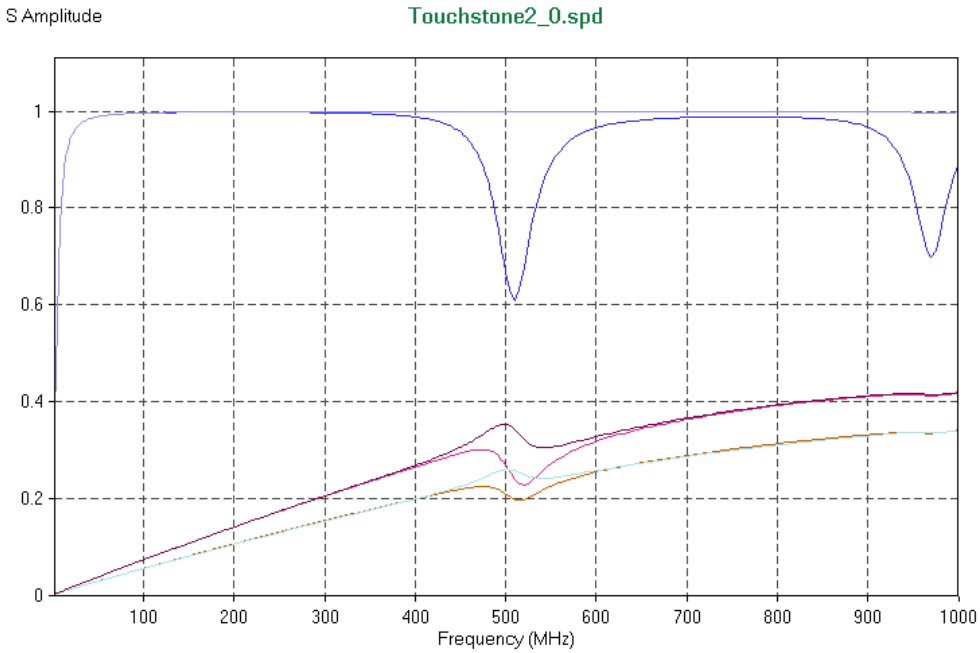
特色：自动生成Report

3.2 Simulation results curve displays

S	Amplitude	DefaultCurve	to Curve

2.3 Port setup

Port number	Port name	(+) hook	(-) hook	Referen
1	Port1	U17::48::VCC	U17::50::GND	0.1
2	Port2	P1V5::77::VCC	P1V5::90::GND	0.1
3	Port3	U17::100::D1	U17::98::GND	50
4	Port4	U17::99::D2	U17::98::GND	50
5	Port5	8::D1	10::GND	50
6	Port6	7::D2	10::GND	50

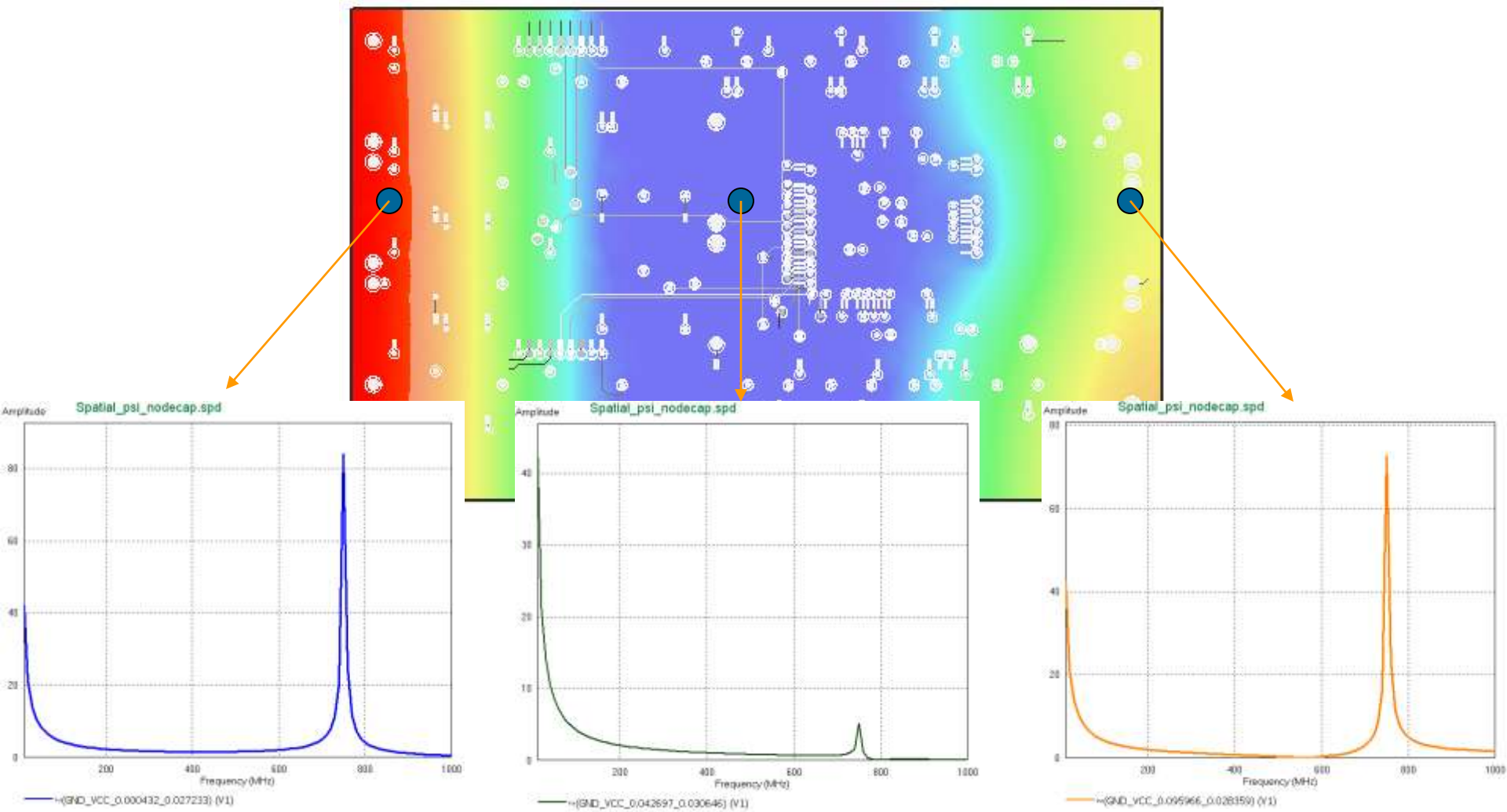


端口设置

S参数结果

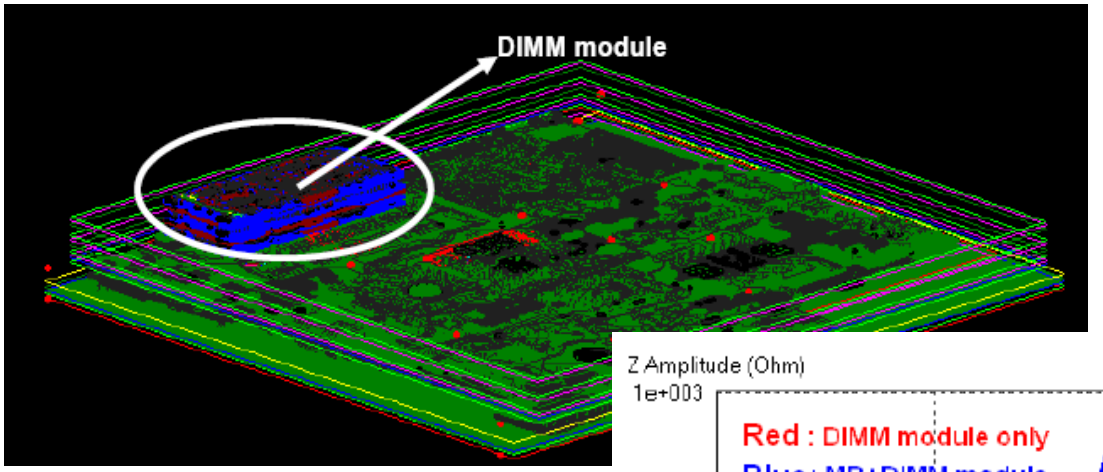
- PowerSI Ver10.0的仿真自动化程度得到了较大的提高
- 点击File>Report则可生成相应的仿真报告，报告内容主要包括基本的设置信息和常见的仿真结果（如S/Y/Z参数等），使用户可以在最短时间内对仿真信息一目了然

特色：空间模式



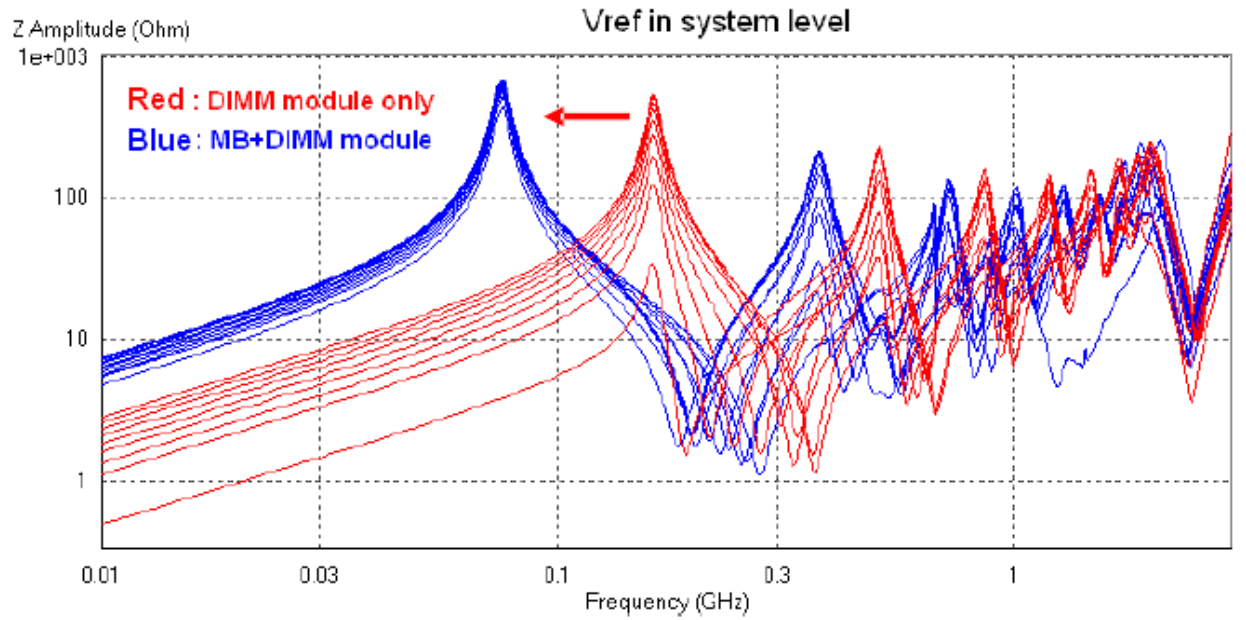
- PowerSI能在指定扫频源下得出整板各个位置处的电压波动频域响应
- 该模式可以从全局上把握PCB设计的好坏，并用于指导去耦电容的放置

特色：多板的联合仿真



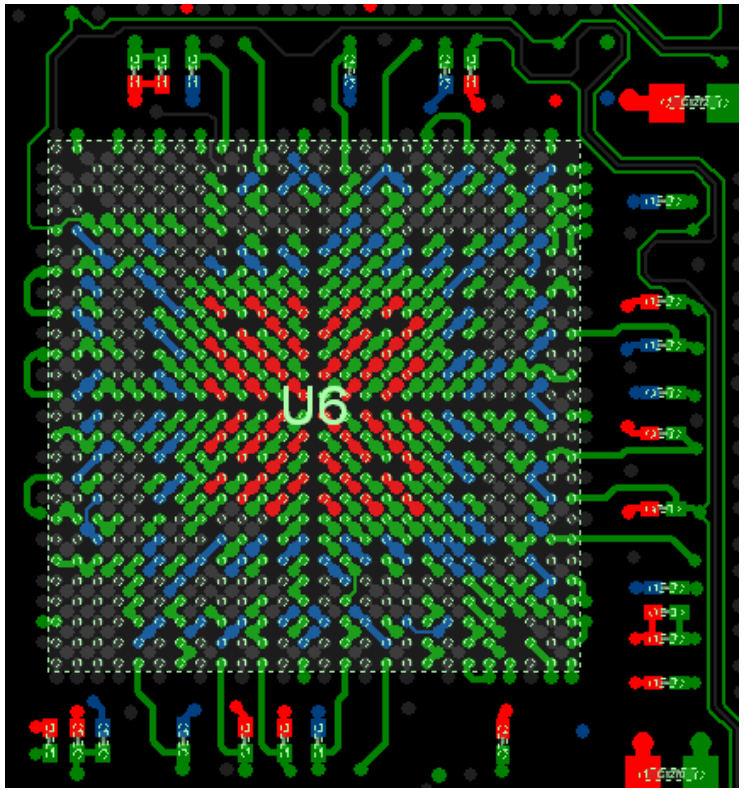
子板+主板的结构

子板对主板Z参数的影响



- 使用File>Merge功能，PowerSI能完成多板的级联仿真
- 从而使多板仿真具有更高的精度，并发现更多设计上的隐患

特色：高密度过孔的自动检测和处理



FPGA的BGA管脚处为高密度过孔区域

- 在一些重要的IC芯片（如CPU或FPGA）BGA管脚的Fanout区域，通常有高密度的过孔、反焊盘区域
- PowerSI的仿真引擎将自动去检测和补偿这部分RLGC的突变效应，大大提高了仿真的精度

特色：支持多阶SPICE模型

Definition :

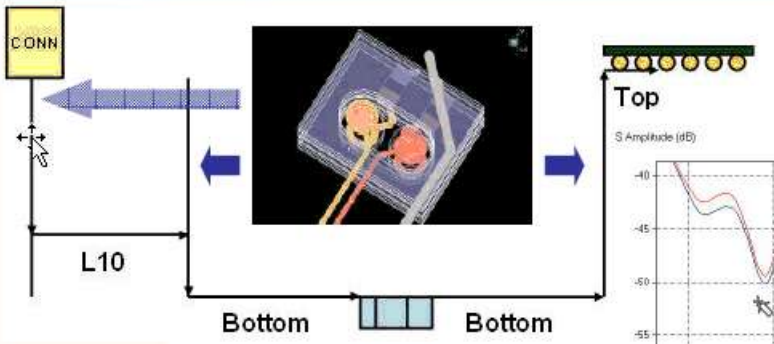
```
lloop 1 2 1n
Ll1  2     3a     4.067255e-010
C11  3a    32a       9.270603e-009
R11  32a    4a       2.064223e-001
Lr1  4a    3         4.067255e-010
Ll2  3a    5a         1.553709e-011
C2   5a      31a     9.270603e-009
R2   31a   6a         2.064223e-001
Lr2  6a    4a         1.553709e-011
Ll3  5a    7a        1.553709e-011
C3   7a    30a       9.270603e-009
R3   30a   8a        2.064223e-001
Lr3  8a    6a        1.553709e-011
Ll4  7a    9a           1.553709e-011
C4   9a    29a       9.270603e-009
R4   29a   10a       2.064223e-001
Lr4  10a   8a        1.553709e-011
Ll5  9a    11a       1.553709e-011
C5   11a   28a       9.270603e-009
R5   28a   12a       2.064223e-001
Lr5  12a   10a       1.553709e-011
Ll6  11a   13a       1.553709e-011
C6   13a   27a       9.270603e-009
R6   27a   14a       2.064223e-001
Lr6  14a   12a       1.553709e-011
1 3 4 esr
rdum 2 3 10Meg
vsense 4 5 0 ac=0
```

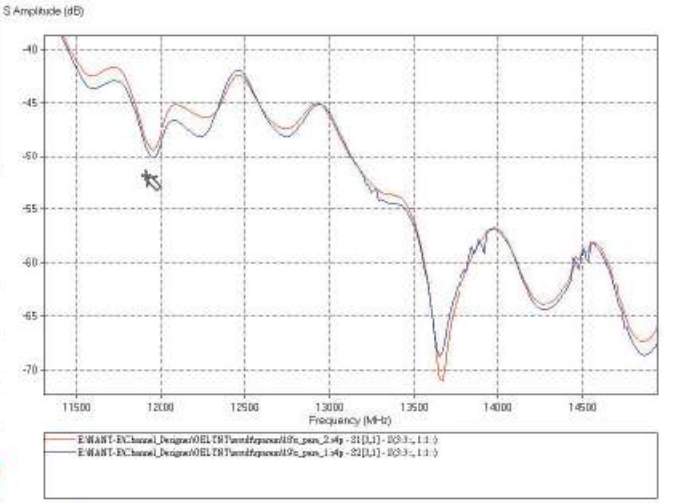
- 仿真模型不仅支持S参数/CPM模型/MCP模型，同时也支持多阶SPICE模型，保证模型输入的灵活性

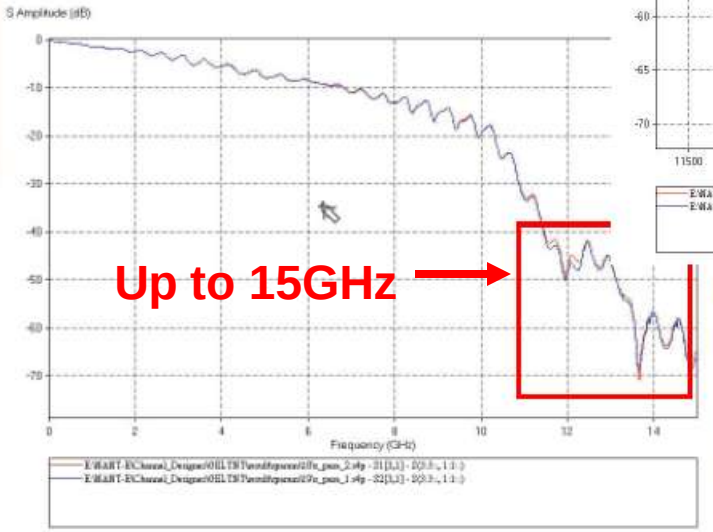
案例1：PCB局部结构的高频模型提取

4. Tools

❶ Frequency Domain Tool







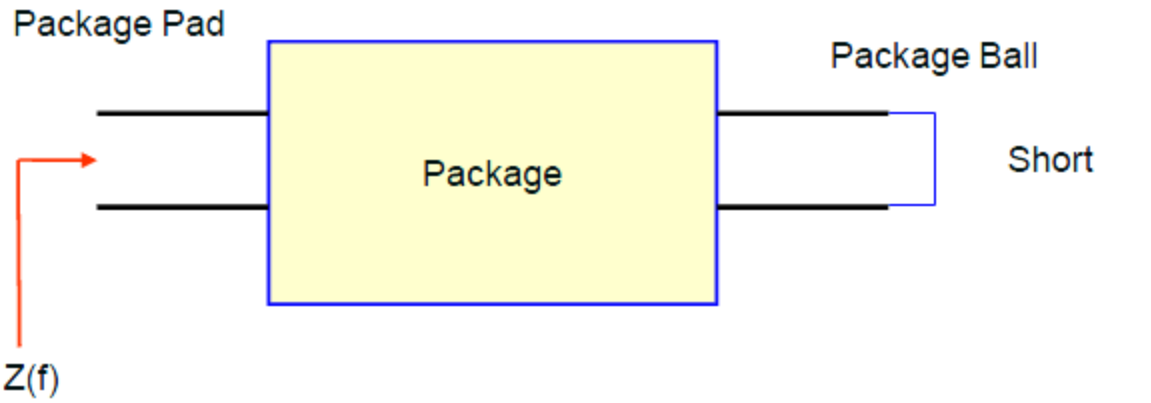
RED: Sigrty's PowerSI 9.1 – about 1.5hr

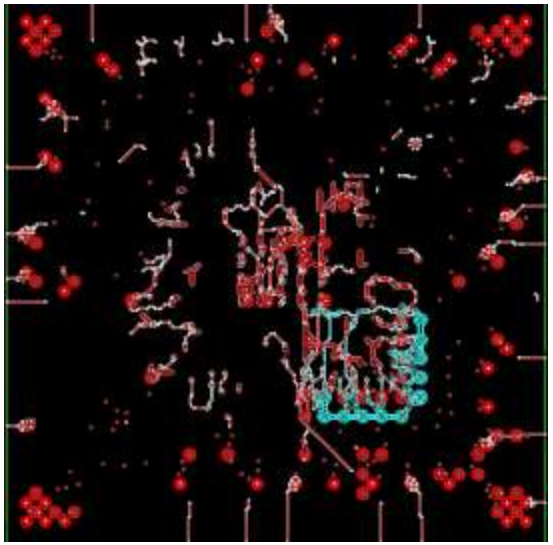
BLUE: Third-Party Tool – about 5hr

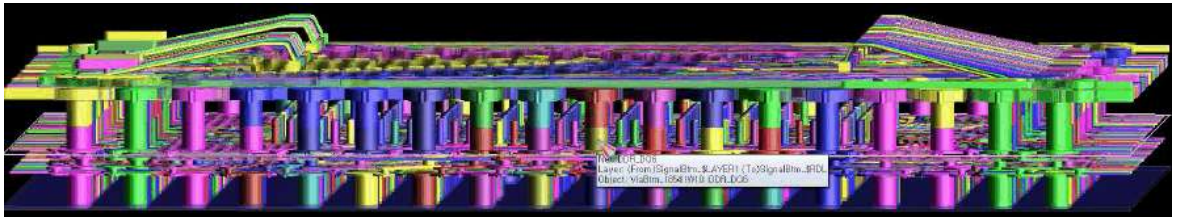
8 Cores 2.63GHz (but only 4 cores activated during computation) + 48GB DDRIII +WinXP 64bit

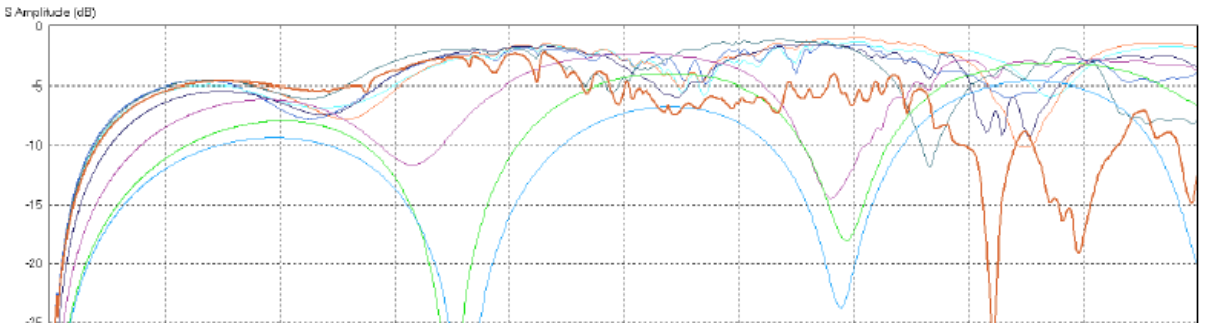
➢ 来源: Optimization for 10Gbps Serdes, Delta Networks, May2010.

案例2：PKG关键信号的模型提取



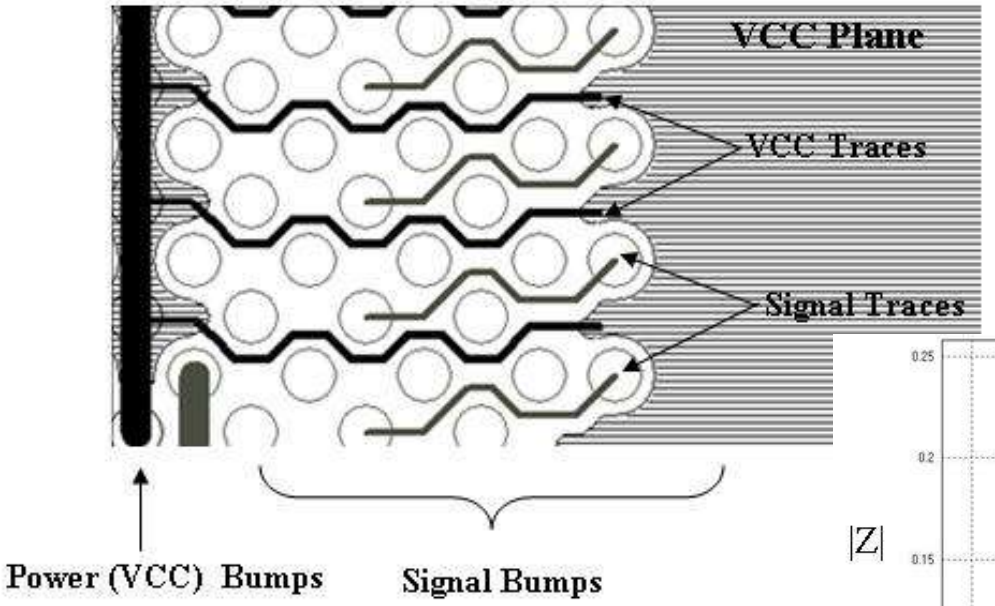






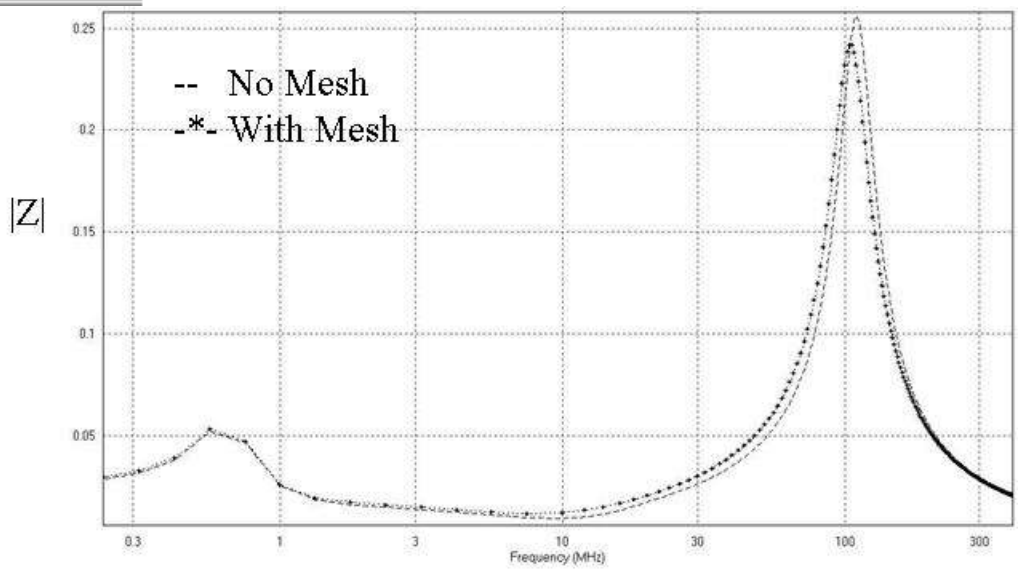
- 来源: Mobile Package Design and Simulations, Samsung, Mar2009.

案例3：带Power Mesh的PDN模型提取



待研究的网格化电源

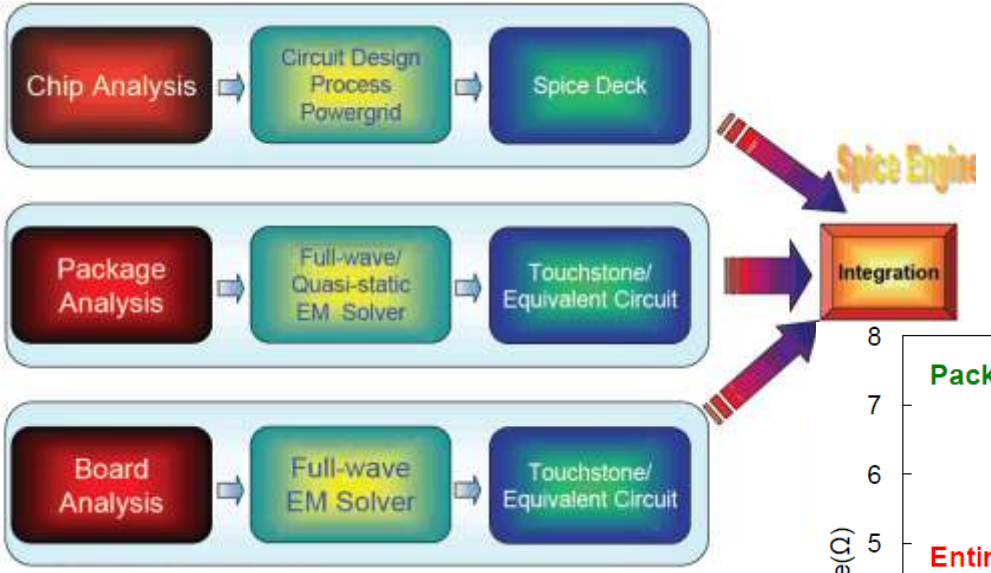
PDN性能曲线的比较



Frequency

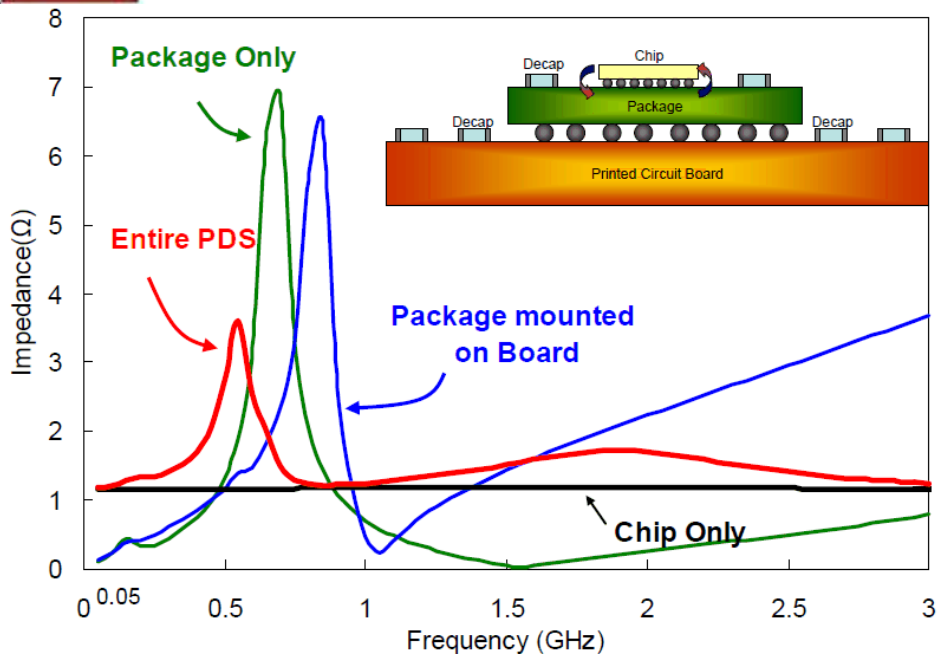
➢ 来源: A novel methodology to handle the layout constraints for designing an optimal Power Delivery Network, Intel, Feb2009.

案例4：IC+PKG+BRD的PDN模型提取



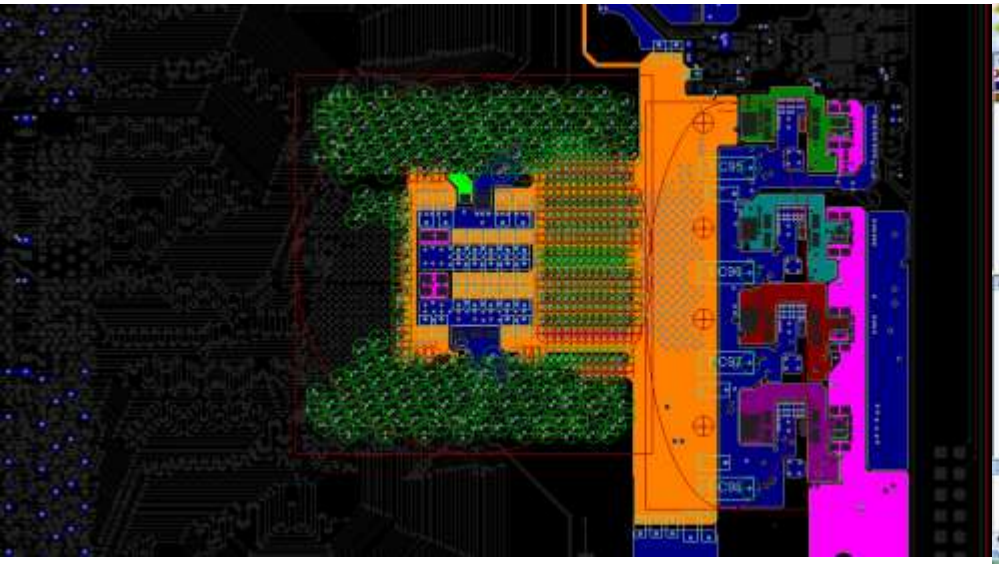
传统的PDN全系统仿真流程

各结构对PDN性能的影响

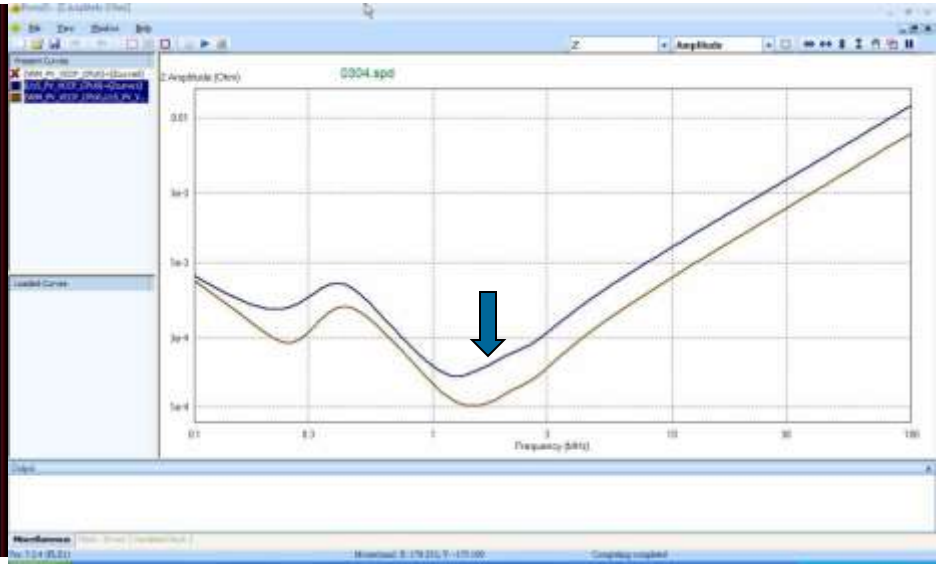


➢ 来源: Analysis of Entire Power Distribution System of Chip, Package and Board for High Speed IO Design, Azurewave, Oct2008.

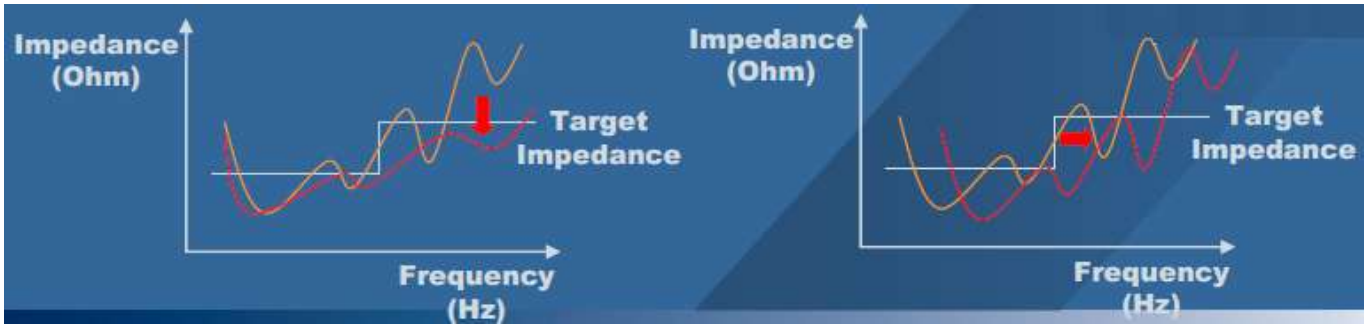
案例5：PCB的PDN阻抗优化



Port设置



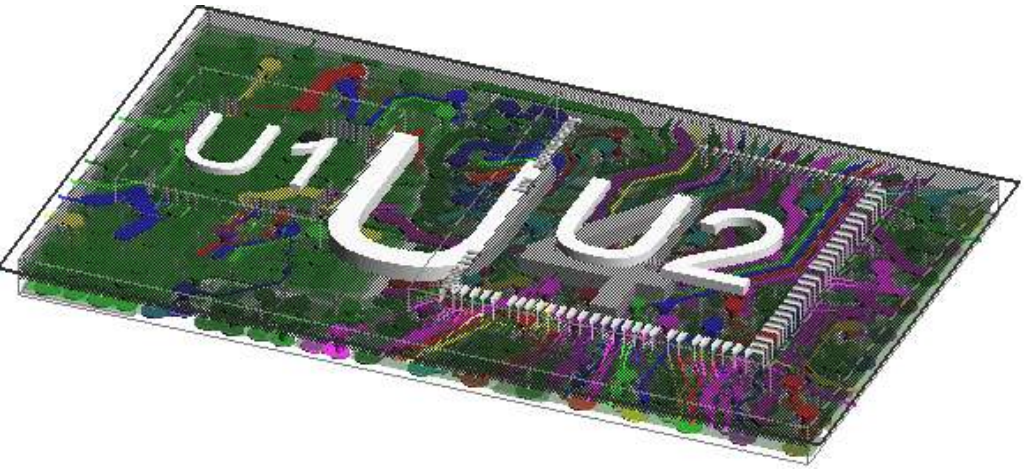
Impedance优化



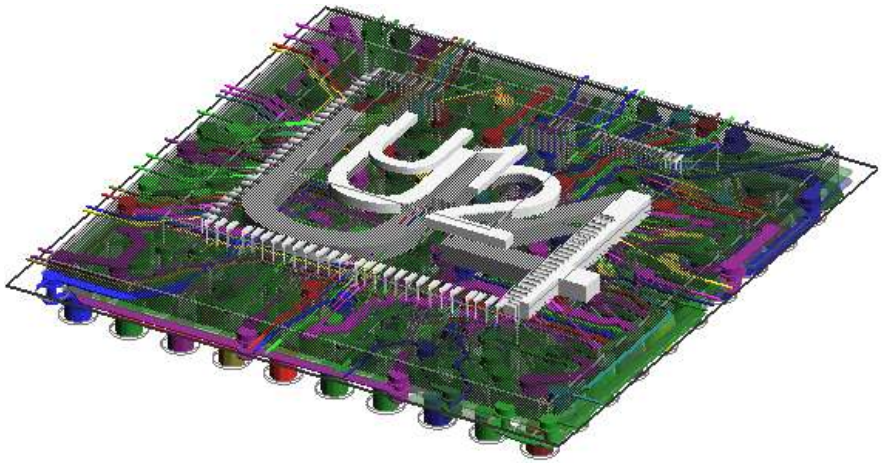
优化**Input Impedance**以满足**Target Impedance**的要求

- 来源: Power Integrity in System Design, Flextronics, May2008.

案例6：CMMB芯片RF与Digital信号的仿真（1）



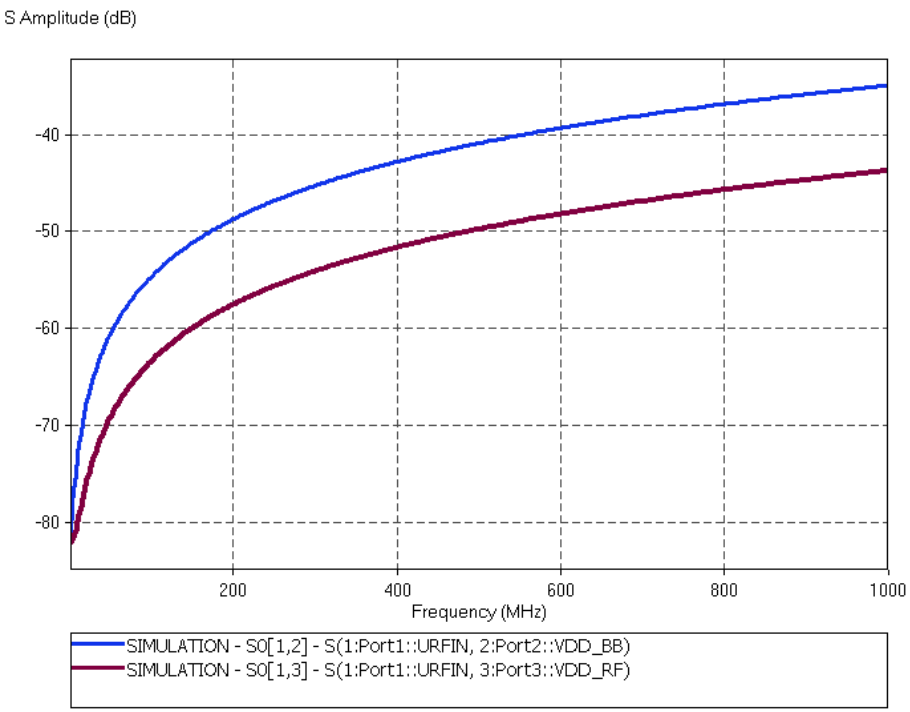
Side-by-side Die SiP



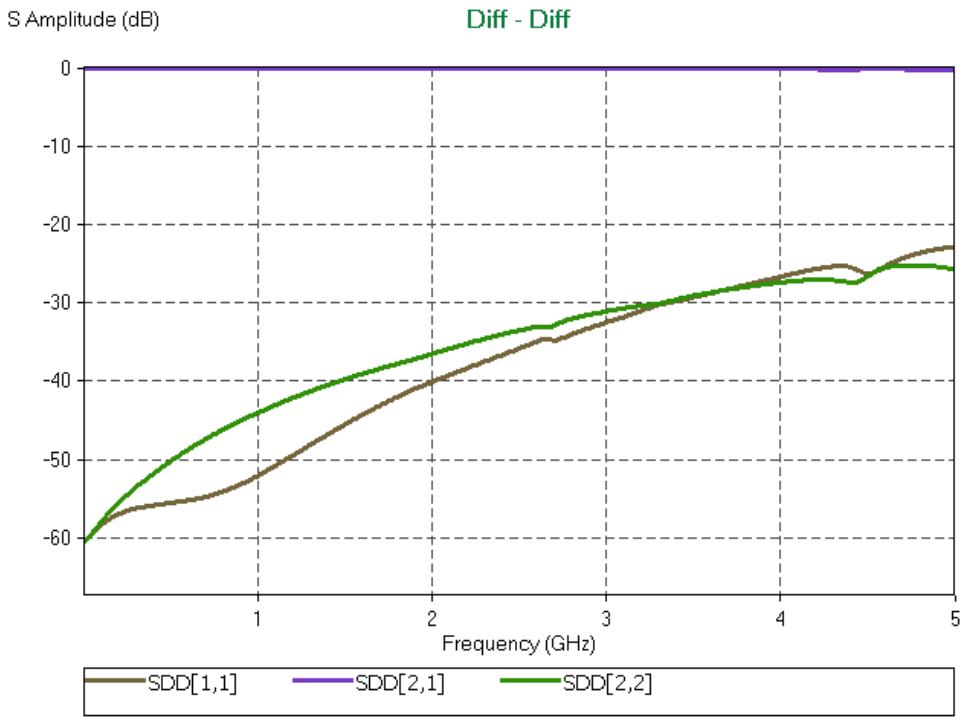
Stacked-die SiP

- CMMB芯片通常包含一块RF射频接收芯片，以及一块DSP数字处理芯片。其射频部分采用高性能的RF变频模块，支持的频段范围为：50MHz ~ 870MHz。
- PSI 可以用来分析信号走线的S参数，关键信号线与其他信号线以及电源之间的隔离度，电源网络的频域阻抗特性等。

案例6：CMMB芯片RF与Digital信号的仿真（2）



RF的隔离度仿真



Digital的差分对仿真

- PowerSI可仿真RF接收信号与邻近的信号网络（或电源网络）在各个频点的隔离度指标
- PowerSI还可仿真DSP关键差分对信号的差分性能（如上图的Diff-Diff）

PowerSI 总结

- **PowerSI是一款专业的频域仿真工具，具有以下鲜明特点：**
  - 最大特色之一是，将电源网络和地网络当作非理想的情况来处理，考虑的是非理想的信号返回路径；
  - 最大特色之二是，由于采用了混合仿真引擎（包含电路求解器、电磁场求解器和传输线求解器），因此仿真效率特别高，而且能够处理尺寸特别大、规模特别复杂的系统；
  - 能够提取PCB板级和封装级电源网络与信号网络的阻抗（Z）参数及散射（S）参数，找出关键的谐振频率点分布，为精确分析电源和信号的性能提供依据；
  - 能够分析板上任意位置的空间波动特性，为评估电源的覆铜方式及确定去耦电容的放置位置提供依据；
  - 能够分析PCB的本征谐振模式，为分析PCB本身的结构特性提供依据；
  - 能够分析整板远场和近场的EMI/EMC性能，为解决板级的EMI/EMC问题提供依据；
  - 适用于布线前和布线后的 PI仿真，包含单板或多板；
  - 配合Sigrity公司的另一工具Broadband SPICE，可以得到PCB和封装的SPICE等效电路模型；
  - 评估和优化去耦电容的放置位置；
  - 评估不同的电路模型对PI 性能的影响；
  - 评估不同电路组成部分（平面，线，通孔）之间的电磁耦合；
  - 分析敏感信号之间的隔离度强弱，为射频芯片的封装或高灵敏度的PCB设计提供指导。

电容优化：OptimizePI

为何要使用OptimizePI?

- **困扰**：PDN的电源噪声（包括低频和高频）经常超标，或者性能过设计太多、成本较高，而目前的PCB或PKG设计越来越复杂，电容的位置和容值选择往往大大超出了设计人员的经验所达。

- **解决方案**：OptimizePI可以自动考虑PDN网络中的各种寄生参数，并完成去耦电容位置和容值的自动化排列组合，是目前解决此类问题的唯一可靠途径。

OptimizePI的后仿真

仿真流程

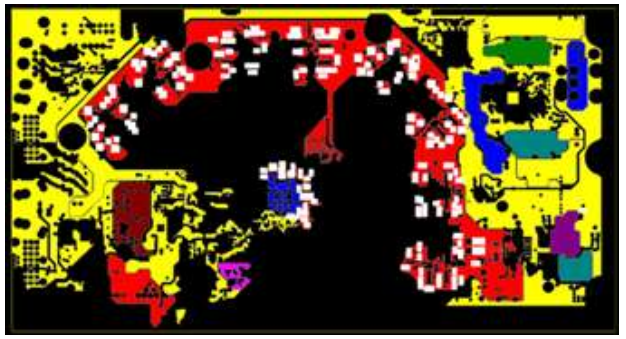
Decap库文件

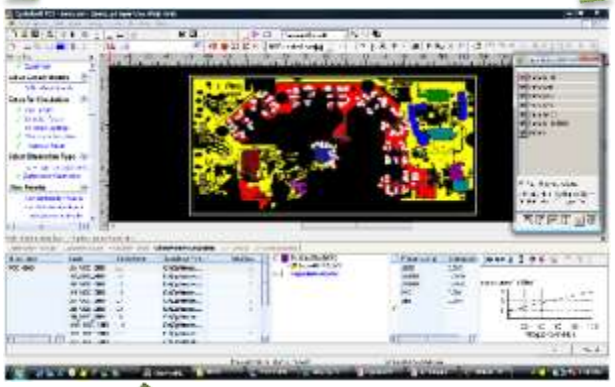
1 输入

- 电容模型
- 成本

(器件成本+安装成本)

初始的PCB

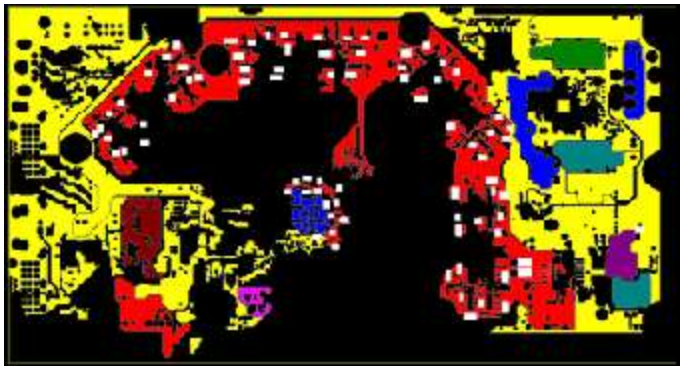




2 OptimizePI优化

3 输出

新的PCB

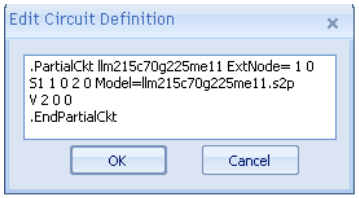


电容库：可采用内置电容库或自己设置

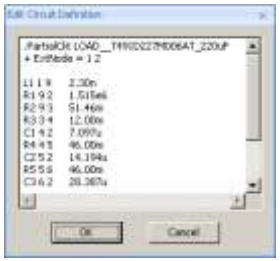
Capacitor Library Manager

Project Library | External Library

ID	Part No.	Size	Model Type	Cnom (nF)	Cact (nF)	L (nH)	R (mOhm)	Component Cost	Mounting Cost	Self-Re...
10	C_10nF_0402_GRM155R71C104KA88	0402	RLC	10	9.5	0.47	78	0.00476	0.001	75.32M
12	C_22nF_0402_GRM155R71C223KA01	0402	RLC	22	21.2	0.45	44	0.00448	0.001	51.53M
14	C_47nF_0402_GRM155R71A473KA01	0402	RLC	47	44.4	0.42	28	0.00742	0.001	36.86M
2	C_100nF_0402_GRM155R71C104KA88	0402	RLC	100	93.9	0.41	19	0.00476	0.001	25.65M
4	C_220nF_0402_GRM155R60J224KE01	0402	RLC	220	195	0.44	20	0.005	0.001	17.18M
6	C_470nF_0402_GRM155R60J474KE18	0402	RLC	470	340	0.45	15	0.008	0.001	12.87M
8	C_1uF_0402_GRM155R60J105KE19	0402	RLC	1000	620	0.4	10	0.02506	0.001	10.11M
17	C_1uF_0603	0603	RLC	1000	1000	0.4	10	0.01	0.001	7.96M
5	C_2p2uF_0402_GRM155R60J225ME15	0402	RLC	2200	1204	0.39	7	0.04113	0.001	7.34M
7	C_4p7uF_0603_GRM188R60J475KE19	0603	RLC	4700	2740	0.49	8	0.07448	0.001	4.34M
1	T495B106M010ATE750	3528	RLC	10000	10000	1.8	227	0.25	0.001	1.19M
11	C_10uF_0603_GRM188R60J106ME47	0603	RLC	10000	4991	0.58	5	0.092	0.001	2.96M
13	C_22uF_0805_GRM21BR60J226ME39	0805	RLC	22000	11360	0.44	2	0.25004	0.001	2.25M
15	C_47uF_1206_GRM31CR60J476ME19	1206	RLC	47000	29400	0.48	3	0.428	0.001	1.34M
3	C_100uF_1206_GRM31CR60J107ME39	1206	RLC	100000	48500	0.71	3	0.529	0.001	857.67K
9	C_220uF_Dcase_T520D227M006ATE040	7343	RLC	220000	220000	2.3	20	0.63	0.001	223.74K
16	C_330uF_Dcase_T520D337M006ATE040	7343	SPICE Model	330000				0.63	0.001	199.53K



S参数模型



SPICE模型

内置的电容库包括：

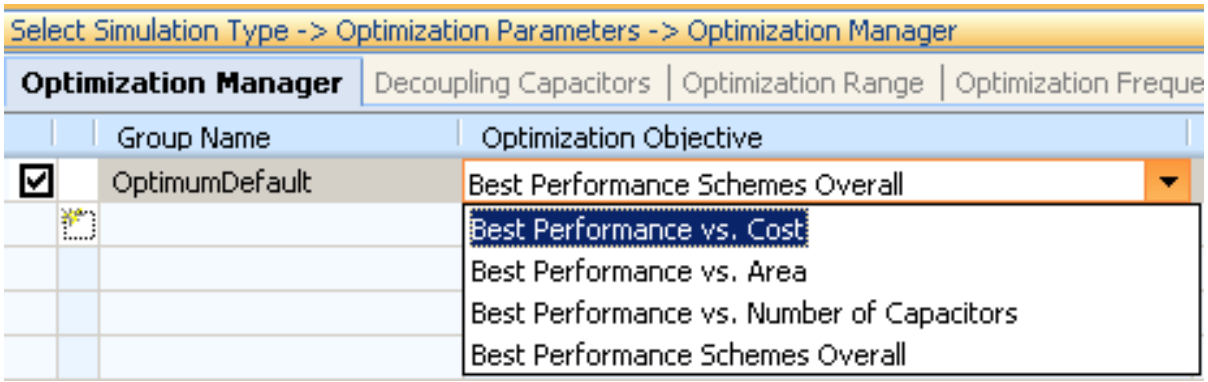
KEMET Electronics Corp.

muRata

TDK

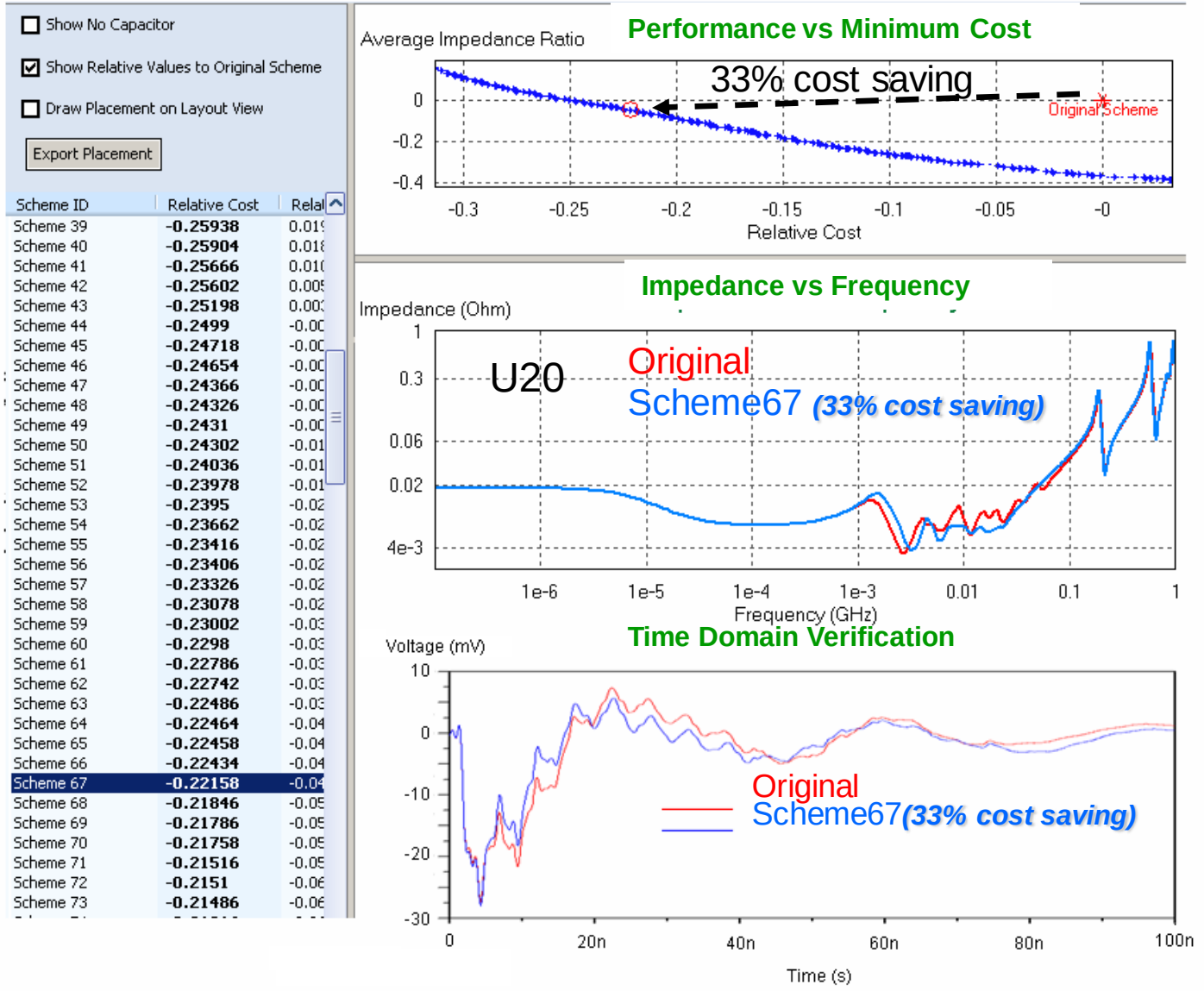
TAIYO YUDEN

优化目标：根据需求设置



1. **最佳性能 vs 成本** ➔ 默认的优化方案，改善性能并降低使用电容的总成本，适用于对性能和成本都比较关心的产品
2. **最佳性能 vs 面积** ➔ 改善性能并减少使用电容的总面积，适用于高密度的产品
3. **最佳性能 vs 电容数** ➔ 改善性能并减少使用电容的数目，适用于找到对系统PI性能影响最小的电容序列
4. **总体最佳性能** ➔ 性能是唯一关心的要素，有时可能会增加少许成本，适用于对性能要求非常高的产品

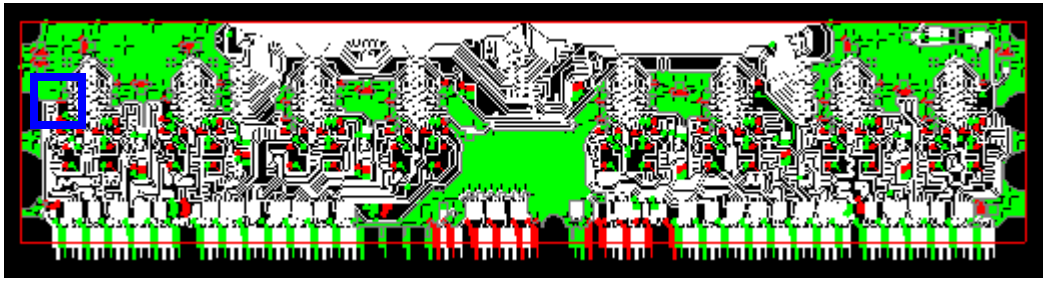
仿真结果：生成一系列最佳性价比方案

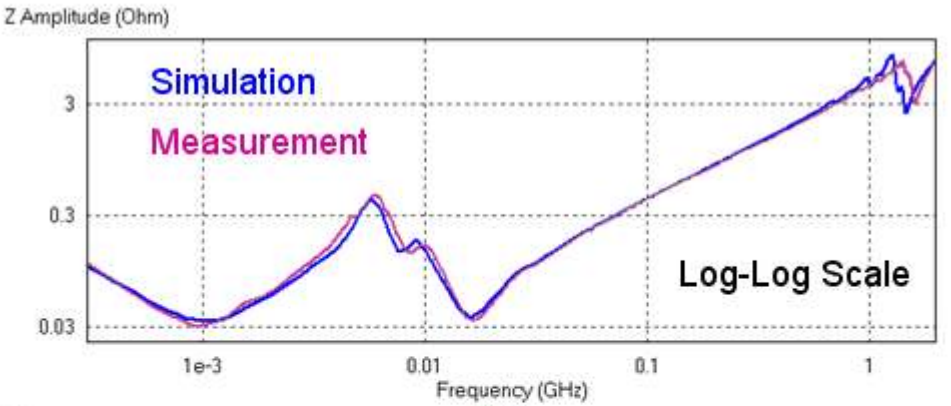


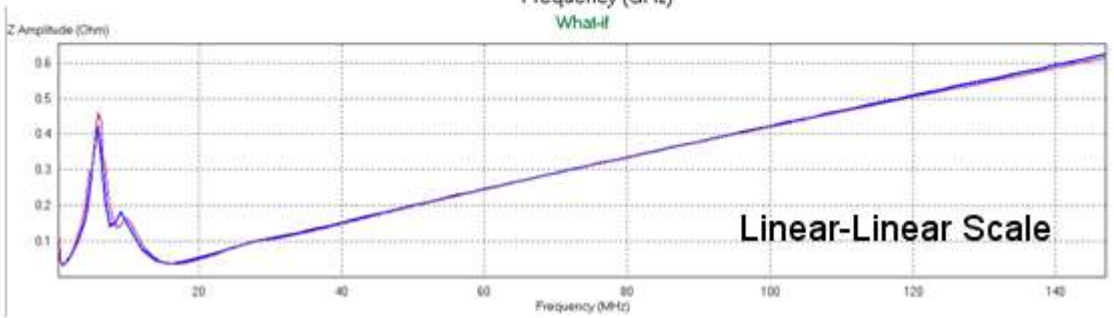
优化方案：电容放置清单

Scheme ID	Cost	Impedanc	C1_1	C2_1	C3_1	C4_1	C5_1	C6_1	C7_1	C8_1	C9_1	C10_	C11_	C12_	C13_	C14_	C15_	C16_	C17_	C18_	C19_	C20_	C21_	C22_	C23_
Scheme 1	0.201	19.965131	X	4	X	X	X	X	2	X	2	X	X	X	X	X	4	4	X	X	X	X	X	3	X
Scheme 2	0.202	19.918919	X	X	X	X	4	X	X	4	X	X	X	X	X	X	X	X	X	X	4	3	X	5	3
Scheme 3	0.21	19.725069	4	X	X	X	X	X	X	3	X	X	2	4	X	X	X	X	2	X	X	X	4	5	4
Scheme 4	0.227	19.676452	X	X	X	5	X	X	X	4	X	2	X	X	2	X	X	X	X	X	X	X	X	5	4
Scheme 5	0.229	19.667312	X	X	X	4	X	X	X	X	2	2	4	X	3	X	X	X	X	X	2	X	X	3	4
Scheme 6	0.236	19.539375	X	X	X	5	3	X	X	X	2	X	X	4	X	5	4	X	4	4	X	X	X	X	X
Scheme 7	0.237	19.285003	3	X	X	X	X	X	X	4	X	X	X	2	X	X	2	X	X	X	X	3	4	5	3
Scheme 8	0.246	19.259111	X	X	X	4	X	X	2	X	X	X	X	X	X	X	X	X	X	X	2	X	X	4	4
Scheme 9	0.256	19.194559	X	4	X	X	X	X	2	X	4	X	X	X	X	X	4	X	X	X	X	X	X	3	X
Scheme 10	0.269	18.857856	X	X	X	X	X	2	4	X	X	X	X	3	X	X	X	X	X	X	X	X	X	1	X
Scheme 11	0.335	18.755864	X	X	X	5	2	X	X	4	X	X	3	X	5	2	X	X	X	2	X	X	X	X	X
Scheme 12	0.337	18.73206	X	X	X	X	4	2	4	X	X	X	X	3	3	X	X	X	X	X	3	3	X	1	X
Scheme 13	0.338	18.702451	X	2	X	X	X	X	3	4	X	X	X	X	X	X	4	X	X	X	X	5	2	1	3
Scheme 14	0.35	18.689192	X	X	X	5	X	X	5	X	X	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 15	0.379	18.624997	4	X	4	X	X	X	X	X	X	X	4	X	X	X	X	X	1	4	X	X	X	5	X
Scheme 16	0.38	18.620311	2	X	X	X	X	4	3	X	X	X	X	5	4	X	X	X	1	X	X	X	4	1	3
Scheme 17	0.382	18.543074	4	2	X	X	X	X	3	X	X	X	X	3	X	X	3	X	X	4	X	X	2	5	X
Scheme 18	0.385	18.516154	X	1	X	X	5	X	X	X	2	X	X	X	X	X	4	X	X	X	2	X	4	X	4
Scheme 19	0.388	18.477548	X	X	X	X	4	4	5	4	4	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 20	0.393	18.427117	X	X	X	5	X	X	X	4	5	X	X	X	5	2	2	X	X	4	X	X	4	4	X
Scheme 21	0.43	18.411733	3	X	X	X	X	X	X	3	X	2	X	X	X	X	X	X	X	X	5	X	1	3	X
Scheme 22	0.439	18.296769	X	X	X	X	2	2	5	4	2	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 23	0.46	18.268527	X	X	X	5	X	X	5	X	X	X	X	X	X	X	X	4	X	X	2	3	X	1	1
Scheme 24	0.486	18.241662	X	X	4	X	X	X	4	4	X	X	X	X	X	X	X	X	X	4	X	2	4	1	5
Scheme 25	0.504	18.20095	3	X	5	X	X	2	X	3	X	X	X	X	X	X	X	X	5	3	X	X	1	1	2
Scheme 26	0.514	18.190489	X	5	X	5	X	5	4	X	2	X	X	X	4	X	X	3	3	2	3	X	3	1	X

精度比对：输入阻抗的仿真测试比对

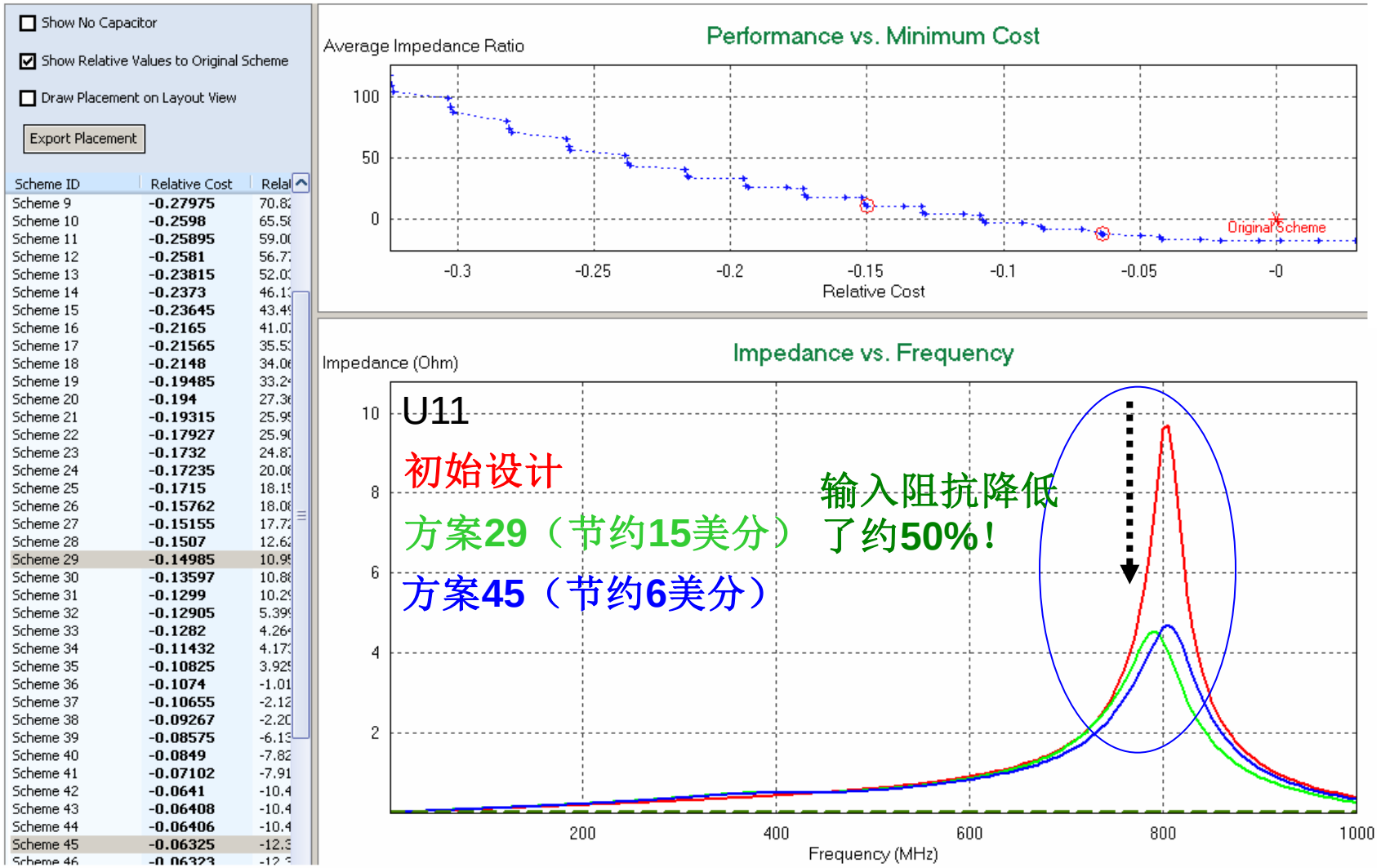






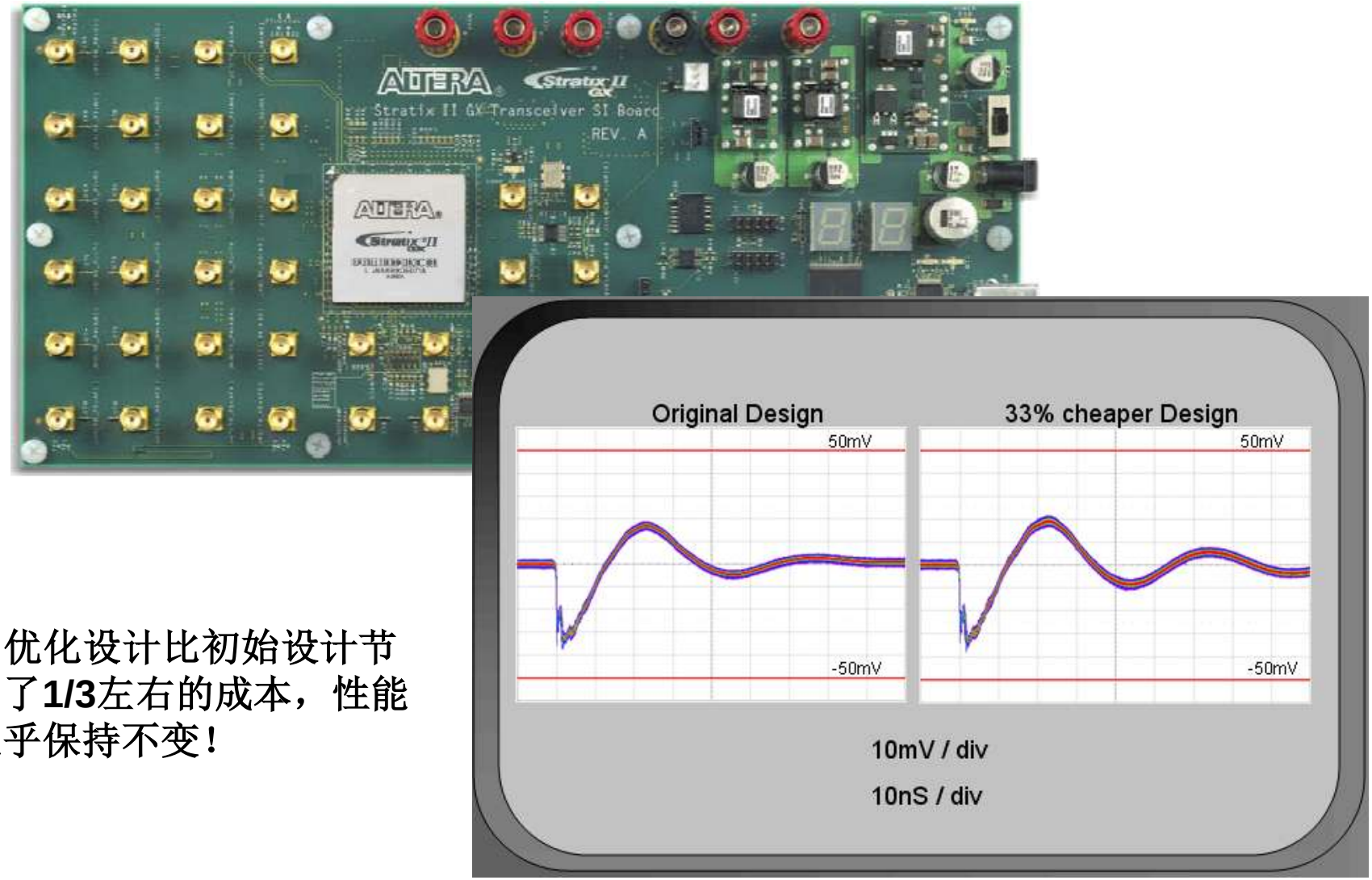
典型应用1：性能优化案例

（DDR2内存模块的阻抗优化）



典型应用2：成本优化案例

（Altera / Sigrity合作项目）



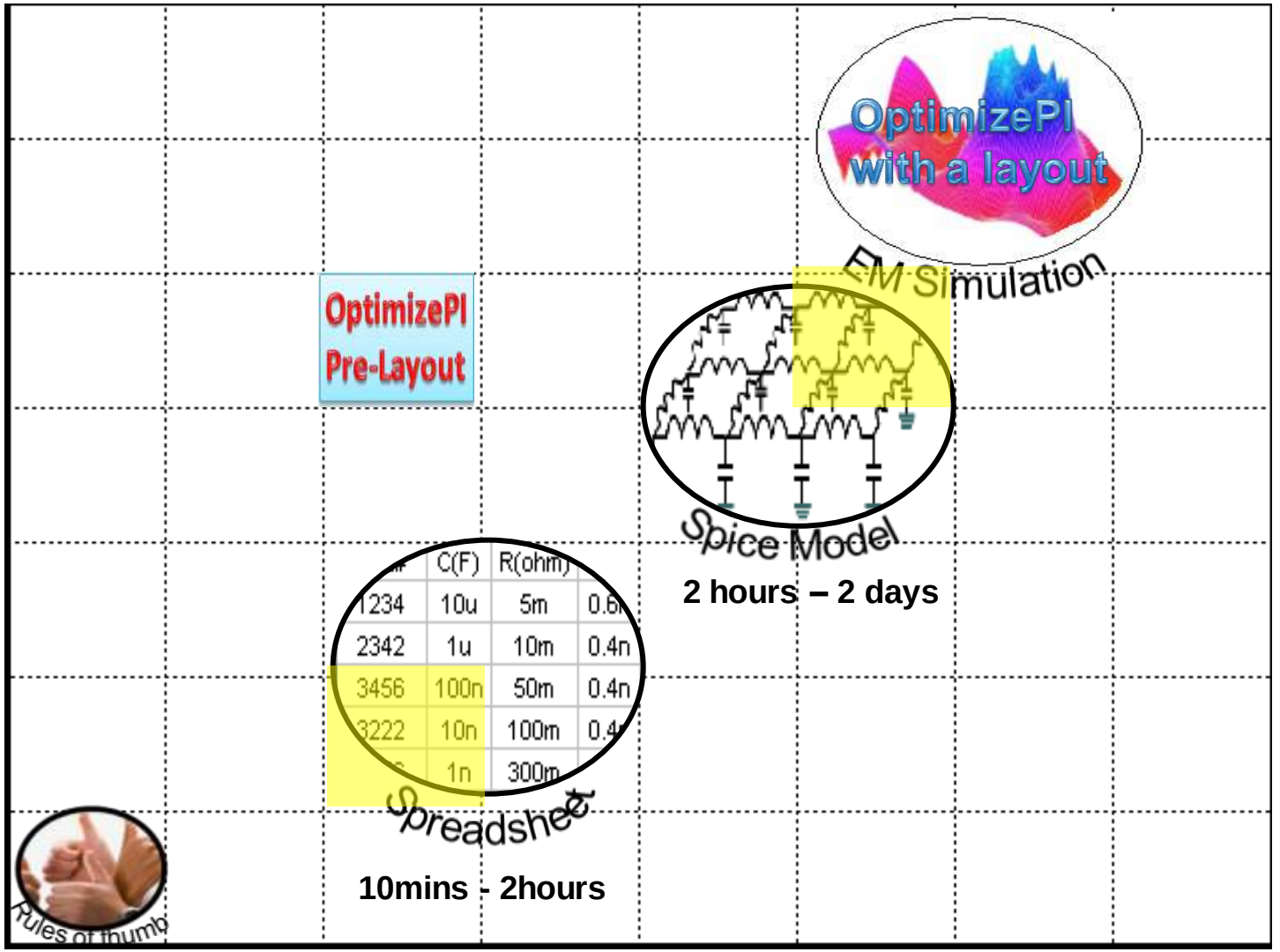
- 优化设计比初始设计节约了**1/3**左右的成本，性能几乎保持不变！

OptimizePI的前仿真

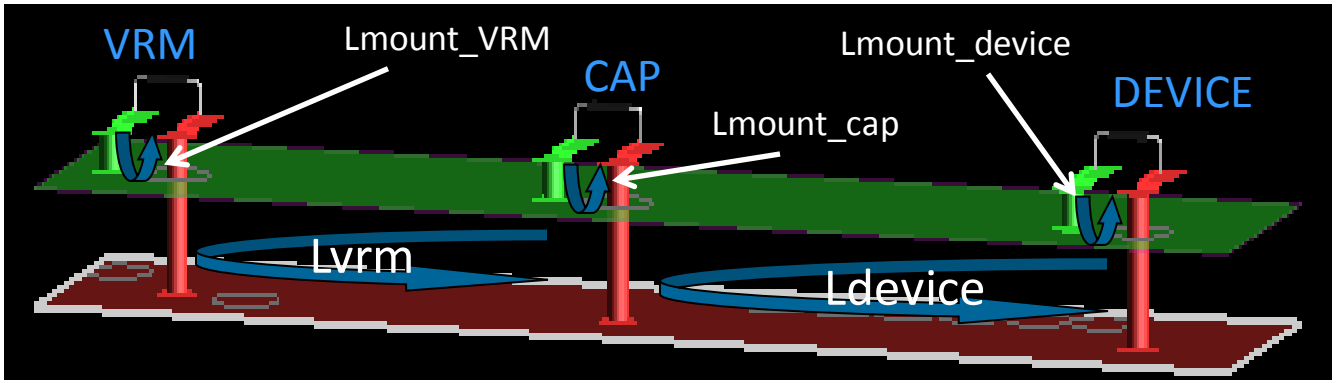
OPI v2.1版本的新功能

- **Pre-layout 前仿真**
  - 设计的早期进行电容优化
  - 无需 Layout文件
  - 设置和分析速度快
  - 用户输入
    - Stackup和平面尺寸
    - 器件和VRM 的位置
    - Decap的区域，固定的VRM 或Device的decap
    - VRM/Device/Decap的mounting结构
    - 目标阻抗
  - 从用户设置中自动提取 R/L/C 模型
  - 高精度
  - Target Impedance是严格的阻抗上限
  - Threshold impedance是非严格的阻抗下限

Pre-Layout分析



为何Pre-layout分析设置快，精度高？

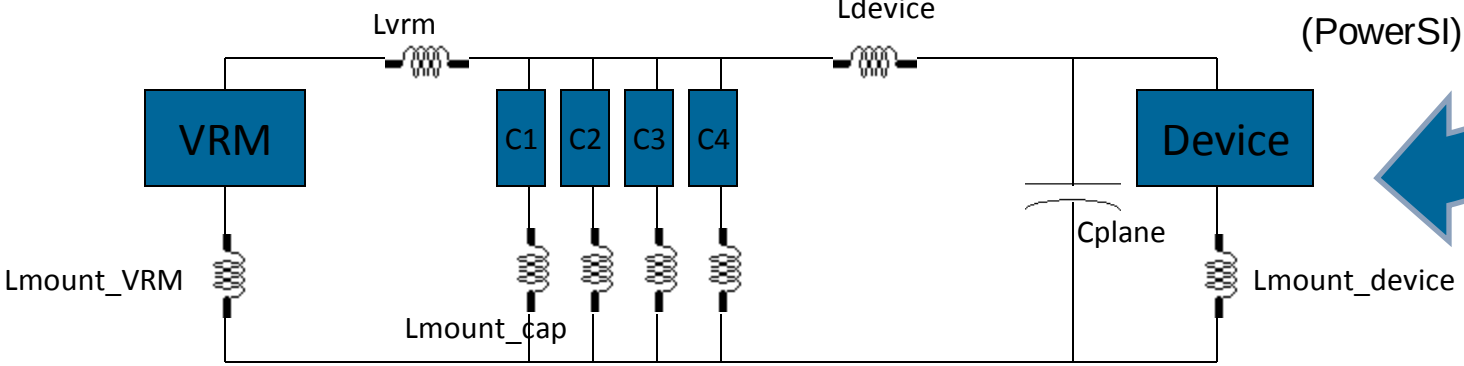


Fast Setup

•Every structure is auto created by the tool from user given input.

High Accuracy

•Every structure is modeled and extracted by EM simulation tool (PowerSI).

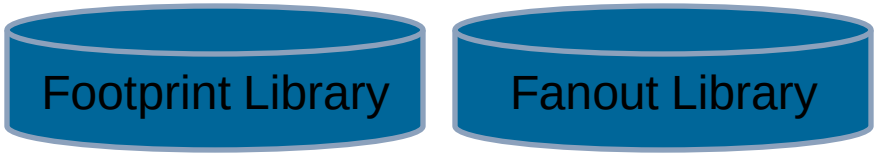


Note:

•Resistance is always in series with Inductance but it is not shown in the picture to simplify the diagram

•VRM, Device,decaps may have more than one power and ground pin.

Pre-Layout分析的总体流程



Generate mounting

Decap Mounting
VRM Mounting
Device Mounting

1. VRM/Device Location
2. Stackup
3. Target Impedance
4. Decap Regions
5. Min/Max # of decaps

1. Structure Generation
2. Resistance, Inductance, Capacitance extraction
3. Circuit Simulation
4. Decap Optimization

Pre-Layout分析的具体Workflow

Specify Stackup parameters

Load Project Decap Library. All decap models in the library will be used as candidates in optimization.

Create VRM and Device

Identify which circuit is VRM

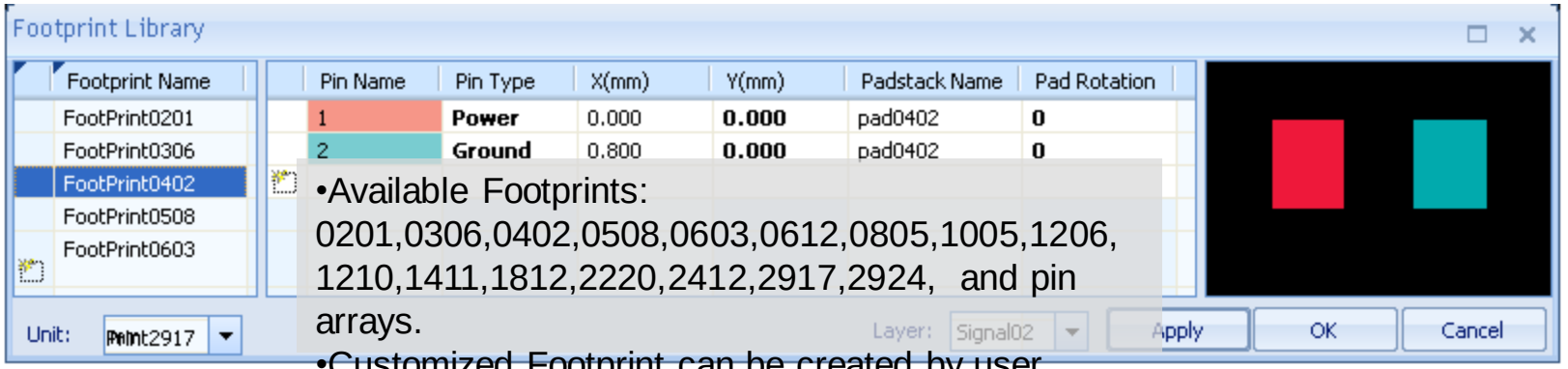
Identify which circuit is Device,
Specify Component Clearance
Specify Target Impedance

Specify Footprint and Fanout for each decap and Specify Bulk decaps if any

Specify Frequency

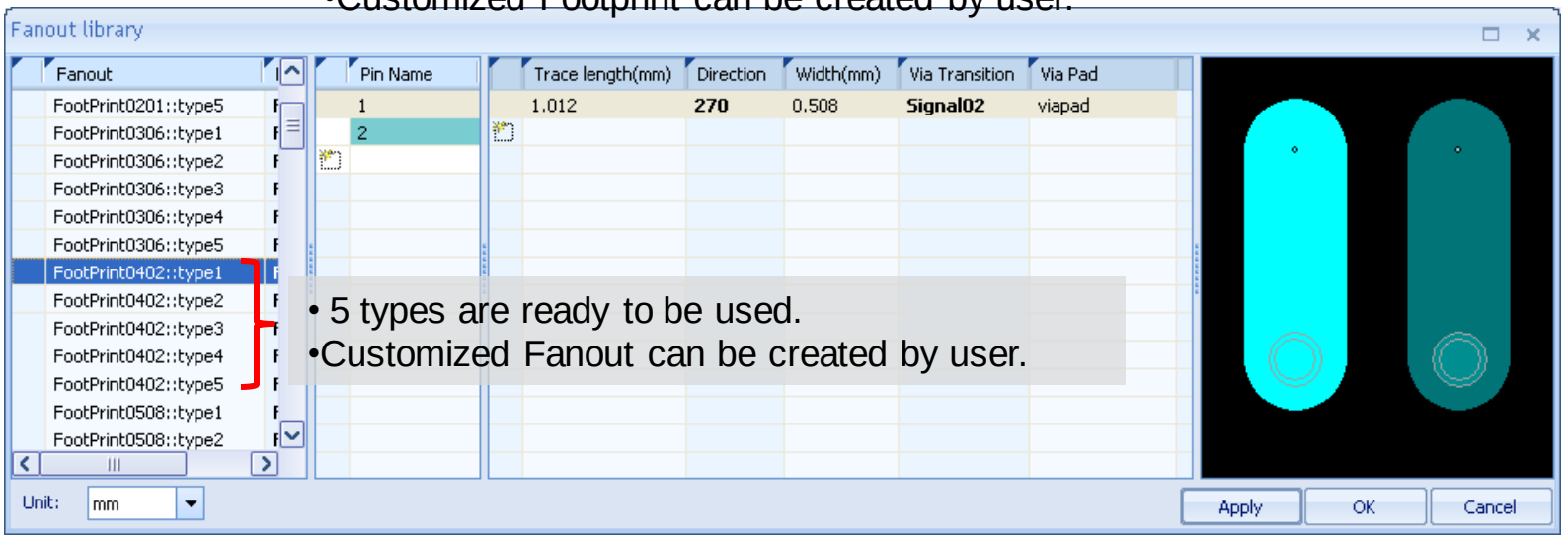
Select Decap Obtimization Objective
Specify Fixed decaps if any
Specify area constraint and max # of decaps for each decap type
Specify Min and Max # of total decaps
Optimization Frequency Range
Specify Impedance Constraint if any

Footprint 和 Fanout 库



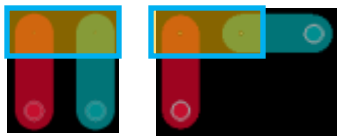
•Available Footprints: 0201,0306,0402,0508,0603,0612,0805,1005,1206, 1210,1411,1812,2220,2412,2917,2924, and pin arrays.

•Customized Footprint can be created by user.



• 5 types are ready to be used.

•Customized Fanout can be created by user.



type1

type2

type3

type4

type5

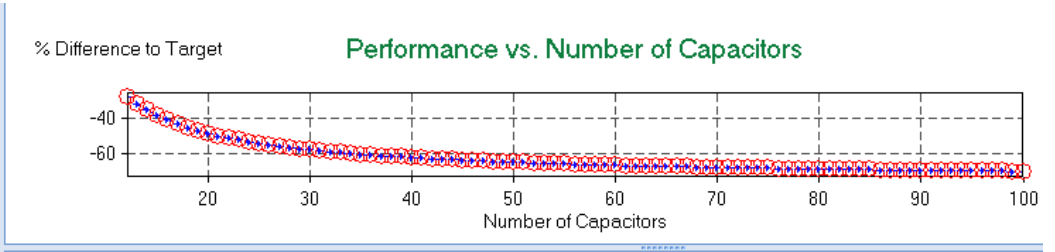
default footprint and fanout for decaps are from industrial standard.

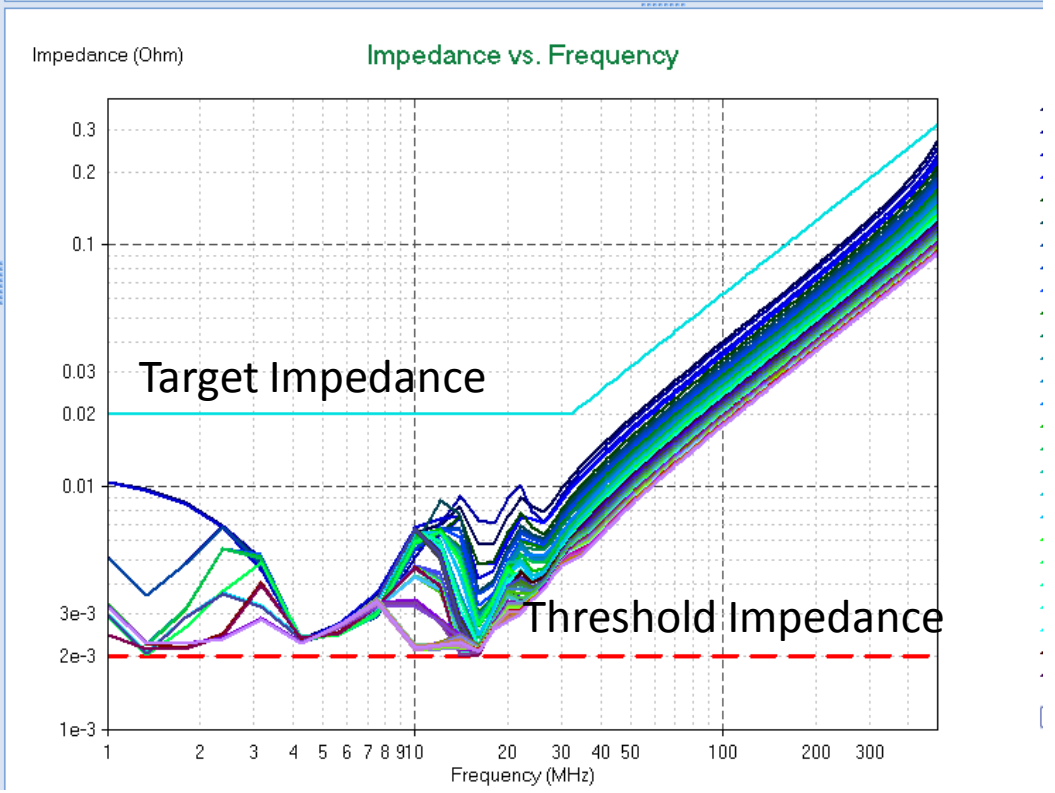
优化结果

Min # of decaps = 12

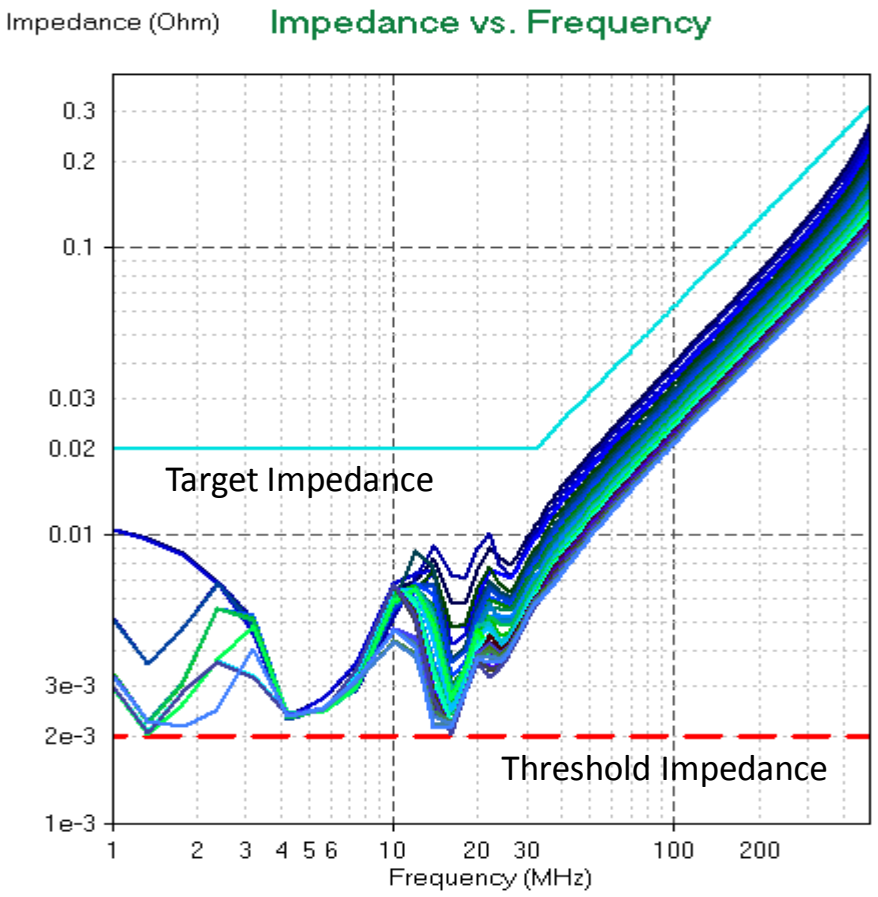
Show No Capacitor

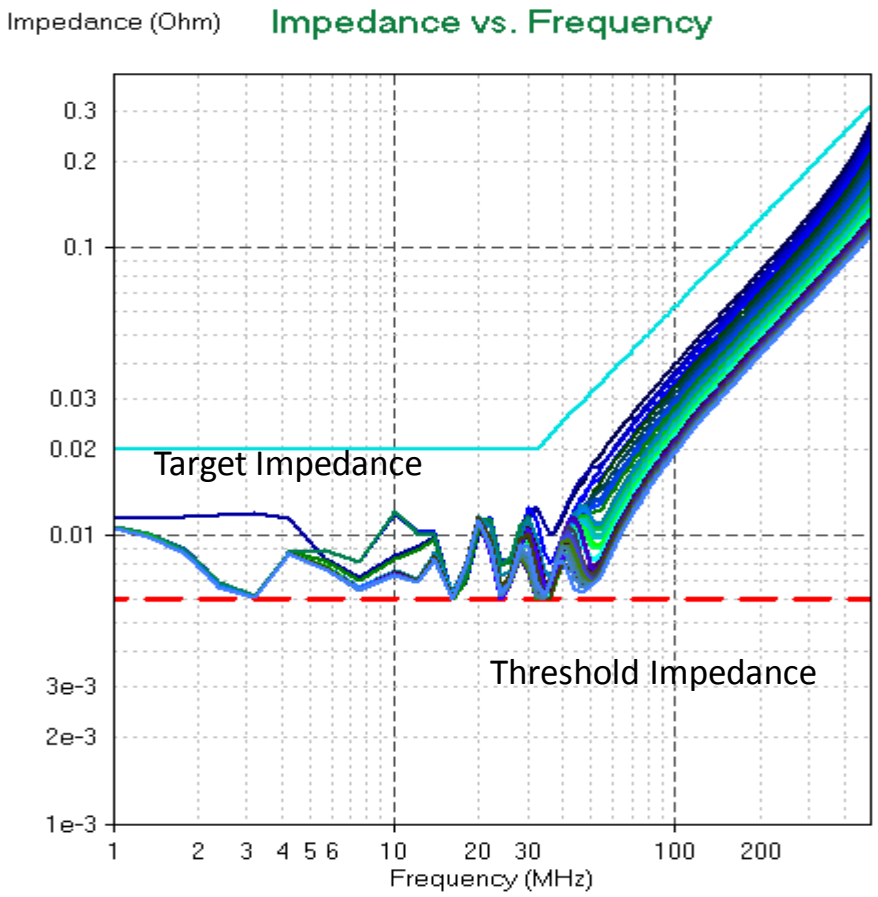
Scheme ID	Cost	Area
Scheme 1	12	9600
Scheme 2	13	13600
Scheme 3	14	11200
Scheme 4	15	15200
Scheme 5	16	16000
Scheme 6	17	16800
Scheme 7	18	17600
Scheme 8	19	21600
Scheme 9	20	22400
Scheme 10	21	23200
Scheme 11	22	24000
Scheme 12	23	24800
Scheme 13	24	25600
Scheme 14	25	26400
Scheme 15	26	27200
Scheme 16	27	28000
Scheme 17	28	29800
Scheme 18	29	31600
Scheme 19	30	32400
Scheme 20	31	32200
Scheme 21	32	33000
Scheme 22	33	34800
Scheme 23	34	35600
Scheme 24	35	36400
Scheme 25	36	37200
Scheme 26	37	38000
Scheme 27	38	38800
Scheme 28	39	39600
Scheme 29	40	40400
Scheme 30	41	41200
Scheme 31	42	42000
Scheme 32	43	42800
Scheme 33	44	41400
Scheme 34	45	42200
Scheme 35	46	43000
Scheme 36	47	43800
Scheme 37	48	44600
Scheme 38	49	45400
Scheme 39	50	46200
Scheme 40	51	47000
Scheme 41	52	47800
Scheme 42	53	48600
Scheme 43	54	49400
Scheme 44	55	50200
Scheme 45	56	51000
Scheme 46	57	51800





Target Impedance和Threshold Impedance





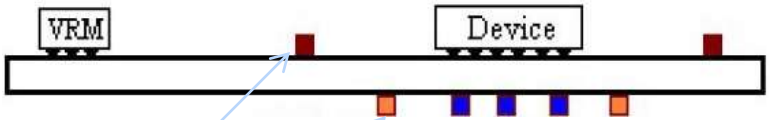
•Target Impedance控制所有方案的阻抗都要低于它；
•Threshold Impedance控制所有的阻抗方案都要高于它，这是个非严格的指标，所以在某些频点上有些阻抗曲线仍然可以低于它。

仿真报告

* Decap Report
* Generated by: OptimizePI2.1.b1.02031
* Enabled Power Nets:
PWR
* Enabled Ground Nets
GND

* Optimized Capacitors Summary

ID	Part No.
3	C100nF0402
5	C220nF0402
6	C2p2uF0402
7	C470nF0402
8	C4p7uF0603
11	C10uF0603
12	C22nF0402
13	C22uF0805
15	C47nF0402
Total	----



* Optimized Capacitors Placement

Refdes		ID	Decap Count	Part No.
CapacitorsOnSameLayer	Top Layer	3	2	C100nF0402
CapacitorsOnSameLayer		13	1	C22uF0805
CapacitorsOnOppositeLayer	Bottom Layer	3	10	C100nF0402
CapacitorsOnOppositeLayer		5	6	C220nF0402
CapacitorsOnOppositeLayer		7	2	C470nF0402
CapacitorsOnOppositeLayer		8	2	C4p7uF0603
CapacitorsOnOppositeLayer		11	2	C10uF0603
CapacitorsOnOppositeLayer		12	8	C22nF0402
CapacitorsOnOppositeLayer		15	31	C47nF0402
CapacitorsUnderneathDevice	Underneath	3	6	C100nF0402
CapacitorsUnderneathDevice		5	3	C220nF0402
CapacitorsUnderneathDevice		6	4	C2p2uF0402
CapacitorsUnderneathDevice		12	1	C22nF0402
CapacitorsUnderneathDevice		15	3	C47nF0402

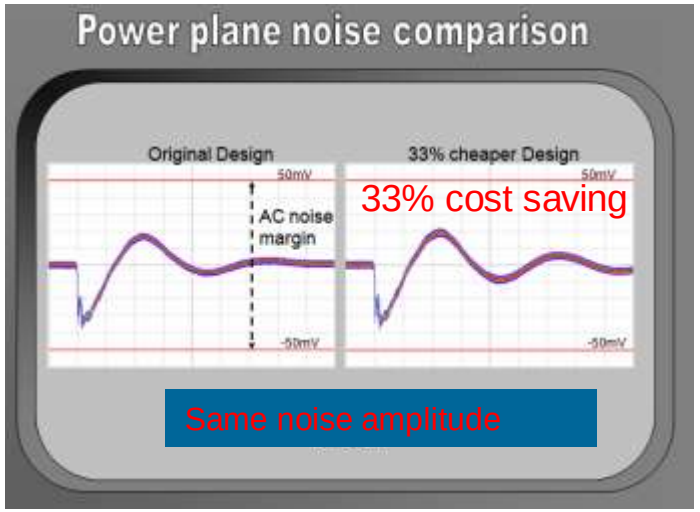
10类典型案例分享

1. Decap Cost Saving *[ASIA,USA, EUROPE]*
2. Determine decaps to meet a target impedance *[USA,ASIA,EUROPE]*
3. Determine decaps for the best power plane impedance in high-end products *[USA,EUROPE]*
4. Optimize Decaps with limited decap candidates for cheaper cost while maintains same or better performance. *[ASIA]*
5. Decap BOM simplification (Reducing decap part numbers) *[ASIA,USA]*
6. Multi-vender decap sensitivity study *[USA,ASIA]*
7. Determine which decaps can be removed and have the least impact to the impedance profile. *[ASIA]*
8. Reducing high frequency anti-resonance *[USA]*
9. Optimize multiple devices on the same plane simultaneously with considering mutual impedance *[USA]*
10. Review Decap Mounting in a flash *[USA,EUROPE, ASIA]*

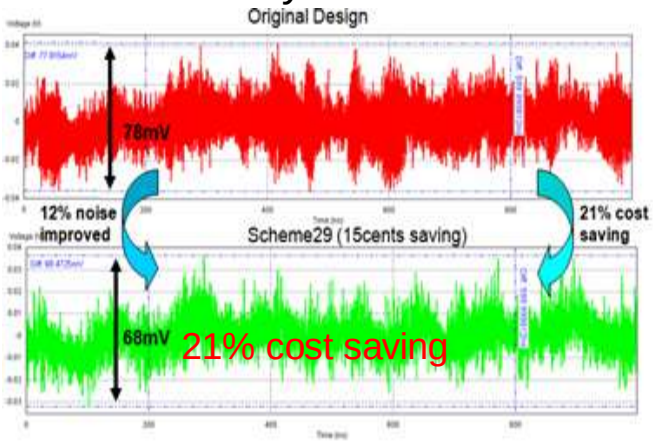
案例1：保证性能并节省成本

CPU core

FPGA VDD

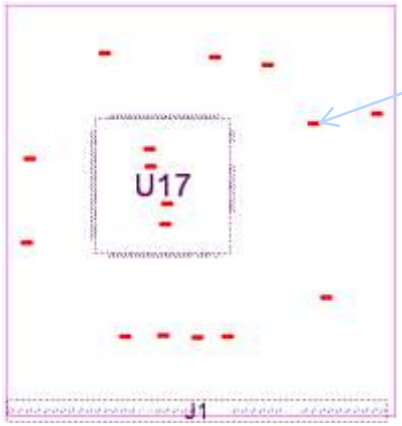


Memory DIMM Module



ASIC devices

案例2：决定去耦电容方案以保证目标阻抗



Decap Location

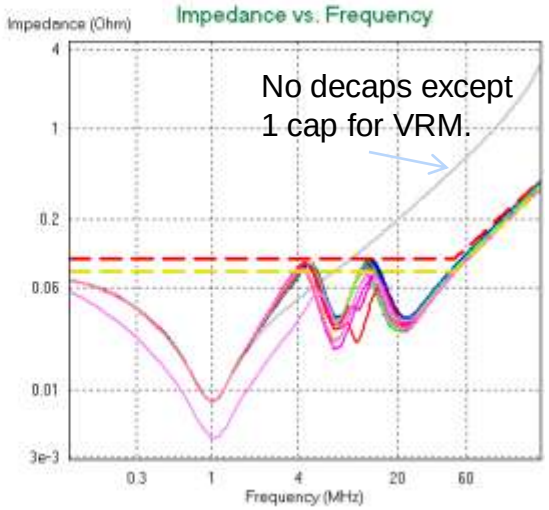
Show No Capacitor

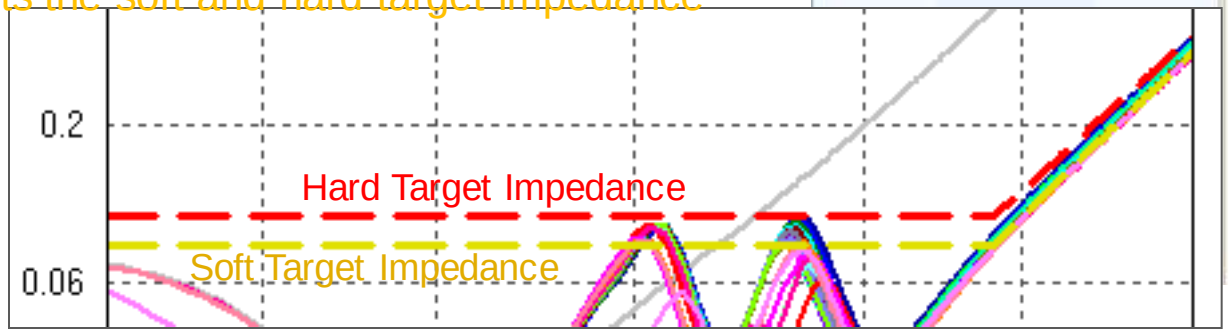
Show Relative Values to Original Scheme

Scheme ID	Cost	Number	Impedance Measure
Original Scheme	0	0	8.25252
Scheme 1	0.06	9	0.488039
Scheme 2	0.061	9	0.391485
Scheme 3	0.062	9	0.305836
Scheme 4	0.063	9	0.282899
Scheme 5	0.064	9	0.269991
Scheme 6	0.065	9	0.2697
Scheme 7	0.066	9	0.257976
Scheme 8	0.067	10	0.196668
Scheme 9	0.068	10	0.131697
Scheme 10	0.069	10	0.10946
Scheme 11	0.07	10	0.103986
Scheme 12	0.072	10	0.0979035
Scheme 13	0.073	11	0.073095
Scheme 14	0.074	11	0.0528772
Scheme 15	0.075	11	0.0450194
Scheme 16	0.076	11	0.0398243
Scheme 17	0.077	11	0.039707
Scheme 18	0.078	11	0.0382537
Scheme 19	0.08	12	0.0379627
Scheme 20	0.081	11	0.0143741
Scheme 21	0.082	11	0.0102942
Scheme 22	0.083	11	0.00739497
Scheme 23	0.084	11	0

Scheme1 ➔Cheapest decap solution that meets the hard target impedance

Scheme23 ➔Cheapest decap solution that meets the soft and hard target impedance



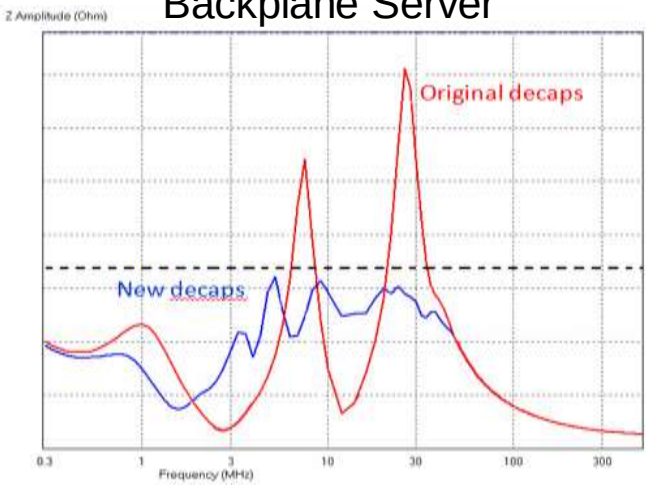


Hard Target Impedance = Target Impedance (OptimizePI)

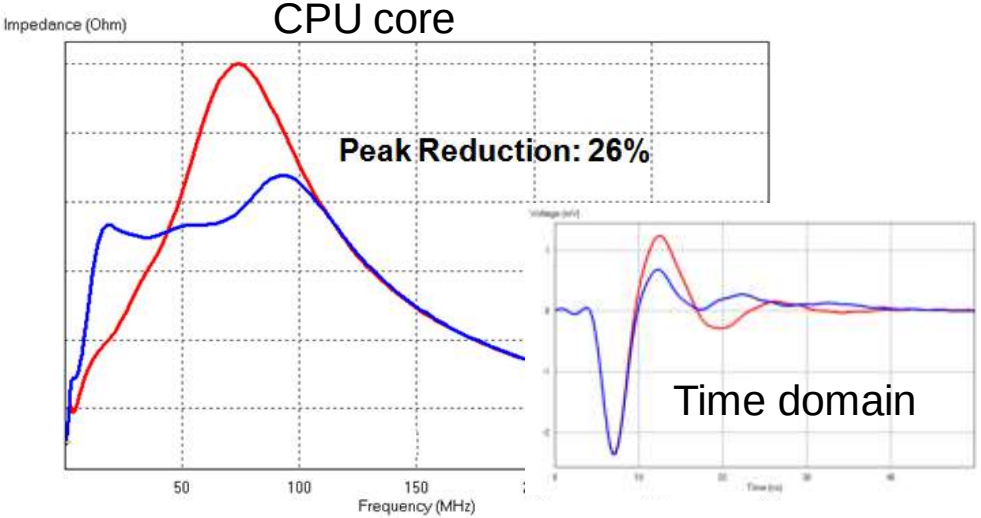
Soft Target Impedance = Threshold Impedance (OptimizePI)

案例3：决定去耦电容方案以获得最优性能

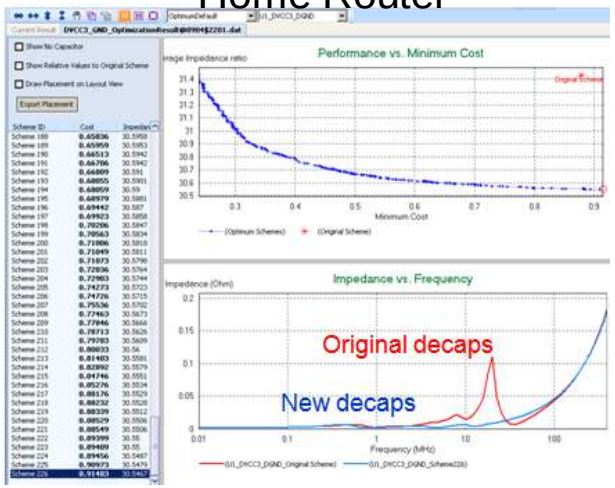
Backplane Server



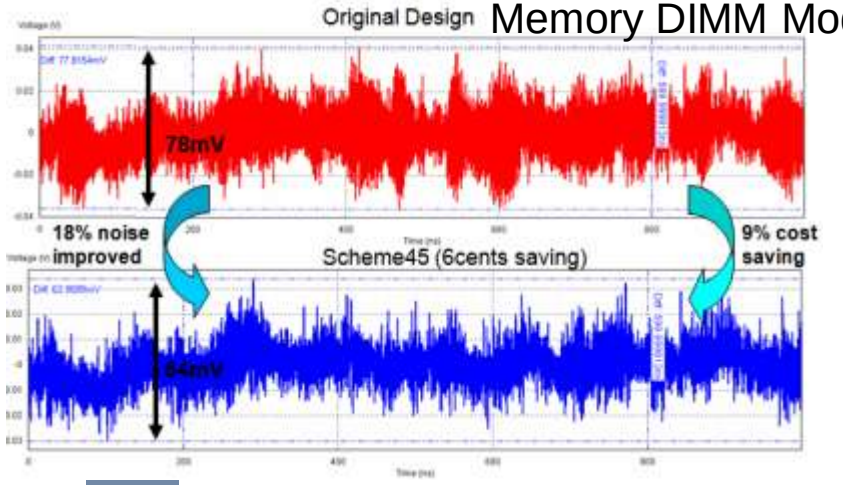
CPU core



Home Router



Memory DIMM Module

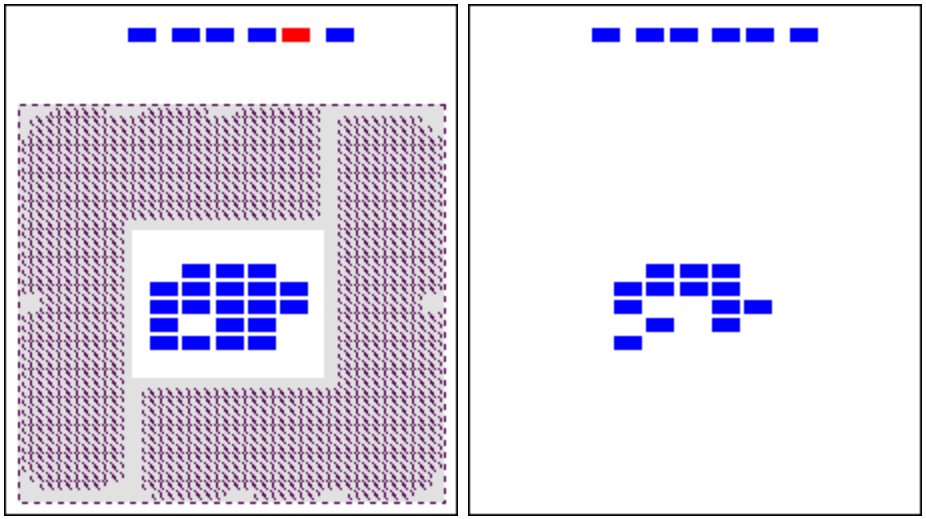


案例4： 优化电容数目并保证性能

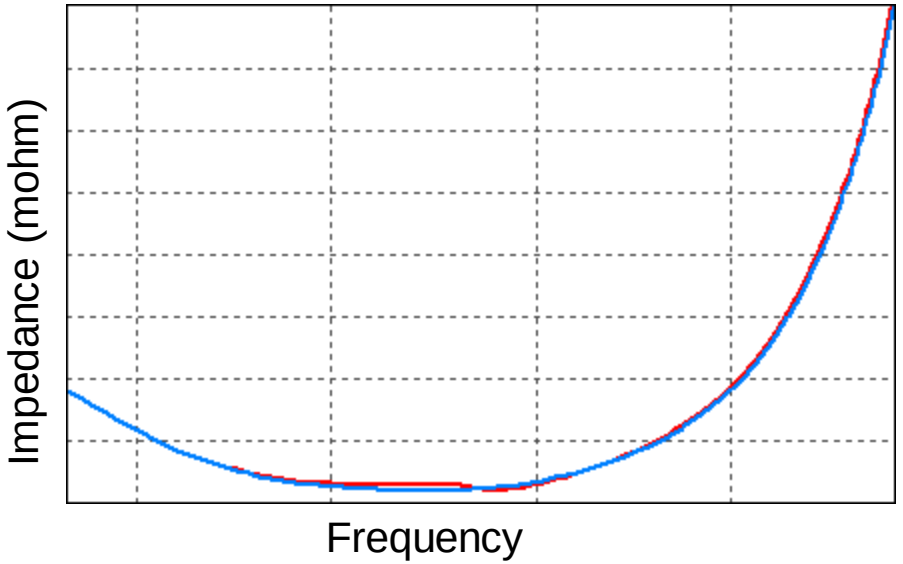
Project Library

ID	Part No.	Unit of Size	Size	Model Type	Cnom...	Cact ...	L (nH)	R (m...	Component Cost
1	C_10uF_0805	English	0805	SPICE Model	10000				0.010
2	C_22uF_0805	English	0805	SPICE Model	22000				0.016

ORIGINAL DESIGN NEW DESIGN



TOP BOTTOM



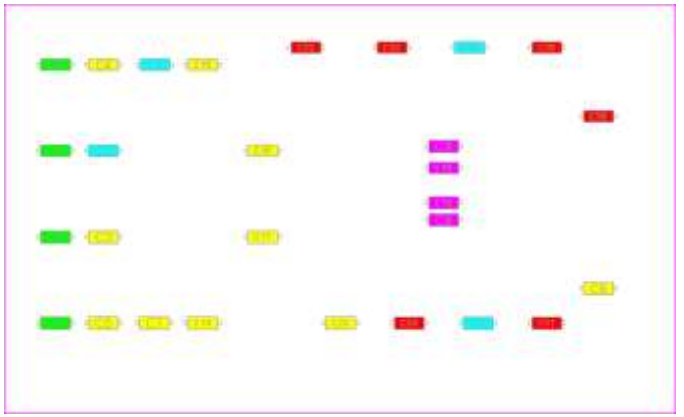
10uF

22uF

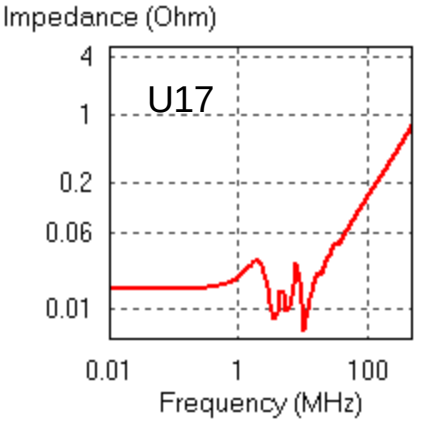
案例5：减少电容种类

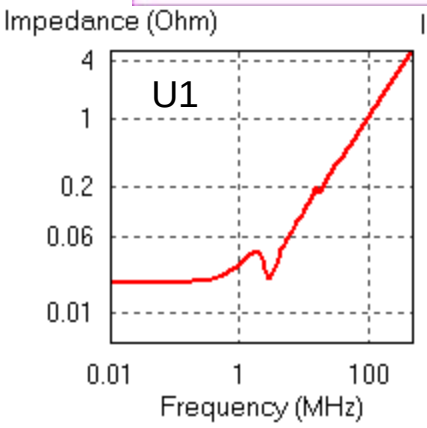
Project Library

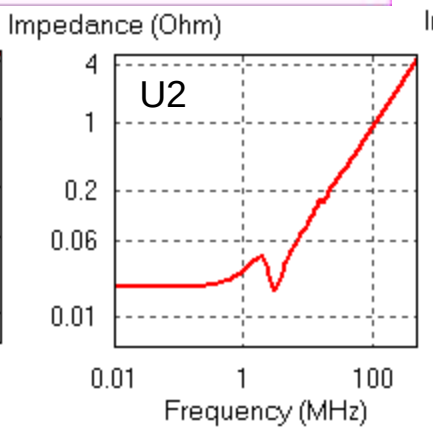
I.	Part No.	Unit of Size	Size	Model Type	Cnom (nF)	Component Cost	Additional Mounting Cost
1	10nF	English	0402	SPICE Model	10	1e-6	1
2	47nF	English	0402	SPICE Model	47	1e-6	1
3	100nF	English	0402	SPICE Model	100	1e-6	1
4	220nF	English	0402	SPICE Model	220	1e-6	1
5	470nF	English	0402	SPICE Model	470	1e-6	1

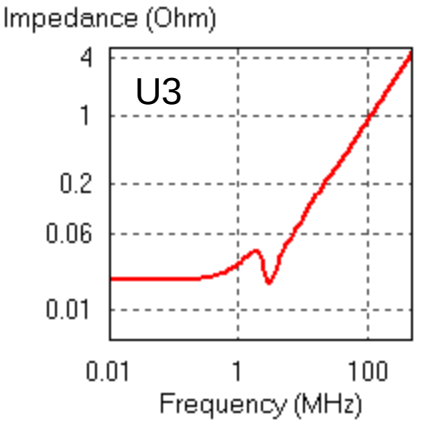


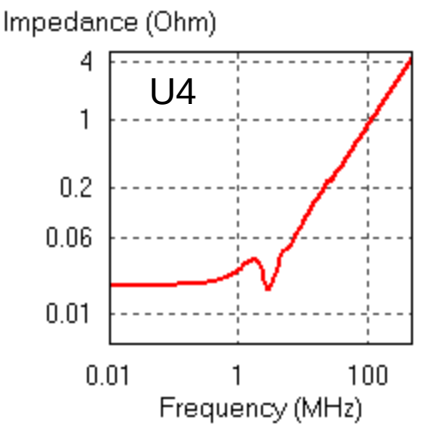
10 nF
47 nF
100 nF
220 nF
470 nF









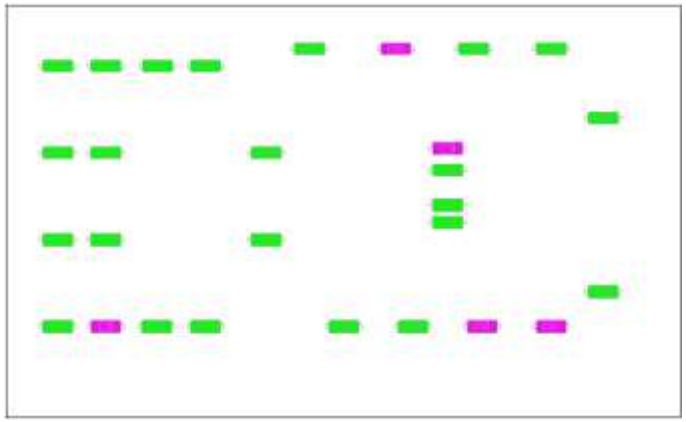


OptimizePI 优化结果

☐ Show No Capacitor

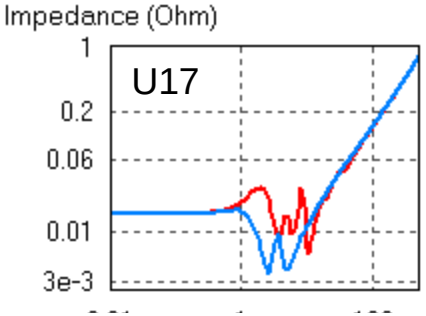
☐ Show Relative Values to Original Scheme

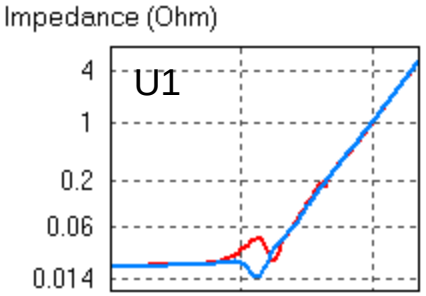
Scheme ID	Cost	Area	Number
Original Scheme	**5.00003**	22400	**28**
Scheme 1	**1**	800	**1**
Scheme 2	**1**	1600	**2**
Scheme 3	**1**	2400	**3**
Scheme 4	**1**	3200	**4**
Scheme 5	**1.00001**	4000	**5**
Scheme 6	**1.00001**	4800	**6**
Scheme 7	**1.00001**	5600	**7**
Scheme 8	**1.00001**	6400	**8**
Scheme 9	**1.00001**	7200	**9**
Scheme 10	**1.00001**	8000	**10**
Scheme 11	**1.00001**	8800	**11**
Scheme 12	**1.00001**	9600	**12**
Scheme 13	**1.00001**	10400	**13**
Scheme 14	**1.00001**	11200	**14**
Scheme 15	**1.00002**	12000	**15**
Scheme 16	**1.00002**	12800	**16**
Scheme 17	**1.00002**	13600	**17**
Scheme 18	**1.00002**	14400	**18**
Scheme 19	**1.00002**	15200	**19**
Scheme 20	**1.00002**	16000	**20**
Scheme 21	**1.00002**	16800	**21**
Scheme 22	**2.00002**	17600	**22**
Scheme 23	**2.00002**	18400	**23**
Scheme 24	**2.00002**	19200	**24**
Scheme 25	**2.00002**	20000	**25**
Scheme 26	**2.00003**	20800	**26**
Scheme 27	**2.00003**	21600	**27**
Scheme 28	**2.00003**	22400	**28**

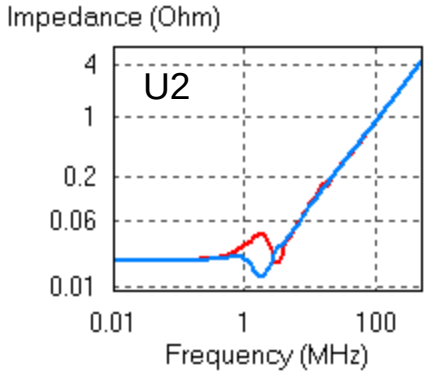


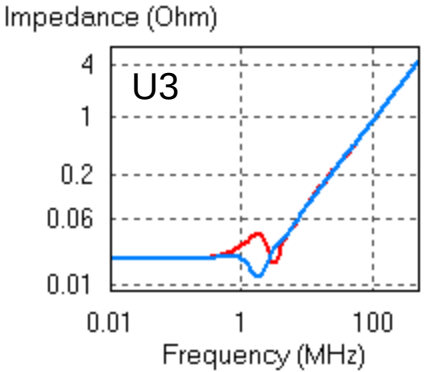
10 nF
47 nF
100 nF
220 nF
470 nF

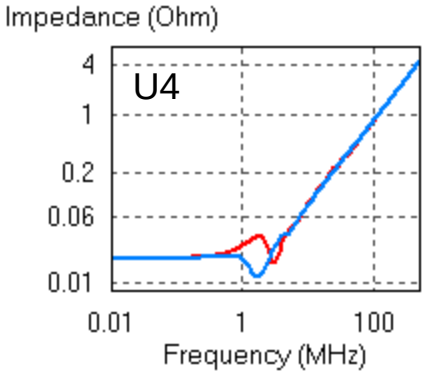
Original Design











Original Decaps

Optimized Decaps

案例6： 电容厂家变化情况分析

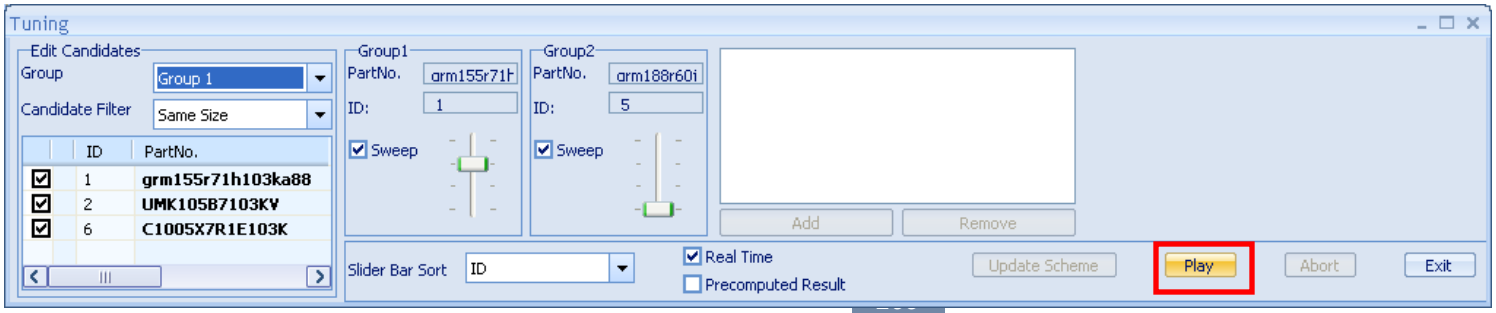
ID	Part No.	Unit of Size	Size	Model T...	Cn...	Uppe...	Lowe...	Self-Re...	TCC	Manufacturer	Mfg. Part No.
1	grm155r71h103ka88	English	0402	SPIC...	10	10	-10	79.43M	X7R	Murata	grm155r71h103ka88
2	UMK105B7103KV	English	0402	SPIC...	10	10	-10	79.43M	X7R	TaiYuYoDen	UMK105B7103KV
6	C1005X7R1E103K	English	0402	SPIC...	10	10	-10	79.43M	X7R	TDK	C1005X7R1E103K
5	grm188r60j106me47	English	0603	SPIC...	10000	20	-20	3.16M	X5R	Murata	grm188r60j106me47
4	C1608X5R0J106M	English	0603	SPIC...	10000	20	-20	2.51M	X5R	TDK	C1608X5R0J106M
3	JMK107BJ106MA	English	0603	SPIC...	10000	20	-20	2.51M	X5R	TaiYuYoDen	JMK107BJ106MA

Select Simulation Type -> What-if Analysis Parameters -> Decoupling Capacitors

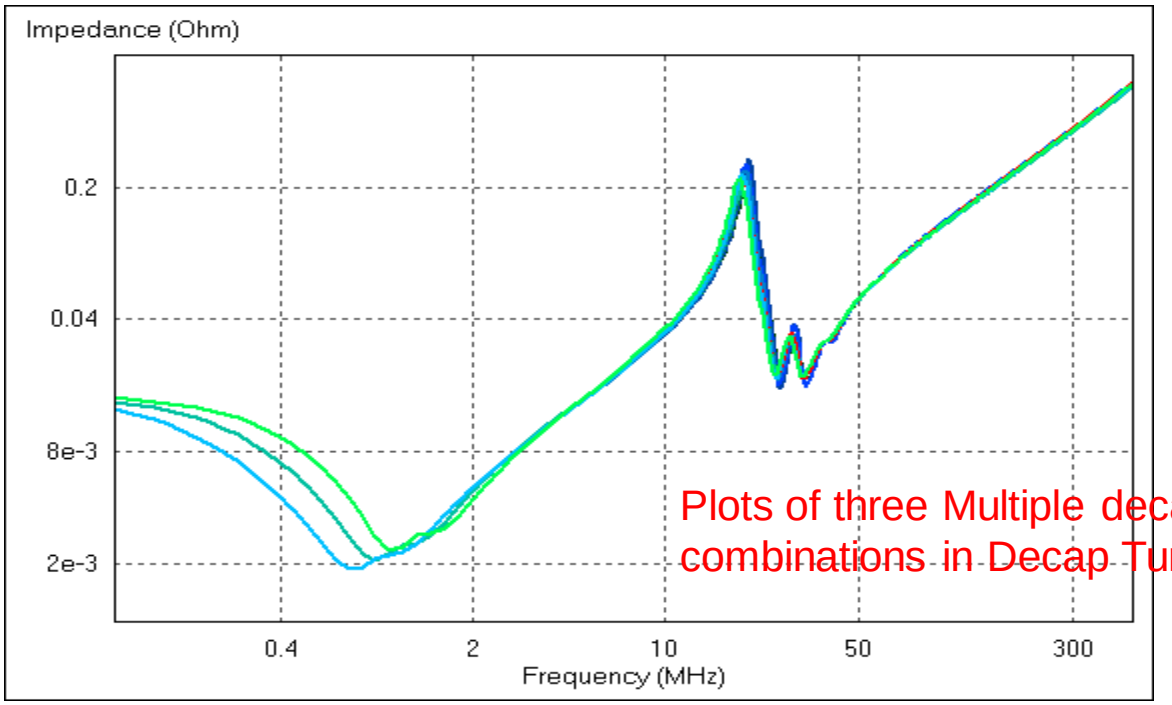
Select Scheme | VRM | **Decoupling Capacitors** | Impedance Observations

Circuit Name	Circuit Model	Original Design	Modified Scheme	Group ID
C26	CAP_10UF_0603	5	5	2
C27	CAP_10UF_0603	5	5	2
C28	CAP_10UF_0603	5	5	2
C29	CAP_10UF_0603	5	5	2
C30	CAP_10UF_0603	5	5	2
C31	CAP_10nF_0402	1	1	1
C32	CAP_10nF_0402	1	1	1

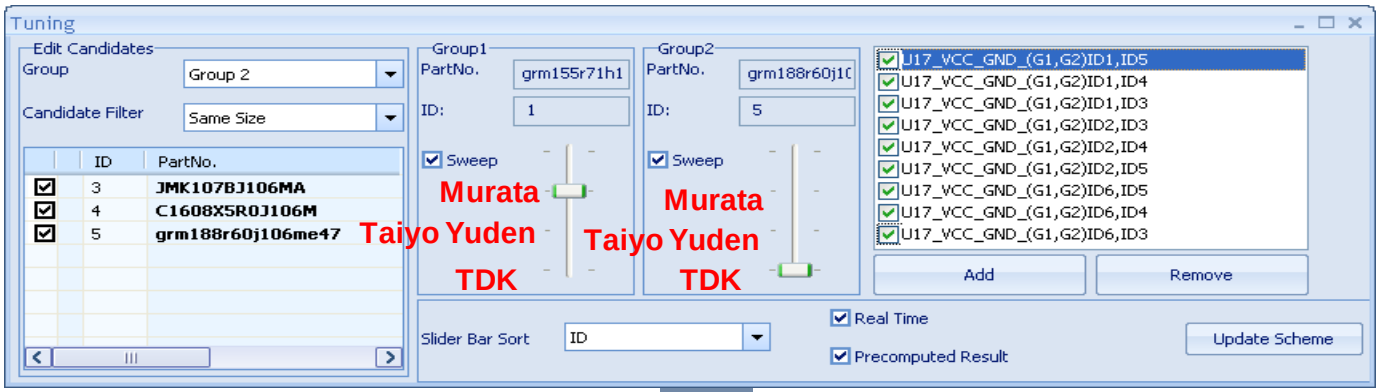
Tune | Group By: ID



What-if模式分析结果



Plots of three Multiple decap venders combinations in Decap Tuning



案例7：分析哪些去耦电容去除后的影响最小

Setup for Simulation -> Impedance Observations -> Target Impedance

Impedance Observations | **Target Impedance** | Current Excitation

Circuit Name	Circuit Model	Link to Original	Target Impedance
U17_VCC_GND	I803865-1_	☑	

Target Impedance = Original Impedance

Optimization Manager | Decoupling Capacitors | Optimization Range | Optimization Frequency | Impedance Observations | Impedance Constraints

	Group Name	Optimization Objective	Impedance Measure
☑	OptimumDefault	Best Performance vs. Number of Capacitors	Average Impedance Percentage Difference to Target

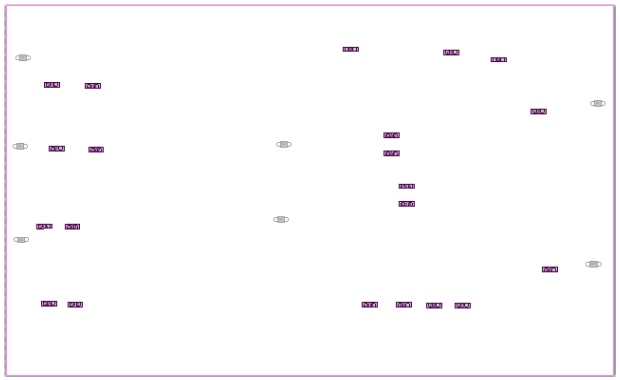
Optimization Objective options:
- Best Performance vs. Cost
- Best Performance vs. Area
- Best Performance vs. Number of Capacitors
- Best Performance Schemes Overall

Impedance Measure options:
- Average Impedance Ratio to Threshold-log
- Average Impedance Ratio to Threshold-linear
- Average Impedance Percentage Difference to Target

Optimize decaps based on Target Impedance.

Decoupling Capacitors | Optimization Range | Optimization Fr

Circuit Name	Original Model	Candidate Filter
C2	5	Same Component
C3	5	Same Component
C4	5	Same Component
C5	5	Same Component
C6	5	Same Component
C7	5	Same Component
C8	5	Same Component
C9	5	Same Component
C10	5	Same Component
C13	5	Same Component
C18	5	Same Component
C24	11	Same Component
C25	11	Same Component
C29	11	Same Component
C30	11	Same Component
C31	5	Same Component
C32	5	Same Component



Decap locations

Decap on Top layer

Decap on Bottom layer

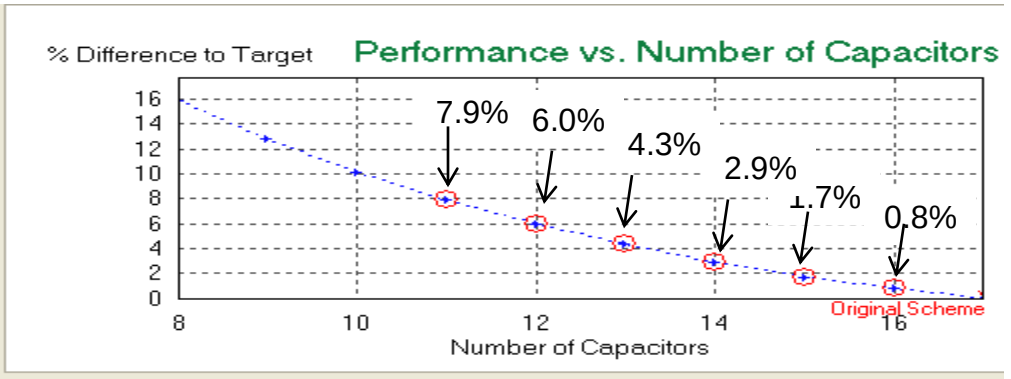
During optimization, all decaps will be either stayed or removed, no changing decap ID.

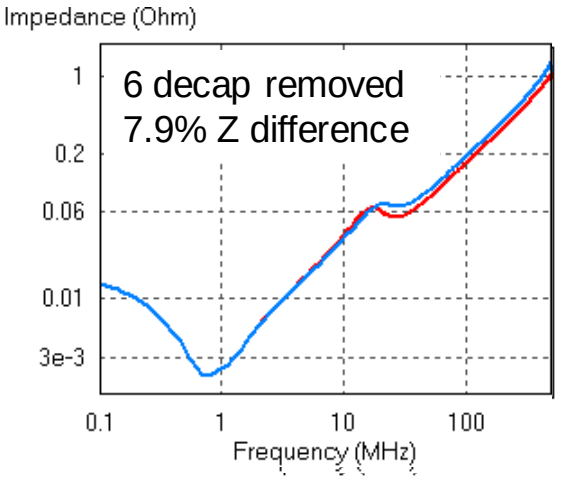
OptimizePI 优化结果

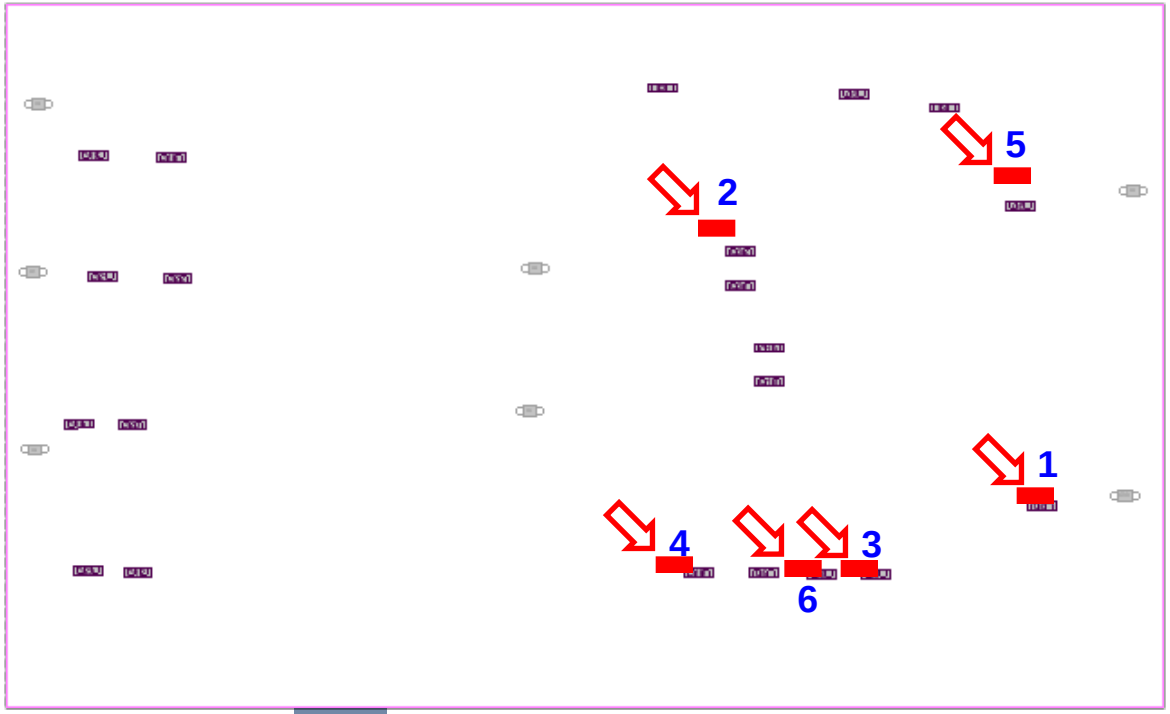
Show No Capacitor

Show Relative Values to Original Scheme

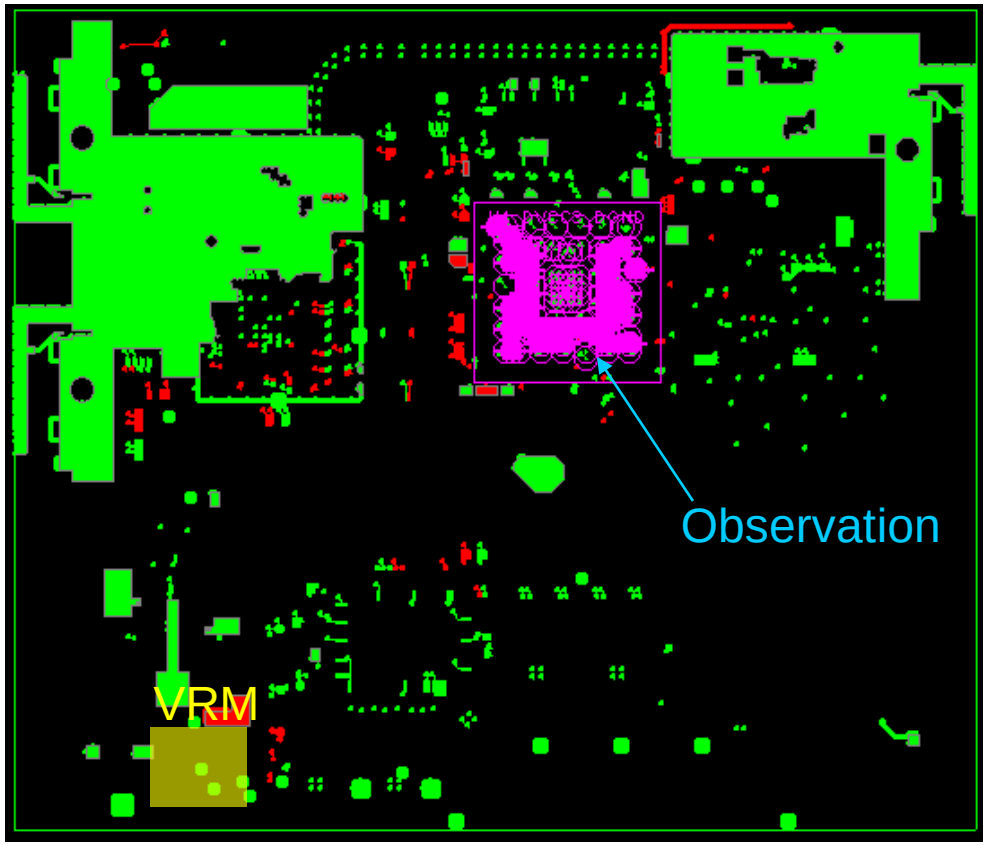
Scheme ID	Cost	Number	Impedance Measu
Original Scheme	**0.129**	**17**	0
Scheme 1	**0.084**	**8**	15.9081
Scheme 2	**0.089**	**9**	12.8032
Scheme 3	**0.094**	**10**	10.1147
Scheme 4	**0.099**	**11**	7.87291
Scheme 5	**0.104**	**12**	5.9916
Scheme 6	**0.109**	**13**	4.30578
Scheme 7	**0.114**	**14**	2.87706
Scheme 8	**0.119**	**15**	1.70722
Scheme 9	**0.124**	**16**	0.783124
Scheme 10	**0.129**	**17**	0

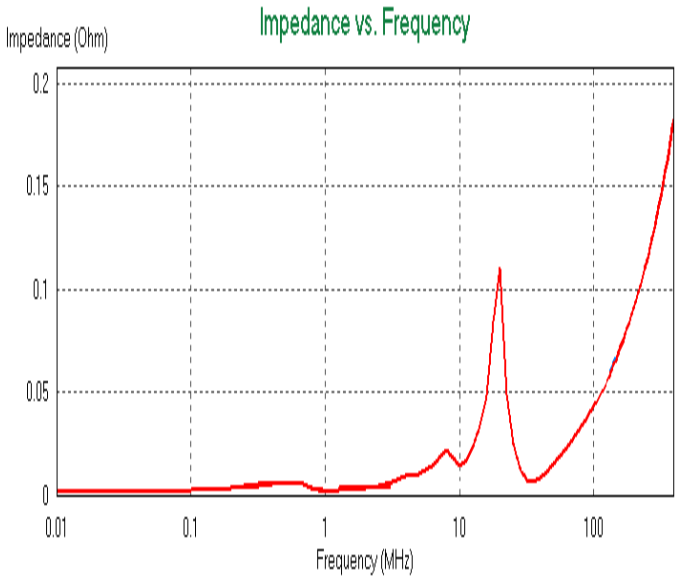






案例8： 消除阻抗谐振点
（得到性能最优情况下的去耦电容方案）





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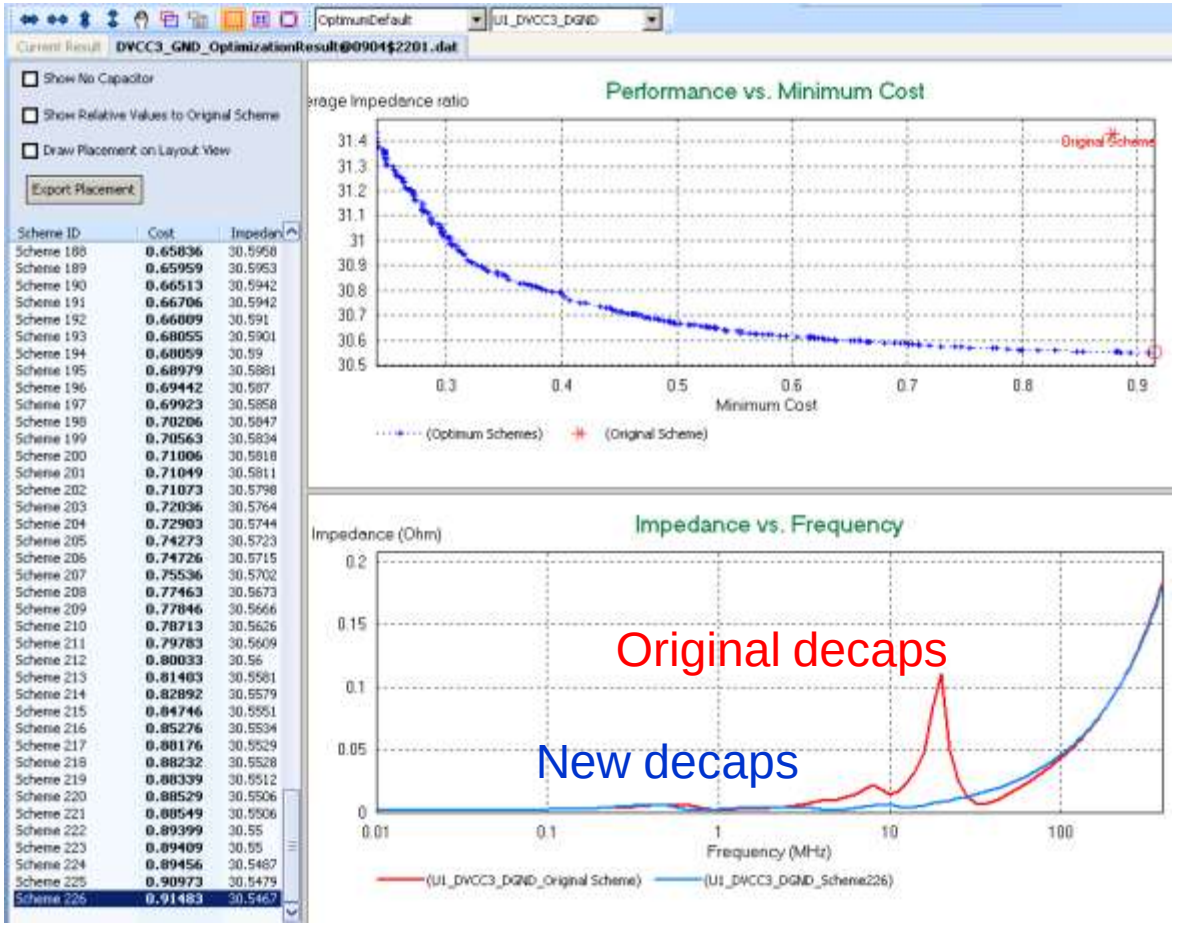
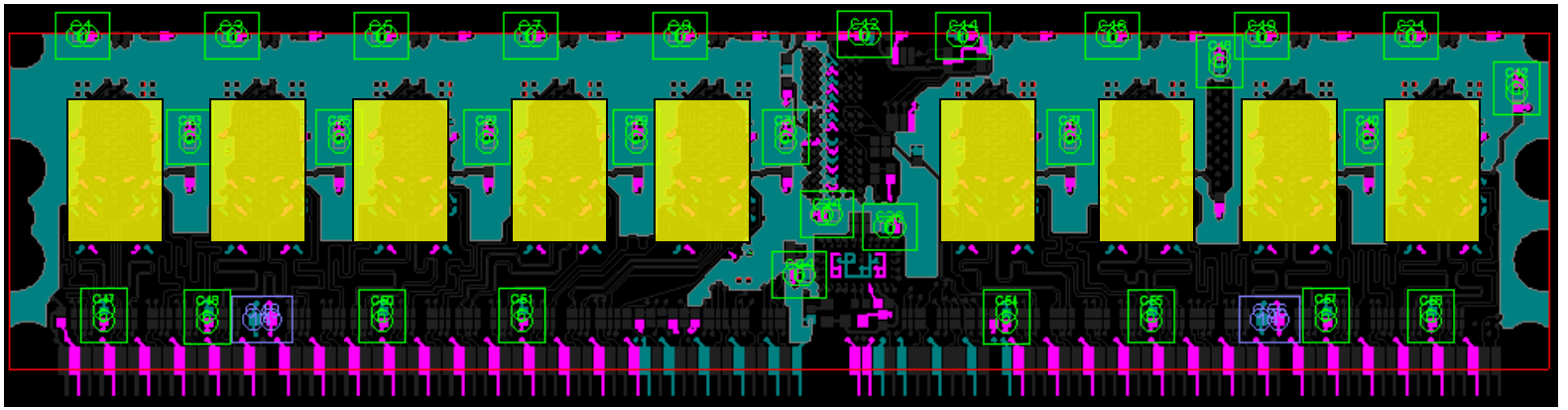
OptimizePI 优化结果



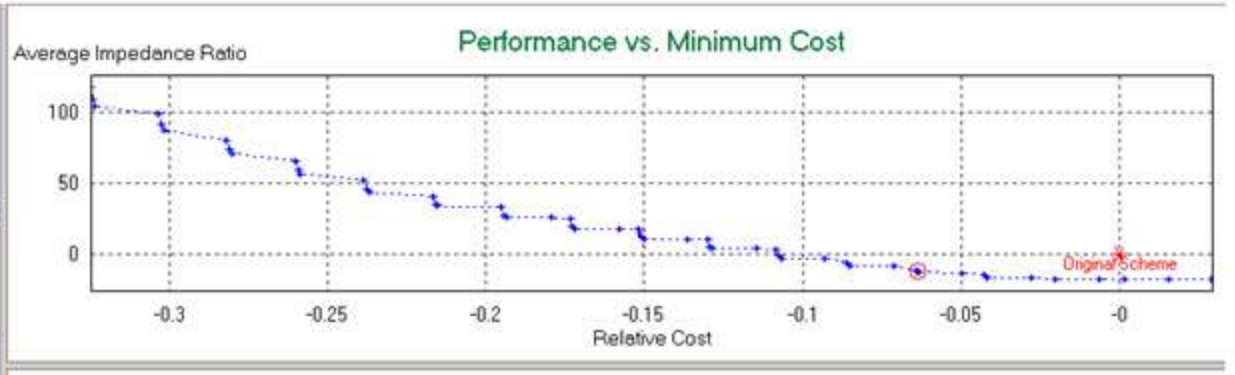
114

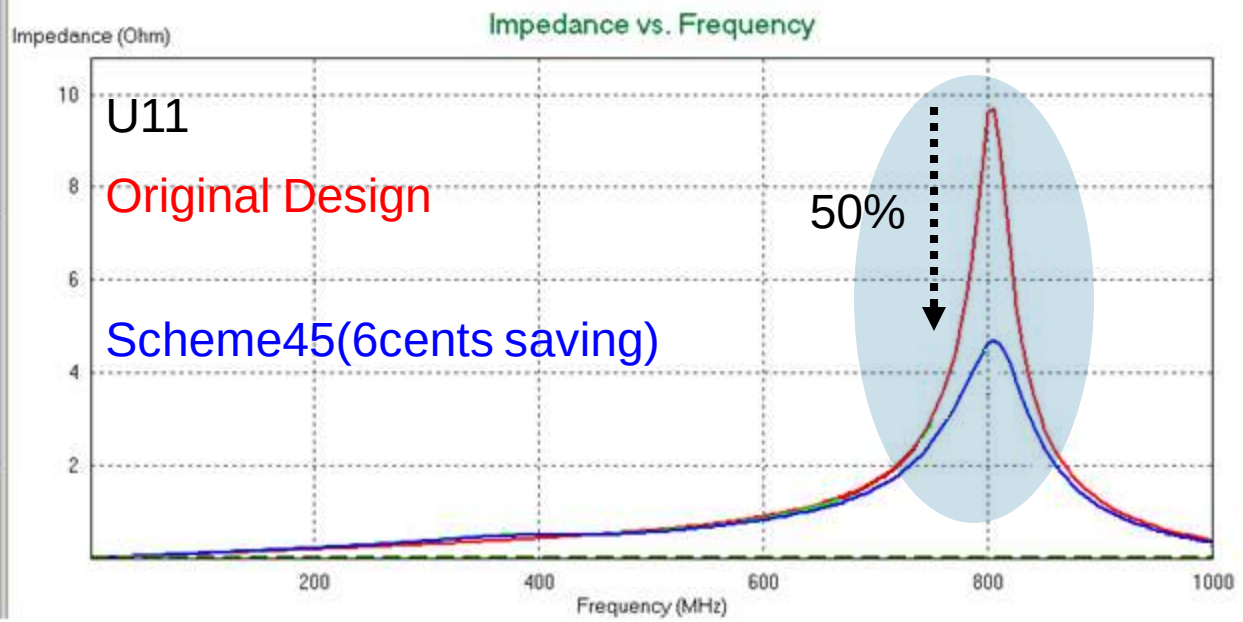
案例9：减小电源噪声



OptimizePI 优化结果

阻抗谐振点峰值降低50%，每块板成本节省 6美分





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去耦电容设置方案

C3	DecapLib_6
C40	DecapLib_6
C49	DecapLib_14
C56	DecapLib_14
C1	DecapLib_6
C16	DecapLib_6
C18	DecapLib_6
C19	DecapLib_6
C21	DecapLib_6
C23	DecapLib_6
C25	DecapLib_6
C27	DecapLib_6
C29	DecapLib_6
C31	DecapLib_6
C34	DecapLib_6
C36	DecapLib_6
C37	DecapLib_6
C42	DecapLib_6
C47	DecapLib_6
C48	DecapLib_6
C5	DecapLib_6
C57	DecapLib_6
C58	DecapLib_6
C7	DecapLib_6
C9	DecapLib_6
C12	DecapLib_6
C14	DecapLib_6
C44	DecapLib_6
C50	DecapLib_6
C51	DecapLib_6
C54	DecapLib_6
C55	DecapLib_6

Original Decaps

DecapLib_13 = 220pF 0402

DecapLib_14 = 2.2uF 0603

DecapLib_6 = 100nF 0402

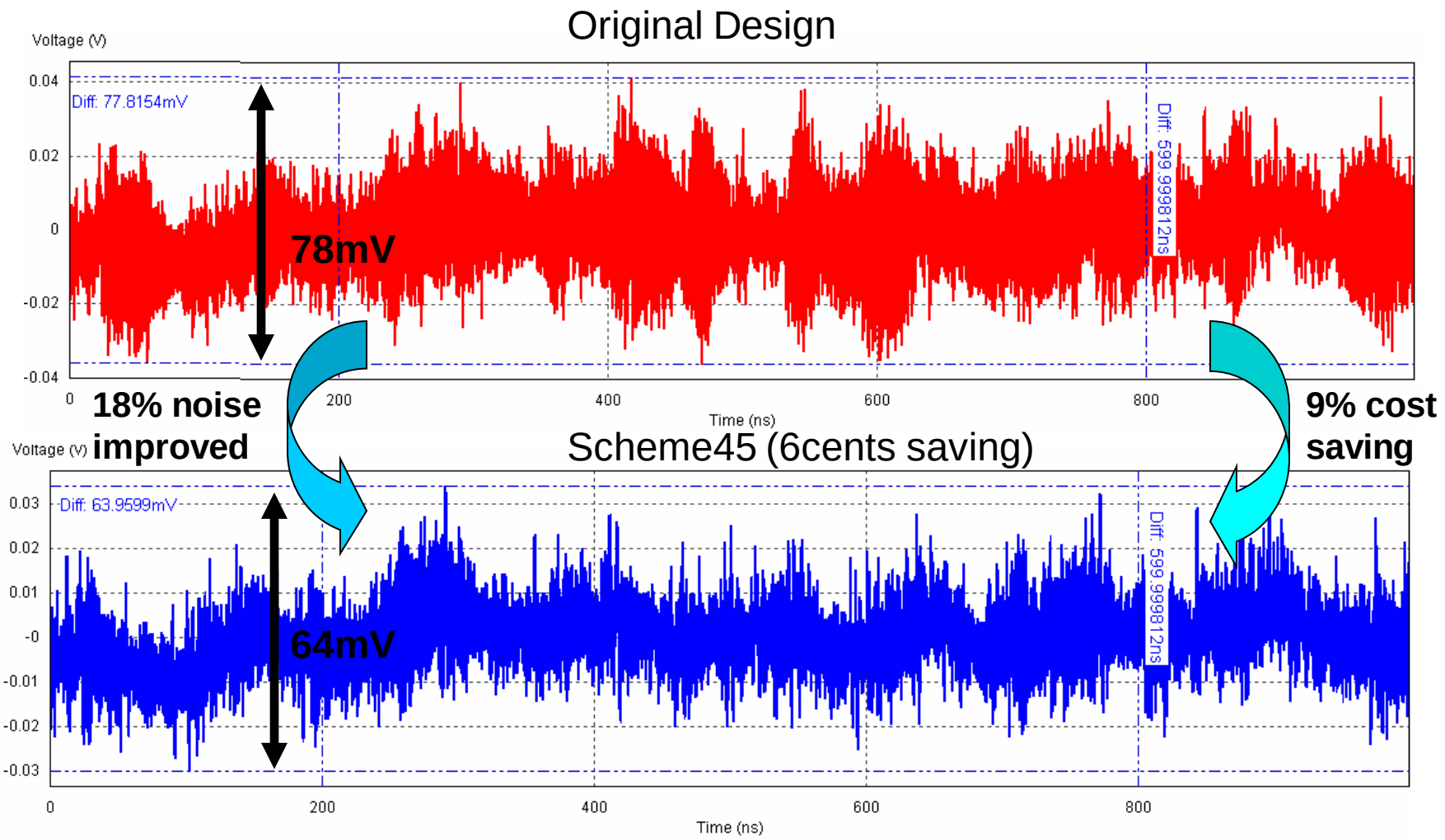
DecapLib_@OPEN@ = no-pop

Scheme45

C3	DecapLib_13
C40	DecapLib_13
C49	DecapLib_14
C56	DecapLib_14
C1	DecapLib_6
C16	DecapLib_6
C18	DecapLib_6
C19	DecapLib_6
C21	DecapLib_6
C23	DecapLib_6
C25	DecapLib_6
C27	DecapLib_6
C29	DecapLib_6
C31	DecapLib_6
C34	DecapLib_6
C36	DecapLib_6
C37	DecapLib_6
C42	DecapLib_6
C44	DecapLib_6
C47	DecapLib_6
C48	DecapLib_6
C5	DecapLib_6
C50	DecapLib_6
C51	DecapLib_6
C55	DecapLib_6
C57	DecapLib_6
C58	DecapLib_6
C7	DecapLib_6
C9	DecapLib_6
C12	DecapLib_@Open@
C14	DecapLib_@Open@
C54	DecapLib_@Open@

remove

时域电源噪声结果



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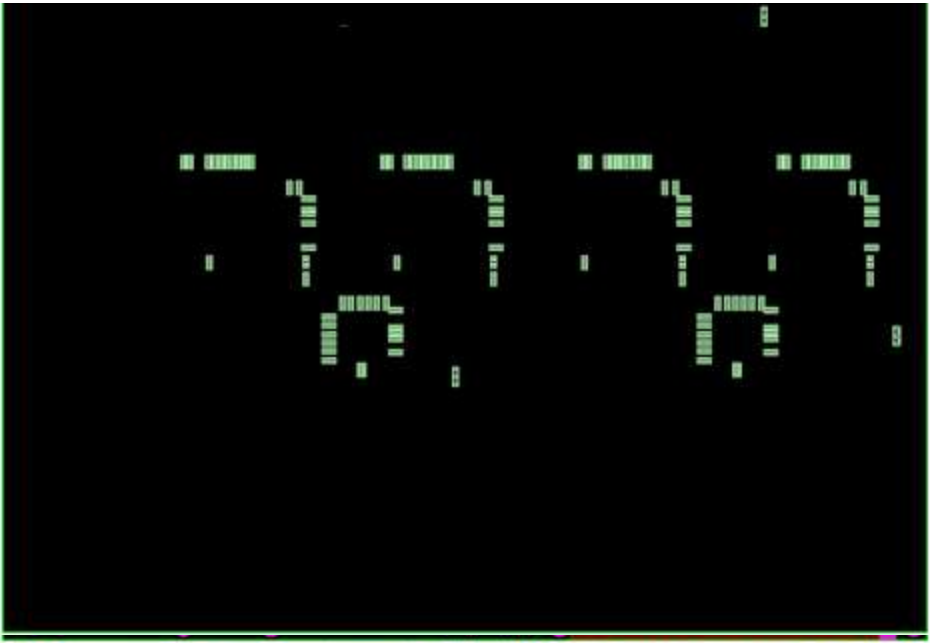
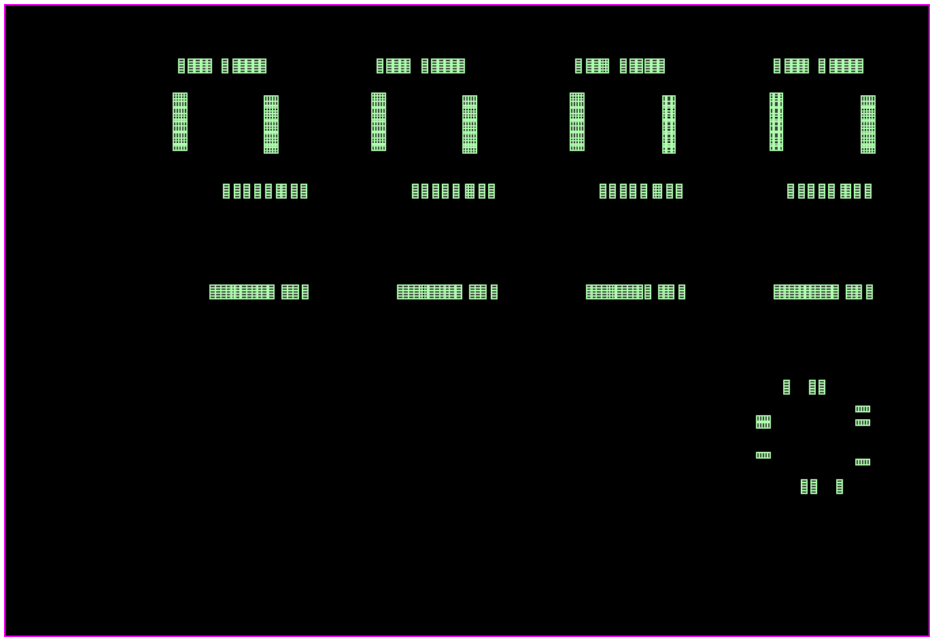
案例10：检查去耦电容安装的环路电感



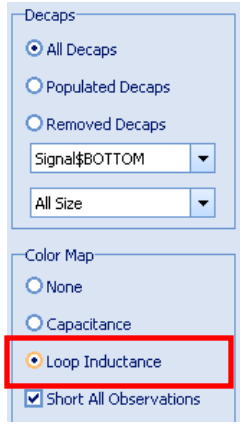
TOP

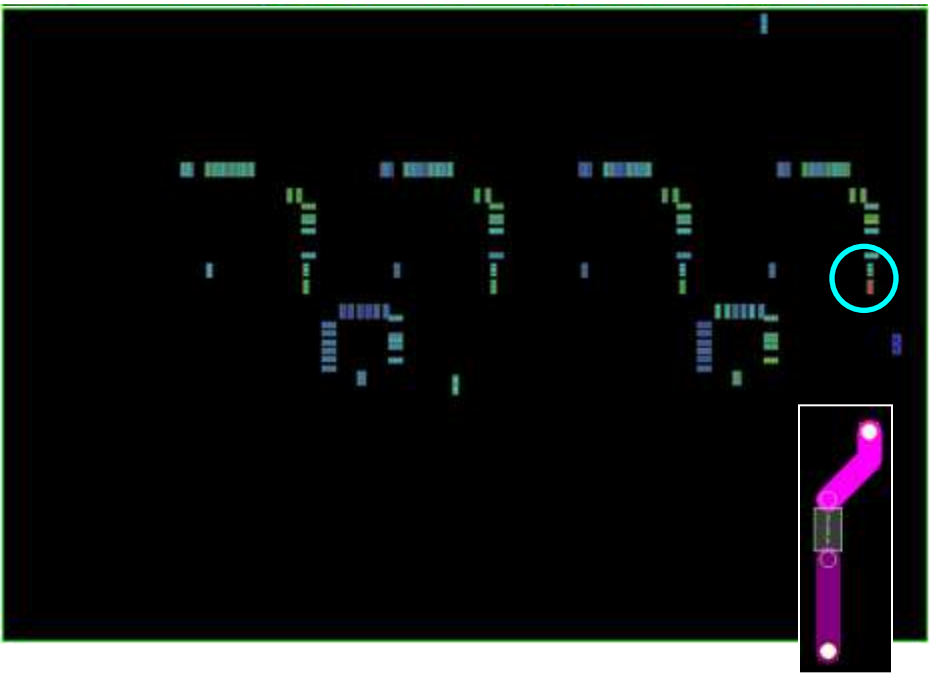


BOTTOM

Total of 394 decap locations for review

找到环路电感最大的电容位置





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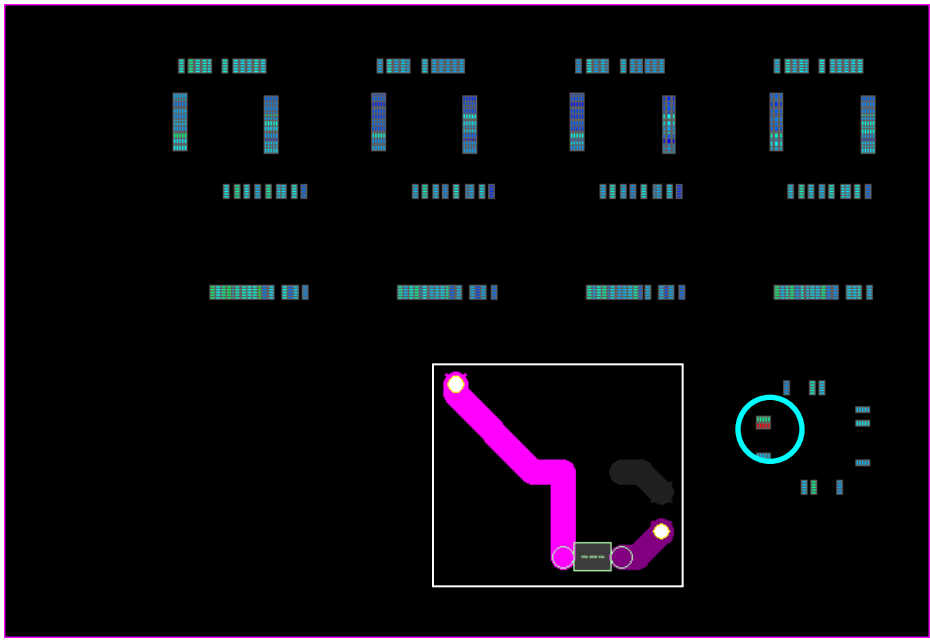


BOTTOM

Total of 394 decap locations for review

OptimizePI 总结

（主要功能列表）

- OptimizePI是业界第一个基于产品性能/成本考虑的PDN优化方案
- 应用Sigrity专利的电磁分析和优化算法可以使PCB板或IC封装PDN网络的性能或成本达到最优
- 仿真各种布局布线后的PCB布线文件
- 仿真各种布局布线前的去耦电容放置方案
- 进行保持PI性能不变情况下的最低成本设计
- 进行基于现有电容种类情况下的最佳PI性能设计
- 进行保持PI性能不变情况下的最小面积设计
- 进行What-if的分析，动态评估PDS性能和成本的关系
- 进行包括IC芯片、封装和PCB板级在内的PDS性能/成本的优化
- 自动化流程选择和放置去耦电容，减小产品中去耦电容的过设计
- 创建最低成本、最佳性能的去耦电容放置表
- 观察每种优化方案中去耦电容在PCB中的实际放置情况

时域分析：SPEED2000

IC封装与PCB设计中主要的电磁问题

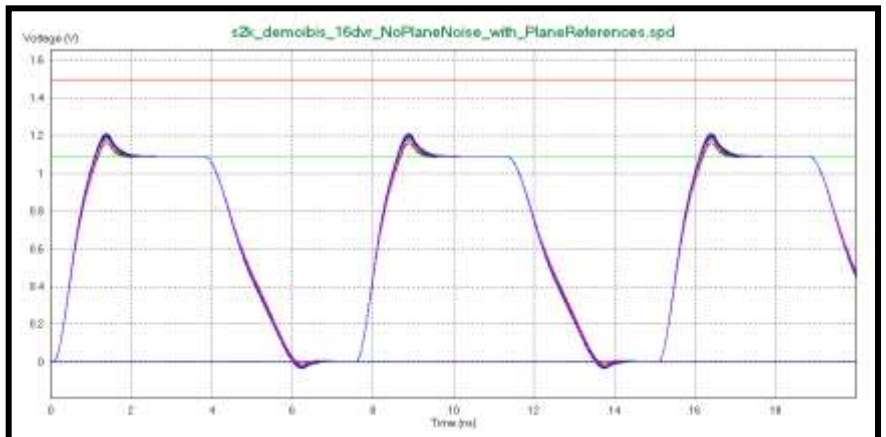
- 反射噪声（振铃）
  → 阻抗不匹配、分支线、过孔、转弯以及其他互连不连续现象
- 串扰噪声
  → 相邻信号线之间的电磁耦合，过孔之间的串扰耦合
- **电源和地之间噪声**
  → 电流切换，尤其是大量的信号同时切换时带来的SSN
- **IC封装与PCB中的谐振与电磁辐射**
- **信号与电源系统的相互作用**

传统SI仿真工具的不足

- **精确度得不到保证**：传统的SI仿真工具基于2D的传输线理论进行仿真，通常将电源和地平面当作***理想情况***进行处理
- **忽略了很多重要的SI的效应**：
  - → 电源和地平面上的电压波动
  - → 信号返回路径上的不连续
  - → 信号与电源系统的相互作用
  - → 多驱动 SSO 的仿真
  - → 过孔间的电磁耦合
  - → PCB/封装中的谐振
  - → 去耦电容的效应
  - → 板边辐射

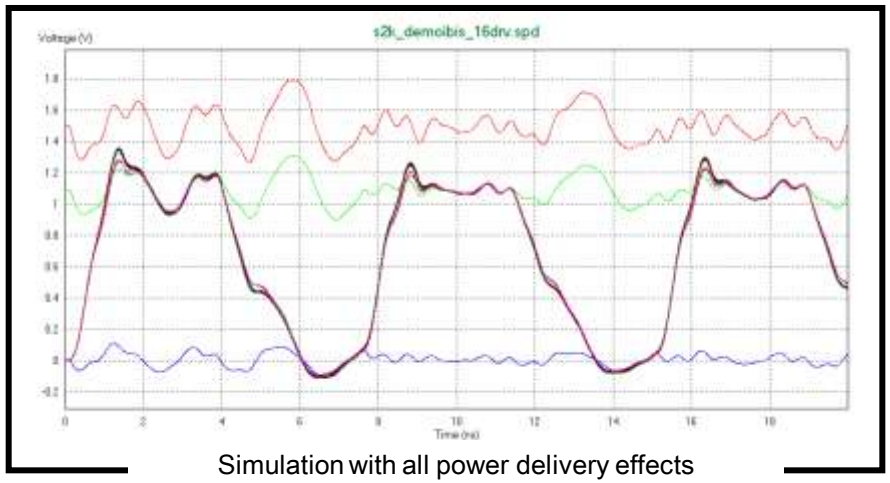
考虑非理想电源地平面的必要性

传统仿真工具
（理想电源地）
=
Risk



Simulation assuming ideal power delivery netwok

Speed 2000
（非理想电源地）
=
Risk Avoided

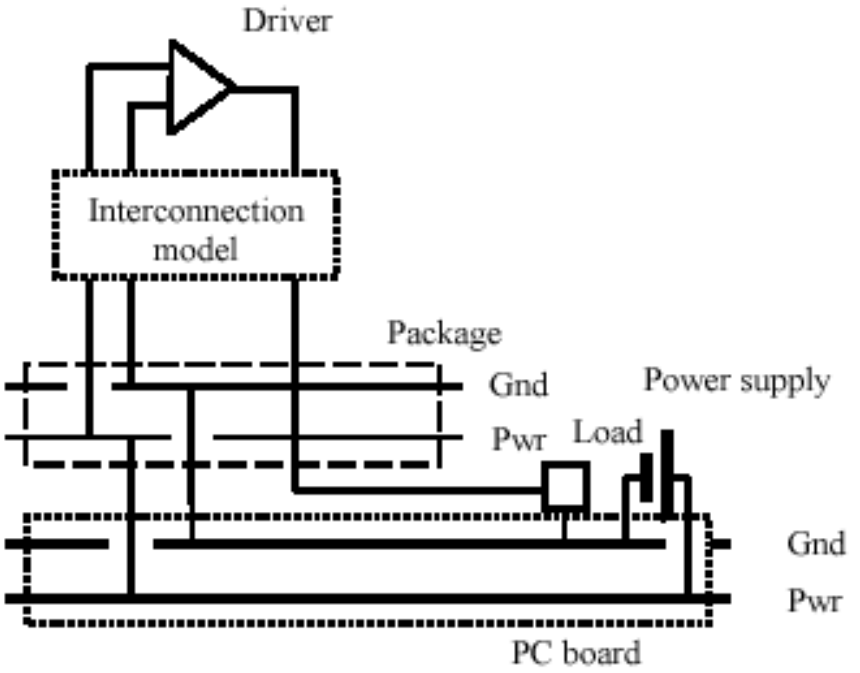


Simulation with all power delivery effects

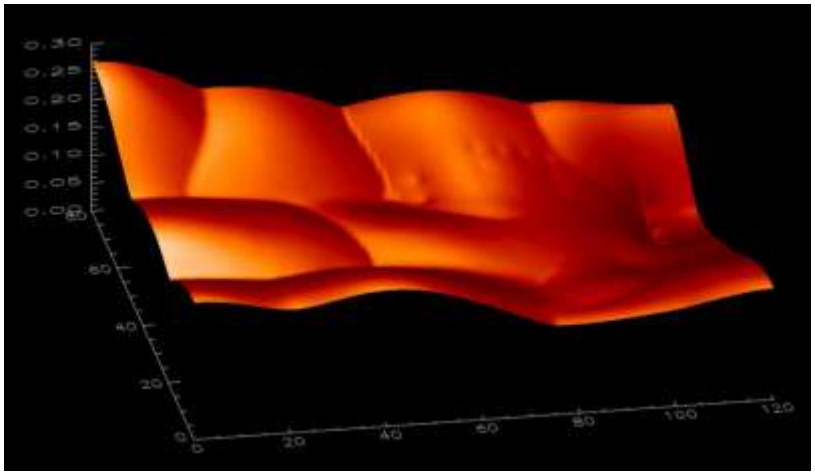
SPEED2000 used for each mode

真正系统级的时域解决方案

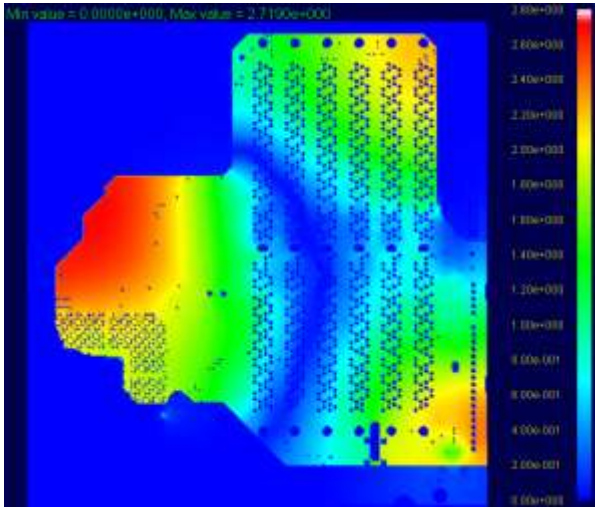
- 片上器件
- 片上电源/地，电容
- 封装
- 插座
- 主板
- 电压供电模块
- 内存模块
- 信号连接线



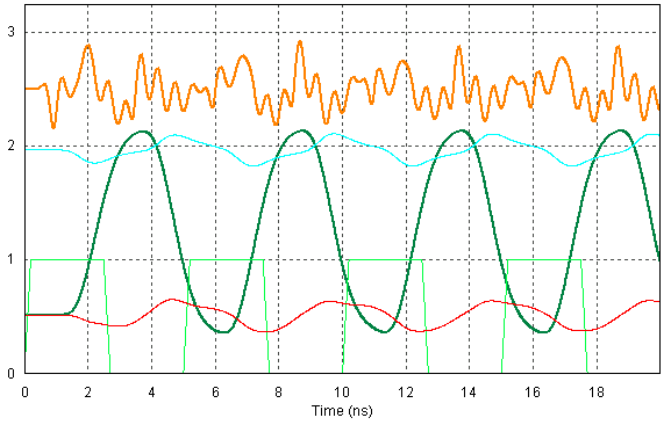
Sigrity的SI/PI解决方案



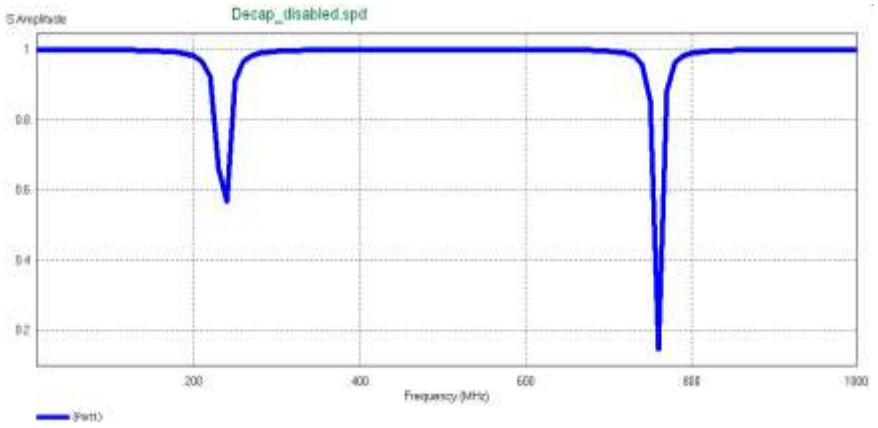
时域电源平面波动



频域 Hot Spot 的仿真

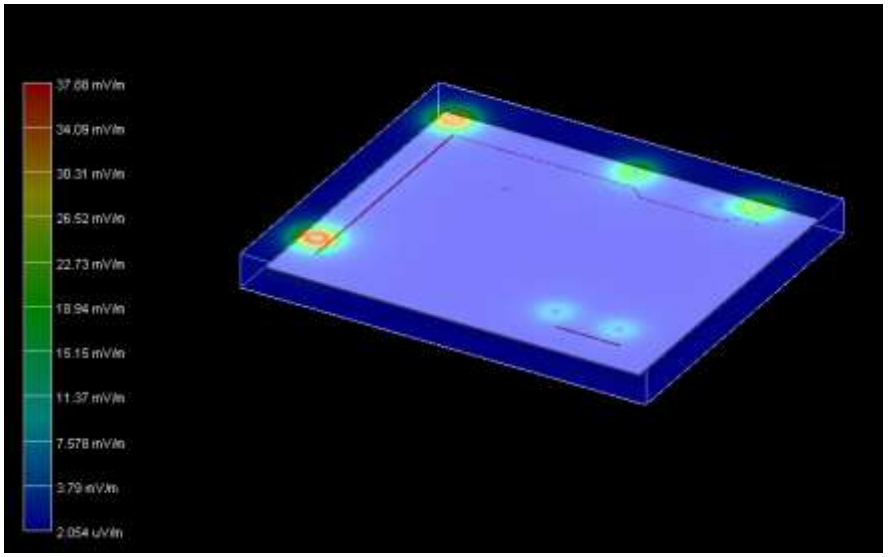


SSN/SSO的仿真

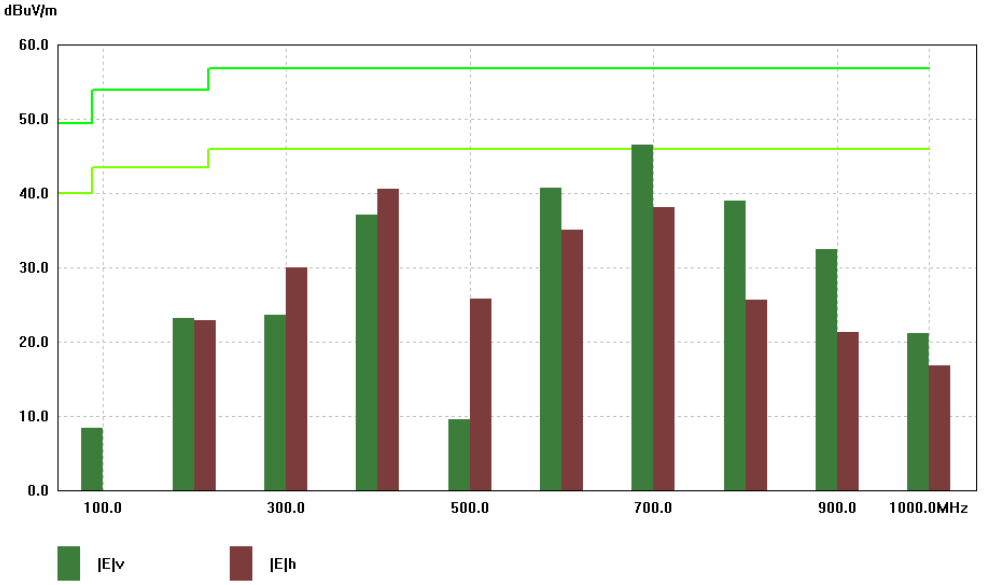


电源及信号的S/Z参数提取

Sigrity的EMI解决方案



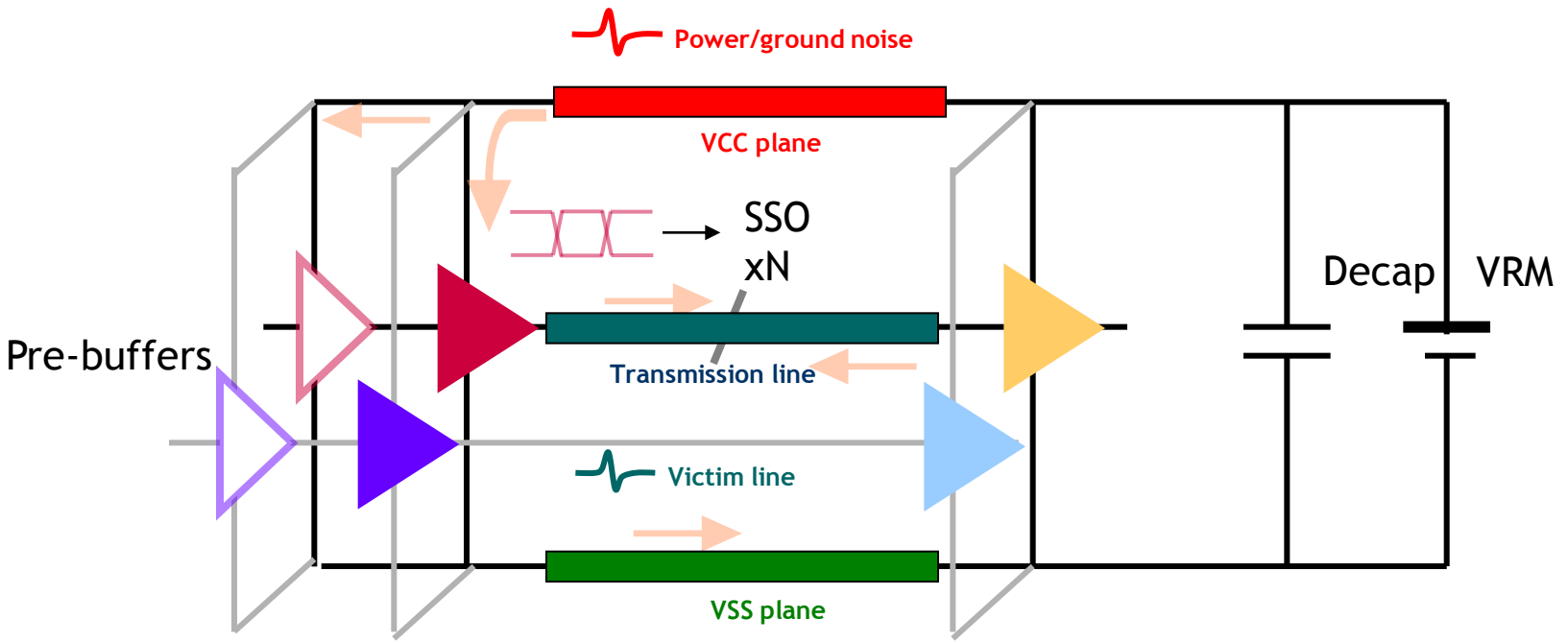
PCB近场仿真



PCB远场仿真

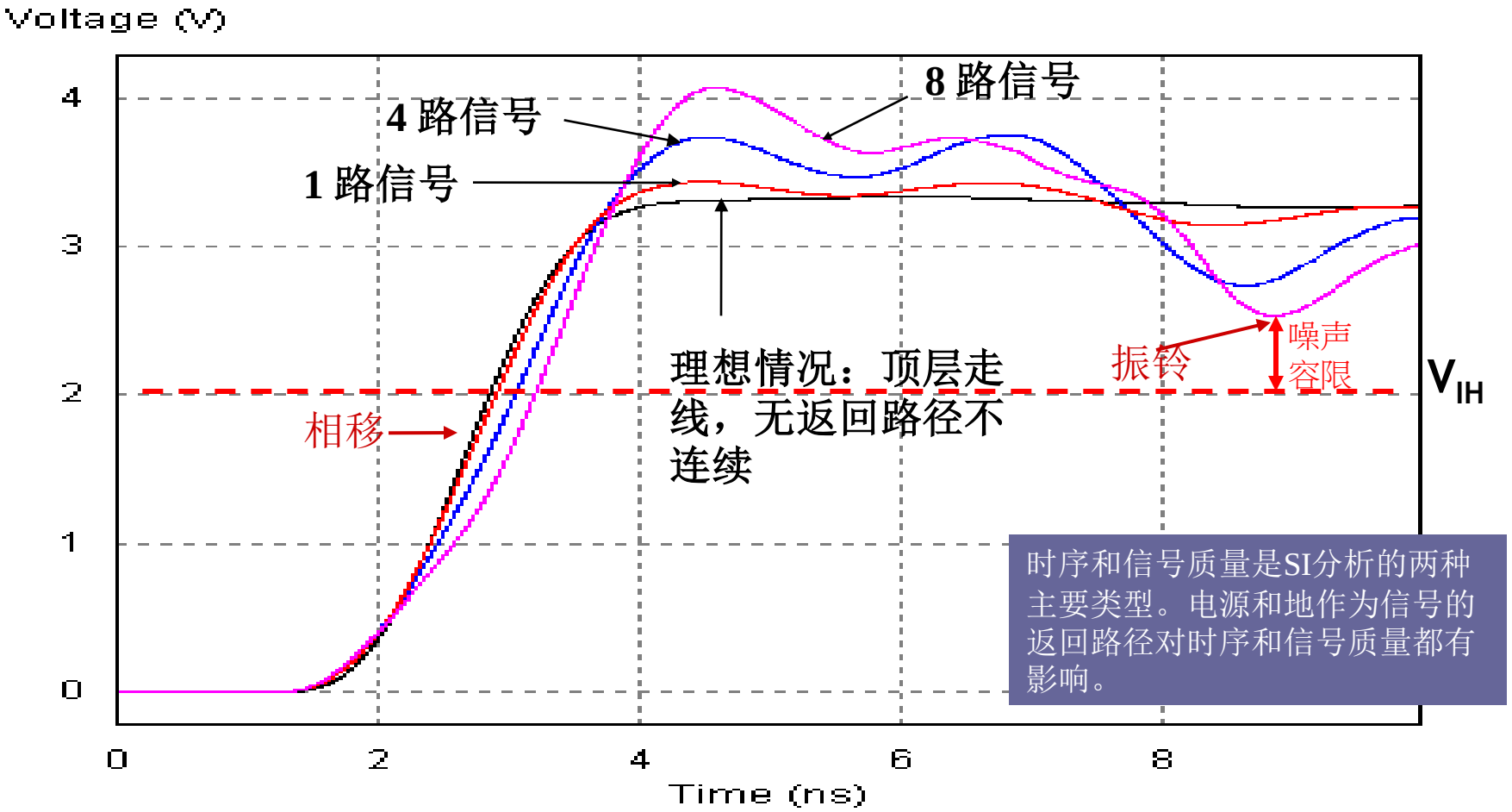
SSN产生的原理

- **SSO/SSN 主要表现:**
  - **PDN noise**
  - **Crosstalk**



同步切换噪声（SSN）影响下接收端的波形1

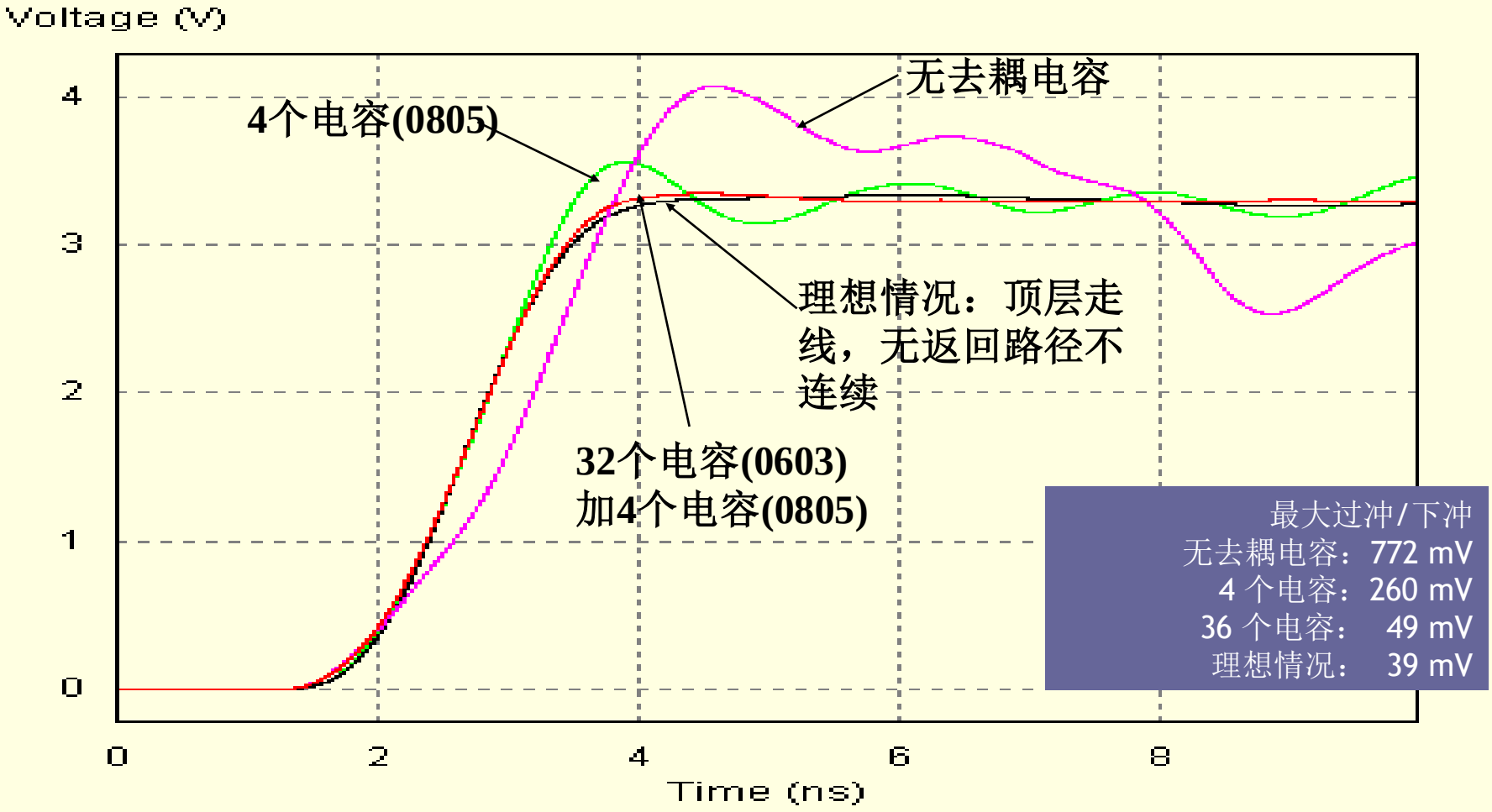
（同步切换的信号数目在变化，无去耦电容，*Speed2000*的结果）



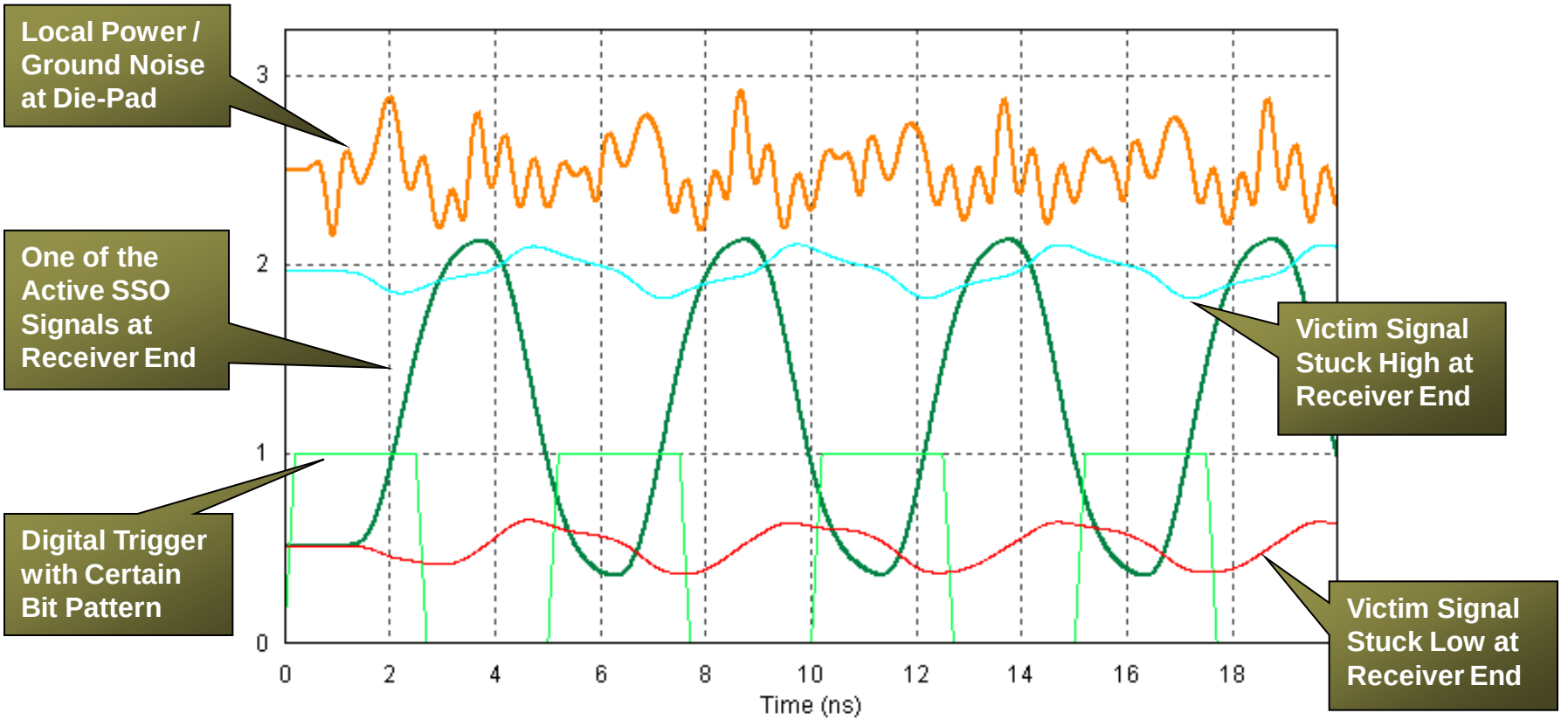
时序和信号质量是SI分析的两种主要类型。电源和地作为信号的返回路径对时序和信号质量都有影响。

同步切换噪声（SSN）影响下接收端的波形2

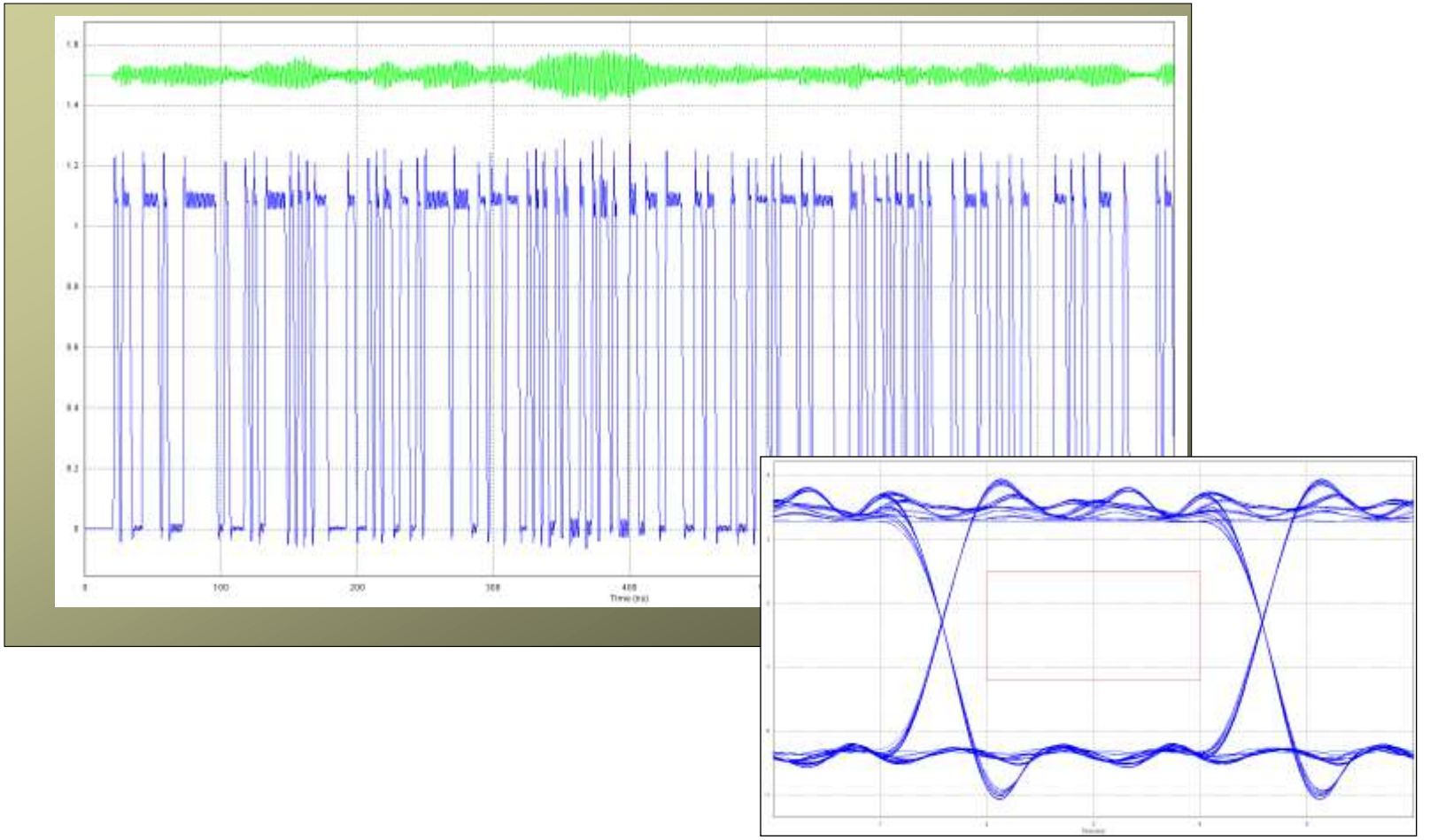
（去耦电容的数目在变化，信号数目为8路，*Speed2000*的结果）



I/O SSN周期信号仿真

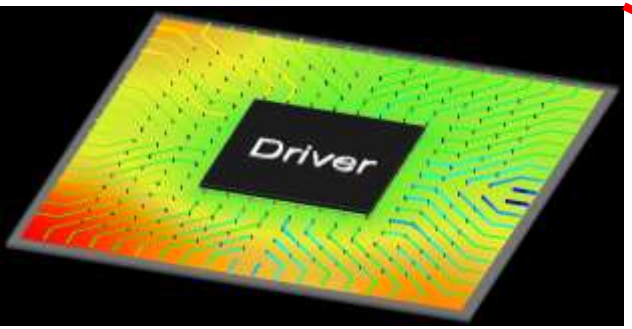


I/O SSN PRBS信号仿真
适用于GHz SI 分析

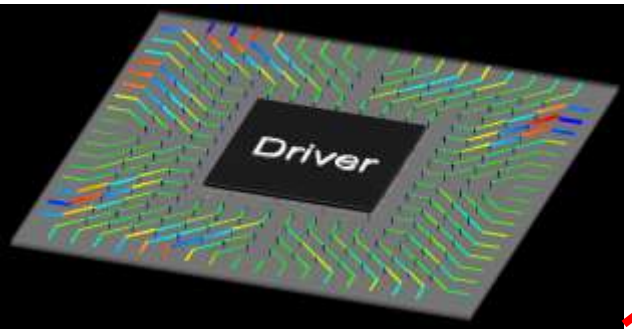


SPEED2000 最新功能介绍

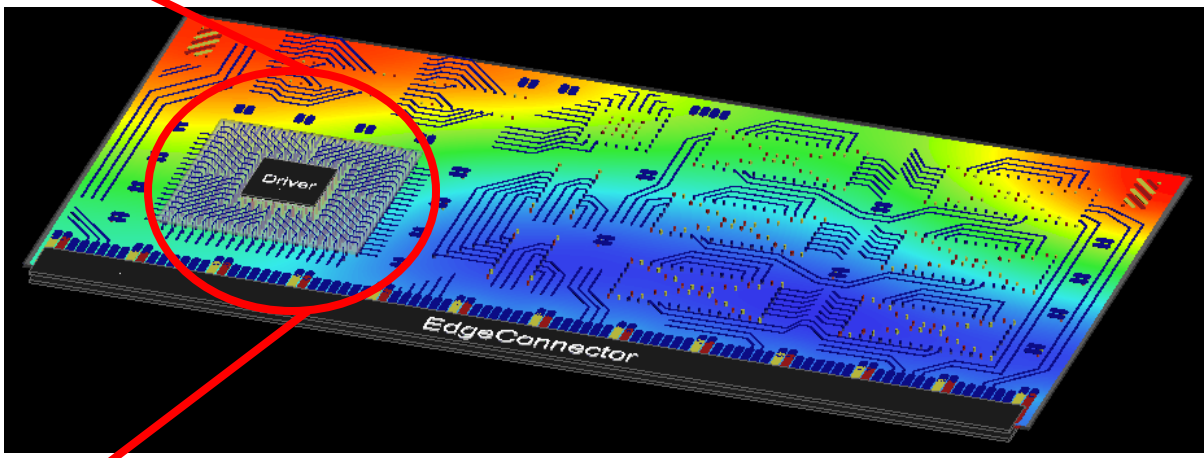
特色1：非理想电源地平面下的SI仿真



Package电压分布



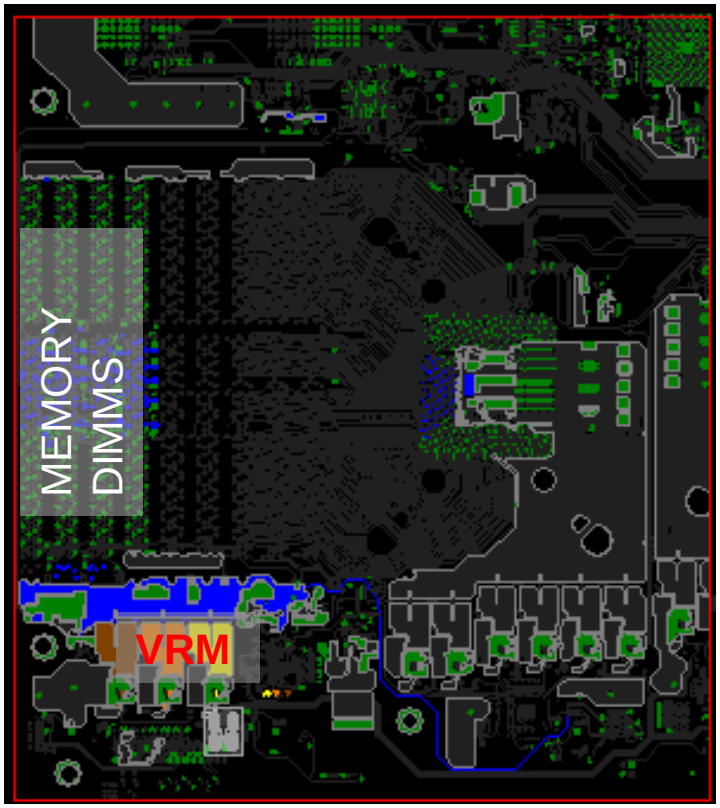
Package电流分布

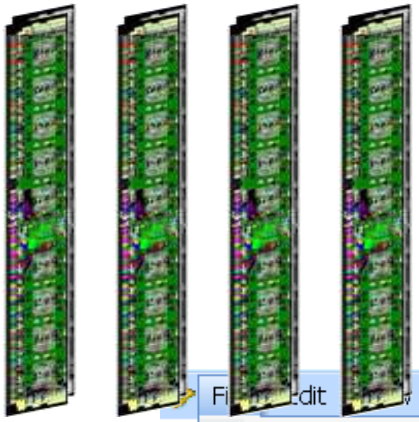


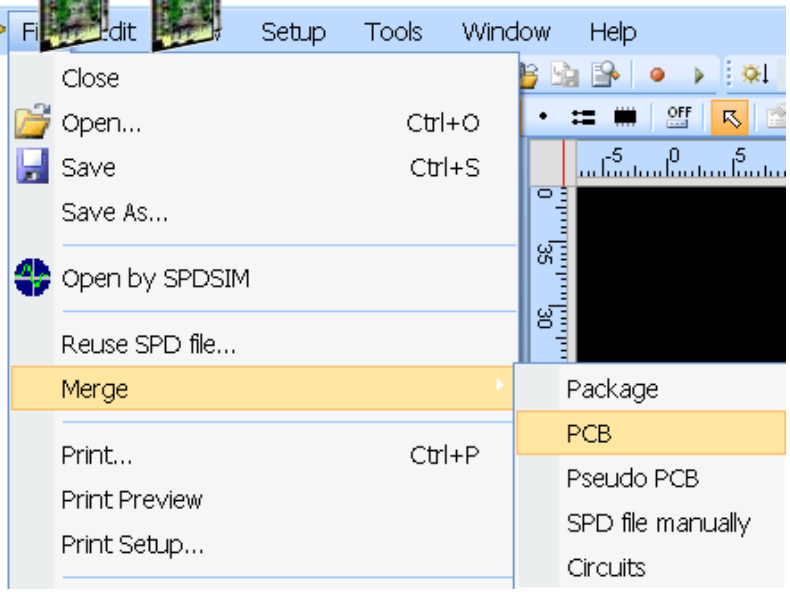
Package_board系统级电压的瞬态分布

- SPEED2000可以考虑非理想的电源、地平面的影响；而传统的SI仿真工具基于2D的传输线理论进行仿真，电源、地平面是当作理想情况来处理的
- SPEED2000考虑的一些重要的SI效应包括：电源和地平面上的电压波动，信号返回路径上的不连续，信号与电源系统的相互作用，多驱动 SSO 的仿真，过孔间的电磁耦合，PCB/封装中的谐振，去耦电容的效应以及板边辐射等

特色2：多板的Merge

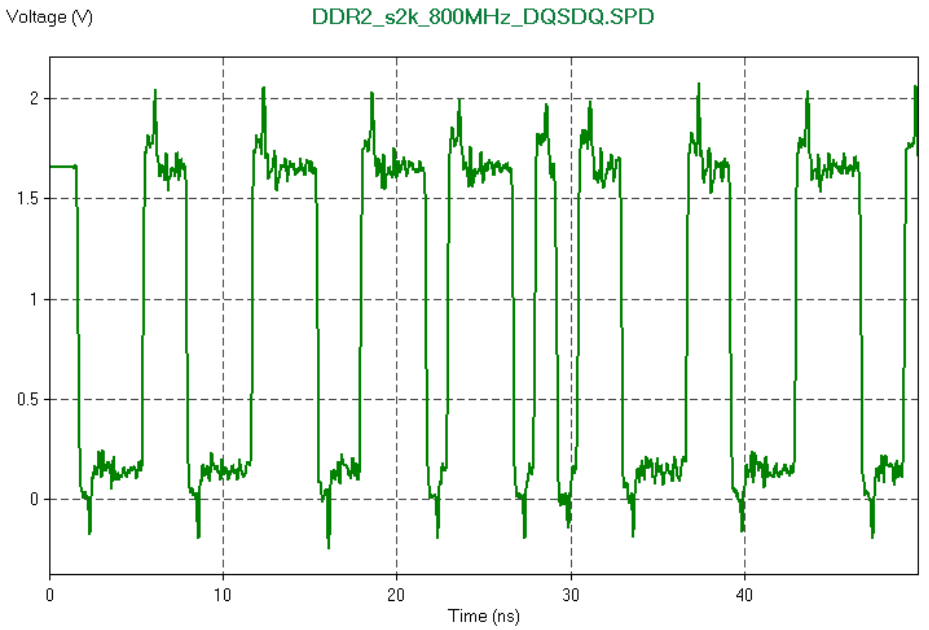


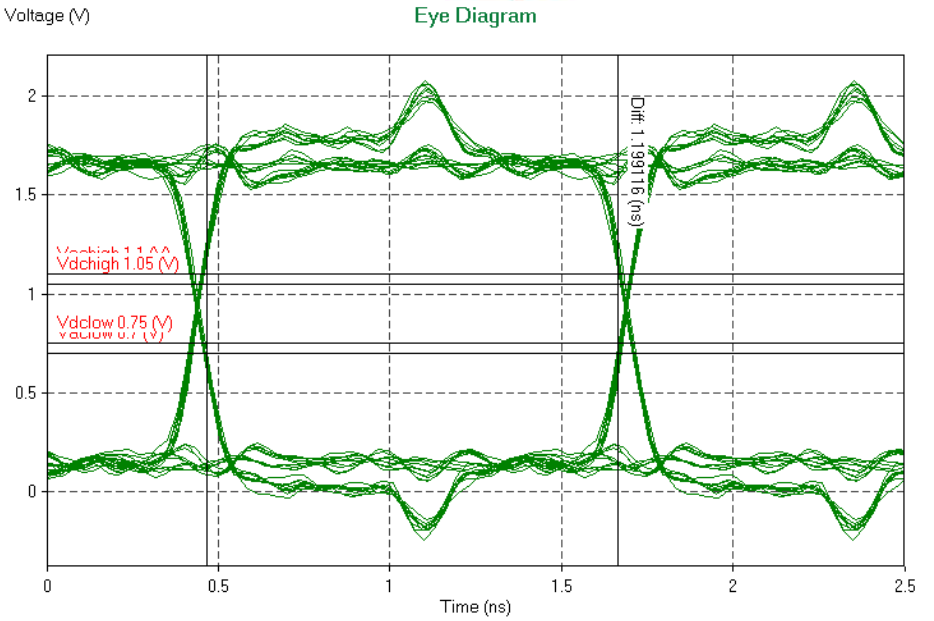




- SPEED2000支持多板联合仿真，利用File > Merge功能可方便的把多个子板拼接到一个总的界面中作仿真；
- 同时Sigrity所倡导的MCP连接协议，已被越来越多的EDA厂商所支持。

特色3：自动生成Report





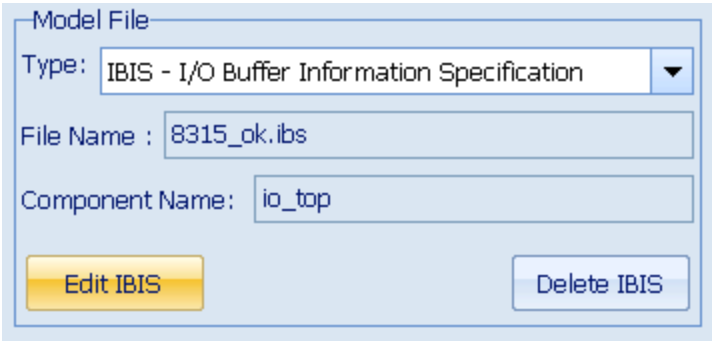
Curve Name	Full Curve Name	Vmax(V)	Time_Vmax(ns)	Vmin(V)	Time_Vmin(ns)
V4	U17.G8::DDR_MDQ<17> ~ U17.H2::GND (V4)	2.07554	37.3534	-0.240612	16.1012

Eye Opening Parameters

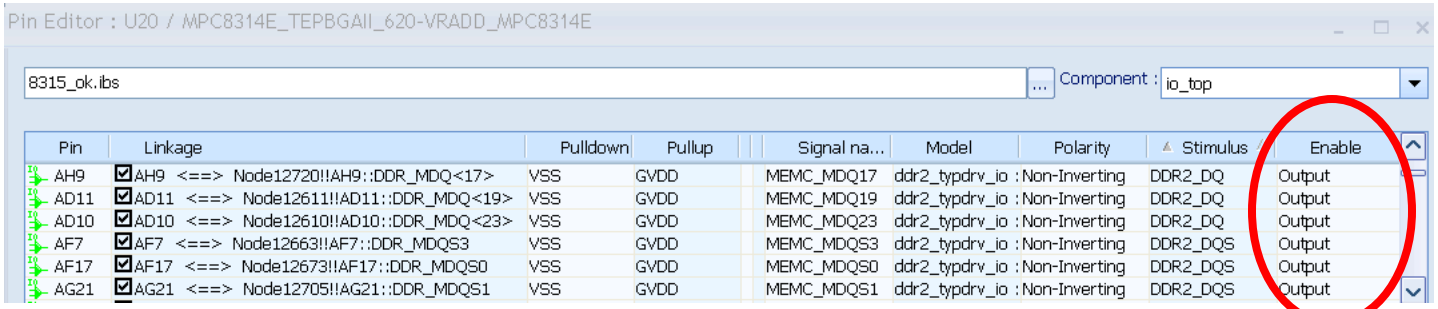
Curve Name	Full Curve Name	Vachigh(V)	Vaclow(V)	Vdchigh(V)	Vdclow(V)	Period(ps)	Offset(ps)	Eye Measurement(ps)
V4	U17.G8::DDR_MDQ<17> ~ U17.H2::GND (V4)	1.1	0.7	1.05	0.75	1250	0	1199.116

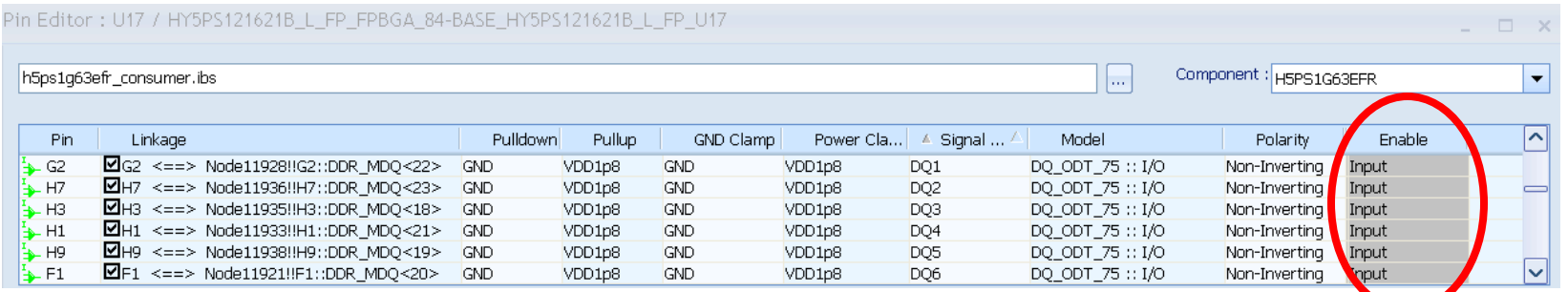
- SPEED2000 Ver10.0的仿真自动化程度得到了较大的提高
- 在SpdSim中点击File>Report，就可以生成相应的仿真报告，其中包括了基本的设置信息，以及仿真波形的常见后处理结果，如Overshoot，Undershoot，Eye Opening等

特色4：自动赋IBIS模型

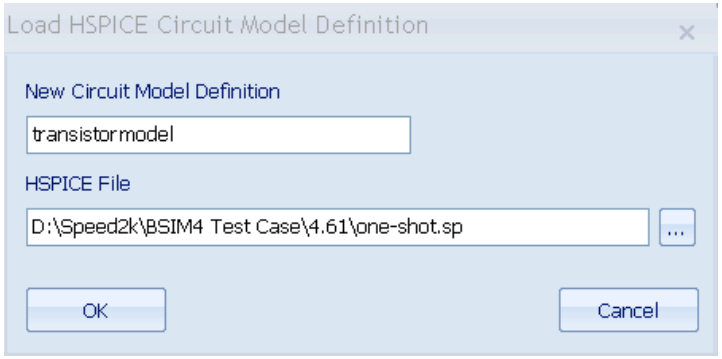


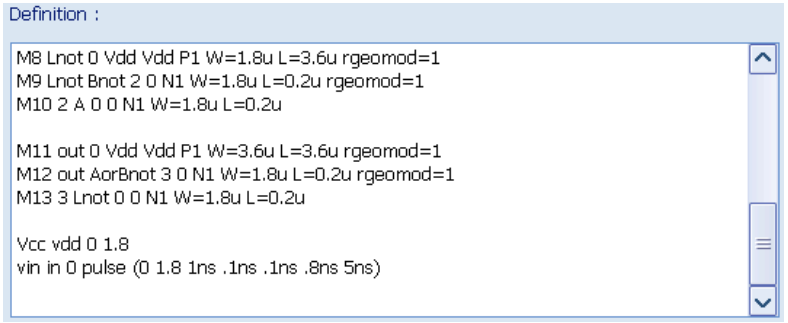
➢ SPEED2000可以自动对全芯片的所有管脚赋上IBIS模型，并对不同的管脚指定输出或输入属性

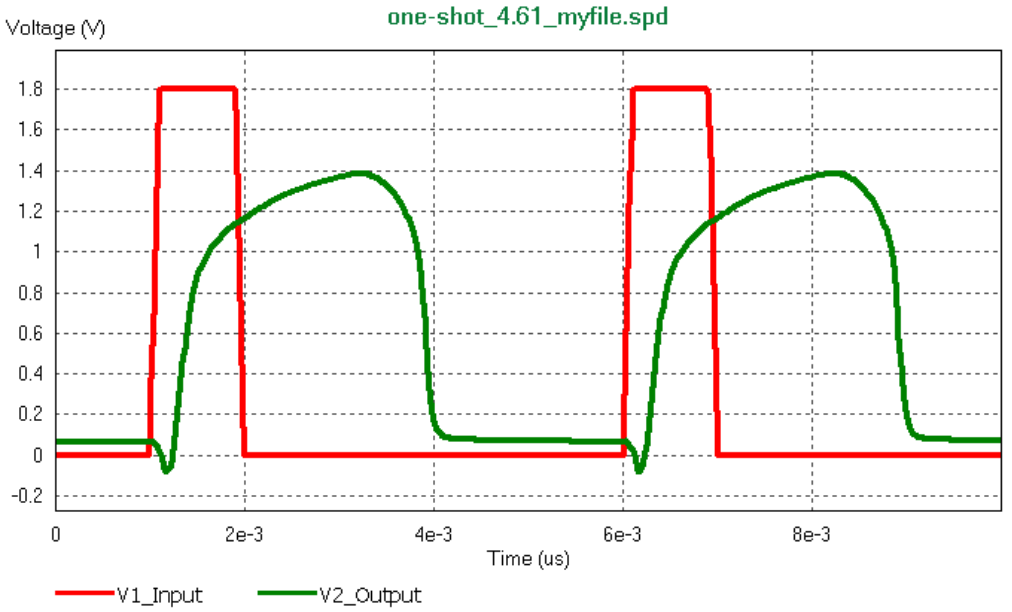




特色5：支持晶体管模型

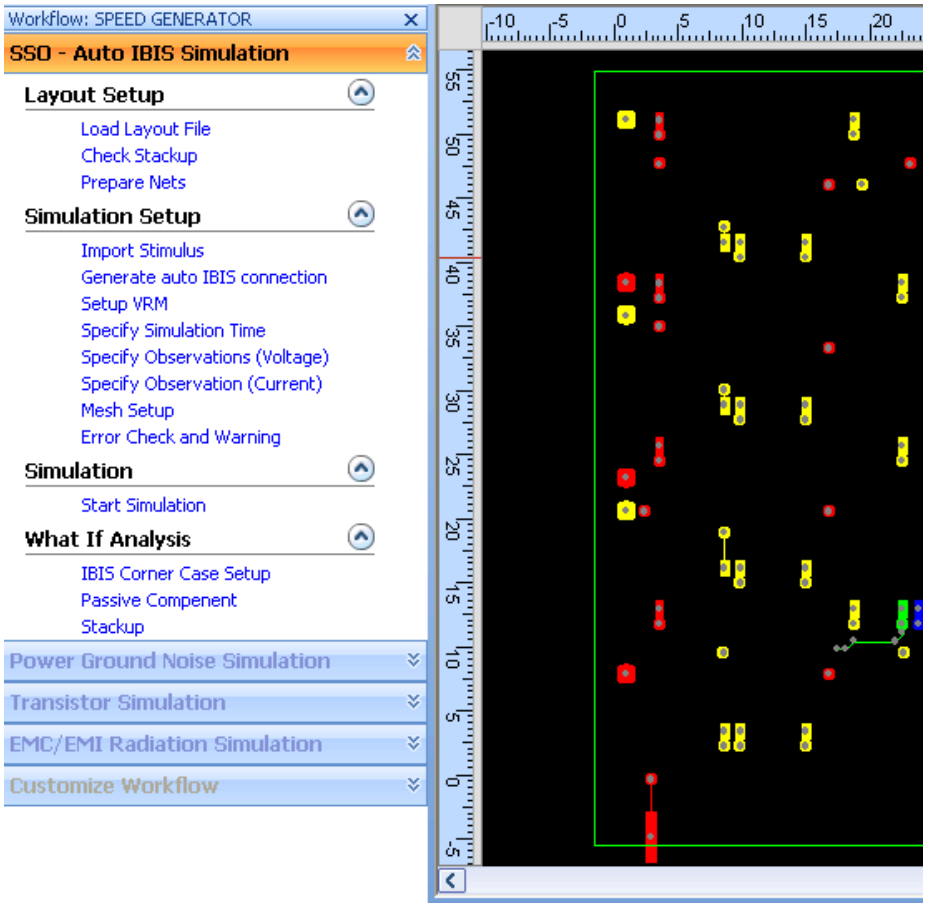






- SPEED2000支持大部分的 Hspice 的语法，可直接加载 Hspice 仿真语句
- 支持MOSFET BSIM3v3 Level 49/53和MOSFET BSIM4 Level 54

特色6：流程化操作

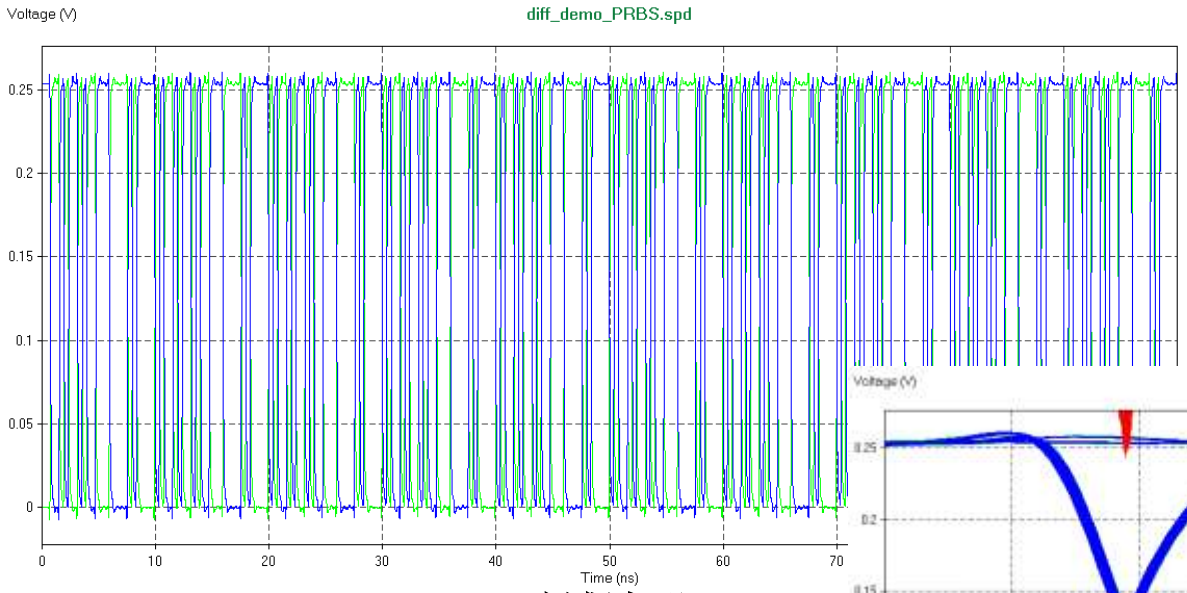


SPEED2000 **共有4个内置的流程：**

- **a.** 同步切换输出（**SSO**），可自动为电路加载**IBIS**模型，仿真信号的传输并考虑返回路径的影响，仿真**SSN**
- **b.** 电源地噪声仿真（**Power Ground Noise Simulation**），可仿真电源地的噪声
- **c.** 晶体管模型仿真（**Transistor Simulation**），可分析各种晶体管级的**buffer**模型
- **d. EMC/EMI**辐射仿真（**EMC/EMI Radiation Simulation**）,可分析整板的远场和近场辐射

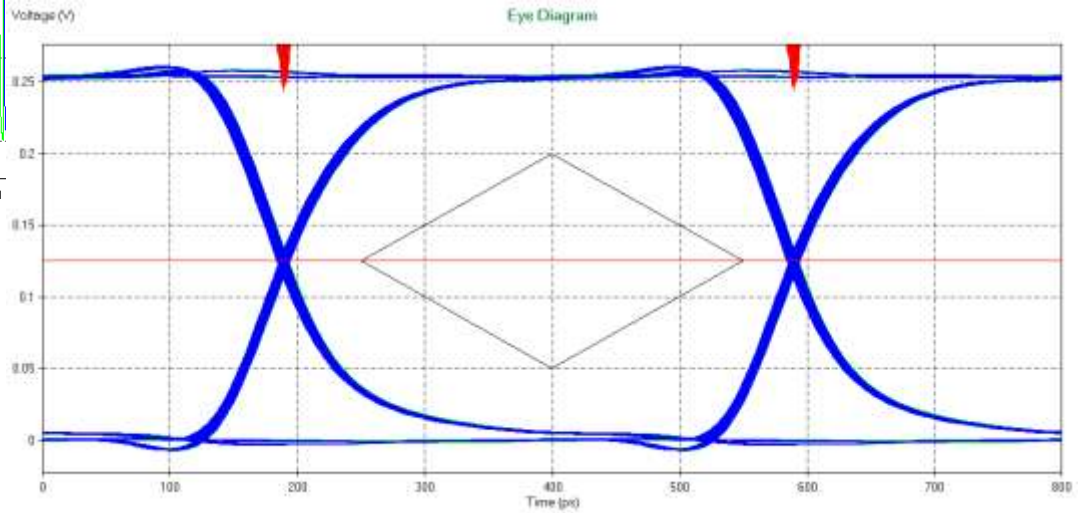
➢ SPEED2000 除了内置有常用的仿真流程外，用户还可以根据实际情况自己定制流程

案例1：2.5Gbps高速串行通道



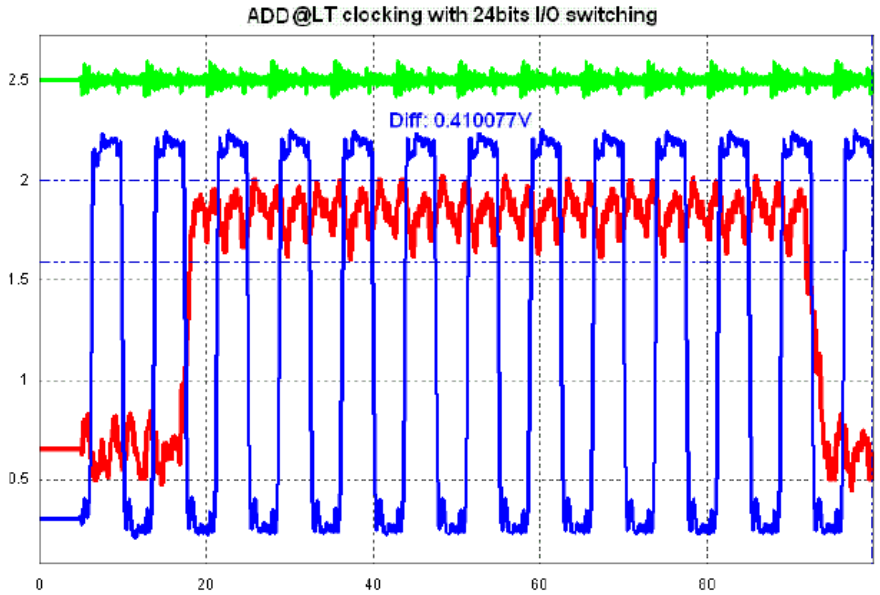
时域波形

眼图和抖动



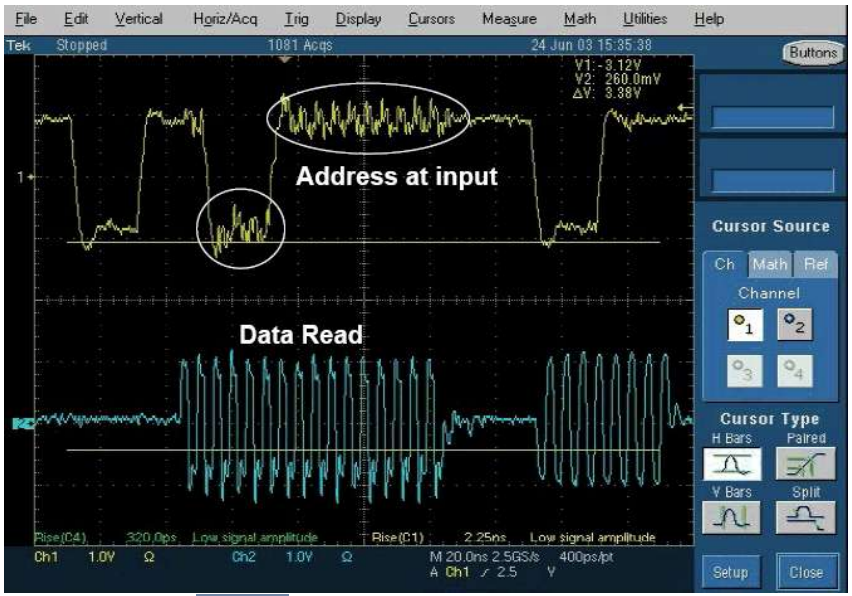
- SPEED2000可以输入各种伪随机序列(PRBS)作为激励，从而得到高速串行通道的时域波形；
- 能生成各种 Eye Mask，并以Histogram和Density两种方式显示Jitter的大小。

案例2：DDR系统级验证

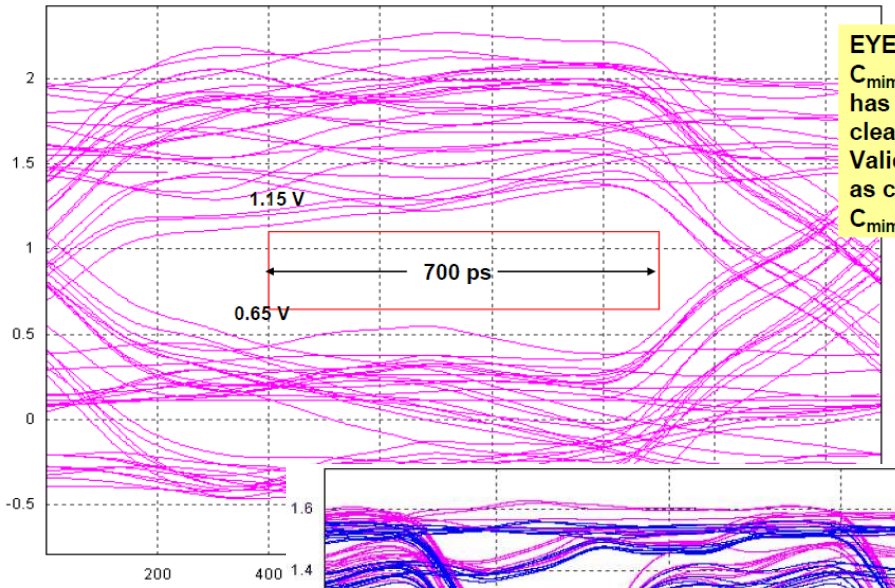


SPEED2000仿真波形

示波器测量结果

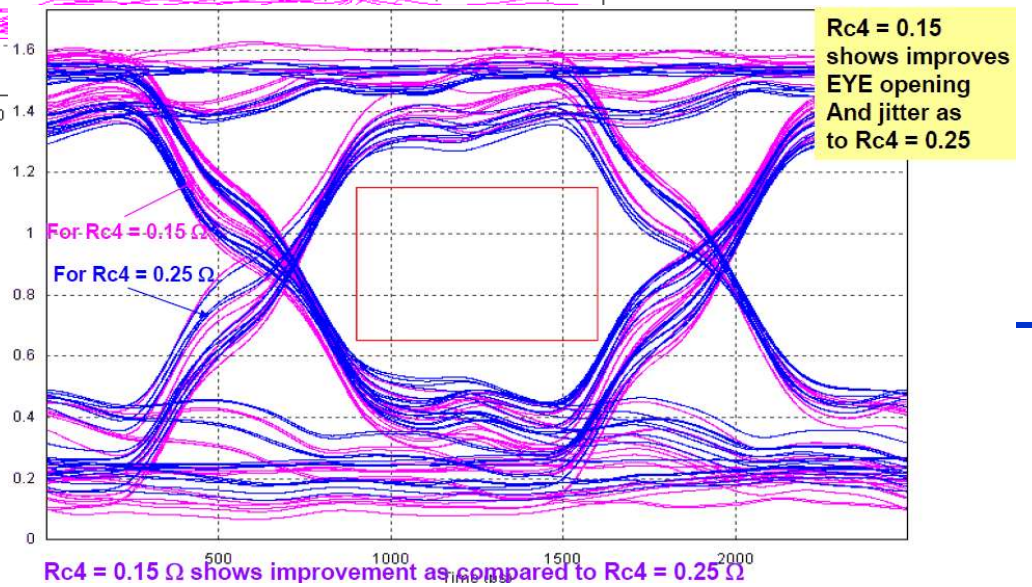


案例5：Cdie+PKG+Test Load的时域仿真



Cdie=10nF

DDR2-667

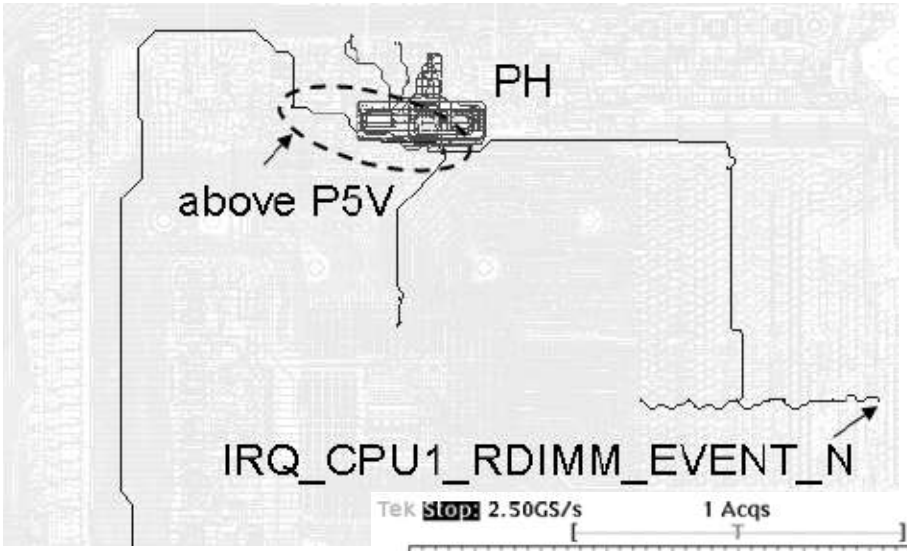


Cdie=10nF

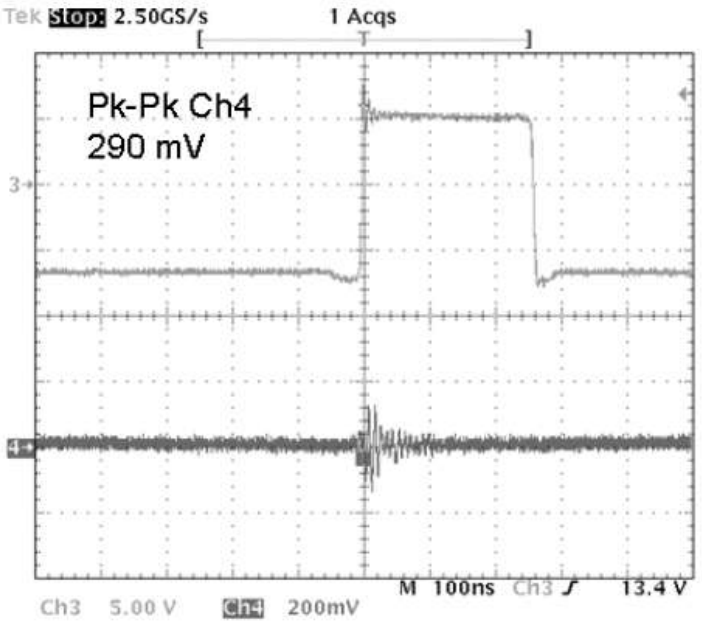
DDR3-800

- 来源: Study of Simultaneous Switching Noise Reduction for Microprocessor Packages by Application of High-K MIM Decoupling Capacitors, Freescale, Feb2007.

案例6：PCB中VR噪声的耦合分析



➢ 来源: Switching Voltage Regulator Noise Coupling Analysis for Printed Circuit Board Systems，Intel，DesignCon Feb 2009.



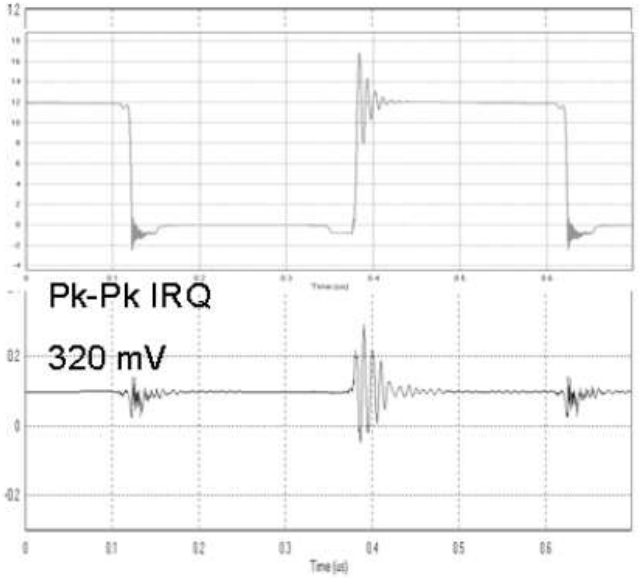
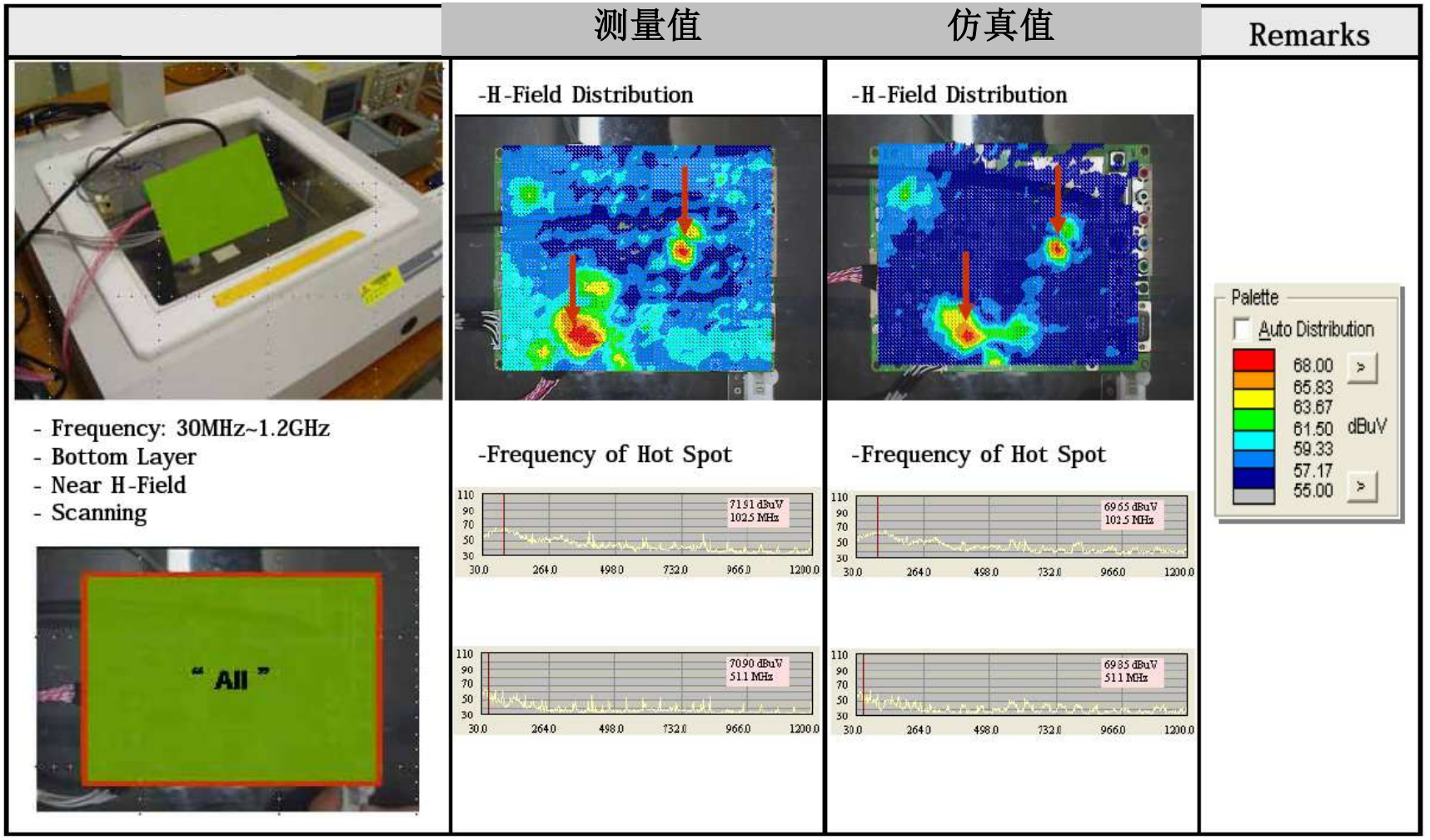


Figure 17: Fab2 IRQ Measurement (left) vs Simulation (right)

案例7：整板级EMC仿真



磁场（H-field）的测量Vs.仿真 – *整板级*

- 来源: How to reduce EMI using CAE, LG, Mar2008.

SPEED2000总结

- **SPEED2000是一款专业的时域仿真工具，具有以下鲜明特点：**
  - 最大特色之一是，将电源网络和地网络当作非理想的情况来处理，考虑的是非理想的信号返回路径；
  - 最大特色之二是，支持最新的 IBIS5.0模型以及最新的Touchstone2.0模型；
  - 唯一不经过任何中间过程，可以直接做全系统级分析的时域仿真工具；
  - 专业的时域仿真工具，专注于IC封装级和PCB板级的SI, PI 和 EMI/EMC仿真；
  - 适用于布线前和布线后的 SI/PI仿真，包含单板或多板；
  - 适用于多路并行通道的SSN/SSO仿真，可进行全芯片的自动IBIS映射；
  - 适用于高速串行通道的电源/地噪声分析，以及高速信号的眼图和抖动等；
  - 适用于含晶体管（Transistor Level）模型的时域仿真；
  - 适用于封装级和板级的 EMC/EMI近场和远场仿真；
  - 适用于观测系统中任意电路、任意位置处的电压或电流波形；
  - 适用于仿真有噪声干扰下关键器件或关键位置的电压电流响应；
  - 适用于评估去耦电容的效应对系统电源或信号质量的影响；
  - 流程化的操作界面和简洁的菜单，极大的方便了用户的使用和全公司的流程统一。

封装模型提取与分析：XtractIM功能介绍

XtractIM综述

- **XtractIM 是Sigrity公司新一代IC封装的模型提取工具**
- **XtractIM 可提取各种IC封装的电模型**
  - 全封装的**IBIS**模型；
  - 单级或多级的**SPICE**等效电路模型
- **XtractIM 的主要技术优势**
  - 能生成精确解析的宽带模型，业界唯一
  - 能进行信号网络和电源网络的性能评估，业界唯一
  - 能生成精确的全封装IBIS/SPICE模型，业界领先
  - 支持的封装种类齐全（包括Leadframe, SiP等流行的封装形式），功能强大
  - 比其他模型提取工具通常快一个数量级以上，提取效率高
  - 流程化的分析步骤，易于使用
  - 与Sigrity的封装布线工具UPD高度集成

XtractIM的主要功能

- **XtractIM 可以产生**
  - 带耦合的RLC参数，用于IBIS模型
  - SPICE RLGC单级模型
    - 非对称的PI或T型的拓扑结构以确保更高的准确性
  - 基于网络或基于管脚的模型
  - 宽带多级的优化模型
- **XtractIM 可以显示**
  - Spreadsheet形式的模型
  - 2D和3D的RLC结果显示
  - 基于Layer的RLC分布
- **XtractIM 可以分析**
  - 全封装模型或某些独立的信号网络
    - 一次仿真即可得到全封装的模型，且速度快精度高
  - 各种类型的封装模型
    - flipchip, wirebond, windowed BGA, stacked-die, package-on-package, multiple side-by-side die; leadframe等
- **XtractIM 可以支持各种EDA的布线工具**
  - 支持类型：upd, mcm, na2, dsn, spd
  - 与Sigrity的布线工具UPD高度集成

XtractIM的最新功能发展

✓ Ver2.1 新功能

- 通过计算每个pin脚的直流电阻和环路电感，评估电源、地网络的性能

✓ Ver3.0 新功能

- 通过计算信号网络的阻抗和耦合，评估信号网络的性能
- 支持更多的 Leadframe类型，如QFN，QFP等
- 支持宽度渐变的走线仿真

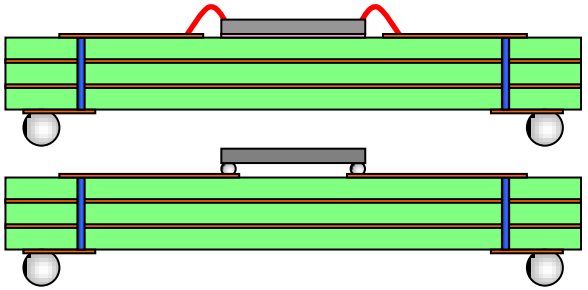
✓ Ver3.1 新功能

- 对于多Die的封装类型，可生成基于基于管脚的模型
- 基于管脚的SPICE等效模型的模型大小更加紧凑
- 改善了模型内互阻的计算，使模型更精确
- 改善了3D模型结构的显示，可显示bump，Soldball，Lead和PCB的地平面
- 改善了3D仿真结果的显示，支持更多的显示方式

Ver4.0 新功能

- Pin-based的宽带模型提取
- 串扰分析：给定Tr，可仿真得出各个Net之间的近端串扰与远端串扰
- Per-Pin RL: 报告总电感
- 对于多die封装：报告各支路之间的互感和互容

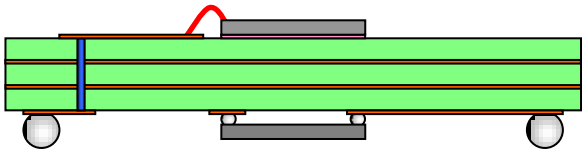
支持的封装类型

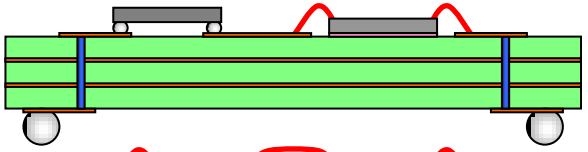


wirebond

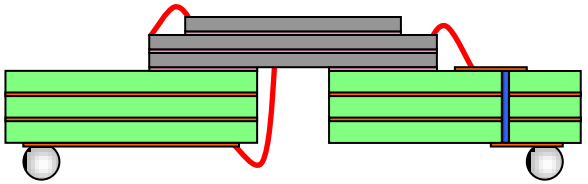
flipchip

2-sided die



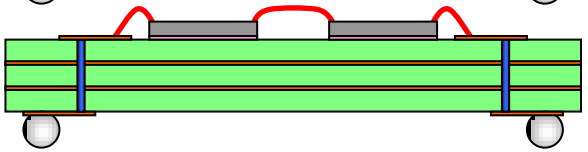


side-by-side die

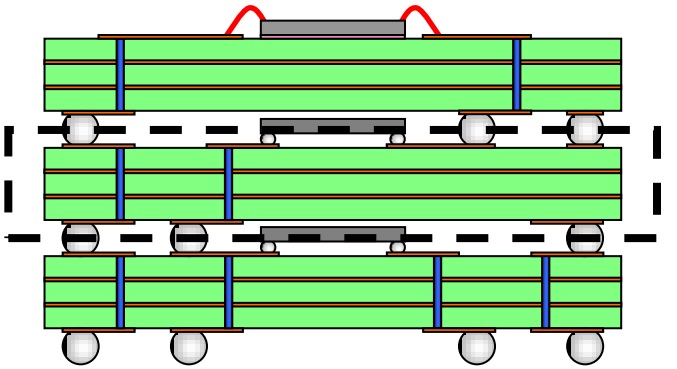


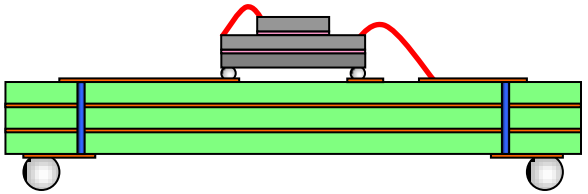
W-BGA

die-to-die bondwires



package-on-package

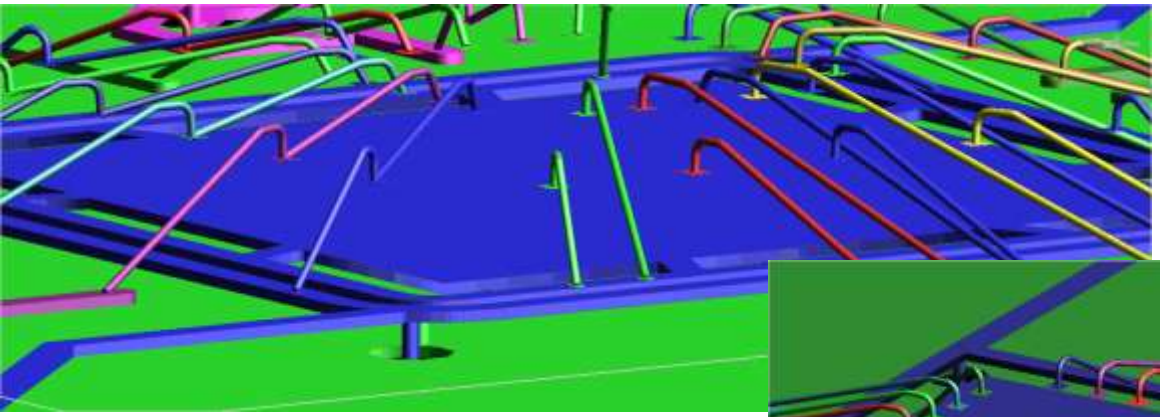




stacked-die

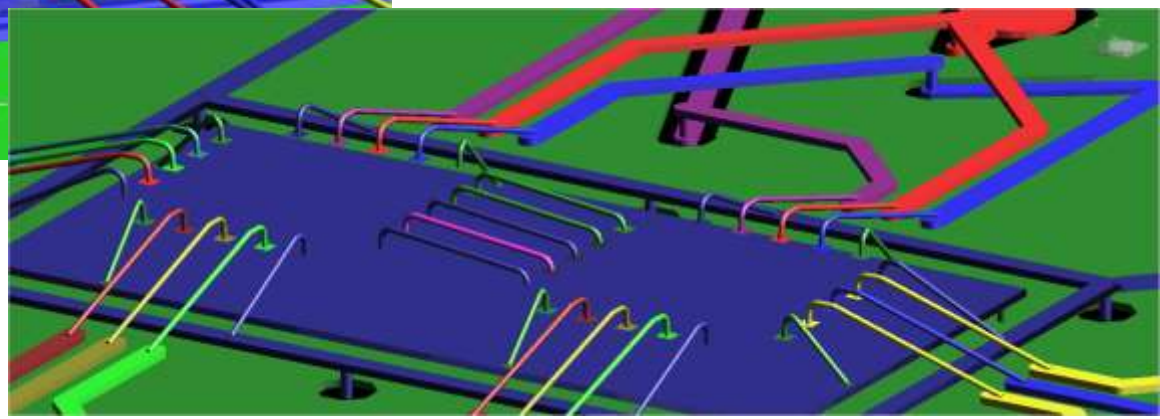
支持Multi-Die封装

- 封装类型不断增加
  - System-in-Package (SiP)
  - 多Die层叠的Memory模块
- 支持
  - wirebond, flipchip, 或是两者的组合
  - 基于信号Net的模型

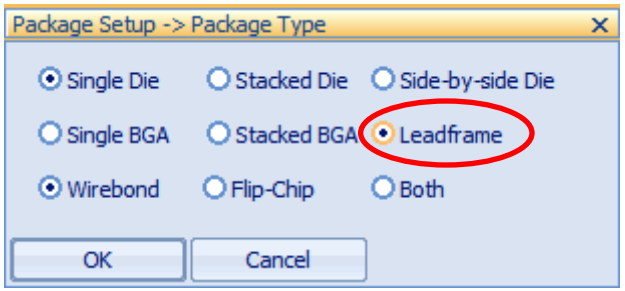


Stacked Die

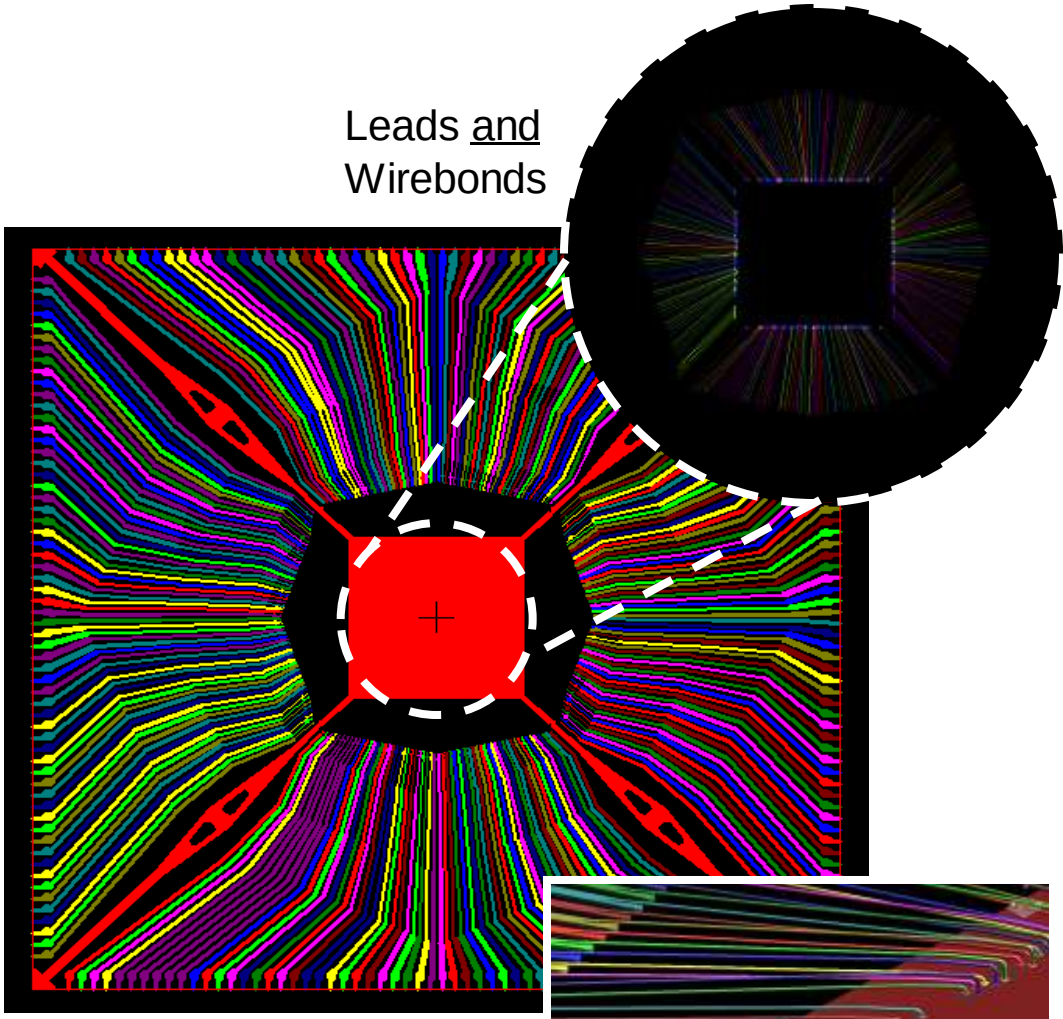
Side-by-Side Die



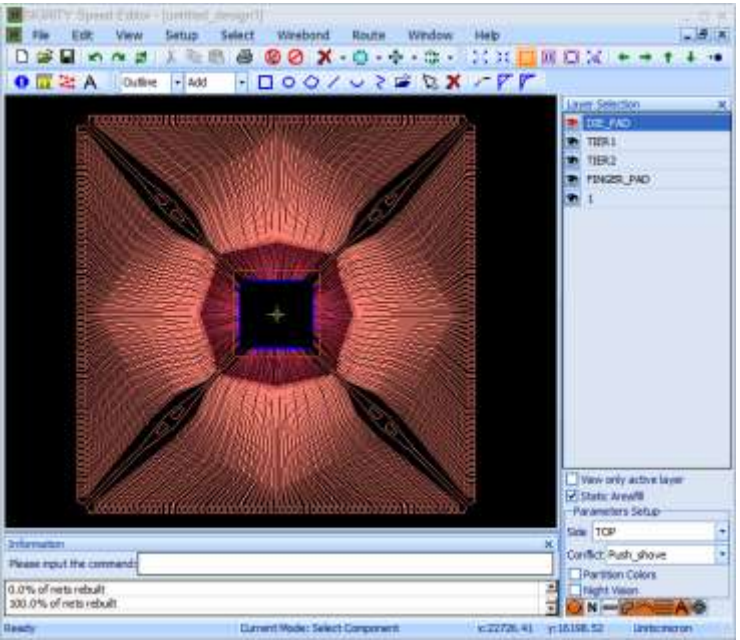
支持Leadframe封装



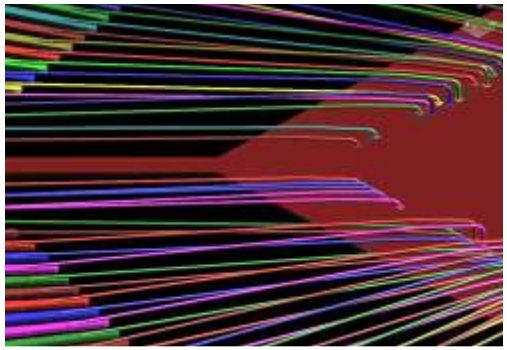
Leads and Wirebonds



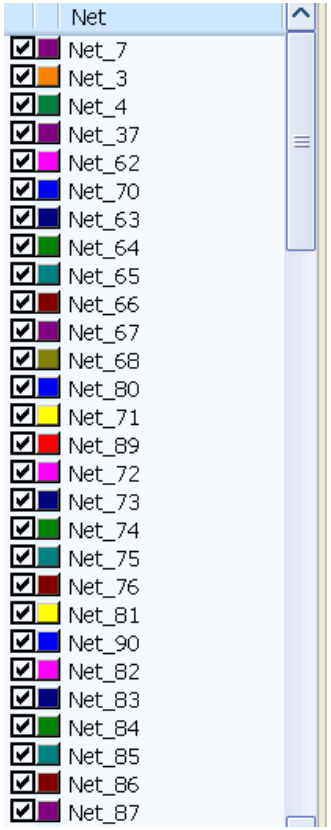
DXF design file support

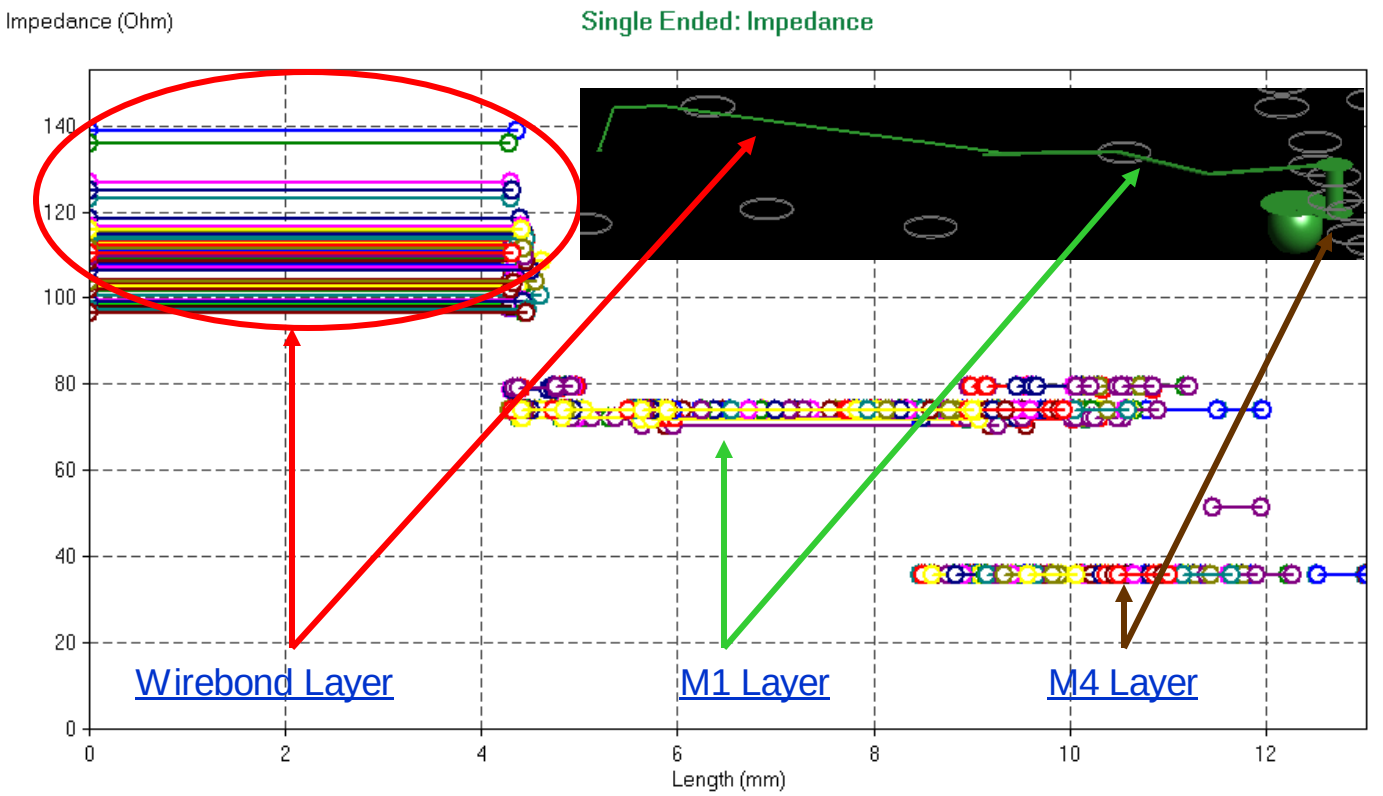


multi-level wirebonds



电性能评估1：信号的阻抗Vs长度

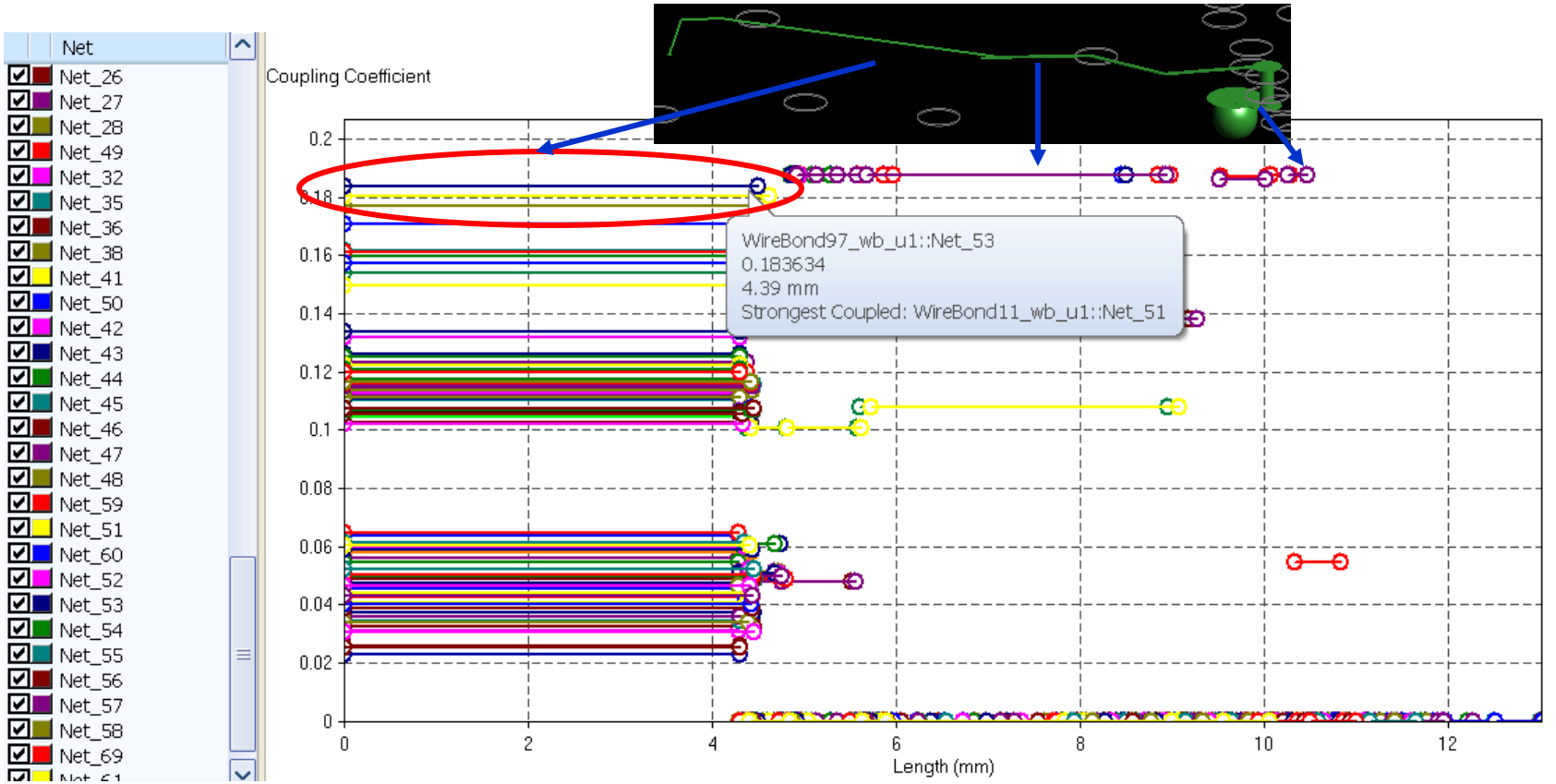




Note：

1. 该功能通过各网络每段**Trace**所对应的特性阻抗大小来评估信号**Net**的设计性能；
2. 从上图可以清楚的看出封装设计中的最大和最小阻抗的分布；
3. **Highlight**部分：由于**Wirebond**的弧高各不相同，因此他们的阻抗也不一样。

电性能评估2：信号的耦合系数Vs长度

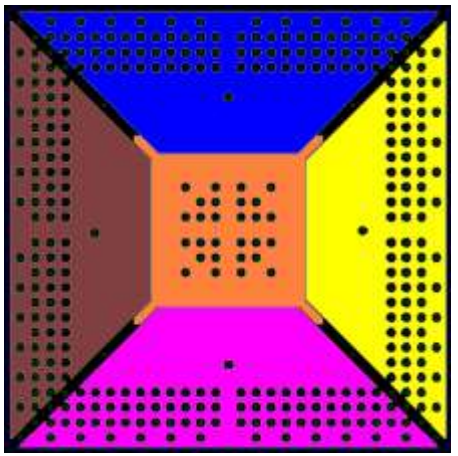


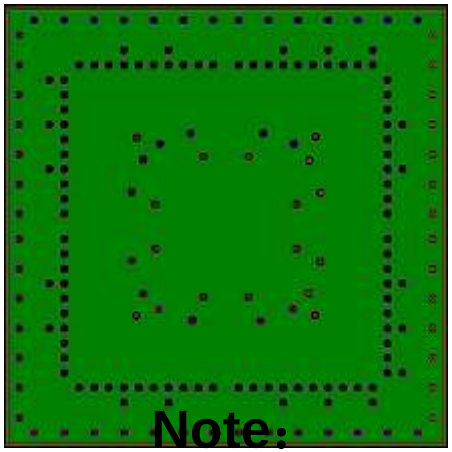
Note：

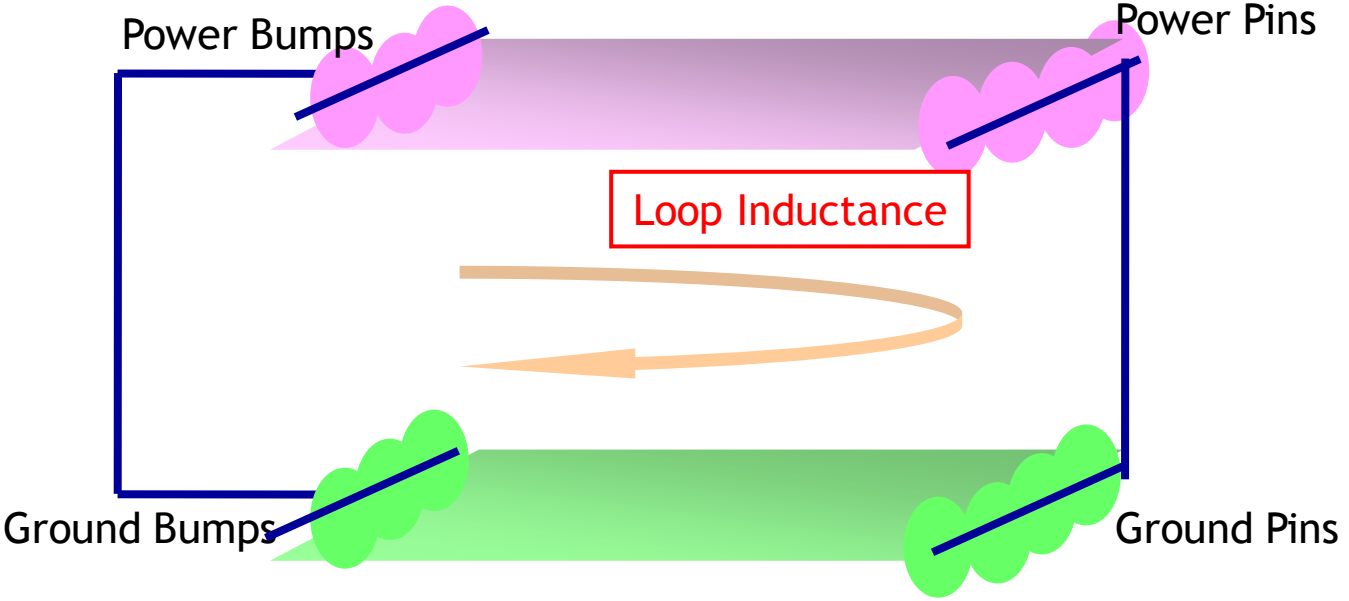
1. 该功能通过<u>各网络每段**Trace**所对应的耦合系数的大小来评估信号**Net**的设计性能</u>；

- 结果中显示的是各网络之间最大的耦合系数；
- **Highlight**部分：在**Wirebond**部分，**Net_53**与**Net_51**的耦合程度最高。

电性能评估3：电源地网络的环路电感







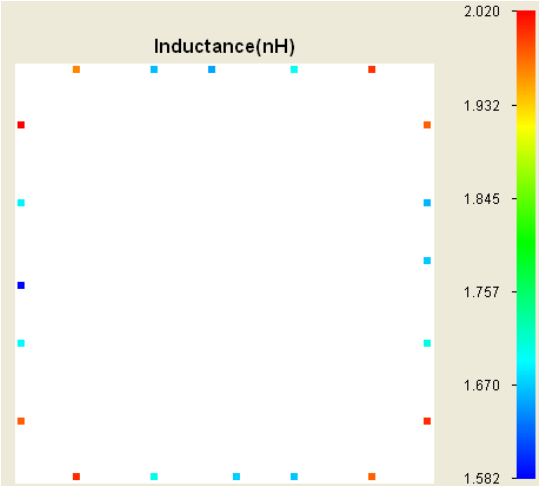
Power Net	Ref Ground Net	Min L(nH)
VDD_1	VSS	0.458915
VDD_2	VSS	0.459036
VDD_3	VSS	0.454683
VDD_4	VSS	0.453262
VDDcore	VSS	0.20675

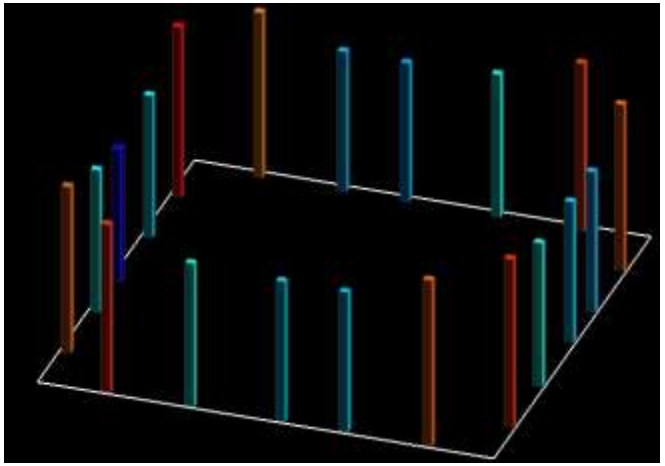
Note:

1. 该功能通过各电源Net与参考地Net之间的环路电感（Loop L）的大小来评估电源Net的设计性能

电性能评估4：电源地网络各个管脚的电阻和电感

Net	Pin NodeName	Self L(nH)	Total L(nH)	R(mOhm)
VDDcore	Node118!!U1-112::VDDcore	1.99973	4.3085	77.1796
VDD_1	Node120!!U1-136::VDDcore	1.70344	3.81504	63.2961
VDD_2	Node122!!U1-162::VDDcore	1.6711	3.80332	59.611
VDD_3	Node124!!U1-180::VDDcore	1.66677	3.75291	63.6274
VDD_4	Node126!!U1-204::VDDcore	1.97828	4.24882	77.2378
VSS	Node88!!U1-217::VDDcore	1.99949	4.28723	77.1914
	Node90!!U1-241::VDDcore	1.70398	3.80692	63.3361
	Node92!!U1-267::VDDcore	1.66812	3.7974	59.4338





Note：

1. 该功能通过电源/地各管脚的电阻和电感大小来评估电源Net的设计性能

性能基准
IBIS/SPICE模型提取

- XtractIM运行于上一代的 workstation
  - **32-bit 3.0GHz Pentium-class CPU，2Gb内存**

Package	Pin #	Net #	Layer #	Via #	Trace #	Memory (MB)	Simulation Time
Wirebond 1	182	179	4	462	1,611	524	2min 52s
Wirebond 2	369	201	4	1,047	4,608	132	7min 27s
Wirebond 5	484	351	4	1468	5238	715	13min 8s
Wirebond 3	665	400	6	1,565	7,831	500	13min 31s
Wirebond 4	703	545	8	4,273	7,820	385	24min 3s
Flip-Chip 1	140	48	6	1,130	698	488	3min 13s
Flip-Chip 2	269	178	4	4,139	3,325	606	15min 33s
Flip-Chip 3	523	310	8	11,163	6,033	603	30min 46s
Flip-Chip 4	502	130	12	18,129	8,042	1,055	30 min 44 s
Flip-Chip 5	931	610	8	15,563	15,647	1,158	1hr 27 min 50s

性能基准
IBIS/SPICE模型提取

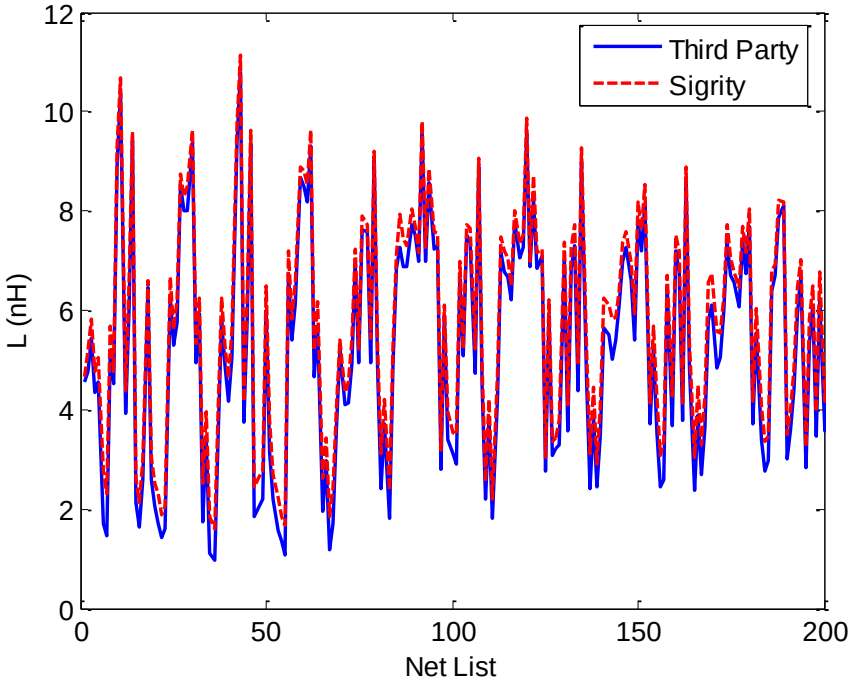
- XtractIM运行于当前的workstation
  - 64-bit 3.2GHz X86/64 class CPU，8Gb内存

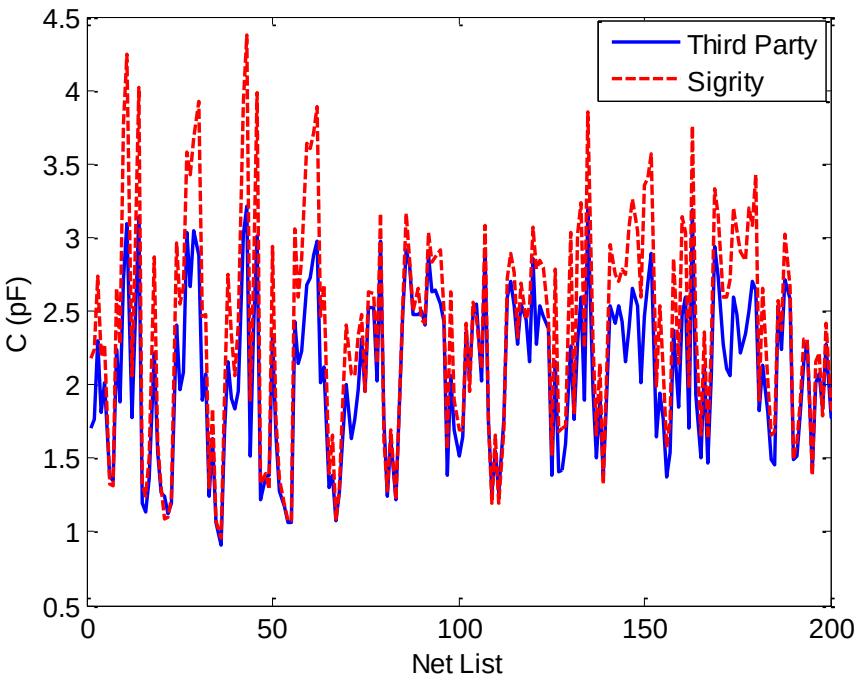
Package	Pin #	Net #	Layer #	Via #	Trace #	Memory (MB)	Simulation Time
Flip-Chip 7	885	519	12	20,206	15,318	1,590	1 hr 9 min 55s
Flip-Chip 8	1760	1261	8	34,233	32,903	3,809	6 hr 42 min

- 对于Flip-Chip 8，目前市面上的其他工具最快也需要仿真3天
  - XtractIM的速度整整快了一个数量级!
  - 对于一些比较大型的IC封装，其速度比其他工具快了20X，40X甚至更多。

精度基准

200个net 的LC提取结果：XtractIM Vs 第3方工具



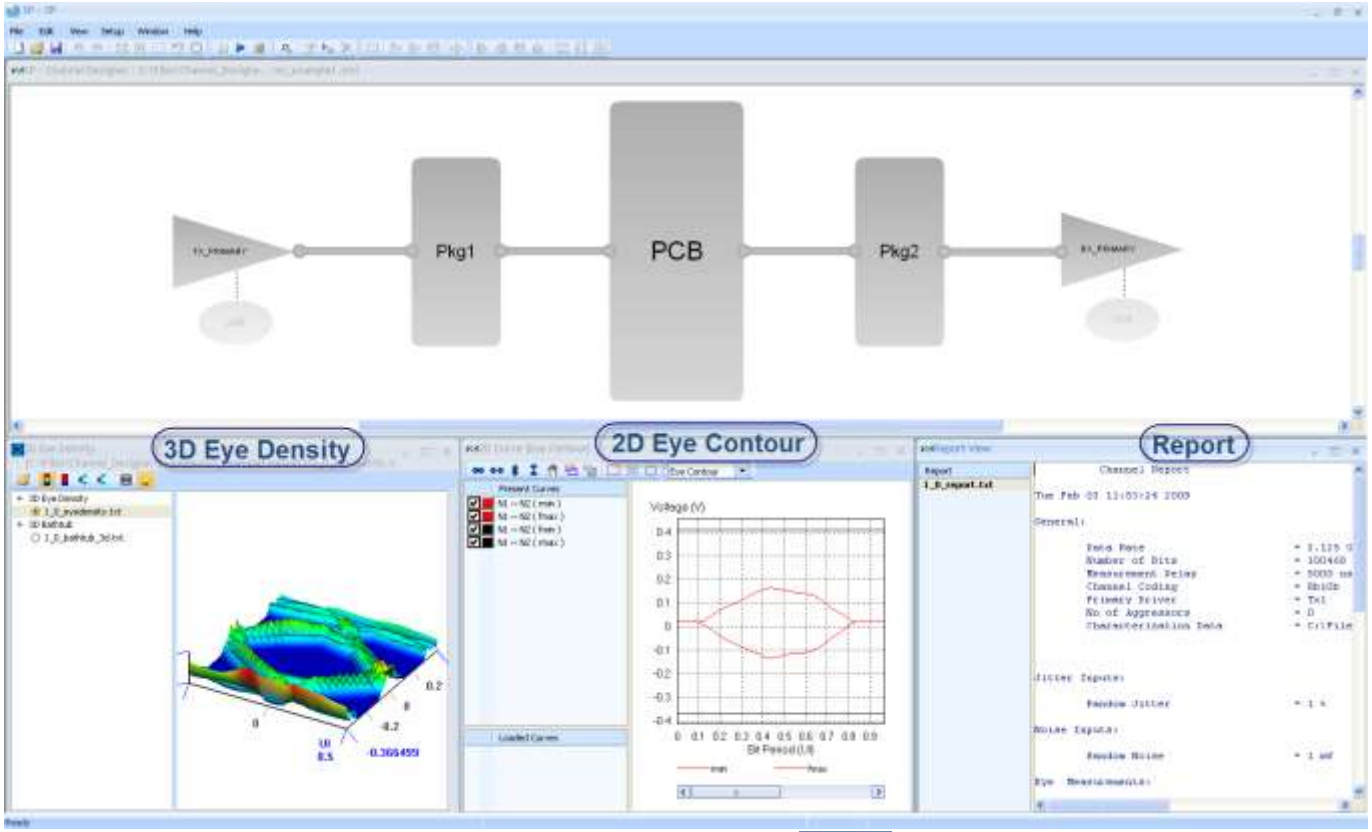


NOTE: *第3方工具忽略了PCB-package接头附近的电容效应，而XtractIM却准确的建模了这种效应！*

高速串行互连分析：Channel Designer

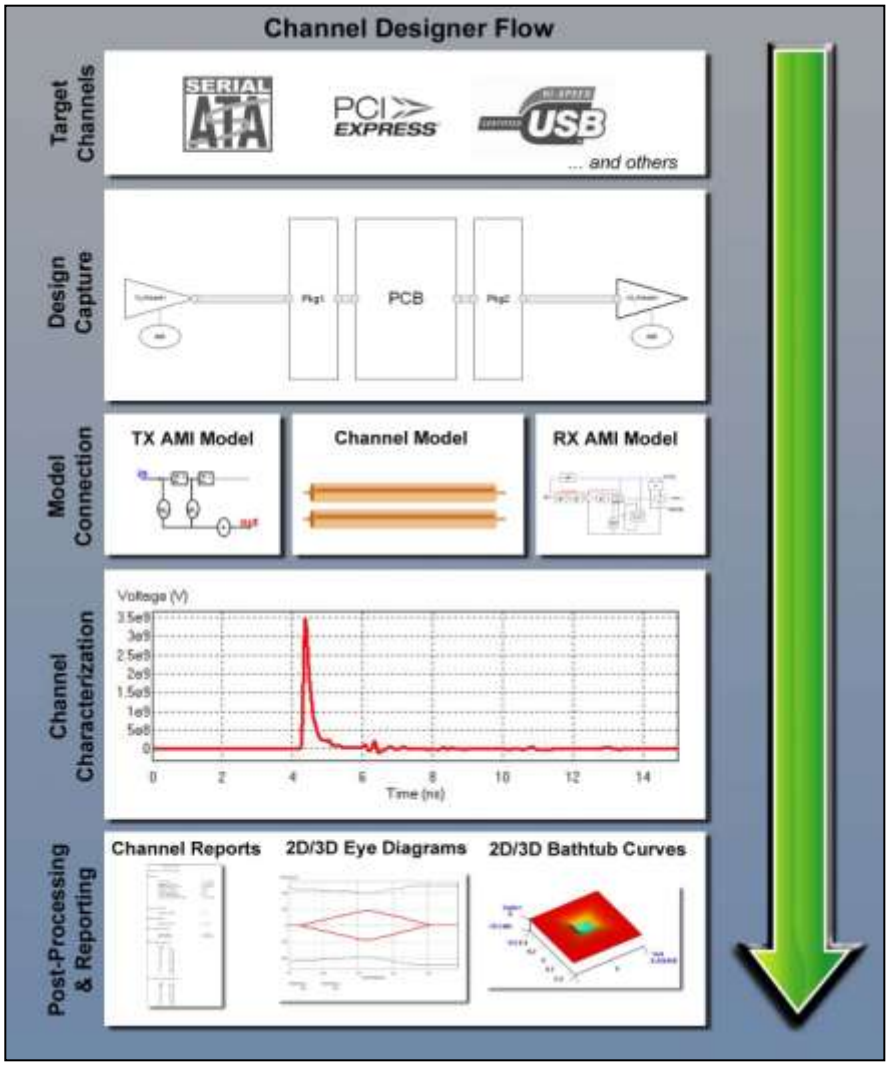
Sigrity 高速串行通道分析工具
Channel Designer

- Channel Designer 提供了一个精确评定高速串行互连通道的综合环境以确保芯片，封装和PCB设计能够实现设计目标

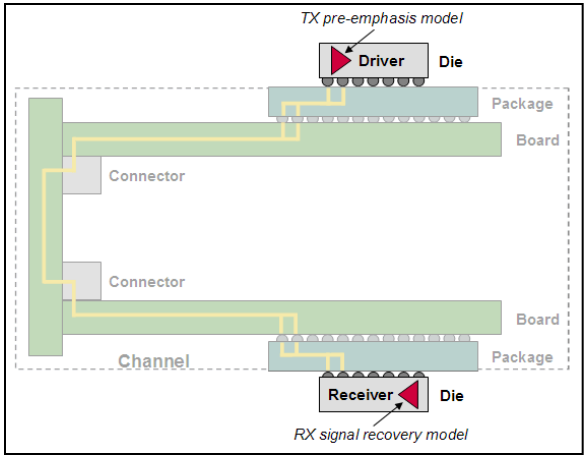


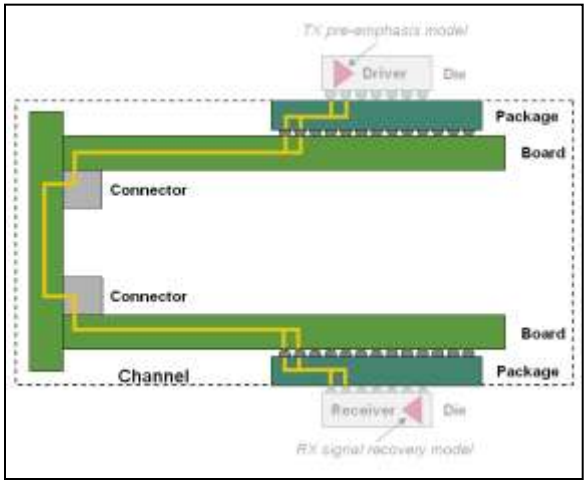
高速串行通道分析流程

- 设计目标 Target Channels
  - 高速串行互连标准
- 设计原理图 Design Capture
  - 图形界面
  - 设计模板
  - 解决从简单到复杂的互连通道分析
- 模型互连 Model Connection
  - 算法模型接口 (AMI)支持
  - 从物理设计提取互连通道模型
  - 模型互连协议 (MCP)使得模型互连非常方便
- 互连模型特性 Model Characterization
  - 支持大容量数据码分析
  - 串扰， 抖动和噪声建模分析
  - 支持非理想电源分布分析
  - S参数模型分析
  - 参数扫描分析
- 后处理与分析报告 Post processing & Reporting
  - 互连通道分析报告
  - 2D / 3D 眼图与统计浴盆曲线



高速串行通道分析
灵活的设计评定





发送接收器件模型

- 在设计中首先用IC厂家模型取代缺省通用模型
- 完全支持IBIS AMI 标准
- 不同厂家模型的支持

互连器件

- 设计模板支持前期评定
- S参数模型支持
- 采用不同互连结构的假定分析以决定互连方案

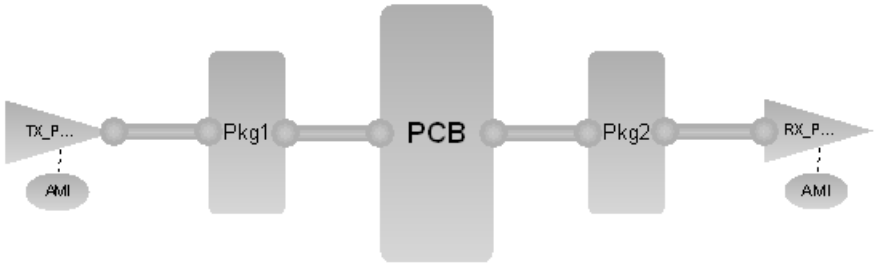
Sigrity 高速串行通道分析

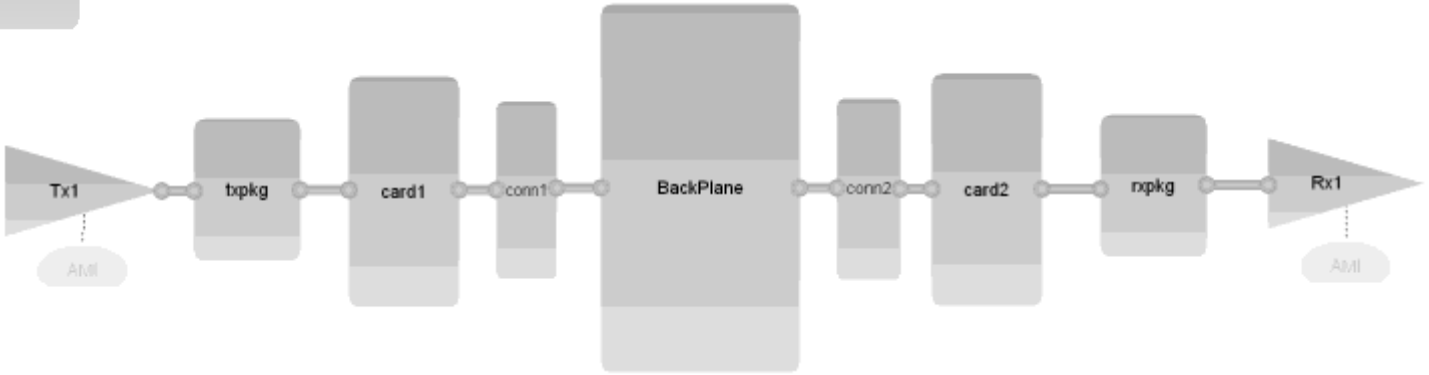
Key Advantages

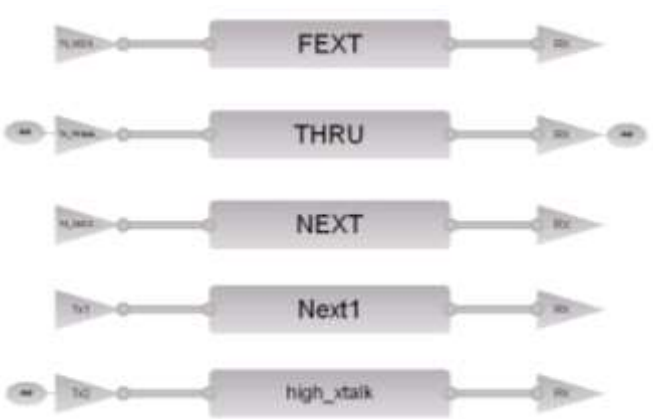
- 易用的模块化的拓扑编辑
- SPICE子电路形式的模型
  - Native IBIS, HSPICE, Touchstone, BNP syntax
- 独一无二的集成频域，时域与统计分析的技术
  - 频域响应与S参数分析
  - S参数模型与通道特性的时域分析
  - 大容量数据码的分析
  - 误码率分析
- 先进的串扰与抖动分析技术
- 能够考虑非理想电源分析
- 灵活的参数扫描分析
- 领先的AMI模型技术支持
- 高速串行传输工业标准的设计包接口

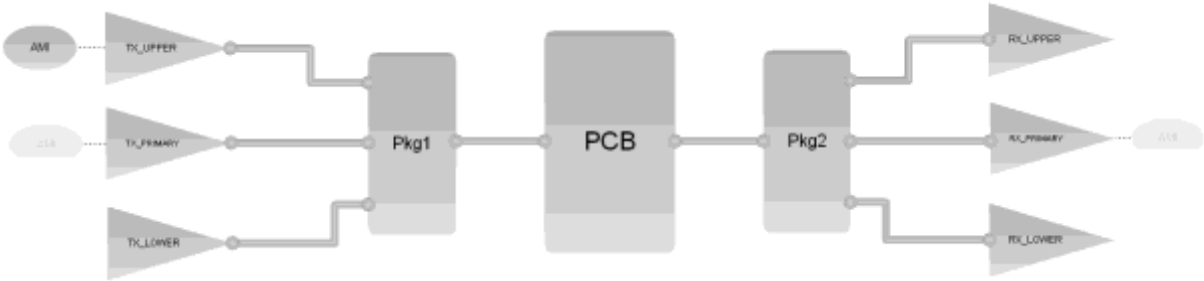
Channel Designer 设计模板

帮助进行前期评估

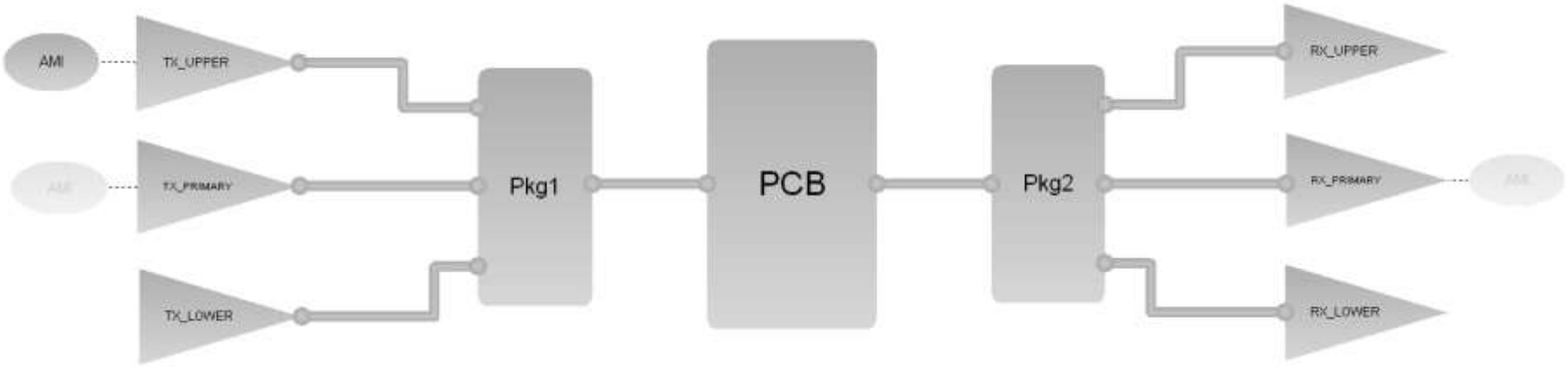






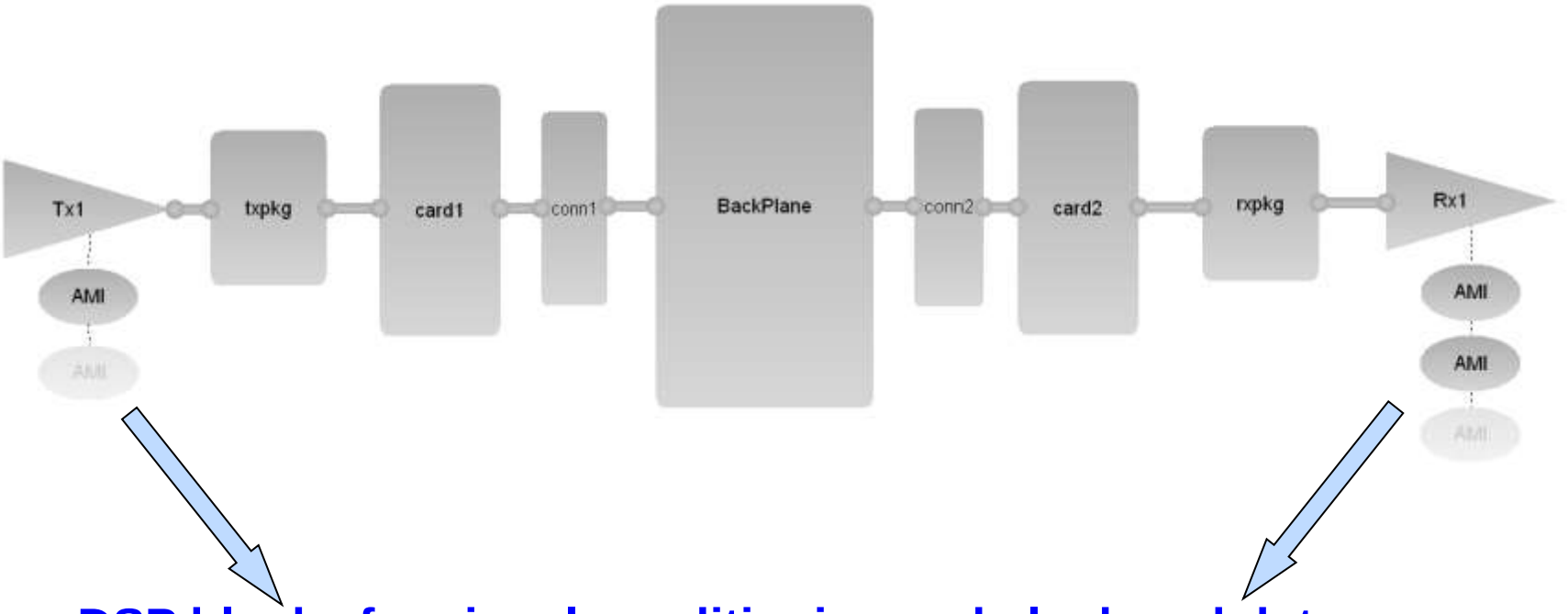


串扰通道建模



* 时域仿真
* 串扰通道的发送端可以用不同器件
* 串扰通道的发送端可以用不同激励
* 偶模，奇模， 随机码与统计分析四种串扰分析模式

完全支持IBIS AMI模型



DSP blocks for signal conditioning and clock and data recovery

Cascaded AMI → Allows flexible Modeling and debug

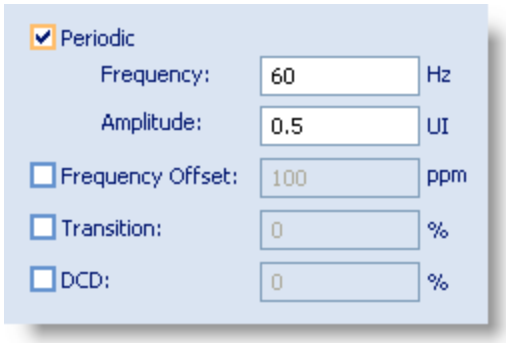
Example: cascade equalizer model with stand alone CDR

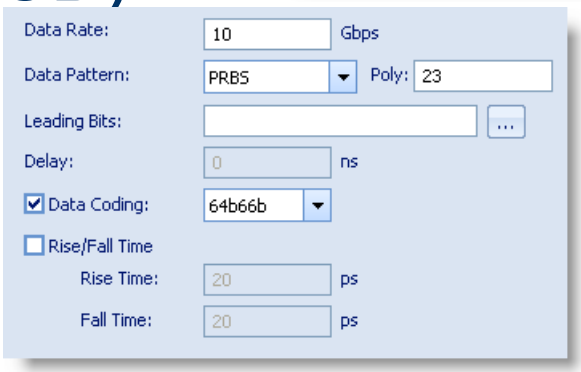
Sigrity工具提供的AMI模型

- Amicdr2
  - Stand alone CDR
- Amiffe
  - Feed forward filter model; tap optimization
- Amictf
  - Analog filter model
- Amidfe
  - DFE with blind adaptation
- Amidfenl
  - DFE with look ahead equalizer

全面的抖动/噪声分析

- Random jitter/noise
- Tx edge jitter/noise
- Periodic jitter/noise
- Frequency offset
- Duty Cycle Distortion (DCD)

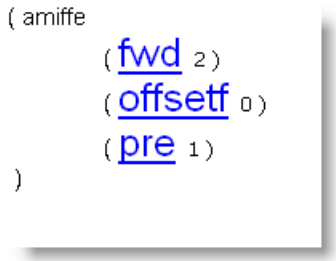




Jitter/Noise at Rx (post processing) and at Tx input (time domain simulation)

灵活的参数扫描分析

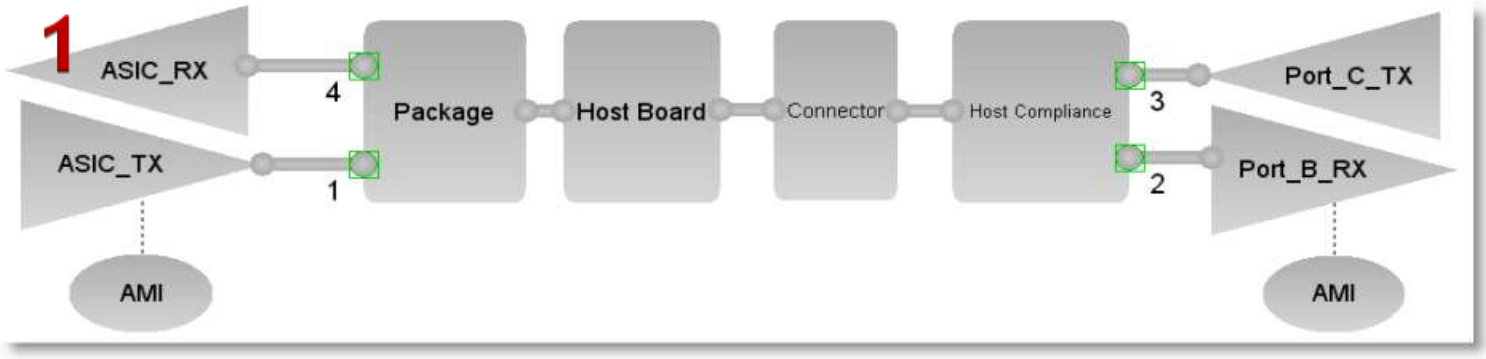
- Channel Designer可以扫描下列参数，使得假定分析更加快速:
  - Jitter/Noise settings
  - Equalization parameters
  - Various channel component models: connectors, cables, packages, boards, …etc
  - Subcircuit parameters such as die cap, R and Tx drive level

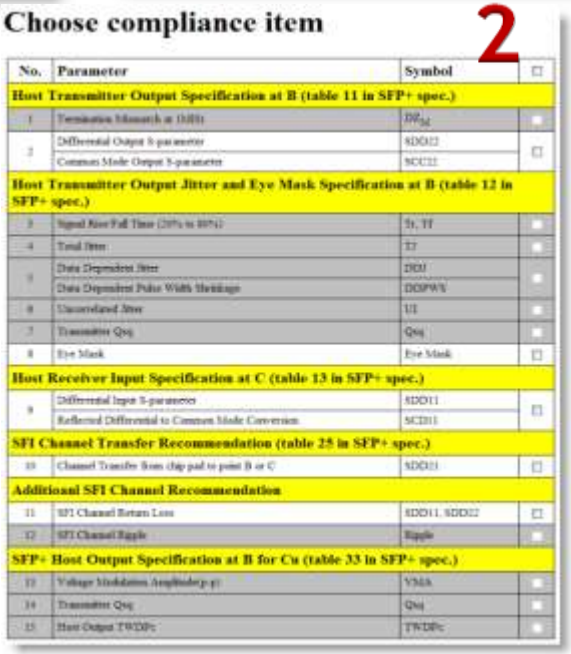


Parameter	Value	Circuit File	Line
nmos_imp	25	C:\Sigrity_Fil...	1
tx_rt	50	C:\Sigrity_Fil...	1
tx_c_comp	1p	C:\Sigrity_Fil...	1
tx_scale	1	C:\Sigrity_Fil...	1

Property	Value
Number of Bits	100000
Bit Sampling Rate	32
Random Jitter (Rj) (%)	0.88
Deterministic Jitter (Dj) (%)	0
Random Noise (Rn) (mV)	1
Deterministic Noise (Dn) (mV)	0
Data Rate (Gbps)	10
Delay (ns)	0
Periodic Jitter Frequency (Hz)	1.0238e+008
Periodic Jitter Amplitude (UI)	0.043
Periodic Noise Frequency (Hz)	60
Periodic Noise Amplitude (mV)	5
Transition Jitter (%)	0
Transition Noise (mV)	0.1
DCD (%)	0.67

高速串行传输工业标准的设计包接口





设计报告

SFP+ Compliance Report

Generated by Sigrity Channel Designer, 9.0.4.10211
27th of October 2009

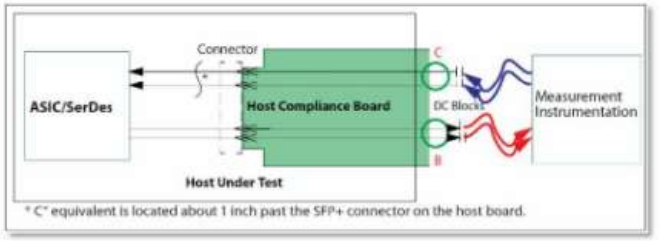


Figure 1: Host Compliance Board

Summary of Results

This report shows the results of the SFP+ compliance testing using Sigrity Channel Designer.

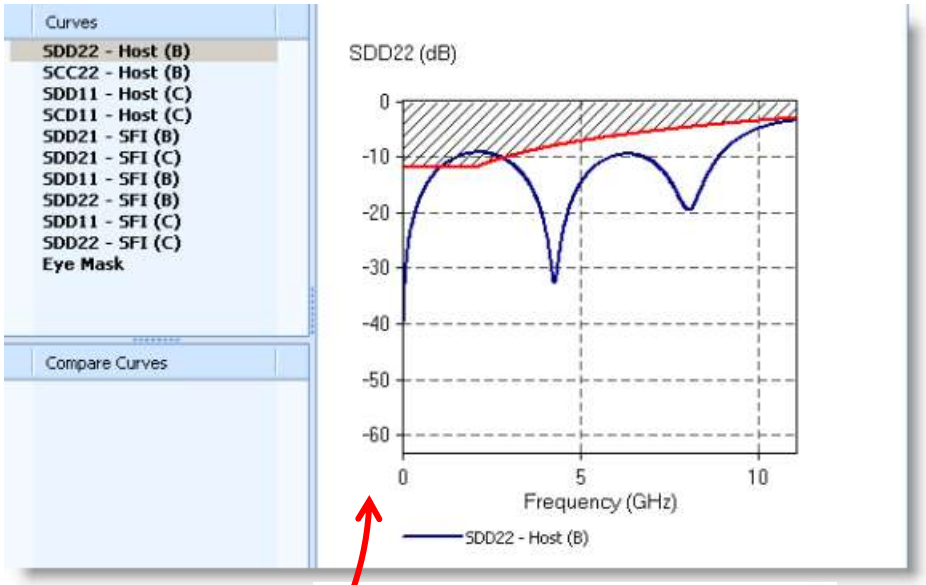
The channel simulated violates one or more SFP+ compliance requirements.

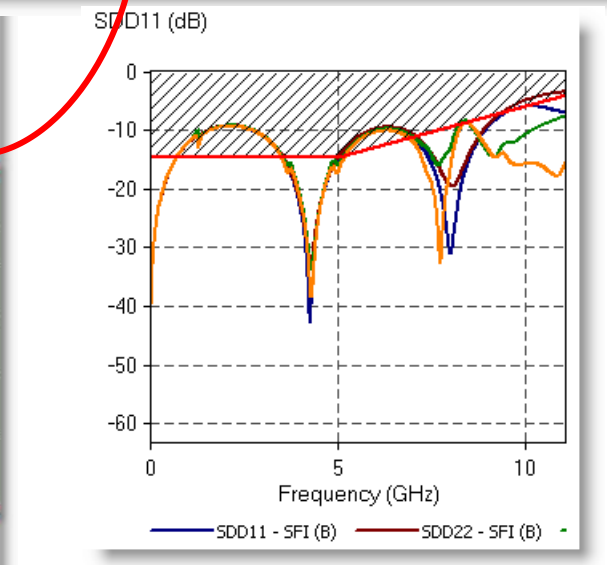
Host Transmitter Output Electrical Specifications at B

Parameter - B	Symbol	Conditions*	Min	Max	Units	Simulation Results	Pass/Fail
Termination Mismatch at 1 MHz	ΔZ_M	See D.16, Figure 55		5	%		
Single Ended Output Voltage Range			-0.3	4.0	V	N/A	N/A
Output AC Common Mode Voltage		See D.15		15	mV (RMS)	N/A	N/A
Differential Output S-parameter	SDD22	0.01 to 2 GHz		-12	dB	SDD22	Fail
		2 to 11.1 GHz		see 1	dB		
Common Mode Output S-parameter	SCC22	0.01 to 2.5 GHz		see 2	dB	SCC22	Fail
		2.5 to 11.1 GHz		-3	dB		

1. Reflection coefficient given by equation SDD22(dB) < -6.68 + 12.1* log10(f/5.5), with f in GHz.
2. Reflection coefficient given by equation SCC22(dB) < -7 + 1.6*f, with f in GHz

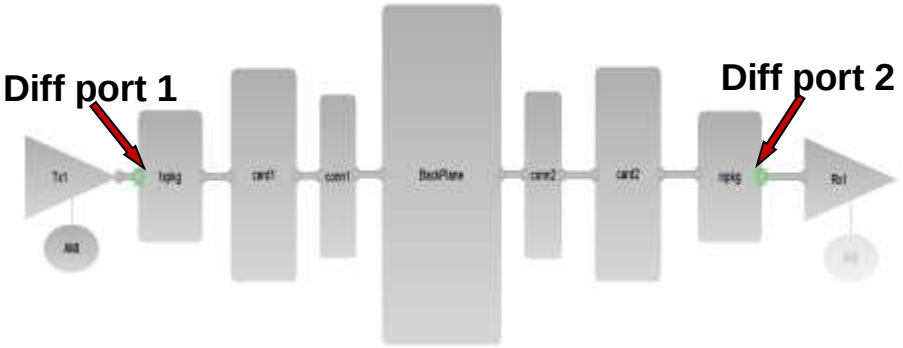
* Refer to SFF-8431 Rev4 specification



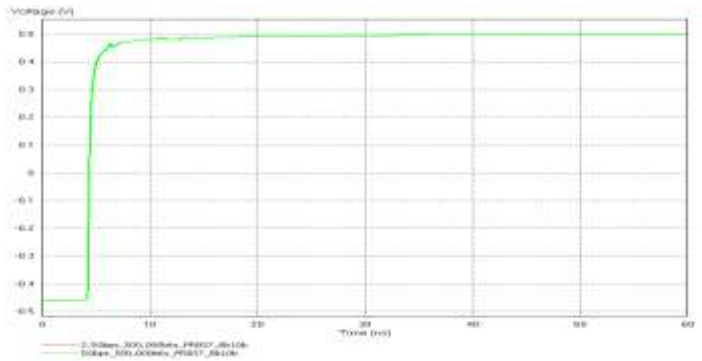


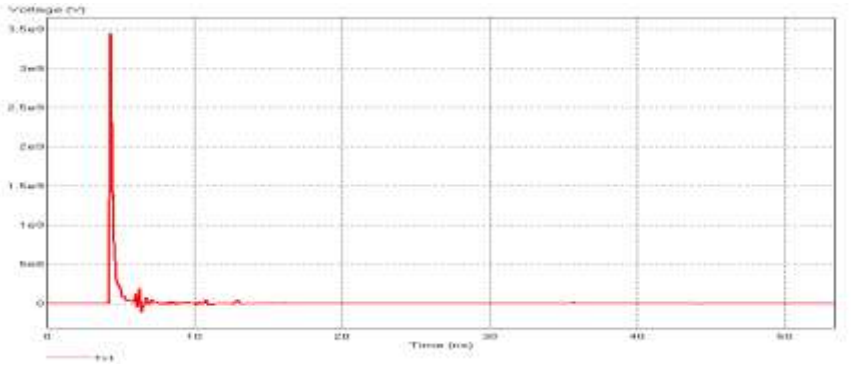
通道特性分析

- S参数分析



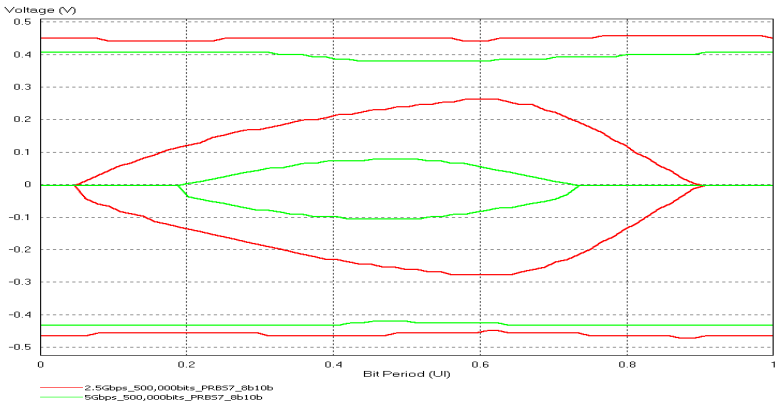
- 阶跃/脉冲响应

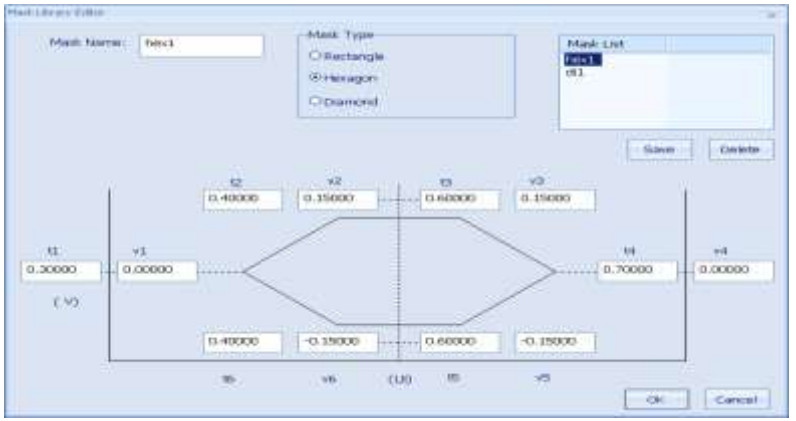




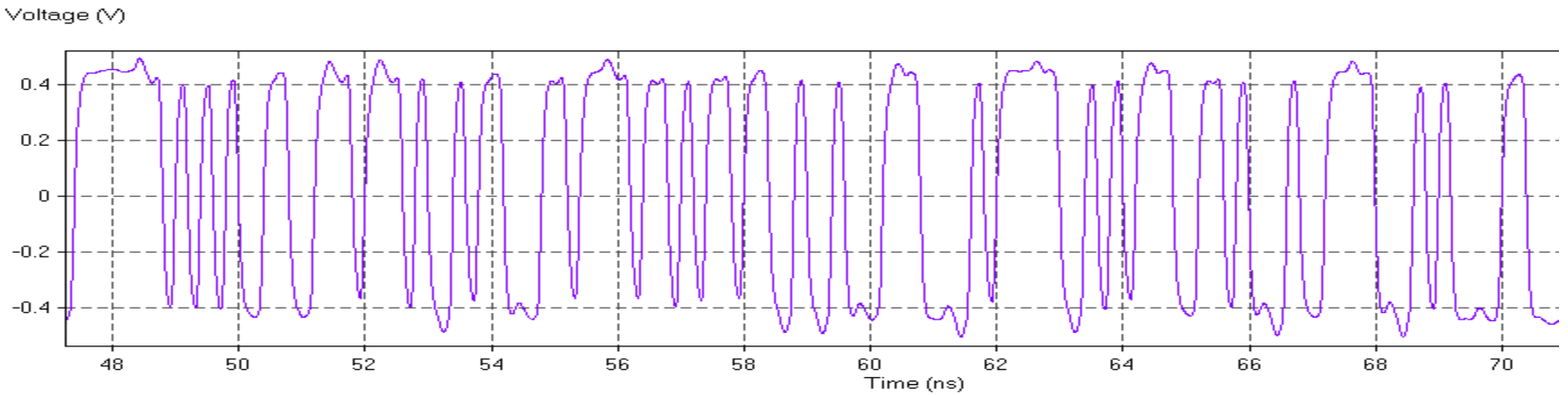
时域分析

- 眼图轮廓/眼图模板



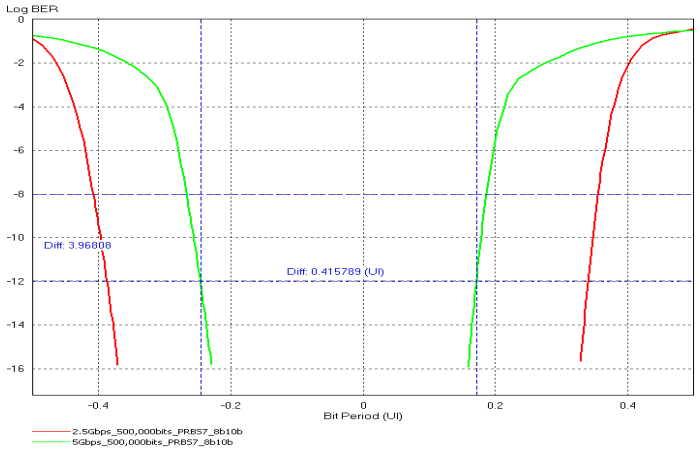


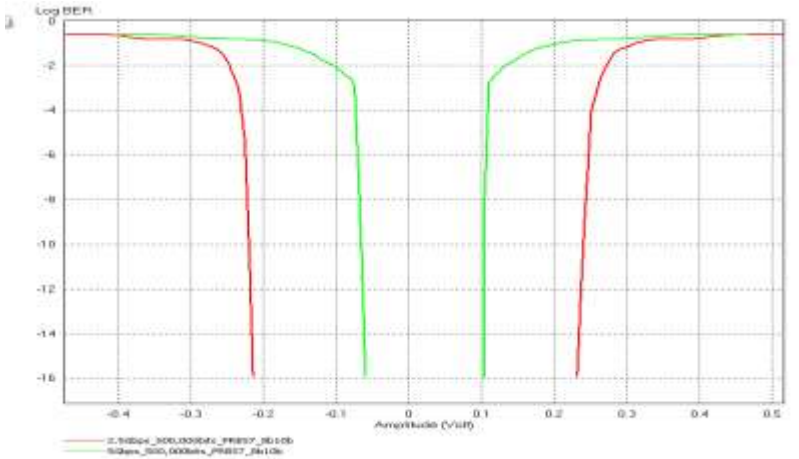
- RX 波形



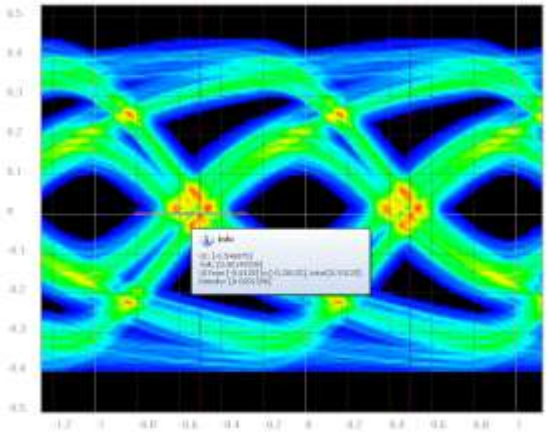
统计分析

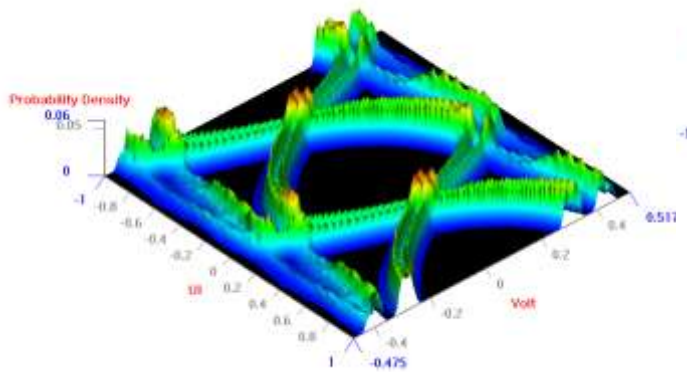
- 误码率/噪声 浴盆曲线

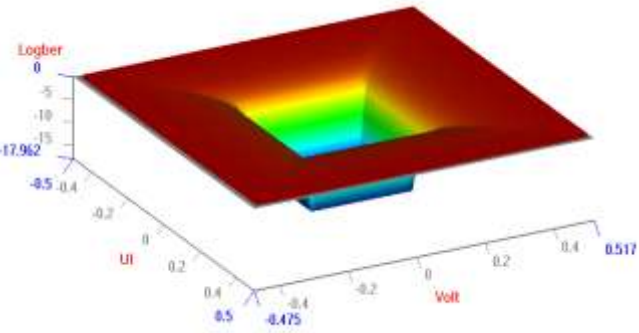




- 眼图， 3D眼图密度分布， 3D 浴盆曲线





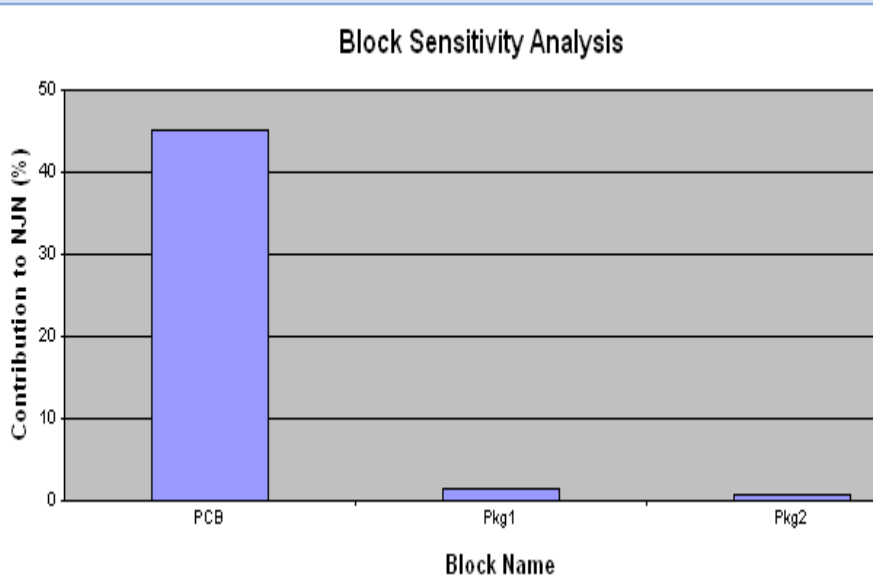


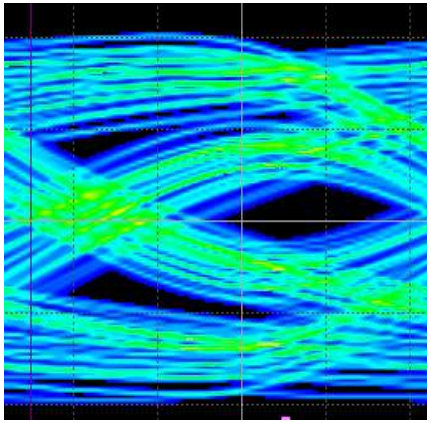
模块敏感度分析

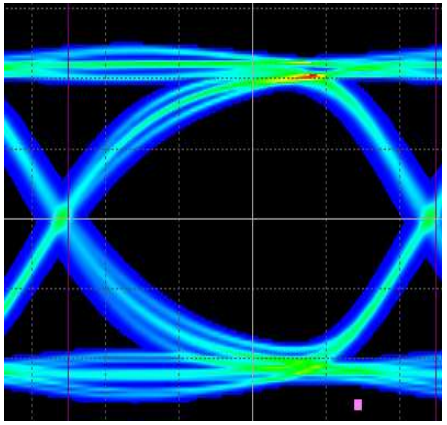
Block Sensitivity Result:

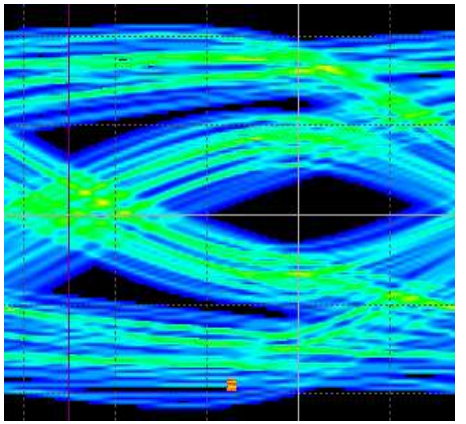
Export... Show Result...

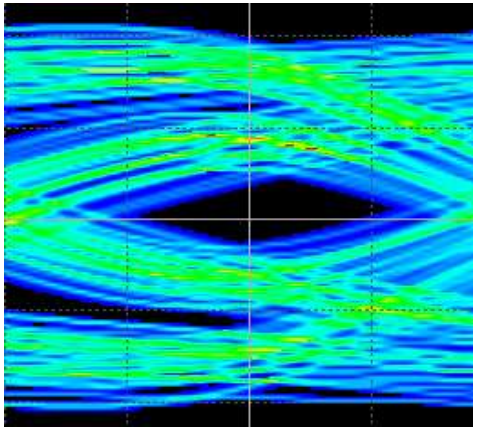
Iteration	Block Shorted	NJN	NJN Contribution (%)
1	**no block shorted**	0.9450181412224392	
2	**PCB**	0.5179835740583404	**45.19**
3	**Pkg1**	0.9304569968776610	**1.54**
4	**Pkg2**	0.9381848833942119	**0.72**











分析报告

Channel Report

Thu Jul 30 17:35:10 2009

General:

Data Rate	= 2.5 Gbps
Number of Bits	= 500417
Measurement Delay	= 5000 nsec
Channel Coding	= 8b10b
Primary Driver	= Tx1
Data Pattern	= random
No of Aggressors	= 0
Characterization Data	= C:\Sigrity_Files\D620\Channel_Designer\Demo\single1\result\1\channel1_rx.cur

Jitter Inputs:

Random Jitter	= 1 %

Noise Inputs:

Random Noise	= 1 mV

Eye Measurements:

Eye height	= 499 mV
Eye Jitter	= 0.14 UI
Eye Norm Jitter and Noise (NJN)	= 0.68

BER Measurements:

LBER	UI
-16	0.69
-15	0.70
-14	0.71
-13	0.71
-12	0.72
-11	0.73
-10	0.74
-9	0.75
-8	0.76
-7	0.77
-6	0.78
-5	0.79
-4	0.81
-3	0.83

Volt BER Measurements:

总结

Sigrity 一直致力于解决高速串行传输分析的挑战

- Sigrity业界领先的模型提取技术提供了串行互连通道建模的基础， 并且可以建立非理想电源分布的模型
- 业界领先的算法模型技术知识使得您可以应用前沿的高速器件进行您的设计
- 频域，时域和统计分析技术的结合进行高速的串行互连传输的分析
- 简单灵活的界面和与高速串行传输工业标准的设计包接口提高设计效率

Thank You!