MOSFET S)-(D 17V Channel-N Dual

DESCRIPTION GENERAL

power mode enhancement logic Channel-N Dual the is 9926A The DMOS density, cell high using produced are transistors effect field to tailored especially is process density high This technology. trench suited particularly are devices These resistance. state-on minimize notebook and phone cellular as such application voltage low for circuits powered battery other and management power computer very a in needed are loss power line-in low and switching where package. mount surface outline small

FEATURES

- $R_{DS(ON)} \leqq 29m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 42m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

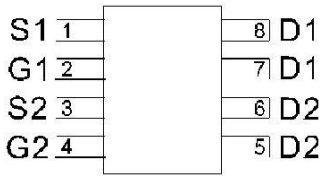
APPLICATIONS

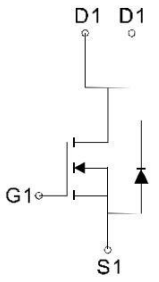
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

CONFIGURATION PIN

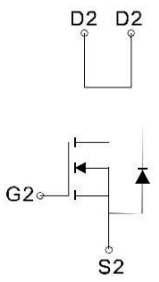
(SOP-8)

View Top





N-Channel MOSFET



N-Channel MOSFET

Noted) Otherwise Unless ℃=25A(T **Ratings Maximum Absolute**

Parameter		Symbol	10sec		SteadyState		Unit
Voltage Source-Drain		DSSV	17				V
Voltage Source-Gate		GSSV	±8				V
*Current Drain Continuous	℃=25AT	DI	6.6		5.2		A
	℃=70AT		5.2		4.2		
Current Drain Pulsed		DMI	30				A
*Dissipation Power Maximum	℃=25AT	DP	2.0		1.25		W
	℃=70AT		1.2		0.8		
Temperature Junction Operating		JT	150 to 55-				℃
*Ambient to Junction-Resistance Thermal		θJAR	Typ	45	Typ	80	℃/W
			Max	62.5	Max	100	

1in on mounted device The * The ^{2}copper oz 2 with board FR4

MOSFET S)-(D 17V Channel-N Dual

Specified) Otherwise Unless ℃=25 A(T **Characteristics Electrical**

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
DSSBV	Voltage Breakdown Source-Drain	A μ =250DI 0,GS=V	17			V
GS(th)V	Voltage Threshold Gate	A μ =250DI ,GS=VDSV	0.4		1.2	V
GSSI	Leakage Body Gate	=±8VGSV =0V,DSV			±100	nA
DSSI	Current Drain Voltage Gate Zero	=0VGSV =17V,DSV			1	A μ
DS(ON)R	Resistance-On Source-Drain	=4.5V,GSV 6.0A =DI			29	Ωm
		=2.5V,GSV 5.2A =DI			42	
SDV	Voltage Forward Diode	=0VGSV =1.7A,SI			1.2	V
DYNAMIC						
Qg	Charge Gate Total	=6.0ADI =4.5V,GSV =10V,DSV		8		nC
Qgs	Charge Source-Gate			2.1		
Qgd	Charge Drain-Gate			2.3		
d(on)t	Time Delay On-Turn	=4.5VGENV =1.0A,D=10V,IDDV Ω=6GR		14		ns
rt	Time Rise On-Turn			17		
d(off)t	Time Delay Off-Turn			43		
ft	Time Fall Off-Turn			5		
Ciss	capacitance Input	f=1.0MHz =0V,GSV =15V,DSV		550		pF
Coss	Capacitance Output			130		
Crss	Capacitance Transfer Reverse			40		

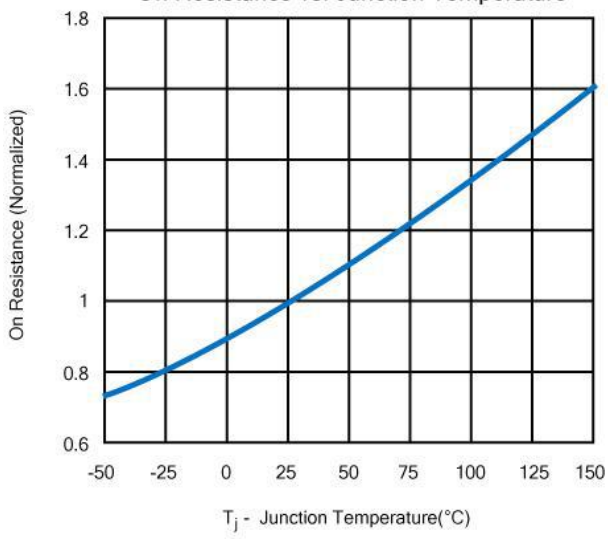
testing. production to subject not design, by 2%,Guaranteed ≦cycle duty 300us, ≦width pulse test: Pulse a. Notes:

notice. without reliability and functions design, product improve to right the reserves b.suchtech

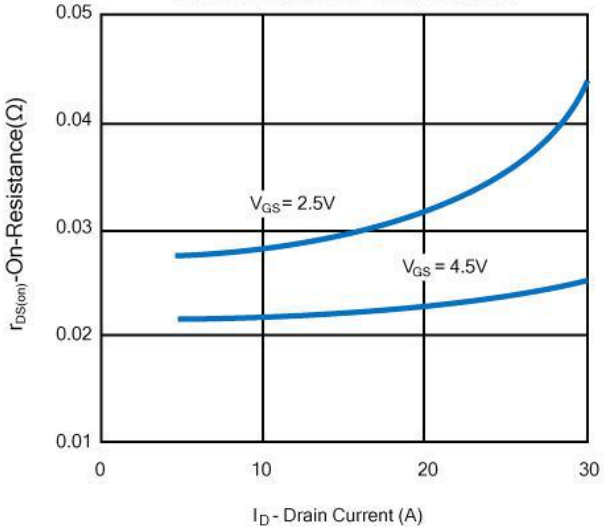
MOSFET S)-(D 17V Channel-N Dual

Noted) ℃=25 J(T Characteristics Typical

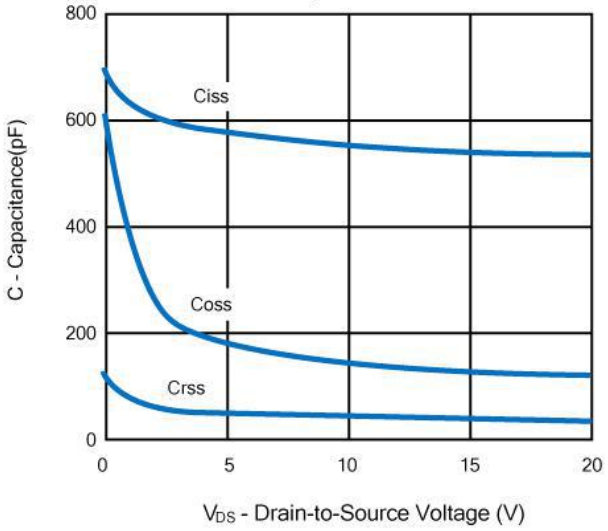
On Resistance vs. Junction Temperature



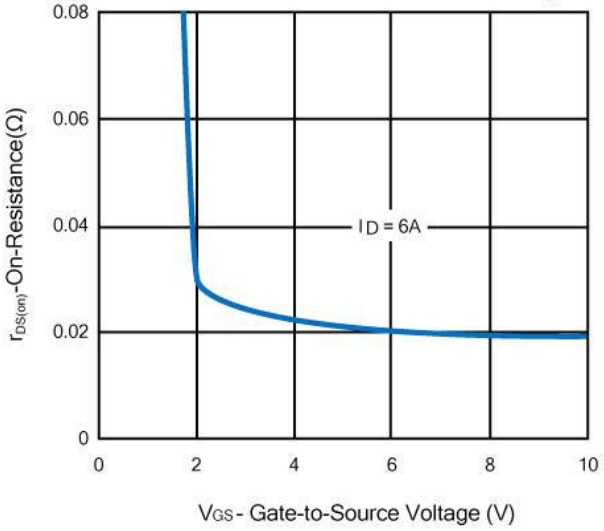
On-Resistance vs. Drain Current



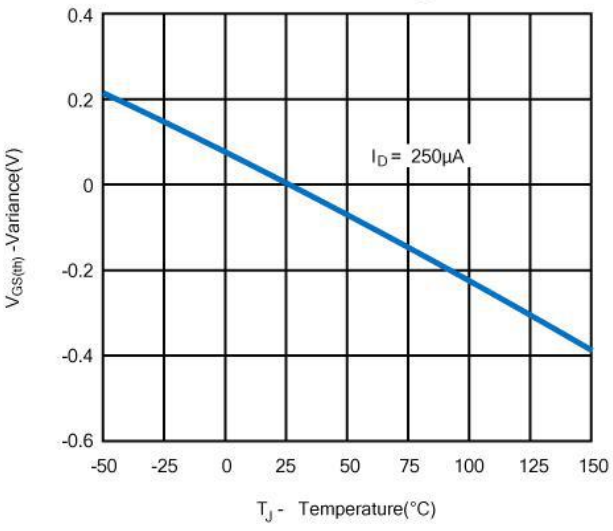
Capacitance



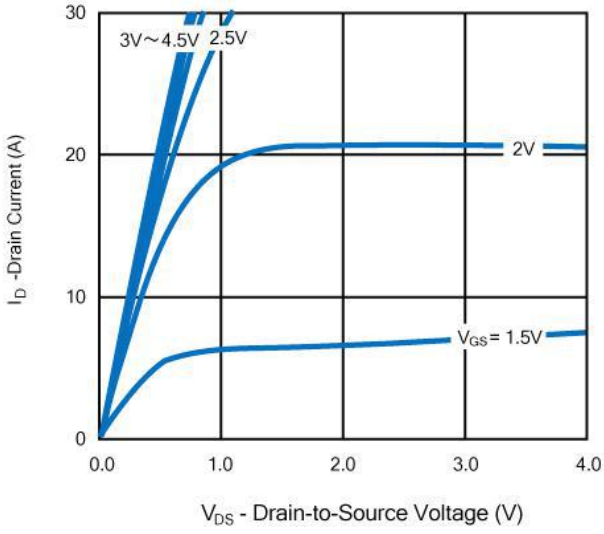
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



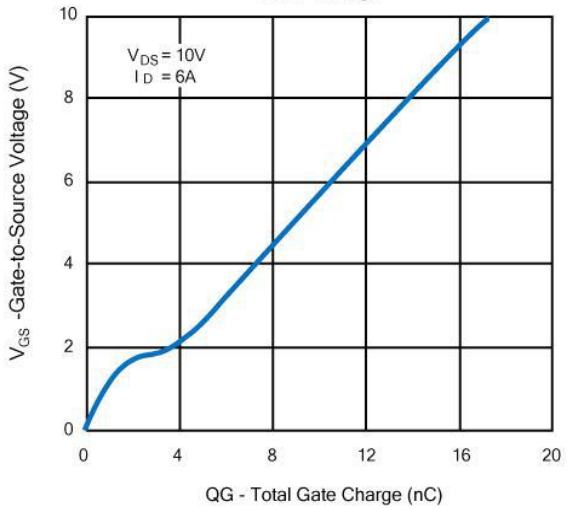
On-Region Characteristics



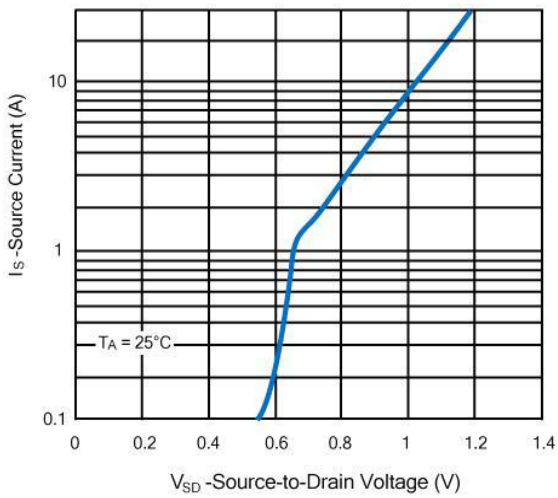
MOSFET S)-(D 17V Channel-N Dual

Noted) ℃=25 J(T Characteristics Typical

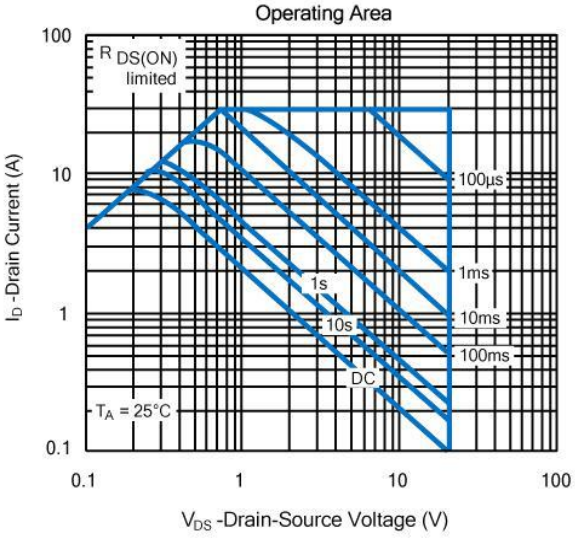
Gate Charge



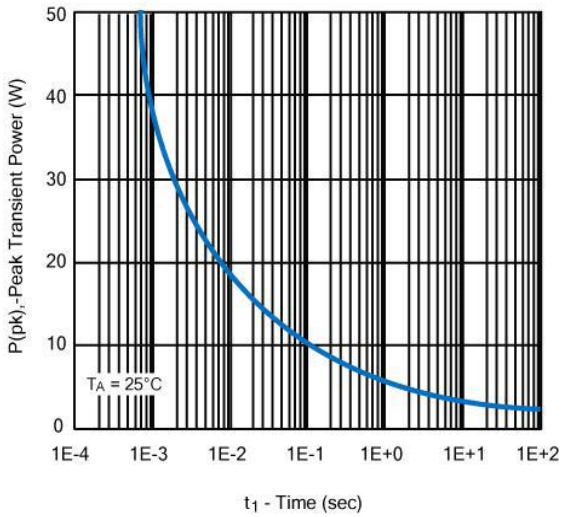
Source to Drain Diode Forward Voltage



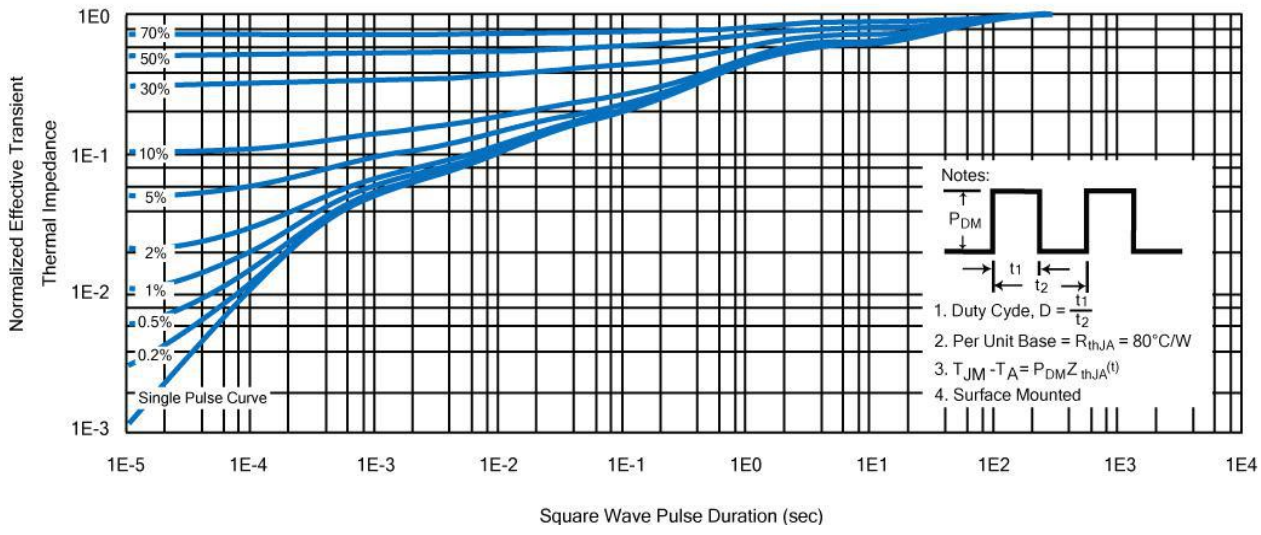
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



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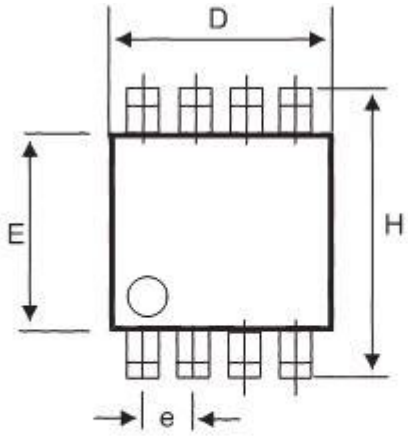
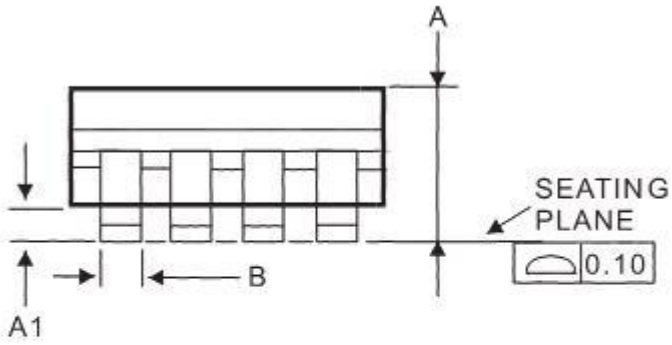
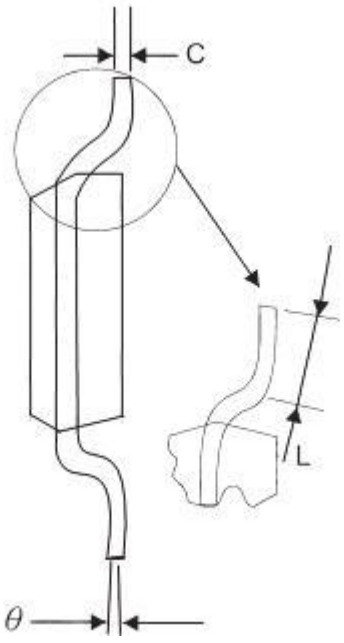
Outline Package 8-SOP







DIM	(mm) MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	BSC 1.27	
H	5.80	6.20
L	0.40	1.25
θ	0°	°7

012AA.-MS JEDEC to Refer 1. NNote:

2. protrusions flash, mold include not does "D"

Dimension not shall burrs gate or protrusions flash,

Mold . burrs gate or side. per mm 0.15 exceed

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