

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

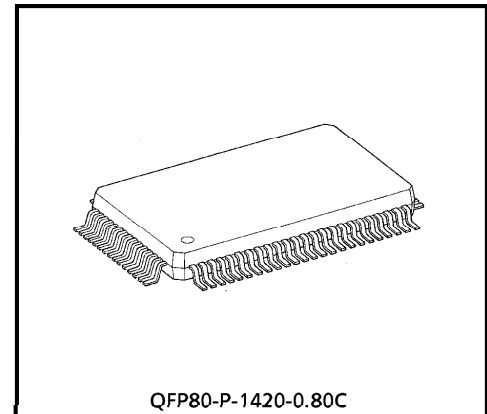
**TD62C805F****48BIT THERMAL HEAD DRIVER**

The TD62805F is a general purpose 48bit driver IC consisting of 8 block 8bit shift register and 48bit drivers (Open Drain).

This device is best suited as a 48 dot thermal printer head drivers.

**FEATURES**

- 8bit parallel input and 6 block 8bit shift register
- CMOS compatible input.
- High driverability . . . 30V / 100mA / ch
- Built in monostable multivibrator for head protection
- 16 steps gray scale operating with 4bit data
- 48bit open drain outputs
- Package . . . . .  $\mu$ PPF-80PIN



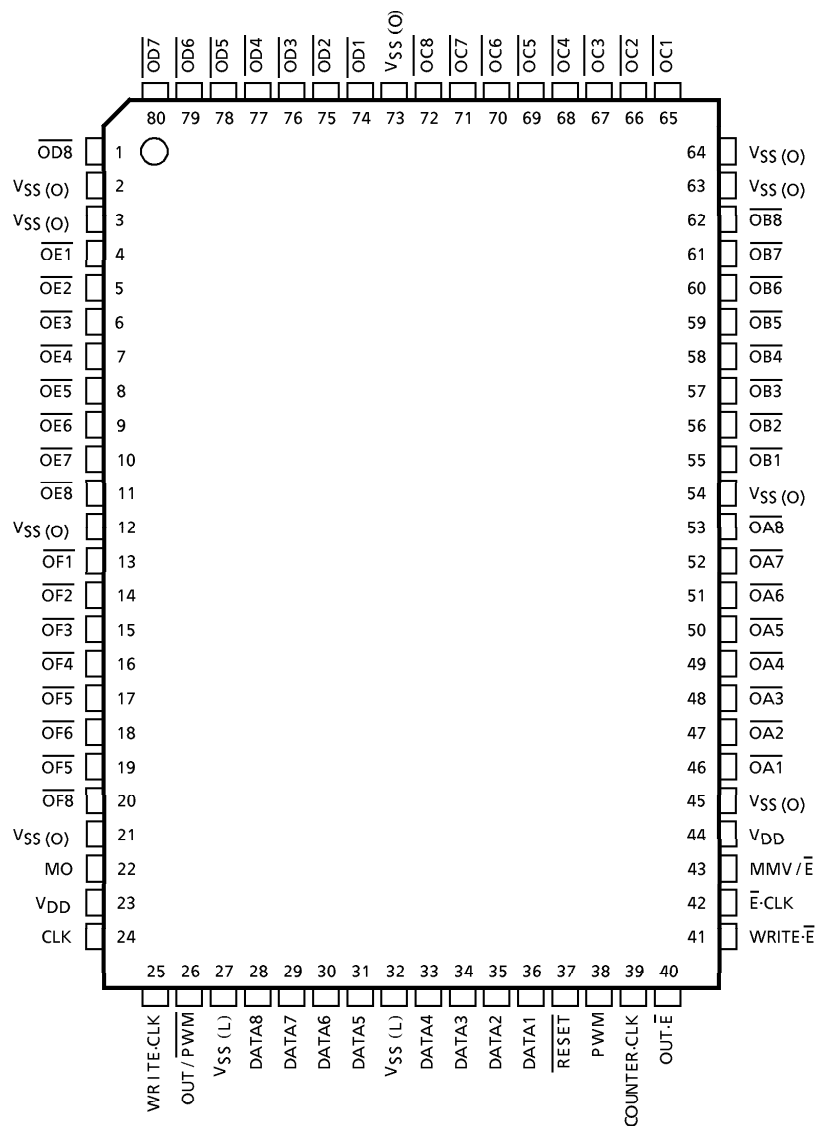
QFP80-P-1420-0.80C

Weight : 1.53g (Typ.)

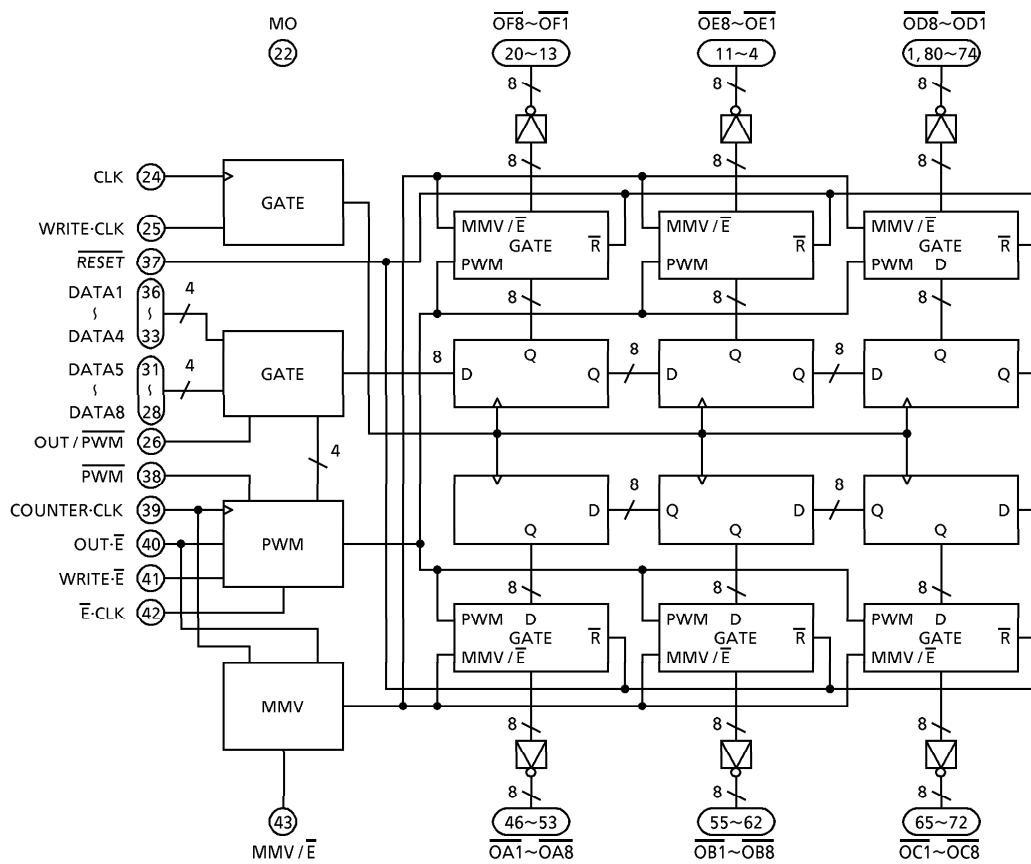
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PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

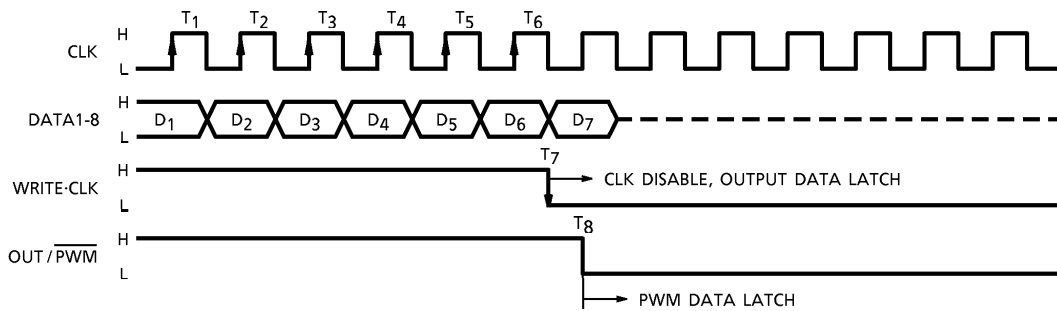


## PIN FUNCTION

PIN No.	PIN NAME	FUNCTION
24	CLK	" $\downarrow$ " : Data shift
25	WRITE-CLK	"H" : enable clock signal, "L" : disable clock signal pull-up input terminal
37	RESET	"L" : all outputs "OFF", reset PWM counter reset PWM counter and MMV circuit Pull-up input terminal
28~36	DATA1~8	Input terminals for output data "H" : output "ON", "L" : output "OFF" And input terminals for PWM data
26	OUT/PWM	"H" : enable output data for shift register "L" : enable PWM data for counter
38	PWM	"L" : output enable (PWM operating)
39	COUNTER-CLOCK	Input terminal for clock of PWM counter and for trigger of MMV
40	OUT·E	"L" : all outputs "ON"
42	E-CLK	" $\downarrow$ " : outputs "OFF" when OUT·E is "High". Outputs "ON" when OUT·E is "Low". Pull-up input terminal
41	WRITE·E	"H" : enable E-CLK signal pull-up input terminal
43	MMV/E	CR connection terminal for MMV
22	MO	ON/OFF monitor terminal of output $\overline{OF8}$
23, 44	V <sub>DD</sub>	Supply voltage terminal for control logic
—	V <sub>SS</sub> (O)	GND terminals for driver PIN No. : 2, 3, 12, 21, 45, 54, 63, 64, 73
27, 32	V <sub>SS</sub> (L)	GND terminals for control logic

(1) Data Input

D<sub>1</sub>~D<sub>6</sub> of Input Dates are entered to shift Register by the clock signal with the timing of rise.  
 Outputs are latched by holding the WRITE·CLK "Low" or to stop the clock signal.  
 PWM Data (DATA1~4) are latched by OUT / PWM signal "Low".

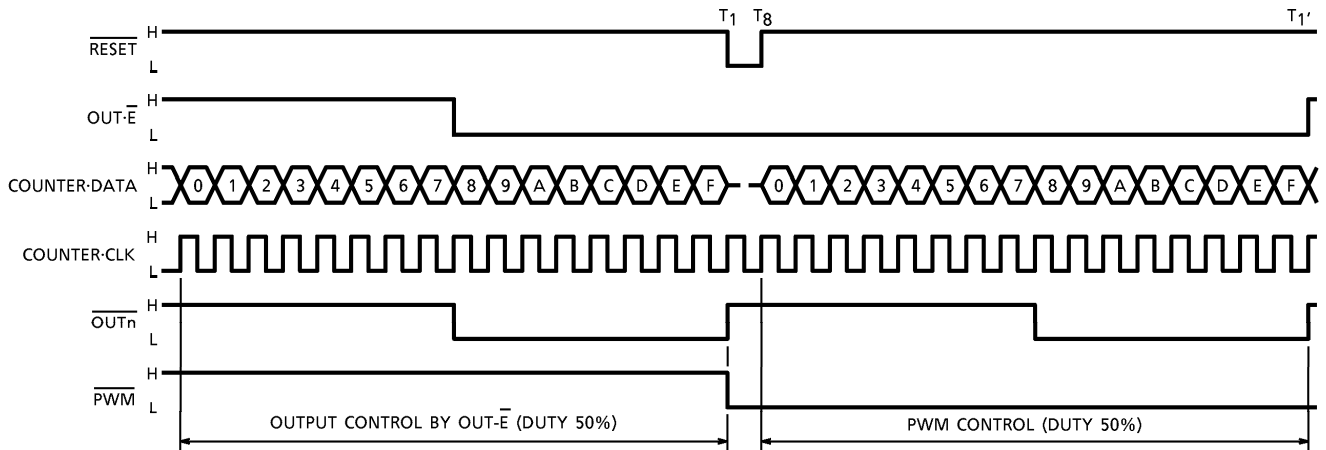


(2) Output Enable

Outputs become "OFF" at the first rising edge of E·CLK after the OUT·E to "High", and become "ON" at the first rising edge of E·CLK after the OUT·E to "Low".  
 Output ON/OFF duty is controlled by controlling OUT·E signal directly or to change the timing of WRITE·E and E·CLK.

(3) PWM Control

Outputs ON / OFF duty are controlled by  $\overline{\text{OUT-E}}$  and PWM DATA of  $D_1 \sim D_4$ . PWM control is performed by comparing the internal 4bit PWM Counter out and PWM DATA of  $D_1 \sim D_4$ . For example, when PWM DATA is 7, 50% Output Duty is obtained. (Refer to tables below.)



PWM DATA	0	1	2	3	4	5	6	7	8	9
Duty (%)	0	6.25	12.50	18.75	25.00	31.25	37.50	43.75	50.00	56.25

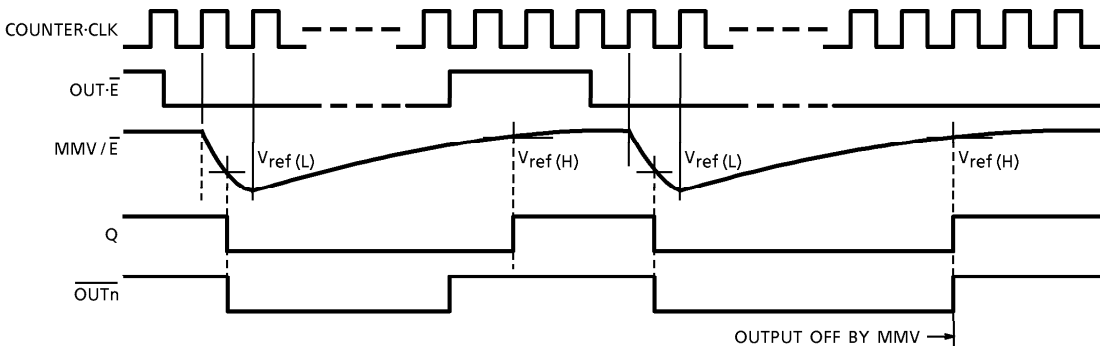
PWM DATA	A	B	C	D	E	F
Duty (%)	62.50	68.75	75.00	81.25	87.50	100.00

**MMV OPERATION**

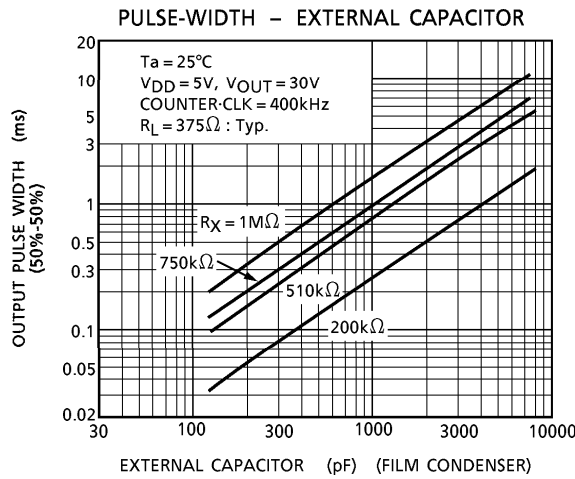
MMV output of Q becomes "L" when the MMV/E voltage becomes less than  $V_{ref(L)}$  after the first rising edge of INTERNAL CLOCK.

And becomes "H" when the MMV/E voltage above  $V_{ref(H)}$  after re-charging of external capacitance connect to MMV/E. The external capacitance and Resistor connect to MMV/E control MMV Output "ON" period.

So Output Load is protected from burn-out. It's required enough discharging time of external capacitance. (Refer to figure below)

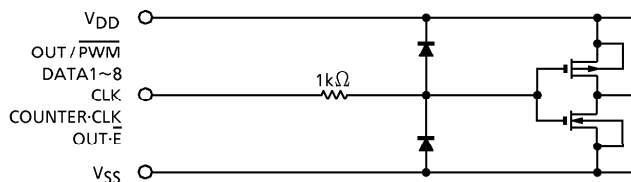


- Pulse width of MMV

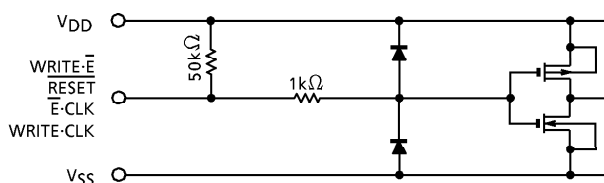


**INPUT CIRCUIT**

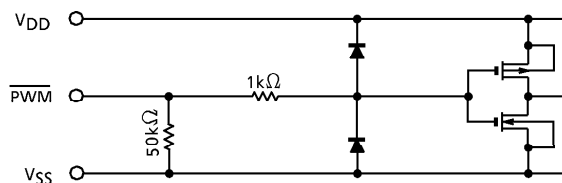
1. DATA1~8, CLK, COUNTER-CLK, OUT/ $\overline{\text{PWM}}$ , OUT $\cdot\overline{\text{E}}$



2.  $\overline{\text{E}}\cdot\text{CLK}$ ,  $\overline{\text{RESET}}$ , WRITE $\cdot\overline{\text{E}}$ , WRITE-CLK

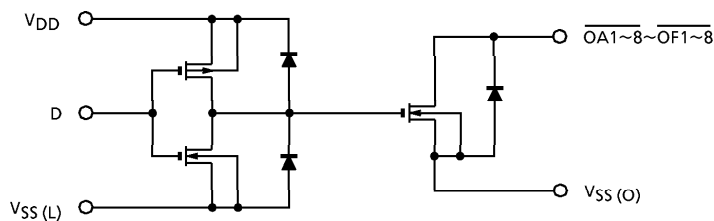


3.  $\overline{\text{PWM}}$



**OUTPUT CIRCUIT**

1.  $\overline{\text{OA}}1\sim\overline{\text{8}}\sim\overline{\text{OF}}1\sim\overline{\text{8}}$





**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	7	V
Output Voltage	V <sub>DS</sub>	30	V
Output Current	I <sub>DS</sub>	100	mA / ch
Input Current	I <sub>IN</sub>	± 5	mA
Input Voltage	V <sub>IN</sub>	- 0.4~V <sub>DD</sub> ± 0.4	V
Power Dissipation	Free Air	1.0	W
	On PCB (Note)	1.3	
Operating Temperature	T <sub>opr</sub>	- 40~85	°C
Storage Temperature	T <sub>stg</sub>	- 55~150	°C

(Note) On Glass Epoxy PCB (100 × 100 × 1.6mm, Cu 40%)

**RECOMMENDED OPERATING CONDITIONS (Ta = - 40~85°C)**

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V <sub>DS</sub>	—	—	—	26	V
Supply Voltage	V <sub>DD</sub>	—	4.5	—	5.5	V
Output Current	I <sub>DS</sub>	Duty 50%	—	—	33.3	mA / ch
		Duty 80%	—	—	26.4	
		Duty 100%	—	—	23.6	
Input Voltage	V <sub>IN</sub>	—	GND	—	V <sub>DD</sub>	V
Operating Clock Frequency	f <sub>CLK</sub>	Duty 50%	—	—	5	MHz
Clock Pulse Width	t <sub>w</sub>	COUNTER·CLK	50	—	—	ns
		CLK				
Data Set-Up Time	t <sub>setup</sub>	—	20	—	—	ns
Data Hold Time	t <sub>hold</sub>					

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V<sub>DD</sub> = 5.5V)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Input Voltage	"H" Level	V <sub>IH</sub>	—	—	3.5	—	V <sub>DD</sub> + 0.4	V	
	"L" Level	V <sub>IL</sub>	—	—	-0.4	—	1.5		
Input Current	WRITE·CLK E·CLK, RESET WRITE·E	I <sub>INH</sub>	—	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 5V	-34	-70	-145	μA	
	PWM	I <sub>INL</sub>	—	V <sub>IN</sub> = 5V, V <sub>DD</sub> = 5V	34	70	145		
Output Voltage		V <sub>DS</sub>	—	OA1~OF8	I <sub>DS</sub> = 80mA	—	—	960	mV
					I <sub>DS</sub> = 50mA	—	—	600	
Output On Resistor		R <sub>ON</sub>	—	I <sub>DS</sub> = 50mA	—	—	12.0	Ω	
Output Leak Current		I <sub>OZ</sub>	—	V <sub>DS</sub> = 30V	—	—	10	μA	
Quiescent Current		I <sub>DD</sub>	—	—	—	—	20	μA	
Operating Supply Current		I <sub>DDopr</sub>	—	V <sub>DD</sub> = 5V, f <sub>CLK</sub> = 5MHz Output OPEN	—	—	5	μA	

**SWITCHING CHARACTERISTICS** ( $V_{DD} = 5.5V$ ,  $V_{DS} = 26V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT						
Maximum Operating Clock Frequency		$f_{MAX}$	Duty 50%	10	—	—	MHz						
Propagation Delay Time "L"- "H"	CLK-OUT <sub>n</sub> , WRITE-CLK-OUT <sub>n</sub>	$t_{pLH}$	Duty 50% $V_{IN(H)} = 4.5V$ $V_{IN(L)} = 0V$ $R_L = 375\Omega$ $C_L = 15pF$	—	80	—	ns						
	RESET-OUT <sub>n</sub>			—	100	—							
	COUNTER, CLK-OUT <sub>n</sub> (Note)			—	110	—							
	OUT- $\bar{E}$ -OUT <sub>n</sub> , WRITE- $\bar{E}$ -OUT <sub>n</sub>			—	100	—							
	$\bar{E}$ -CLK-OUT <sub>n</sub>			—	130	—							
MMV / $\bar{E}$ -OUT <sub>n</sub>	$t_{pHL}$	—		60	—								
CLK-OUT <sub>n</sub> , WRITE-CLK-OUT <sub>n</sub>		—		100	—								
RESET-OUT <sub>n</sub>		—		90	—								
COUNTER, CLK-OUT <sub>n</sub> (Note)		—		70	—								
OUT- $\bar{E}$ -OUT <sub>n</sub> , WRITE- $\bar{E}$ -OUT <sub>n</sub>		—		80	—								
$\bar{E}$ -CLK-OUT <sub>n</sub>		—	—	—									
MMV / $\bar{E}$ -OUT <sub>n</sub>		25	—	—									
Minimum Clock Pulse Width		$t_w$		25		—							
Data Set Up Time	DATA-OUT / PWM	$t_{setup}$	—	—	10	—							
	DATA-CLK												
	OUT- $\bar{E}$ - $\bar{E}$ -CLK												
Data Hold Time	DATA-OUT / PWM	$t_{hold}$		—	—	10		—					
	DATA-CLK												
	OUT- $\bar{E}$ - $\bar{E}$ -CLK												
Maximum Rise Time	COUNTER-CLK	$t_r$			—	—		—		1	$\mu s$		
	CLK												
Maximum Fall Time	COUNTER-CLK	$t_f$				—		—		—		1	$\mu s$
	CLK												
Output Rise Time	OUT <sub>n</sub>	$t_{or}$	—				—	0.02		1		$\mu s$	
Output Fall Time		$t_{of}$						—		0.05			
MMV Pulse Width		$t_{MMV}$					—			—			

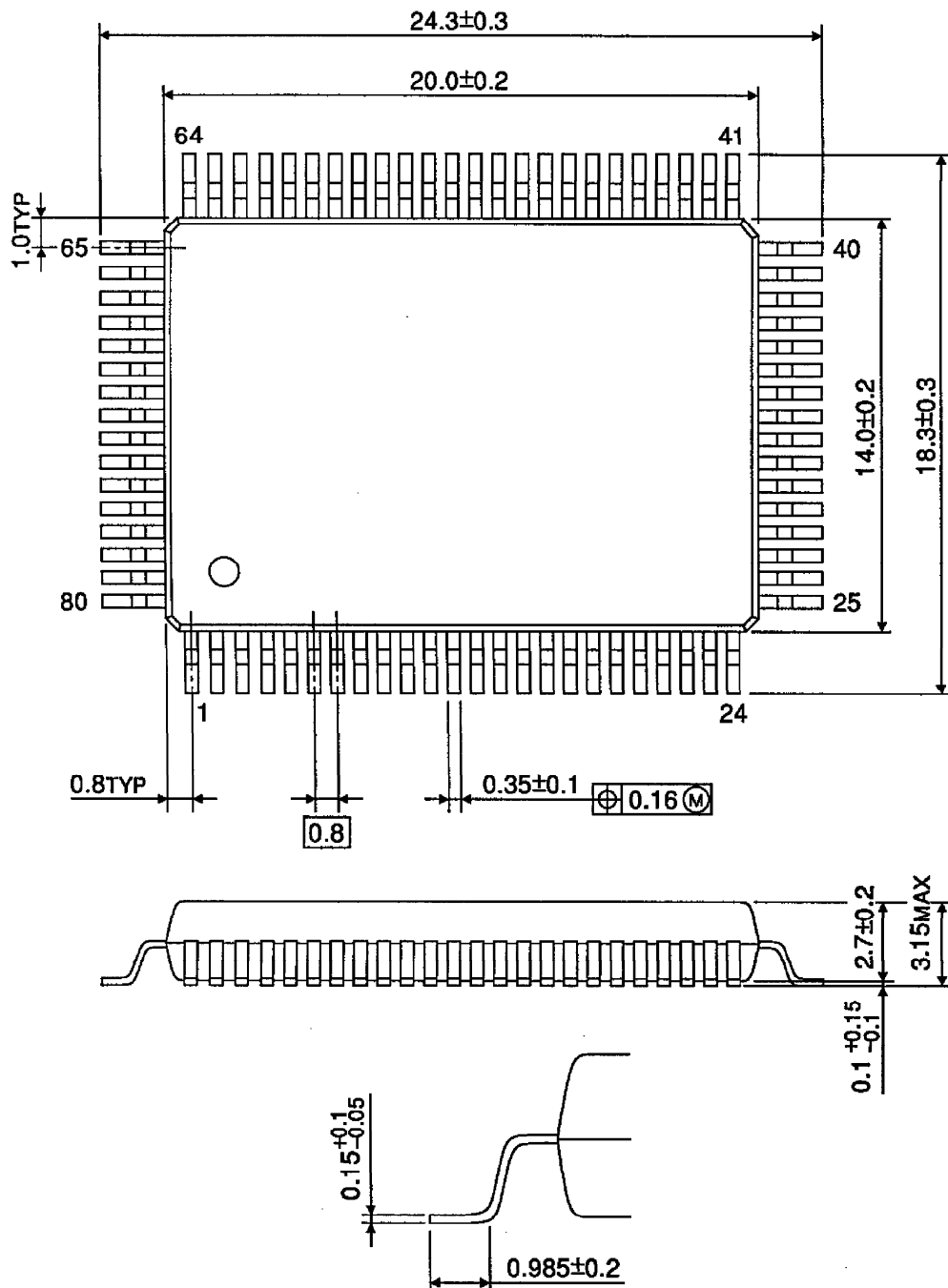
(Note) COUNTER DATA = F

**PRECAUTIONS for USING**

Utmost care is necessary in the design of the output line,  $V_{CC}$  and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

**OUTLINE DRAWING**  
QFP80-P-1420-0.80C

Unit : mm



Weight : 1.53g (Typ.)