



Application Note: SY50133Z

Flyback Regulator With Primary Side CV/CC Control For Adapters and Chargers

General Description

SY50133Z is a single stage Flyback regulator targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 620V/4.4Ω MOSFET in a compact SO8 package to minimize the size. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

SY50133Z adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance. The no-load switching frequency can be as low as 500Hz, minimizing the no-load power loss.

SY50133Z has programmable cable compensation to provide a better load regulation for the output voltage at the cable terminals.

SY50133Z provides reliable protections including VIN Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection (OVP), VSEN/ISEN pin short protection, VSEN pin upper divider resistor disconnect protection.

Features

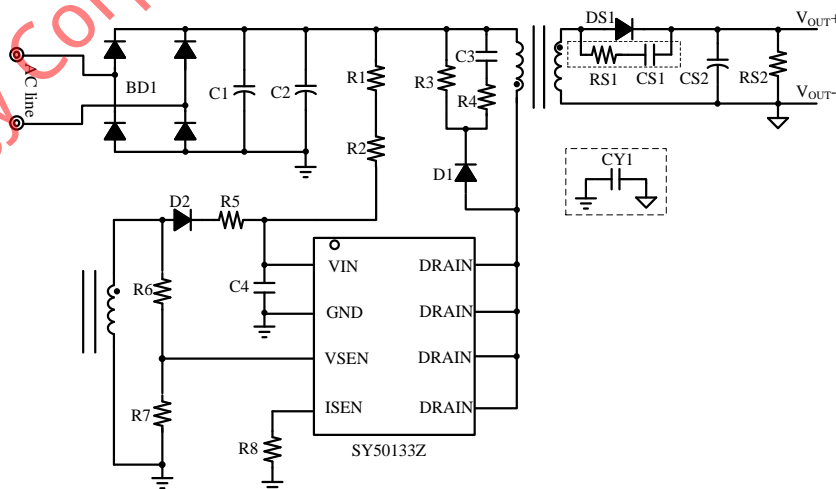
- Tight PSR CC/CV Regulation Over Entire Operating Range
- QR-mode Operation for High Efficiency
- PWM/PFM Control for High Average Efficiency
- Fast dynamic load transient response
- Cable Compensation for Better Load Regulation
- Low Start Up Current: 5μA Max
- Minimum Frequency Limitation 500Hz
- No-load Power is Less than 50mW
- Reliable Protections for OVP, SCP, OTP, OCP
- Reliable Protections for Safety Requirement
- Maximum switching frequency limitation 125kHz
- Integrated 620V/4.4Ω MOSFET
- Compact Package: SO8

Applications

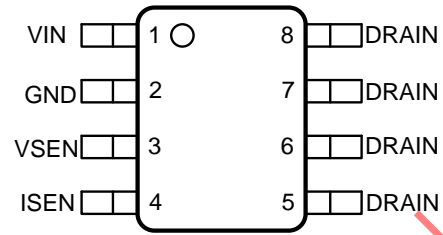
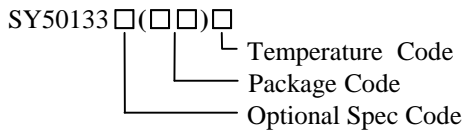
- AC/DC Adapters
- Battery Chargers

Recommended Operating Output Power		
Products	90~264Vac	176~264Vac
SY50133Z	12W	15W

Typical Applications



Ordering Information



Pinout (Top view)

Ordering Number	Package	Top Mark
SY50133ZFAC	SO8	BVNxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	VIN	Power supply pin. Bypass this pin to the GND pin with a 4.7uF/50V ceramic capacitor.
2	GND	Ground pin.
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance. This pin also senses the winding voltage to provide the QR operation.
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin.
5	DRAIN	Drain of the internal power MOSFET.
6	DRAIN	Drain of the internal power MOSFET.
7	DRAIN	Drain of the internal power MOSFET.
8	DRAIN	Drain of the internal power MOSFET.

Absolute Maximum Ratings (Note 1)

VIN	-0.3V~26V
VSEN	-0.3V~3.6V
ISEN	-0.3V~3.6V
Supply Current I _{VIN}	20mA
DRAIN	620V
Power Dissipation, @ T _A = 25°C SO8	1.1W
Package Thermal Resistance (Note 2)	
SO8, θ _{JA}	150°C/W
SO8, θ _{JC}	60°C/W
Junction Temperature Range	-45°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

Recommended Operating Conditions

VIN	9V~20V
ISEN	0V~1V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 105°C

Electrical Characteristics

($V_{VIN} = 12V$ (Note 3), $T_A = 25^\circ C$ unless otherwise specified)

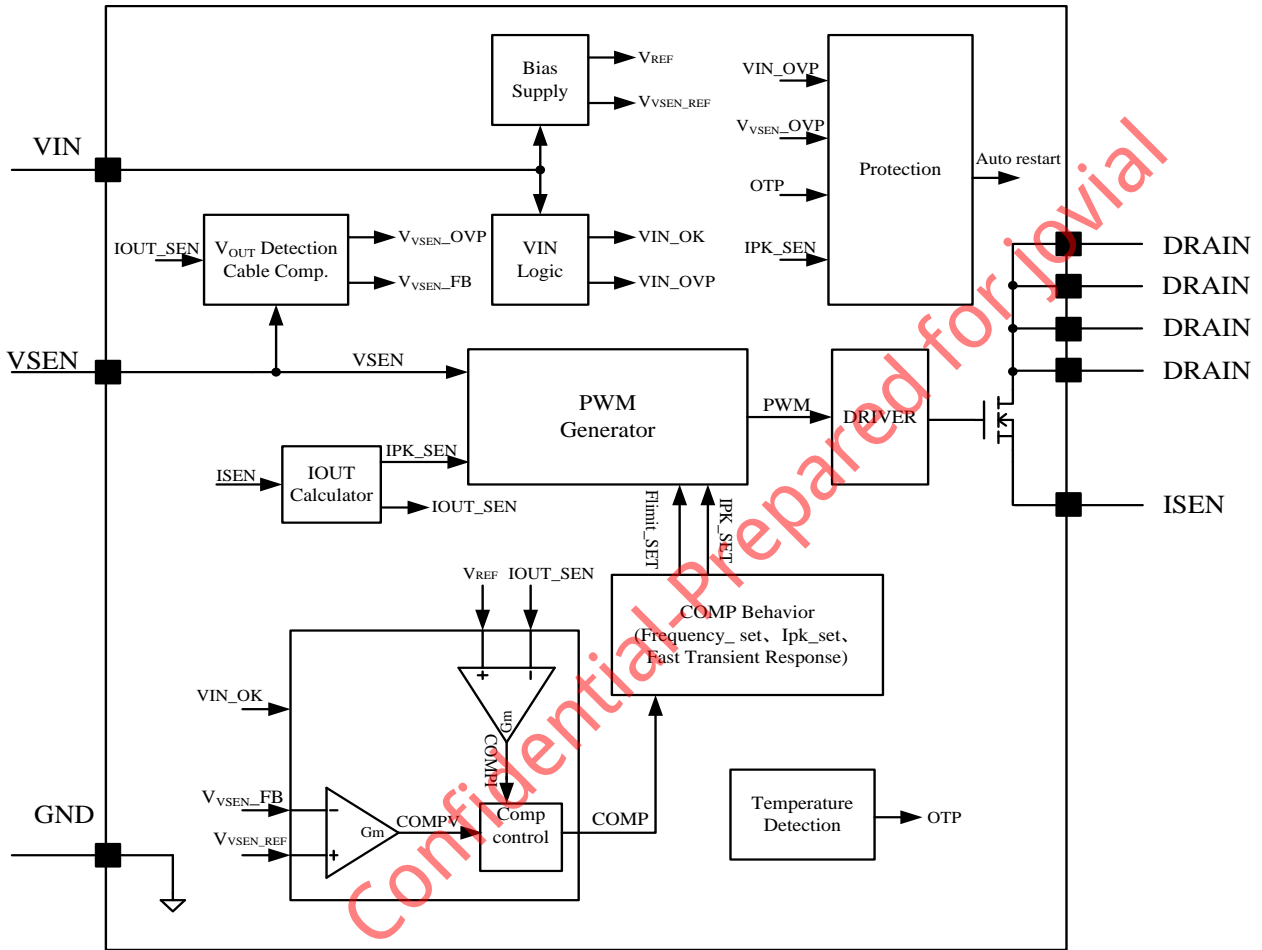
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Operating Range	V_{VIN_RANGE}		9		20	V
VIN Turn-on Threshold	V_{VIN_ON}		19.4	21	23.1	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.8	7.6	8.7	V
VIN OVP Voltage	V_{VIN_OVP}			$V_{VIN_ON}+3$		V
Start Up Current	I_{ST}	$V_{VIN} < V_{VIN_OFF}$	0.5	2	5	μA
Operating Current	I_{VIN}	$f=100kHz$		1.5		mA
Quiescent Current	I_Q	$f=500Hz$		140		μA
Shunt Current in OVP Mode	I_{VIN_OVP}	$V_{VIN} > V_{VIN_OVP}$		14		mA
Current Feedback Modulator Section						
Internal Reference Voltage	V_{REF}		0.413	0.42	0.427	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}	$V_{FBV} < 0.4V$		0.7		V
		$V_{FBV} > 0.4V$	0.89	1	1.16	V
VSEN Pin Section						
OVP Voltage Threshold	V_{VSEN_OVP}		1.42	1.5	1.58	V
Internal Reference Voltage	V_{VSEN_REF}		1.235	1.25	1.265	V
Cable Compensation Coefficient	K_3		16	25	31	$\mu A/V$
Integrated MOSFET Section						
Breakdown Voltage	V_{BV}	$V_{GS}=0V, I_{DS}=250\mu A$	620			V
Static Drain-Source On-Resistance	R_{DSON}	$V_{GS}=12V, I_{DS}=0.02A$		4.4		Ω
Switching Section						
Max ON Time	T_{ON_MAX}			24		μs
Min ON Time	T_{ON_MIN}			360		ns
Max OFF Time	T_{OFF_MAX}		1.58	2	2.42	ms
Min OFF Time	T_{OFF_MIN}		1.4	1.8	2.3	μs
Minimum Switching Period	T_{PERIOD_MIN}		7	8	9.2	μs
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			20		$^\circ C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

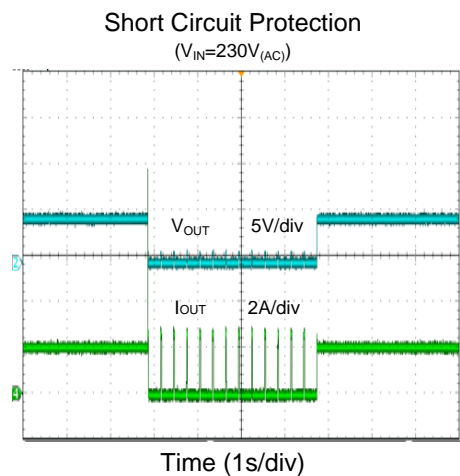
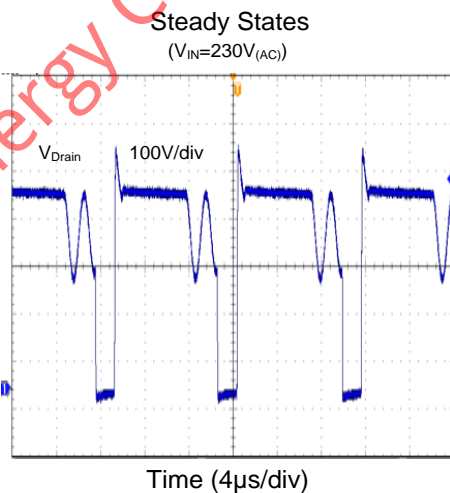
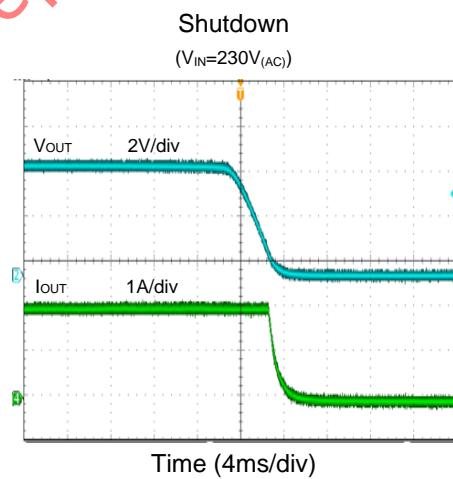
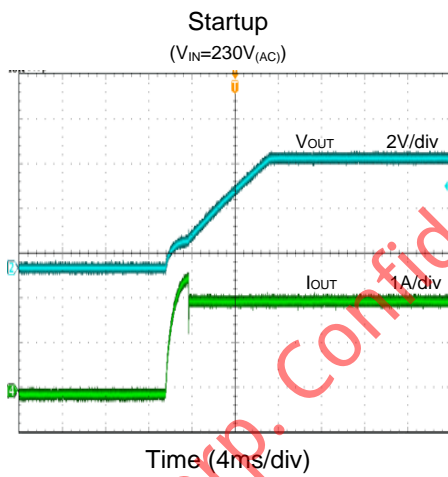
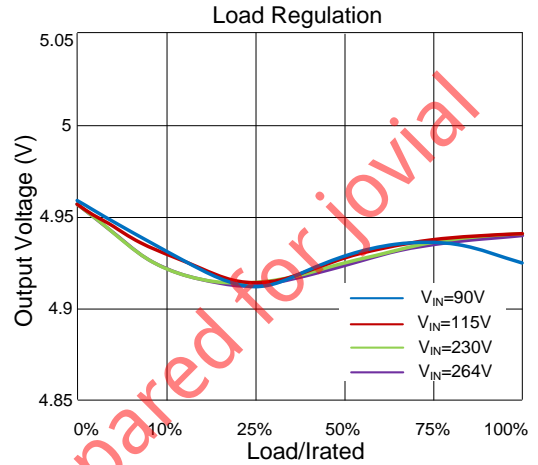
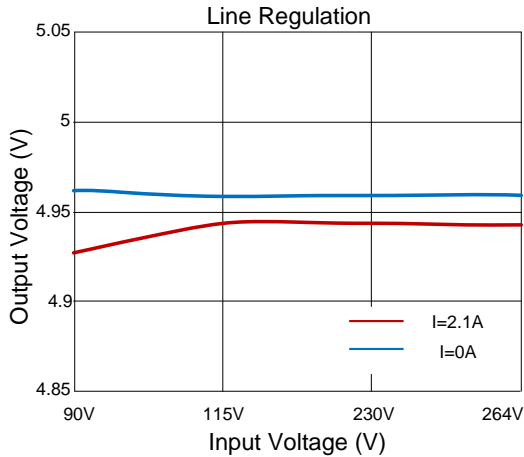
Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage to start the IC first, then set VIN to 12V.

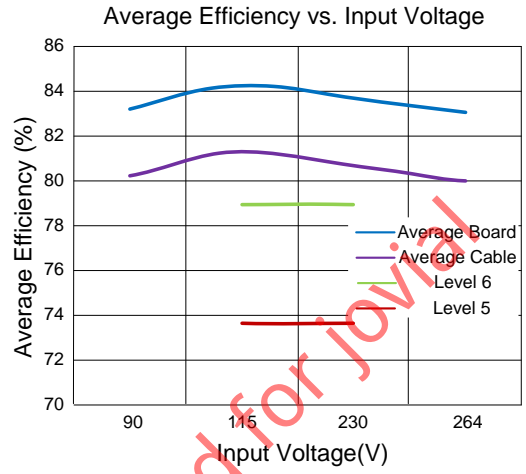
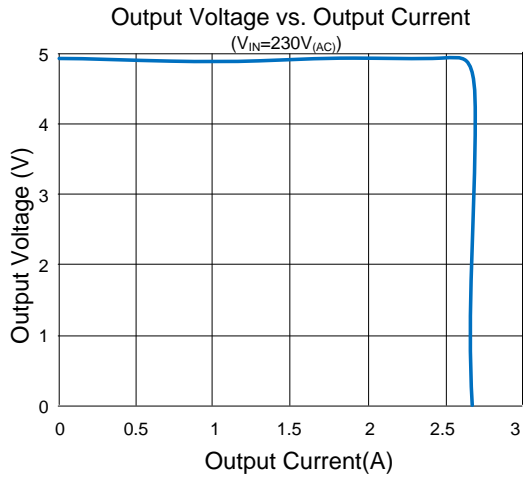
Block Diagram



Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 5Vdc_2.1A; output cable: 22AWG_1.2m; Ambient temperature: 25±5 °C; Ambient humidity: 65±25 %.)





Silergy Corp. Confidential-Prepared for Jovial

Operation Principles

Start-up Operation

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VIN and GND pins, C_{VIN} , is charged up by the BUS voltage through a start up resistor R_{ST} . Once V_{VIN} , the voltage on the VIN pin, rises up to V_{VIN_ON} , the internal blocks starts the operation. V_{VIN} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VIN} above V_{VIN_OFF} .

The start-up procedure is divided into two sections, as shown in Fig.1: t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO} , and usually t_{STO} is much smaller than t_{STC} .

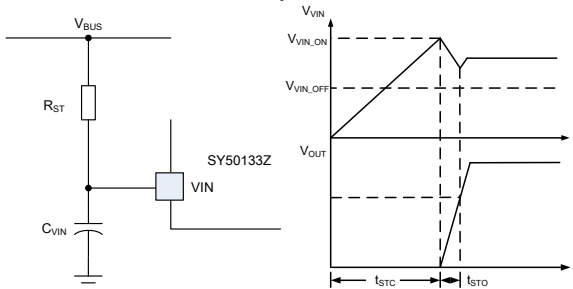


Fig.1 Start up

The start up resistor R_{ST} and C_{VIN} are designed by the following rules:

- (a) Preset start-up resistor R_{ST} , make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS_MAX}}{I_{VIN_OVP}} < R_{ST} < \frac{V_{BUS_MIN}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

- (b) Select C_{VIN} to obtain an ideal start-up time t_{ST} , and ensure the output voltage is built up with only one try.

$$C_{VIN} = \frac{\left(\frac{V_{BUS_MIN}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VIN_ON}} \quad (2)$$

- (c) If the C_{VIN} is not big enough to build up the output voltage with one try, increase C_{VIN} and decrease R_{ST} , go back to step (a) and repeat the same design flow until the ideal start up procedure is obtained.

Shut-down Operation

After AC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin, V_{VIN} will decrease. Once V_{VIN} is below V_{VIN_OFF} , the IC will stop working.

Quasi-Resonant Operation (valley detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

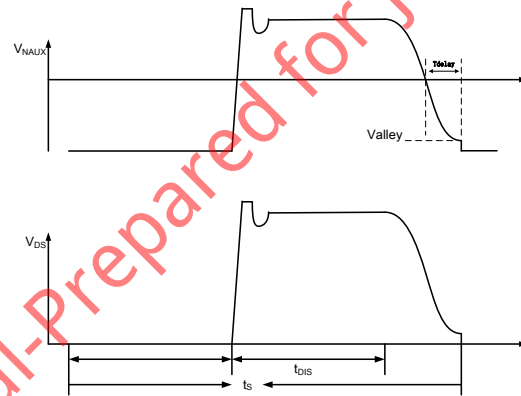


Fig.2 QR mode operation

The voltage across drain and source of the primary integrated MOSFET is reflected to the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.2, when the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output voltage control (CV control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

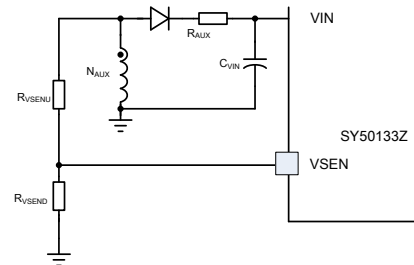


Fig.3 VSEN pin connection

As shown in Fig.4, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX} . The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

where R_{VSEND} and R_{VSENU} are the low side and high resistors at the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V

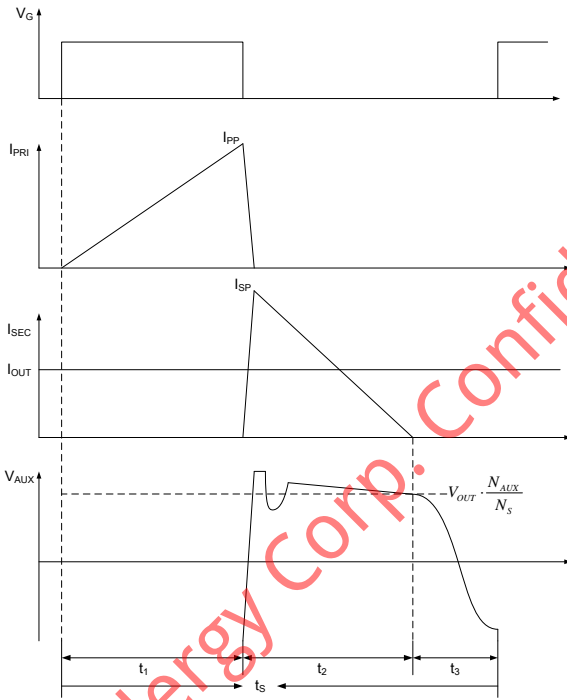


Fig.4 Auxiliary winding voltage waveforms

Output current control (CC control)

The output current is regulated by SY50133Z with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S .

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT_LIM}} \quad (6)$$

k_1 is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM} . The V-I curve is shown as Fig.5.

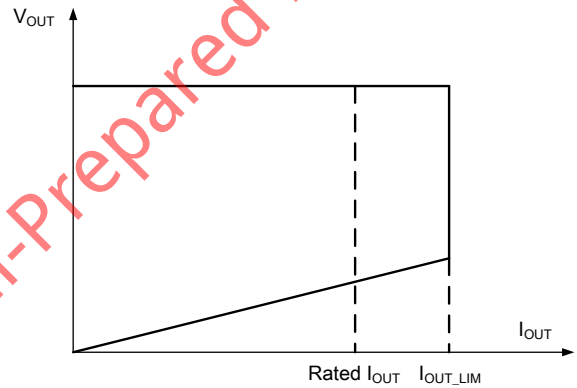


Fig.5 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

Cable impedance compensation

SY50133Z incorporates the cable impedance compensation to provide a better load regulation of output voltage at cable terminals. When the converter output load increases from no load to full load, the resulting voltage decrease on the output cables are compensated by decreasing the voltage feedback signals, which is shown by Fig. 6.

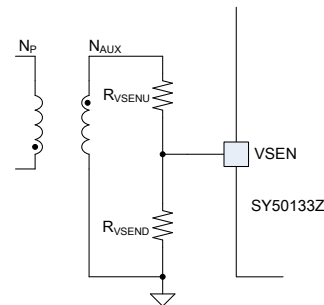


Fig. 6 Cable compensation

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_s} \cdot \frac{N_p}{N_s} \cdot \frac{N_{AUX}}{N_s} \quad (7)$$

where k_3 is set to 25uA/V, R_s is the current sense resistor connecting to the ISEN pin.

R_{cable} is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU} , the stronger cable compensation effect will be.

If the output current is below 10% the OCP point, the cable compensation is disabled.

Fault Protection modes

Over-temperature Protection (OTP)

SY50133Z includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the junction temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, MOSFET cannot be turned on until maximum off time is reached. IC will shut down until V_{VIN} is below V_{VIN_OFF} , and then enter the hiccup mode.

When the output voltage is not low enough to disable the valley detection in short condition, SY50133Z will operate in CC mode until V_{VIN} decreases below V_{VIN_OFF} .

As shown in Fig.7, a filter resistor R_{AUX} is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding.

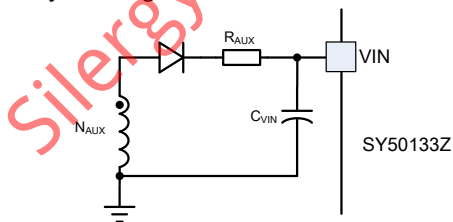


Fig. 7 Filter resistor R_{AUX}

VIN voltage OVP protection

When the V_{IN} voltage exceeds V_{VIN_OVP} threshold, SY50133Z will stop switching and discharge the V_{IN} voltage. Once V_{VIN} is below V_{VIN_OFF} , the SY50133Z will shut down

and V_{IN} will be charged again.

Output voltage OVP protection

When the VSEN pin signal exceeds 1.5V, reflecting an output over-voltage conditions, SY50133Z will stop switching and discharge the V_{IN} voltage. Once V_{VIN} is below V_{VIN_OFF} , the IC will shut down and then enter the hiccup mode.

VSEN pin short protection

The SY50133Z has a protection against the faults caused by shorting VSEN pin to GND. When the VSEN voltage does not reach the sense protection trigger level at the end of startup, the VSEN pin is deemed shorting to GND, and the protection is activated: the IC stops switching and discharge the V_{IN} voltage. Once V_{VIN} decreases below V_{VIN_OFF} , the IC will shut down and then enter the hiccup mode. In order to ensure reliable detection, the pull-down resistor at VSEN pin should be larger than 2kΩ.

ISEN pin short protection

The SY50133Z has a protection against the faults caused by shorting ISEN pin to GND. If ISEN short is detected at startup the IC stops switching and discharge the V_{IN} voltage. Once V_{VIN} decreases below V_{VIN_OFF} , the IC will shut down and then enter the hiccup mode.

VSEN pin upper divider resistor disconnect protection

If the upper divider resistor disconnected lasting for 8 switching cycles, the IC will stop switching and discharge the V_{IN} voltage. Meanwhile, limit the V_{ISEN} at V_{L_MIN} . Once V_{VIN} is below V_{VIN_OFF} , the SY50133Z will shut down and V_{IN} will be charged again.

Power Supply Design Considerations

Power Rating

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50133Z	90Vac~264Vac	10.5W	5V/2.1A	40°C
	90Vac~264Vac	12.5W	5V/2.5A	50°C
	90Vac~264Vac	13W	5V/2.6A	60°C
	90Vac~264Vac	12W	12V/1A	40°C

The test is conducted in a natural cooling condition at 25 °C ambient temperature.

Transformer Design Considerations (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the internal power MOSFET:

$$N_{PS} \leq \frac{V_{MOS_BR/DS} \times 90\% - \sqrt{2}V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D_F}} \quad (8)$$

where $V_{MOS_BR/DS}$ is the breakdown voltage of the integrated MOSFET. V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle, t_s , consists of three parts: current rising time t_1 , current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

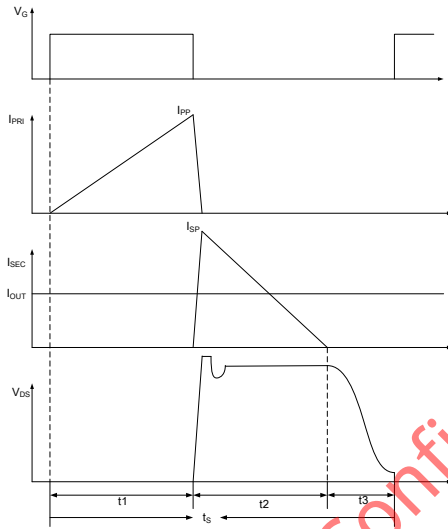


Fig.8 Switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum while the peak current through integrated MOSFET is maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown below:

(a) Select N_{PS}

$$N_{PS} \leq \frac{V_{MOS_BR/DS} \times 90\% - \sqrt{2}V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D_F}} \quad (9)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P_PK_MAX}$

$$I_{P_PK_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S_MIN}} \quad (10)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P_PK_MAX}^2 \times f_{S_MIN}} \quad (11)$$

where C_{Drain} is the parasitic capacitance at drain of integrated MOSFET, η is the efficiency, and P_{OUT} is the rated full load power

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P_PK_MAX}}{V_{BUS}} \quad (12)$$

$$t_2 = \frac{L_M \times I_{P_PK_MAX}}{N_{PS} \times (V_{OUT} + V_{D_F})} \quad (13)$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (14)$$

$$t_s = t_1 + t_2 + t_3 \quad (15)$$

(e) Compute primary maximum RMS current $I_{P_RMS_MAX}$ for the transformer fabrication.

$$I_{P_RMS_MAX} = \frac{\sqrt{3}}{3} I_{P_PK_MAX} \times \sqrt{\frac{t_1}{t_s}} \quad (16)$$

(f) Compute secondary maximum peak current $I_{S_PK_MAX}$ and RMS current $I_{S_RMS_MAX}$ for the transformer fabrication.

$$I_{S_PK_MAX} = N_{PS} \times I_{P_PK_MAX} \quad (17)$$

$$I_{S_RMS_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P_PK_MAX} \times \sqrt{\frac{t_2}{t_s}} \quad (18)$$

Transformer Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P_PK_MAX}$
Primary maximum RMS current	$I_{P_RMS_MAX}$
Secondary maximum RMS current	$I_{S_RMS_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e .

(b) Preset the maximum magnetic flux ΔB

$$\Delta B = 0.22 \sim 0.28 T$$

(c) Compute primary turn N_p

$$N_p = \frac{L_M \times I_{P_PK_MAX}}{\Delta B \times A_e} \quad (19)$$

(d) Compute secondary turn N_s

$$N_s = \frac{N_p}{N_{PS}} \quad (20)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_s \times \frac{V_{VIN}}{V_{OUT}} \quad (21)$$

where V_{VIN} is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P_RMS_MAX}$ and $I_{S_RMS_MAX}$, select appropriate wire to achieve the current density from 4A/mm² to 10A/mm².

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

Diode Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum;

$$V_{D_R_MAX} = \frac{\sqrt{2} V_{AC_MAX}}{N_{PS}} + V_{OUT} \quad (22)$$

where V_{AC_MAX} is maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D_PK_MAX} = N_{PS} \times I_{P_PK_MAX} \quad (23)$$

$$I_{D_AVG} = I_{OUT} \quad (24)$$

where $I_{P_PK_MAX}$ is maximum primary peak current.

Input Capacitor C_{BUS} Selection

Generally, the input capacitor C_{BUS} is selected by

$$C_{BUS} = 2 \sim 3 \mu F / W,$$

or more accurately by

$$C_{BUS} = \frac{\arcsin\left(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC_MIN}}\right) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2 f_{IN} V_{AC_MIN}^2 \left[1 - \left(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC_MIN}}\right)^2\right]} \quad (25)$$

Where ΔV_{BUS} is the voltage ripple of BUS line.

RCD snubber for MOSFET selection

The power loss of the snubber P_{RCD} is evaluated as:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (26)$$

where V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by RCD snubber, L_K is the leakage inductor, L_M is the inductance of the Flyback transformer and P_{OUT} is the output power.

The R_{RCD} is calculated as:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S)^2}{P_{RCD}} \quad (27)$$

The C_{RCD} is calculated as:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C_RCD}} \quad (28)$$

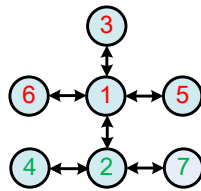
Layout Considerations

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

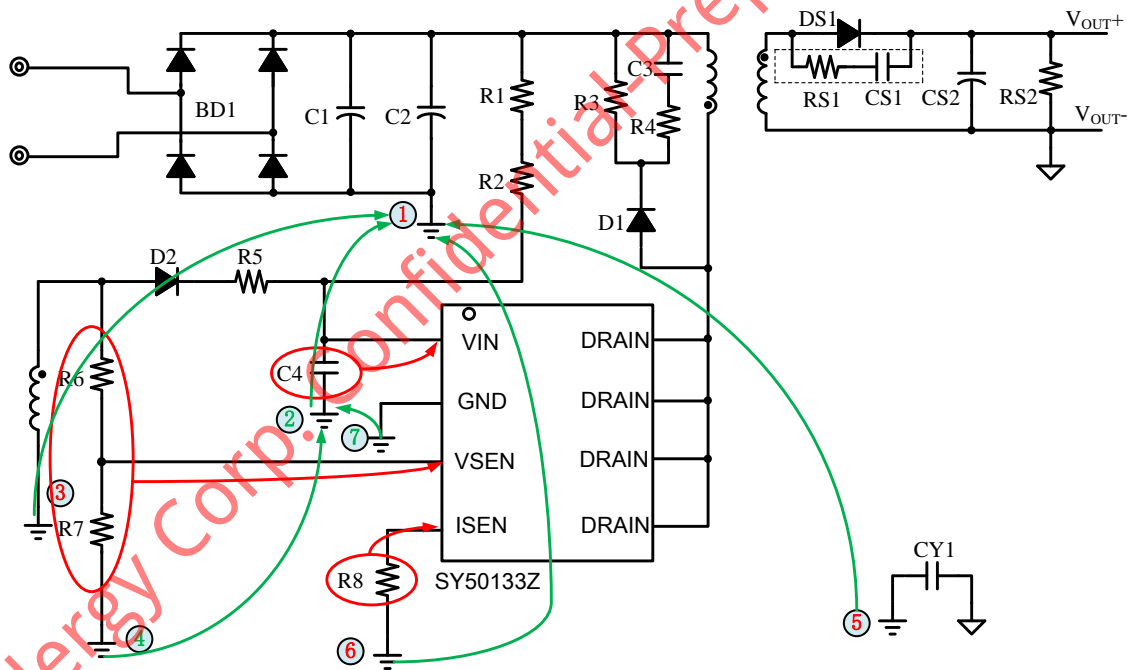


- Ground ①: ground of BUS line capacitor
- Ground ②: ground of bias supply capacitor
- Ground ③: ground node of auxiliary winding
- Ground ④: ground node of divider resistor
- Ground ⑤: primary ground node of Y capacitor
- Ground ⑥: ground node of current sample resistor.
- Ground ⑦: ground of IC GND.

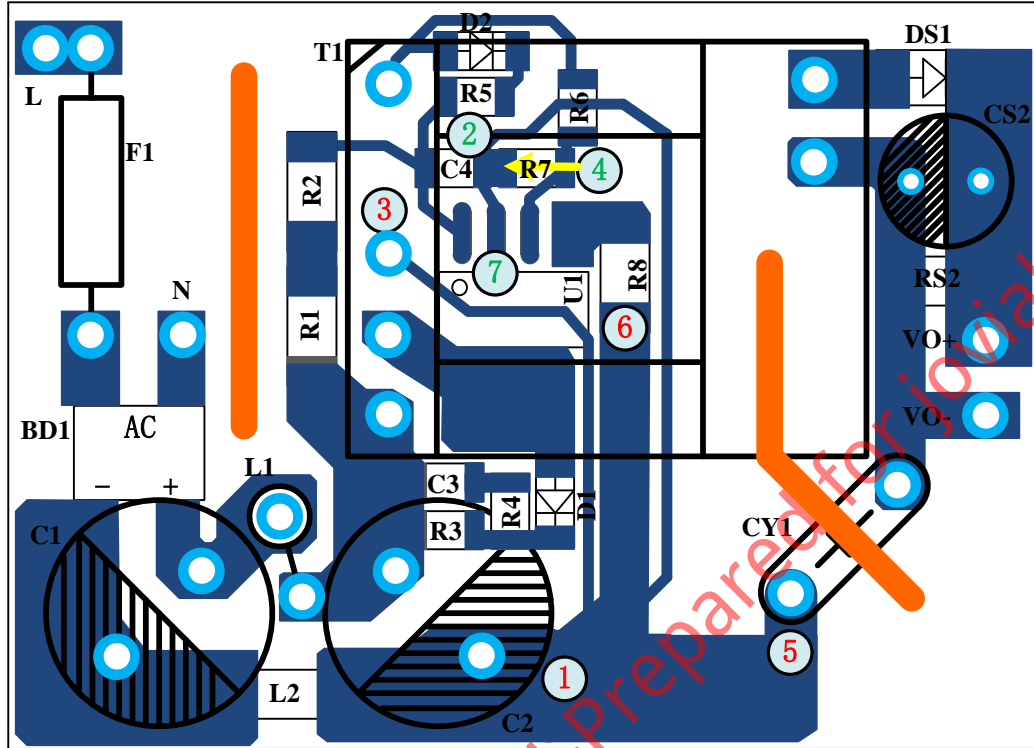
(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The loop consisting of 'Source pin – current sense resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note : Ground node of current sample resistor must be connected to the ground of bus line capacitor



Example layout

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 1.8us.
2. VIN voltage should be designed to higher than 11V for all conditions.
3. RCD snubber's influence:
At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If I_{min} (I_{min}=0.24V/R_s) is 0.1A, the snubber capacitor should be no larger than 470pF.
4. At heavy load, the peak-to-peak voltage at the V_{sen} pin should be less than approximately 100mV_{p-p} after off-min time (1.8us). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
5. R_{VSEN} is the upper resistor of the divider. Normally, its value is recommended between 30kΩ-91kΩ.
6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:
C_{out}= 3.7m*I_{ou} t/V_{out}.
For example, in the 5V/2A output case, C_{out}=3.7*2/5=1.48mF. The output capacitor can choose from 1270uF to 1680uF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of C_{out} properly or use low ESR capacitor.

Design Example

A design example of typical application is shown below step by step. (Cable Test)

Note: All selected parameter (set value) need to adjust according to the practical condition.

#1. Identify design specification

Design Specification			
V _{AC(RMS)}	90V~264V	V _{OUT}	5V
I _{OUT}	2.1A	η	85%

#2. Transformer design (N_{PS}, L_M, N_P, N_S, N_{AUX})

(1) Refer to **Transformer selection (N_{PS} and L_M)**

Conditions			
V _{AC_MIN}	90V	V _{AC_MAX}	264V
ΔV _S	75V	V _{MOS_(BR)DS}	620V
P _{OUT (Max)}	10.5W	V _{D_F}	1V
C _{Drain}	100pF	f _{S_MIN}	60kHz
ΔV _{BUS}	30% V _{BUS_MIN}		

(a) Compute turns ratio N_{PS} first

$$\begin{aligned}
 N_{PS} &\leq \frac{V_{MOS_(BR)DS} \times 90\% - \sqrt{2}V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D_F}} \\
 &= \frac{620V \times 0.9 - \sqrt{2} \times 264V - 75V}{5V + 1.0V} \\
 &= 18.275
 \end{aligned}$$

N_{PS} is set to

$$N_{PS} = 15$$

(b) f_{S_MIN} is preset

$$f_{S_MIN} = 60\text{kHz}$$

(c) Compute inductor L_M and maximum primary peak current I_{P_PK_MAX}

$$\begin{aligned}
 I_{P_PK_MAX} &= \frac{2P_{OUT}}{\eta \times (\sqrt{2}V_{AC_MIN} - \Delta V_{BUS})} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S_MIN}} \\
 &= \frac{2 \times 10.5W}{0.85 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 10.5W}{0.85 \times 15 \times (5V + 1V)} + \pi \times \sqrt{\frac{2 \times 10.5W}{0.85} \times 100\text{pF} \times 60\text{kHz}} \\
 &= 0.59A
 \end{aligned}$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P_PK_MAX}^2 \times f_{S_MIN}}$$

$$= \frac{2 \times 10.5W}{0.85 \times (0.59A)^2 \times 60kHz}$$

$$= 1.183mH$$

Set: $L_M=1.1mH$. (Note: the actual value generally less than the compute value)

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P_PK_MAX}}{V_{BUS_MIN}} = \frac{1.1mH \times 0.59A}{\sqrt{2} \times 90V} = 5.1\mu s$$

$$t_2 = \frac{L_M \times I_{P_PK_MAX}}{N_{PS} \times (V_{OUT} + V_{D_F})} = \frac{1.10mH \times 0.59A}{15 \times (5V + 1V)} = 7.212\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{1.1mH \times 100pF} = 1.042\mu s$$

$$t_s = t_1 + t_2 + t_3 = 5.1\mu s + 7.212\mu s + 1.042\mu s = 13.354\mu s$$

(e) Compute primary maximum RMS current $I_{P_RMS_MAX}$ for the transformer fabrication.

$$I_{P_RMS_MAX} = \frac{\sqrt{3}}{3} I_{P_PK_MAX} \times \sqrt{\frac{t_1}{t_s}} = \frac{\sqrt{3}}{3} \times 0.59A \times \sqrt{\frac{5.1\mu s}{13.354\mu s}} = 0.211A$$

(f) Compute secondary maximum peak current $I_{S_PK_MAX}$ and RMS current $I_{S_RMS_MAX}$ for the transformer fabrication.

$$I_{S_PK_MAX} = N_{PS} \times I_{P_PK_MAX} = 15 \times 0.59A = 8.851A$$

$$I_{S_RMS_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P_PK_MAX} \times \sqrt{\frac{t_2}{t_s}} = 15 \times \frac{\sqrt{3}}{3} \times 0.59A \times \sqrt{\frac{7.212}{13.354}} = 3.755A$$

(2) Refer to **Transformer number of turns selection (N_P , N_S , N_{AUX})**

(a) Select the magnetic core style, identify the effective area A_e . There select EF17 for compute example. Its A_e is 24.4 mm². The EF17 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB . Usually $\Delta B=0.22\sim 0.28T$.

Set: $\Delta B=0.25T$.

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P_PK_MAX}}{\Delta B \times A_e} = \frac{1.1 \times 10^{-3} \times 0.59A}{0.25 \times 24.4 \times 10^{-6}} = 106$$

Set: $N_P=105$

(d) Compute secondary turn N_s

$$N_s = \frac{N_p}{N_{ps}} = \frac{105}{15} = 7$$

Set: $N_s=7$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_s \times \frac{V_{VIN}}{V_{OUT}} = 7 \times \frac{12.5}{5} = 17.5$$

Set: $N_{AUX}=18$

Where V_{VIN} is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P_RMS_MAX}$ and $I_{S_RMS_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm² to 10A/mm².

Primary wire diameter selection: current density j is set to 5 A/mm².

$$\text{The compute primary wire cross-sectional area } S1 = \frac{I_{P_RMS_MAX}}{j} = \frac{0.211}{5} = 0.042\text{mm}^2$$

$$\text{The compute primary wire diameter } D1 = 2 \times \sqrt{\frac{S1}{\pi}} = 2 \times \sqrt{\frac{0.042}{\pi}} = 0.231\text{mm}$$

Set: $D1=0.23\text{mm}$.

Secondary wire diameter selection: current density j is set to 10 A/mm².

$$\text{The compute secondary wire cross-sectional area } S2 = \frac{I_{S_RMS_MAX}}{j} = \frac{3.755}{10} = 0.376\text{mm}^2$$

$$\text{The compute secondary wire diameter } D2_1 = 2 \times \sqrt{\frac{S2/2}{\pi}} = 2 \times \sqrt{\frac{0.376/2}{\pi}} = 0.489\text{mm}$$

Set: $D2=D2_1 \times 2 = 0.5\text{mm} \times 2$

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

(h) Other usually transformer inductance

	Specification	Remark
Thickened EE16 (90~264Vac,5V2.1A)		
Primary-Side Inductance	1.2mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50µH Maximum	Short One of Secondary Winding
N _P		96
N _S		6
N _A		15
EF1510 (90~264Vac,5V2.1A)		
Primary-Side Inductance	1.2mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50µH Maximum	Short One of Secondary Winding
N _P		64
N _S		4
N _A		10
Thickened EE16 (90~264Vac,12V1A)		
Primary-Side Inductance	1.25mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50µH Maximum	Short One of Secondary Winding
N _P		105
N _S		15
N _A		16

#3. Select secondary power diode

 Refer to **Diode selection**

Compute the voltage and the current stress of secondary power diode

$$V_{D,R_MAX} = \frac{\sqrt{2}V_{AC_MAX}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2} \times 264V}{15} + 5V = 29.89V$$

$$I_{D_PK_MAX} = N_{PS} \times I_{P_PK_MAX} = 15 \times 0.59A = 8.851A$$

$$I_{D_AVG} = 2.1A$$

#4. Select the input capacitor CIN

 Refer to **Input capacitor C_{BUS}**

Known conditions at this step			
V _{AC_MIN}	90V	ΔV _{BUS}	30% V _{BUS_MIN}

$$C_{BUS} = \frac{\arcsin\left(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC_MIN}}\right) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN} V_{AC_MIN}^2 \left[1 - \left(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC_MIN}}\right)^2\right]}$$

$$= \frac{\arcsin\left(1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V}\right) + \frac{\pi}{2}}{\pi} \times \frac{10.5W}{0.85} \times \frac{1}{2 \times 50 \times 90V^2 \times \left[1 - \left(1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V}\right)^2\right]}$$

$$= 22.33\mu F$$

Set: $C_{BUS}=20 \mu F$

Where ΔV_{BUS} is the voltage ripple of BUS line.

#5. Set VIN pin

Refer to **Start up**

Conditions			
V_{BUS_MIN}	$90V \times \sqrt{2}$	V_{BUS_MAX}	$264V \times \sqrt{2}$
I_{ST}	$5\mu A$ (max)	V_{VIN_ON}	21V (typical)
I_{VIN_OVP}	14mA (typical)	t_{ST}	3s (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS_MIN}}{I_{ST}} = \frac{90V \times \sqrt{2}}{5\mu A} = 25.452M\Omega,$$

$$R_{ST} > \frac{V_{BUS_MAX}}{I_{VIN_OVP}} = \frac{264V \times \sqrt{2}}{14mA} = 26.66k\Omega$$

Set R_{ST}

$$R_{ST}=4M$$

(b) Design C_{VIN}

$$C_{VIN} = \frac{\left(\frac{V_{BUS_MIN}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VIN_ON}} = \frac{\left(\frac{90V \times \sqrt{2}}{4M\Omega} - 5\mu A\right) \times 3s}{21V} = 3.83\mu F$$

Set C_{VIN}

$$C_{VIN}=4.7\mu F$$

#6. Set current sense resistor to achieve ideal output current

Refer to **Output current control (CC control)**

Known conditions at this step			
k_1	0.5	N_{PS}	15
V_{REF}	0.42V	I_{OUT_LIM}	2.52A

The current sense resistor is

$$R_s = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT_LIM}}$$

$$= \frac{0.5 \times 0.42V \times 15}{2.52A}$$

$$= 1.25\Omega$$

Set R_s

$$R_s = 1.2\Omega$$

#7. Set VSEN pin

Refer to **Output voltage control (CV control)**

First compute R_{VSENU}

Conditions			
V_{OUT}	5V	V_{VSEN_REF}	1.25V
R_{Cable}	0.13Ω(22AWG 1.2m)	N_s	7
N_{AUX}	18	K_3	25uA/V

$$R_{VSENU} = \frac{N_p}{N_s} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_s} \cdot \frac{1}{2K_3 \cdot R_s} = 83.57K\Omega$$

Set R_{VSENU}

$$R_{VSENU} = 51k\Omega$$

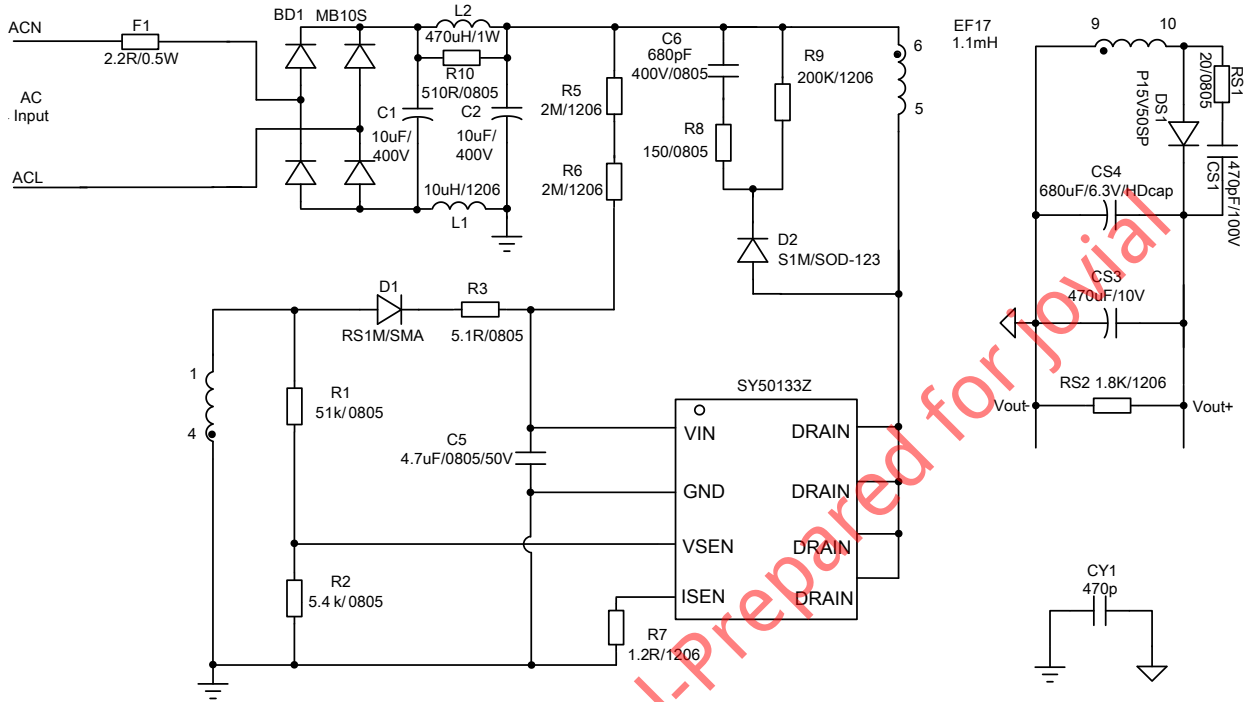
Then compute R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} \cdot N_{AUX}}{V_{VSEN_REF} \cdot N_s} - 1} = \frac{51K}{\left(\frac{5V \times 18}{1.25V \times 7} - 1\right)} = 5.492k\Omega$$

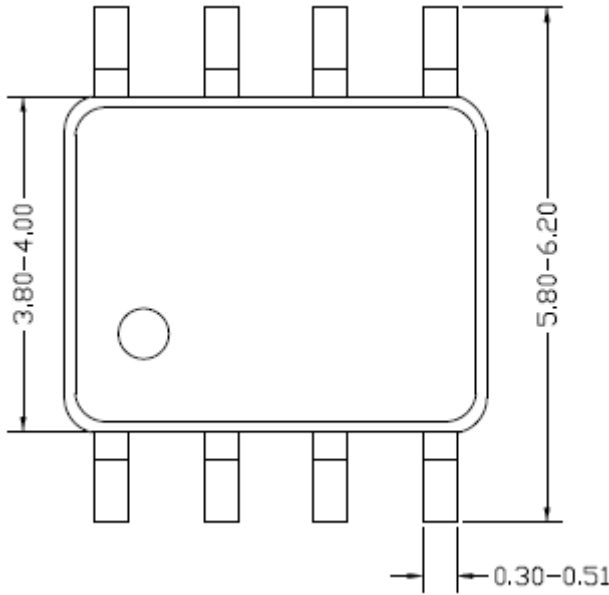
Set R_{VSEND}

$$R_{VSEND} = 5.6//150k\Omega$$

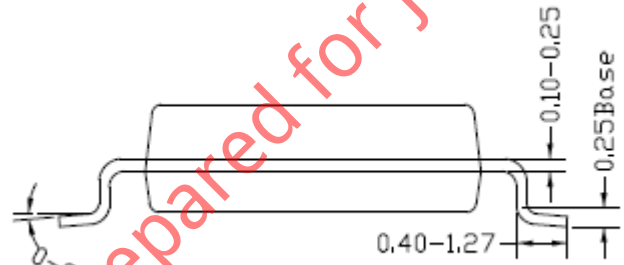
#8. Final result



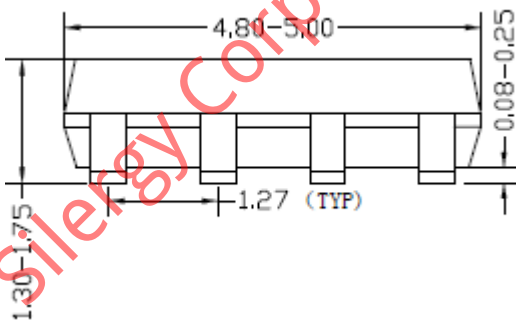
SO8 Package outline & PCB layout design



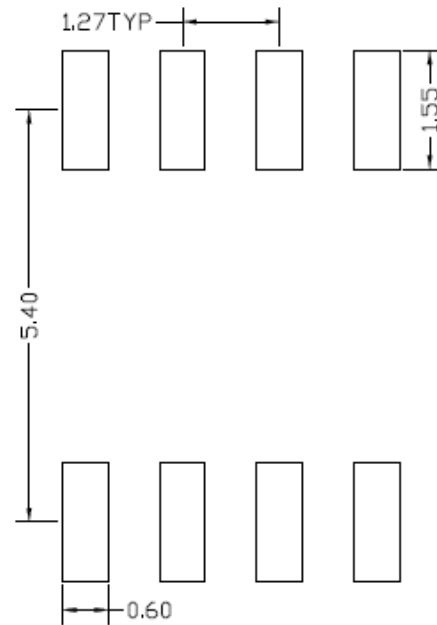
Top view



Side view



Front view

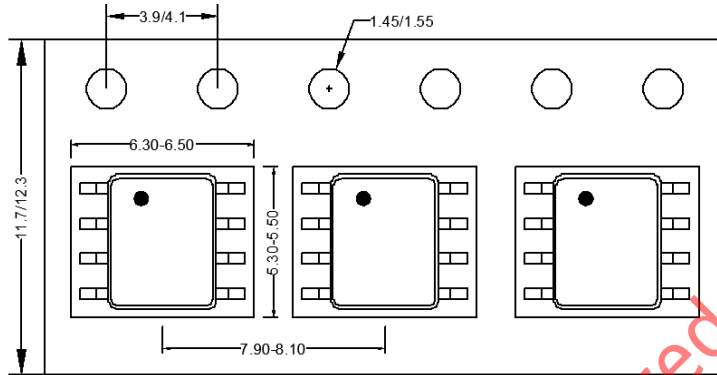


**Recommended Pad Layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

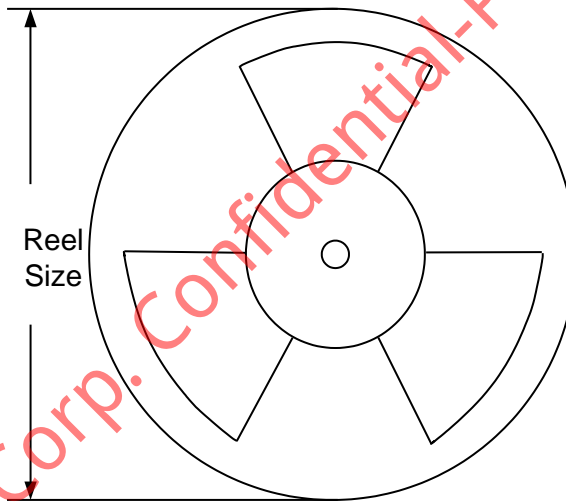
Taping & Reel Specification

1. Taping orientation for packages (SO8)



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 17, 2018	Revision 0.9	Initial Release

Silergy Corp. Confidential-Prepared for Jovial

IMPORTANT NOTICE

- 1. Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
- 2. Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
- 3. Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
- 4. Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
- 5. Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
- 6. No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2018 Silergy Corp.

All Rights Reserved.