# Single-Stage LED Driver with PFC
# Supports Wide Range of Dimming Interfaces

## 1 Description

The iW3636 is a high-performance, single-stage AC/DC power controller for PWM dimmable LED driver with power factor (PF) correction. It supports most commonly used isolated and non-isolated flyback and buck-boost topologies. The device operates in constant on-time mode to achieve high power factor (> 0.9) across a wide load range. It uses Dialog's ***PrimAccurate™*** advanced primary-side sensing technology to achieve excellent output current regulation over line and load variation without the need for secondary feedback components. It also eliminates the need for external loop compensation while maintaining stability over all operating conditions.

The iW3636 offers a 1% to 100% dimming range and provides a dedicated PWM dimming input pin that supports a wide variety of dimming application interfaces such as wireless modules, MCUs or 0-10V interfaces. When working with Dialog's secondary-side SSL PWM signal generator IC, the iW339, the iW3636 adopts a proprietary technique to support accurate dimming by eliminating the impact from the non-ideal characteristics of optocouplers. In addition, the iW3636 accepts a secondary PWM or analog input to allow maximum output current configuration control.

Dialog's innovative proprietary technology maximizes the iW3636 performance in an SOIC-8 package. It provides two multi-function pins to configure IC functions such as the dimming curve and minimum dimming level. The iW3636 also enables the active start-up scheme to achieve the shortest possible start-up time without sacrificing active efficiency. By adaptively controlling the maximum operating frequency at different dimming levels, it helps eliminate audible noise and achieve low standby power consumption.

## 2 Features

- Universal AC input ($90V_{AC}$ - $305V_{AC}$) or DC input with output power up to 90W
- Primary-side control achieves very tight line and load regulation (±3%)
- PF > 0.9 and THD < 20% across wide output power range
- Dual dimming interfaces
- Supports fully isolated 0-10V dimming with Dialog's iW339 interface controller
- Low standby power
- Wide dimming range 1% - 100%
- Configurable 72kHz or 90kHz PWM switching frequency with quasi-resonant operation
- Configurable minimum dimming setting: dim-to-off, 1%, 5% or 10%
- Wide $V_{CC}$ operating range from 7.5V to 30V
- Built-in over-temperature protection or by external NTC
- Configurable dimming curve: linear or logarithmic
- Built-in soft-start achieves fast and smooth start-up for all different operating conditions
- Active start-up scheme enables fastest possible start-up
- Built-in single-point fault protection features: output open, output over-voltage, output short and input voltage under-voltage protections
- Light-off mode with soft-off feature and configurable voltage regulation value

## 3 Applications

- Intelligent and wireless LED lighting
- Dimming LED ballast

## Single-Stage LED Driver with PFC
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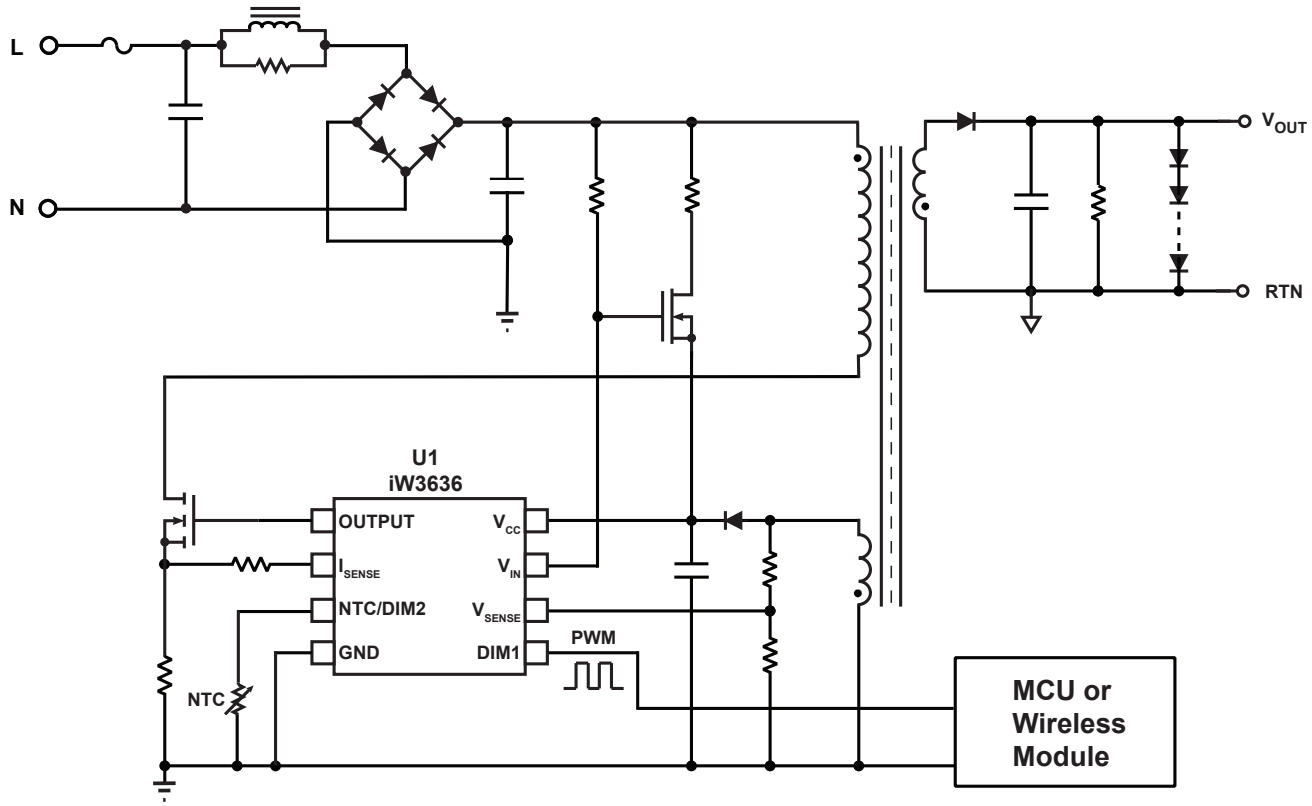



**Figure 3.1 : iW3636 Typical Application Circuit (Wireless Dimming with NTC Derating Using Depletion-mode FET as Active Start-up Device).**

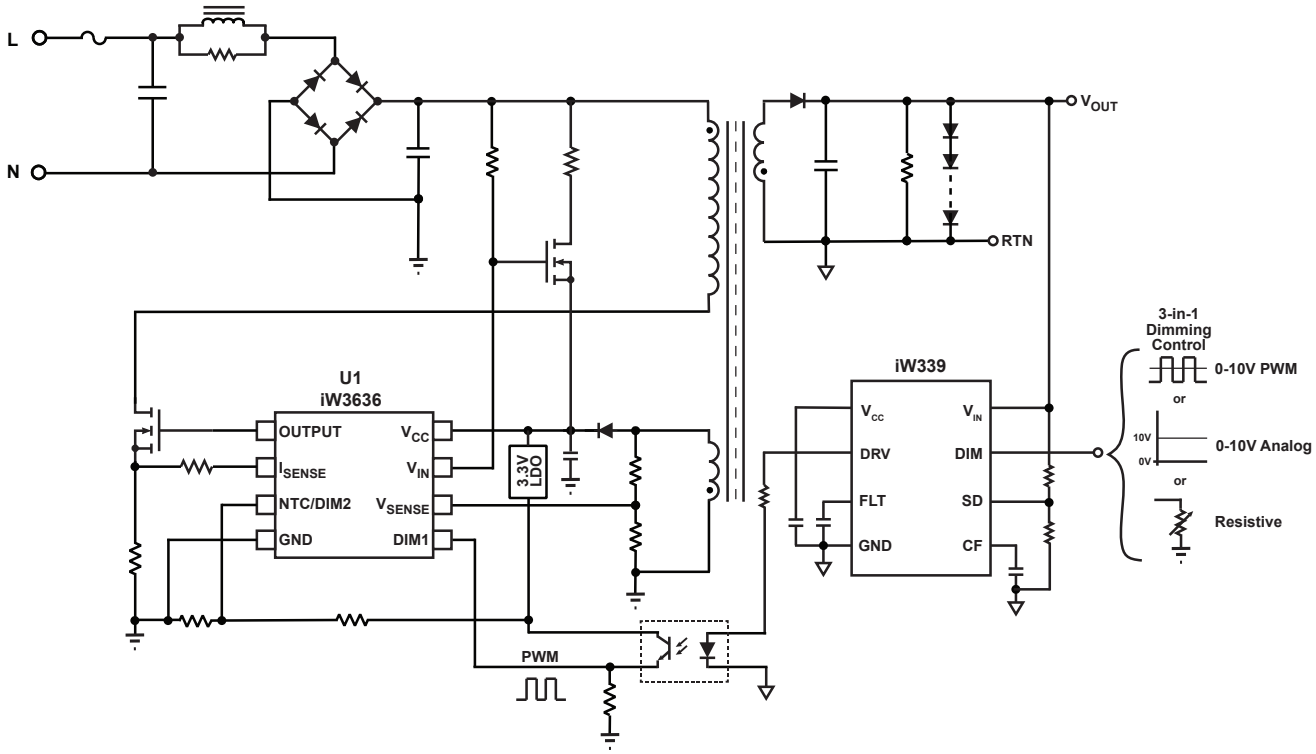



**Figure 3.2 : iW3636 Typical Application Circuit (3-in-1 Dimming with Maximum Current Modulated by the Voltage at NTC/ DIM2 Pin and Using Enhancement-mode FET as Active Start-up Device).**

## 4 Pinout Description

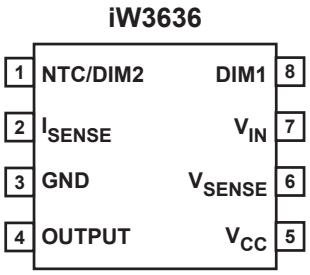



**Figure 4.1 : 8-Lead SOIC-8 Package**

| Pin Number | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | NTC/DIM2 | Digital Input / Analog In/Out | Used for external temperature sensing via an NTC resistor, or to provide a 2nd dimming interface via PWM signal or analog signal (0–1.8V). |
| 2 | $I_{SENSE}$ | Analog Input | Provides primary current sense for cycle-by-cycle peak current control and limit during normal operation, and serves as a configuration pin during startup. |
| 3 | GND | Ground | Ground. |
| 4 | OUTPUT | Output | Gate drive for external MOSFET switch. |
| 5 | $V_{CC}$ | Power | IC power supply. |
| 6 | $V_{SENSE}$ | Analog Input | Provides output voltage sense for primary regulation during normal operation, and serves as a configuration pin during startup. |
| 7 | $V_{IN}$ | Analog Input | Dual function. Used to control active start-up devices and sense line voltage. |
| 8 | DIM1 | Digital Input | PWM dimming input detection. |

## 5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to the Electrical Characteristics section.

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| DC supply voltage range (pin 5, $I_{CC}$ = 10mA max) | $V_{CC}$ | -0.3 to 31 | V |
| Continuous DC supply current at $V_{CC}$ pin | $I_{CC}$ | 20 | mA |
| $V_{IN}$ (pin 7) | | -0.3 to 31 | V |
| OUTPUT (pin 4) | | -0.3 to 31 | V |
| $V_{SENSE}$ input (pin 6, $I_{VSENSE}$ ≤ 10mA) | | -0.3 to 7 | V |
| $I_{SENSE}$ input (pin 2) | | -0.3 to 7 | V |
| NTC/DIM2 (pin 1) | | -0.3 to 7 | V |
| DIM1 (pin 8) | | -0.3 to 7 | V |
| Maximum junction temperature | $T_{JMAX}$ | 150 | °C |
| Operating junction temperature | $T_{JOPT}$ | -40 to 150 | °C |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C |
| Thermal resistance junction-to-ambient | $\theta_{JA}$ | 170 | °C/W |
| ESD rating per JEDEC JESD22-A114 | | ±2,000 | V |
| Latch-up test per JESD78D | | ±100 | mA |

## 6 Electrical Characteristics

$V_{CC}$ = 12V, -40°C ≤ $T_A$ ≤ 85°C, unless otherwise specified.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCC SECTION (Pin 5)** | | | | | | |
| Maximum operating voltage (Note 1) | $V_{CC(MAX)}$ | | | | 30 | V |
| Start-up threshold | $V_{CC(ST)}$ | $V_{CC}$ rising | 16 | 18 | 20 | V |
| Undervoltage lockout threshold | $V_{CC(UVL)}$ | $V_{CC}$ falling | 7.0 | 7.5 | 8.0 | V |
| Start-up Current | $I_{IN(ST)}$ | $V_{CC}$ = 16V | | 10 | | uA |
| Quiescent current | $I_{CCQ}$ | $V_{CC}$ = 14V, without driver switching | | 3 | | mA |
| Zener breakdown voltage | $V_{ZB}$ | Zener current = 1mA | | 34.6 | | V |
| **VSENSE SECTION (Pin 6)** | | | | | | |
| Input leakage current | $I_{BVS}$ | $V_{SENSE}$ = 1V | | | 1 | uA |
| Nominal voltage threshold | $V_{SENSE(NOM)}$ | $T_A$ = 25°C, negative edge | 1.521 | 1.536 | 1.551 | V |
| Output OVP threshold | $V_{SENSE(MAX)}$ | $T_A$ = 25°C, negative edge | | 1.69 | | V |
| **VIN SECTION (Pin 7)** | | | | | | |
| Maximum operating voltage | $V_{IN(MAX)}$ | | | | $V_{CC}$ | V |
| $V_{IN}$ input resistance | $R_{IN}$ | After start-up | 14.55 | 15 | 15.45 | kΩ |
| Brown-in voltage | $V_{BR\_IN}$ | | | 0.368 | | V |
| Brown-out voltage | $V_{BR\_OUT}$ | | | 0.319 | | V |
| $V_{IN}$ range | $V_{IN}$ | During normal operation | 0 | | 1.8 | V |
| **ISENSE SECTION (Pin 2)** | | | | | | |
| Overcurrent threshold | $V_{OCP}$ | $T_A$ = 25°C, positive edge | | 1.725 | | V |
| CC regulation upper limit | $V_{IPK\_HIGH}$ | $T_A$ = 25°C, positive edge | | 1.38 | | V |
| CC regulation lower limit | $V_{IPK\_LOW}$ | $T_A$ = 25°C, positive edge | | 0.3 | | V |
| Input leakage current | $I_{LK}$ | $I_{SENSE}$ = 1V | | | 1 | µA |
| **OUTPUT SECTION (Pin 4)** | | | | | | |
| Output clamp voltage | $V_{CLAMP}$ | $V_{CC}$ = 18V~30V | 14.5 | 16.5 | 18 | V |
| Rising time | $T_{RISE}$ | $C_L$ = 5nF | | 180 | | ns |
| Falling time | $T_{FALL}$ | $C_L$ = 5nF | | 80 | | ns |
| Peak sourcing current | $I_{SOURCE}$ | $C_L$ = 5nF | 0.2 | 0.6 | 1.2 | A |
| Peak sinking current | $I_{SINK}$ | $C_L$ = 5nF | 0.4 | 1.2 | 1.7 | A |
| Maximum switching frequency (Note 2) | $f_{SW\_MAX}$ | | | 90/72 | | kHz |

## 6 Electrical Characteristics (Cont'd)

$V_{CC}$ = 12V, -40°C ≤ $T_A$ ≤ 85°C, unless otherwise specified.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **NTC/DIM2 SECTION (Pin 1) (Note 3)** | | | | | | |
| NTC bias current | $I_{NTC}$ | | 95 | 100 | 105 | uA |
| NTC operating voltage range | $V_{NTC}$ | | 0.2 | | 1.8 | V |
| PWM frequency range | $F_{PWM2}$ | | 0.5 | | 2 | kHz |
| PWM duty cycle range | $D_{PWM2}$ | | 1 | | 100 | % |
| DIM2 PWM logic high threshold | $V_{TH\_DIM2}$ | Rising edge | | 1.0 | | V |
| **DIM1 SECTION (Pin 8)** | | | | | | |
| PWM frequency range | $F_{PWM1}$ | | 0.5 | | 2 | kHz |
| PWM duty cycle range | $D_{PWM1}$ | | 1 | | 100 | % |
| DIM1 PWM logic high threshold | $V_{TH\_DIM1}$ | Rising edge | | 1.0 | | V |

**Notes:**

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization. Refer to Section 9 for operation details.

Note 2: This parameter is determined by external configuration at the beginning of start-up. See Section 9.3 for details.

Note 3: These parameters are applicable to different product options, defined in Section 11.

## 7 Typical Performance Characteristics

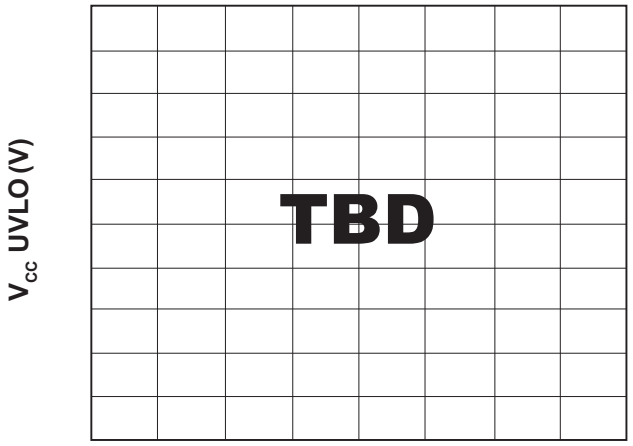



Figure 7.1 : $V_{CC}$ UVLO vs. Temperature

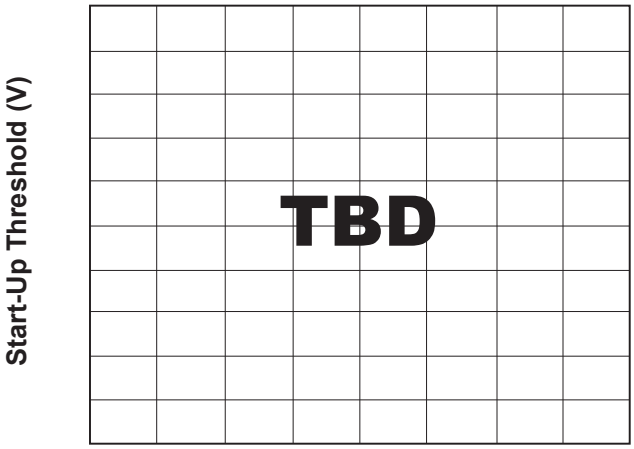



Figure 7.2 : Start-Up Threshold vs. Temperature

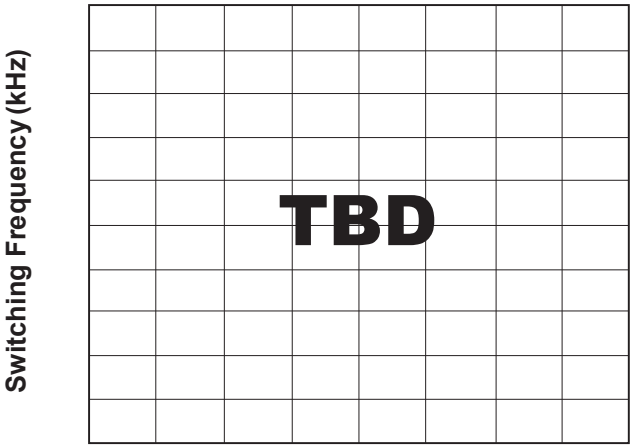



Figure 7.3 : Switching Frequency vs. Temperature

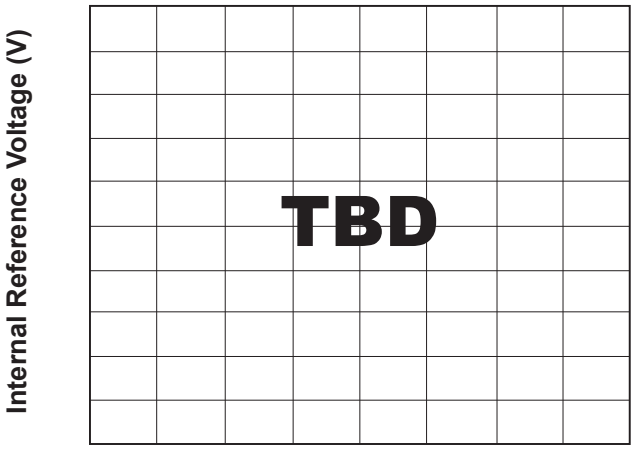



Figure 7.4 : Internal Reference vs. Temperature

## 7 Typical Performance Characteristics (Cont'd)

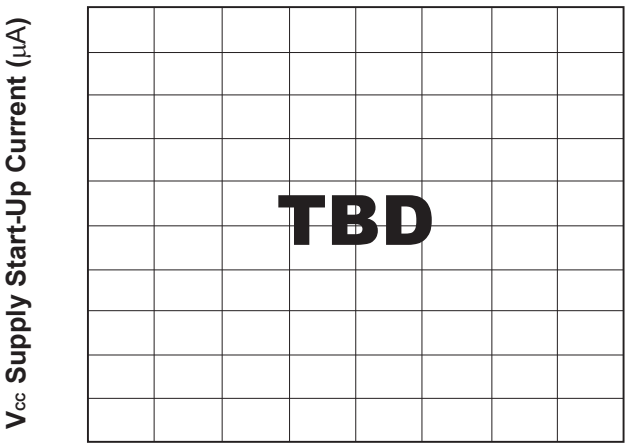



Figure 7.5 : $V_{CC}$ vs. $V_{CC}$ Supply Start-up Current

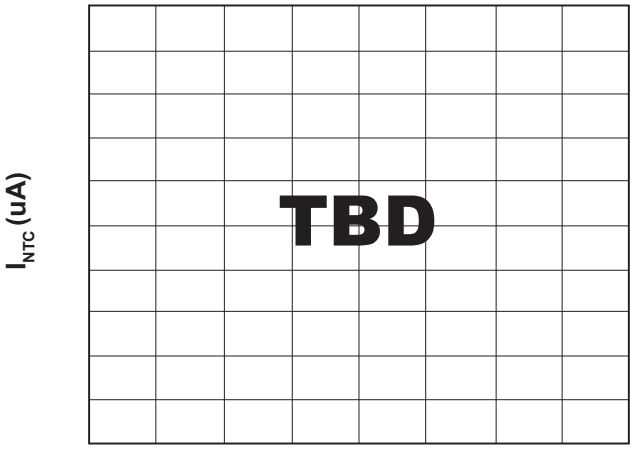



Figure 7.6 : $I_{NTC}$ vs. Temperature

## 8 Functional Block Diagram

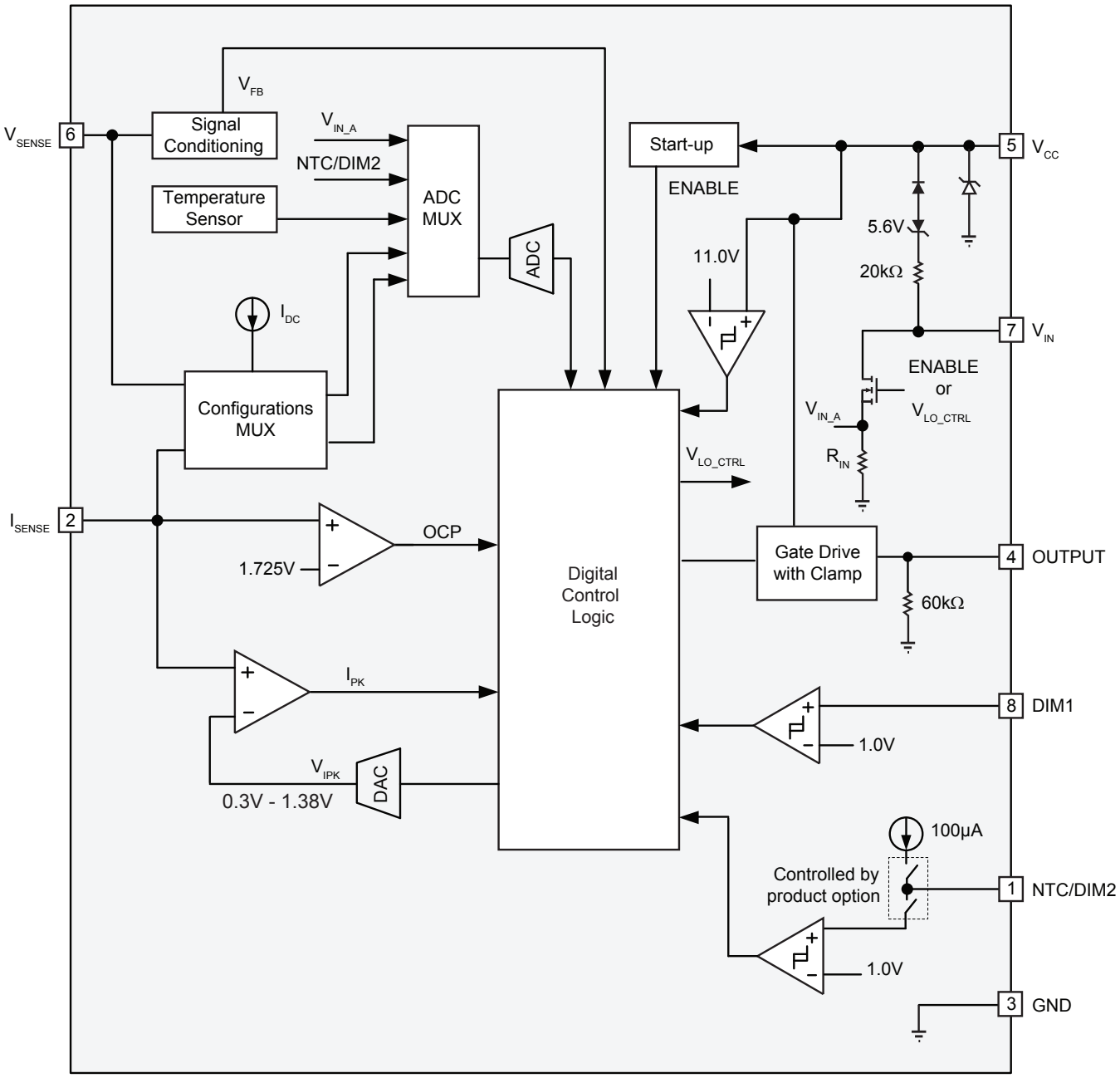



**Figure 8.1 : Functional Block Diagram**

## 9 Theory of Operation

The iW3636 is a digital power controller dedicated for single-stage, off-line PWM dimmable LED drivers with power factor correction. The device uses an innovative, proprietary primary-side control technology to achieve excellent output current regulation without the need for secondary feedback components. The iW3636 provides a dedicated PWM command interface (DIM1) to support wide dimming applications with dimming range from 100% to 1%. Additionally, the device provides a second PWM/Analog command interface (NTC/DIM2) that serves multiple functions: to support output current configuration; a second independent dimming function; or enable NTC-based external temperature detection for thermal derating protection. Furthermore, Dialog's digital control maximizes the iW3636 design performance and flexibility by providing three multi-function pins ($I_{SENSE}$, $V_{SENSE}$ and $V_{IN}$) to configure the IC functions, and it also allows for internal loop compensation to ensure stability to further reduce the solution size and cost.

For proper understanding of the operation of the iW3636, all descriptions in this section refer to Figure 8.1, the functional block diagram. Prior to start-up, the $V_{IN}$ voltage exceeds the $V_{CC}$ voltage by an internal Zener voltage drop (5.6V typically), which allows the active device (depletion-mode or enhancement-mode FET in Figures 3.1 and 3.2) to turn on and charge $V_{CC}$ towards its start-up threshold. Afterwards, the internal resistor $R_{IN}$ is connected and the $V_{IN}$ pin is pulled low to cut off the active device to save power during normal operation, meanwhile it senses the line voltage to generate a reference signal for high power factor correction.

At the beginning of startup, a fixed current source flows out of $I_{SENSE}$ and $V_{SENSE}$ pins alternatively, generating voltage levels proportional to resistance values from the pins to GND, which are then identified by the controller to configure the IC functions such as dimming curve and minimum dimming level. During normal operation, the digital control block constantly reads the signals at the DIM1 and NTC/DIM2 pins, and adjusts the reference current accordingly. The switch on-time and off-time are generated based on the current feedback signal. The $I_{SENSE}$ pin is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the $V_{IPK}$ sets the threshold for the $I_{SENSE}$ to compare with, and it varies in the range of 0.3V (typical) to 1.38V (typical) under different line and load conditions.

The iW3636 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3636 incorporates a number of key built-in protection features, including output short protection (OSP), input brown-in/-out protection, main power MOSFET over-current protection (OCP), and thermal derating and shutdown protection.

### 9.1 Pin Detail

#### Pin 1 – NTC/DIM2

By product option (refer to Section 11): for the -01 option, connect a PWM signal at this pin to dim the output current independently based on the duty cycle of this PWM signal; for the -02 option, connect an NTC resistor from this pin to GND to provide NTC temperature-based thermal derating and shutdown; for the -03 option, connect an analog signal from 0 to 1.8V to dim output current from 0% to 100%.

For -02 option, the device retains internal junction temperature-based over-temperature shutdown (no derating function) and for all other options, the devices enable internal junction temperature-based thermal derating and shutdown as well.

For decoupling purposes, it is recommended to add a ceramic capacitor from this pin to GND. Depending on the pin's functions, the capacitance could be in the range of 100pF to 0.1μF. Care needs to be taken to make sure the capacitance does not cause too much delay to PWM signal that might affect the dimming curve for PWM dimming, or cause too much delay to fail the start-up for NTC option.

**Pin 2 - $I_{SENSE}$**

Provides primary current sense for cycle-by-cycle peak current control and limit. A proper value of ceramic capacitance is recommended to connect from this pin to GND to improve output current line regulation and noise immunity as well.

The $I_{SENSE}$ pin also acts as a configuration pin during startup. See Section 9.3 for additional detail.

**Pin 3 – GND**

Ground.

**Pin 4 – OUTPUT**

Gate drive for external power FET switch; the maximum voltage is clamped to 16.5V (typical) when $V_{CC}$ is high.

**Pin 5 – $V_{CC}$**

Power supply for the controller during normal operation. The controller starts up when $V_{CC}$ voltage reaches 18.0V (typical) and shuts down when the $V_{CC}$ voltage drops below 7.5V (typical) respectively. A decoupling capacitor of 0.1µF or higher should be connected closely between $V_{CC}$ pin and GND.

In the iW3636, the maximum $V_{CC}$ voltage is 30V. When the selected active start-up device has a $V_{GS}$ rating less than 30V, it is required to add a blocking diode between the source of the active device and $V_{CC}$ to protect the device.

**Pin 6 – $V_{SENSE}$**

Used to sense output voltage for primary-side regulation. A low forward drop diode (like Schottky diode) is recommended to connect from this pin to GND to shunt negative current going to this pin. Additionally, a proper capacitance is recommended to add from this pin to GND for decoupling purposes as well as valley mode switching.

The $V_{SENSE}$ pin also acts as a configuration pin during startup. See Section 9.3 for additional detail.

**Pin 7 – $V_{IN}$**

Used to sense input line voltage and control active device. After ENABLE is pulled high, the internal 15kΩ (typical) resistor is connected to sense the input line voltage, meanwhile the pin voltage stays low enough (≤ 1.8V) to cut off the active startup device to minimize no-load standby power consumption and improve active operating efficiency. A decoupling capacitor of approximately 3.3nF or higher should be connected closely between this pin to GND.

During light-off operation, when $V_{CC}$ voltage is below 10.0V (typical), the 15kΩ resistor is disconnected to allow $V_{CC}$ charge via the active startup device before $V_{CC}$ hits its UVLO and causes shutdown, refer to Section 9.8 for the details.

**Pin 8 – DIM1**

PWM dimming input detection. The device detects PWM duty cycle via an edge comparator and sets the output current target accordingly. For decoupling purpose, a ceramic capacitor of approximately 100pF is recommended to connect from this pin to GND.

## 9.2 Active Start-up and Adaptively Controlled Soft-start

The iW3636 features a proprietary soft-start scheme to achieve fast yet smooth ramp-up of the output current for a variety of operating conditions. In addition, the active start-up scheme enables the shortest possible turn-on delay without sacrificing efficiency.

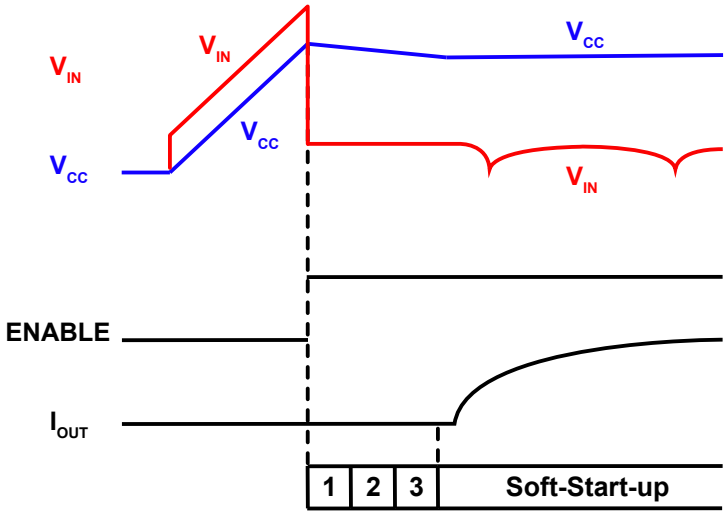
Refer to Figure 8.1 for the block diagram and Figures 3.1 and 3.2 for the active start-up circuit using external

depletion-mode NFET and enhancement-mode NFET respectively. Prior to start-up, the internal ENABLE signal is low, and the $V_{IN}$ pin voltage closely tracks the $V_{CC}$ pin voltage with a certain voltage (typically 5.6V) above $V_{CC}$, as shown in Figure 9.1. Consequently, the NFET (either depletion-mode or enhancement-mode) is turned on, allowing the start-up current to charge the $V_{CC}$ bypass capacitor. When the $V_{CC}$ bypass capacitor is charged to a voltage higher than the start-up threshold (typically 18.0V), the ENABLE signal becomes active and activates the control logic. It turns on the internal switch and pulls $V_{IN}$ pin to ground via the resistor $R_{IN}$. During normal operation, the $R_{IN}$ and the $V_{IN}$ external resistors form a voltage divider to sense the input voltage, and feeds the signal, $V_{IN\_A}$ to the internal ADC. Afterwards, the iW3636 begins to perform $I_{SENSE}$ pin and $V_{SENSE}$ pin configuration (See Section 9.3), and followed by internal OTP and external OTP check (See Sections 9.15 and 9.16). Due to the capacitance at $V_{IN}$ pin, the IC reserves 2ms or so to allow $V_{IN\_A}$ voltage to settle from a voltage higher than $V_{CC}$ (typically 5.6V) to a voltage truly reflecting the line voltage, before it performs input brown-in protection. Once $V_{IN\_A}$ is higher than $V_{BRN\_IN}$, the iW3636 begins a soft-start process, during which the iW3636 identifies dimming inputs and ramps up output current in a fast yet smooth pattern, or, put output in the “light-off” state (i.e. LED is off) by regulating the output voltage to a predetermined value, when the dimming input is zero.

As the ENABLE initiates the control logic, it also pulls down the $V_{IN}$ pin voltage at the same time, which turns off the start-up FET, thus eliminating the start-up resistors power consumption during normal operation.

If at any time the $V_{CC}$ voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, then the iW3636 goes to shutdown. At this time, the ENABLE signal becomes low, and the $V_{CC}$ capacitor begins to charge up again towards the startup threshold to initiate a new start-up process.

In applications where the active start-up is not needed, the start-up resistors can be directly connected to the $V_{CC}$ pin without using the active start-up device, or they can be omitted if AC turn-on delay is not critical.




1. $I_{SENSE}$ and $V_{SENSE}$ configuration
2. OTP check
3. $V_{IN}$ brown -in check

**Figure 9.1 : Start-up Sequencing Diagram**

## 9.3 Configurations

The iW3636 allows users to configure several application parameters such as dimming curve, maximum switching frequency, light-off or minimum current clamp selection to provide design flexibility. The configurations of the parameters are only performed once after ENABLE signal is active, and completed before the thermal shutdown check. The configurations involve $I_{SENSE}$ and $V_{SENSE}$ pins and some resistors connected to the pins, each enabling multi-level configuration.

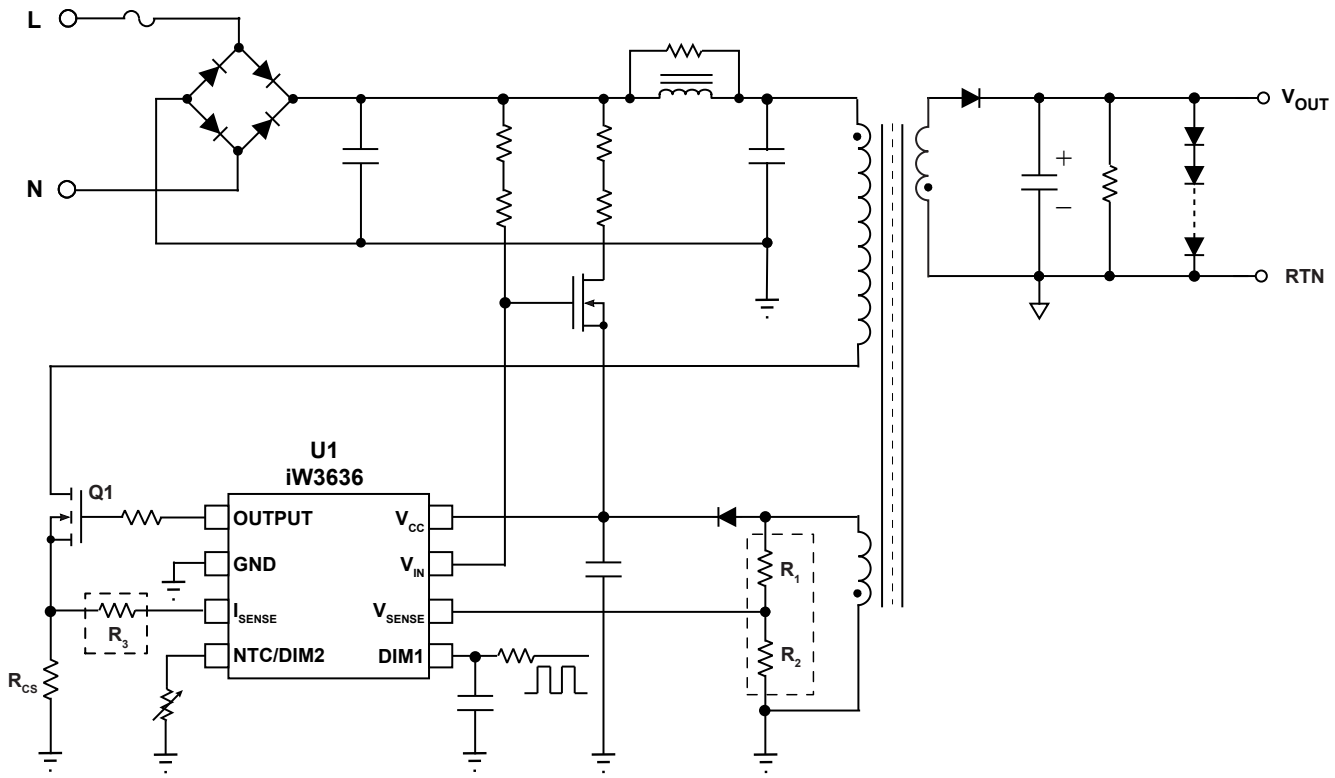



**Figure 9.2 : Typical Application Circuit Highlighting Configuration Resistors**

Figure 9.2 shows the schematic highlighting the resistors used for configurations. During the configurations, the iW3636 holds the OUTPUT pin low, and the switch $Q_1$ remains in off-state. A fixed current flows out of the $I_{SENSE}$ pin, which generates a voltage proportional to the resistance value of $R_3$ and $R_{CS}$ (in series, where $R_{CS}$ is negligible compared to $R_3$). The internal digital control block identifies the resistance value between the $I_{SENSE}$ pin to ground, and then sets the control algorithm accordingly. Table 9.1 lists the resistance range of $R_3$ for configurations.

| Configurations | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| $R_3$ range (kΩ) | 0.1 ~ 0.35 | 0.45 ~ 0.53 | 0.67~0.76 | 0.94~1.09 | 1.31~1.51 | 1.79~2.11 | 2.49~2.94 | 3.45~4.0 |
| Lowest Dimming State | Output Current Clamped at Minimum Dimming Level | | | | Light-off - Output Current Goes to Zero when below Minimum Dimming Level | | | |
| Remapping | No remap | Remap | Remap | Remap | No remap | Remap | Remap | Remap |
| Minimum Dimming Level | 1% | 1% | 5% | 10% | 1% | 1% | 5% | 10% |

**Table 9.1: $I_{SENSE}$ Pin Configurations – Functions and Recommended Resistance Range**

Following the completion of configuring $I_{SENSE}$ pin, the iW3636 enters the stage of configuring the $V_{SENSE}$ pin. During this stage, switch $Q_1$ still remains in off-state, and a fixed current flows out of the $V_{SENSE}$ pin and generates a voltage proportional to the paralleled resistance of $R_1$ and $R_2$. The paralleled resistance of $R_1$ and $R_2$ is used to set one of 7 possible configuration states. During normal operation, the ratio of $R_1$ and $R_2$ determines the voltage level the iW3636 regulates at during constant voltage operation. Based on the two equations, $R_1$ and $R_2$ can be derived. Table 9.2 lists the resistance range of paralleled $R_1$ and $R_2$ for each configuration option.

| Configurations | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Paralleled $R_1$ and $R_2$ range (kΩ) | 1.59~1.65 | 2.44~2.54 | 3.49~3.65 | 4.88~5.10 | 6.83~7.13 | 9.54~9.98 | 13.39~14.0 |
| No-load Output Voltage | ½ of no-load CV voltage | | | | ⅓ of no-load CV voltage | | |
| Dimming Curve | Linear | Linear | Log | Log | Linear | Linear | Log |
| Maximum $F_{SW}$ | 72kHz | 90kHz | 72kHz | 90kHz | 72kHz | 90kHz | 72kHz |

**Table 9.2: $V_{SENSE}$ Pin Configurations – Functions and Recommended Resistance Range**

### 9.3.1 Configured Parameters

For $I_{SENSE}$ configurations, there are three parameters for selection. The first parameter determines whether the output current is clamped to a minimum level or goes to zero (i.e light-off) at deepest dimming. The second parameter determines whether the duty cycle information at DIM1 pin needs to be remapped or not, and the third parameter is the minimum current setting: 1%, 5% or 10% for “Remap” options, and 1% for “No remap” options. Note, the PWM dimming option at NTC/DIM2 pin does not have the “Remap” function.

The iW3636 receives, via an optocoupler, a PWM signal from the secondary-side to the primary-side for 0-10V dimming applications. The iW3636 works with a companion IC, the iW339, which sends a 0% to 100% PWM duty cycle signal that corresponds to the dimmer voltage of 0 to 9V, linearly. On the iW3636 side, the resulting 94.4% and above duty cycle is remapped to 100% and the 11.1% and below duty cycle is remapped to 1%, 5% or 10% depending upon the selected configuration option discussed in Section 9.3. For duty cycles in between 94.4% and 11.1%, the duty cycle is linearly remapped by the iW3636. For PWM signals with good fidelity (e.g. wireless PWM dimming), “No remap” can be selected to allow the PWM input to directly set the output current proportional to the duty cycle.

For Figures 9.3a and 9.3b, please refer to Table 9.1 for the $I_{SENSE}$ configuration states explained here. In Figure 9.3a ($I_{SENSE}$ configuration state 4 - 10% minimum dimming level; 10% lowest dimming state), the minimum PWM duty cycle after remap is clamped to 10% when the input PWM signal at DIM1 pin drops to 11.1% or below; in Figure 9.3b ($I_{SENSE}$ configuration state 8 - 10% minimum dimming level; light-off mode - output current to zero at lowest dimming state), the minimum PWM duty cycle is first clamped to 10% when the input PWM signal at DIM1 pin is between 11.1% to 5.5%, and enters into light-off mode when it is below 5.5%. There is 1.1% hysteresis for the output current to come back to the minimal clamped level.

For the “No-remap” option, the duty cycle threshold for the PWM signal to enter “light-off” mode is 0%. Due to digital resolution, the light is turned off when the duty cycle is less than 0.4% and it recovers when the duty cycle is above 1.2%.

For $V_{SENSE}$ configurations, there are also three parameters to be selected. The first parameter is to choose whether the output voltage at light-off is ½ or ⅓ of the nominal CV voltage (Section 9.12). The second parameter is to select the dimming curve: linear or logarithmic (See Section 9.6). The third parameter is for the maximum switching frequency: 72kHz or 90kHz.

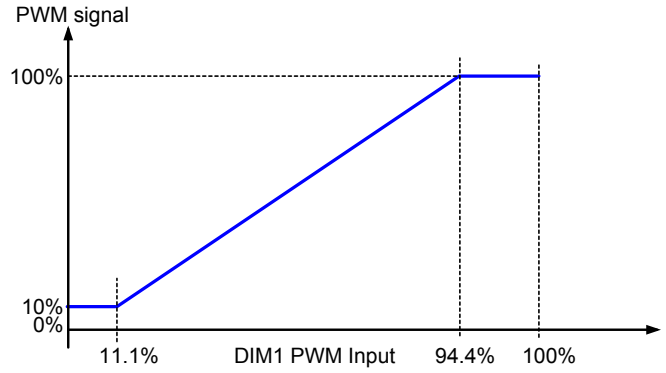



**Figure 9.3a: PWM Duty Cycle Remapping**
**$I_{SENSE}$ Configuration #4**

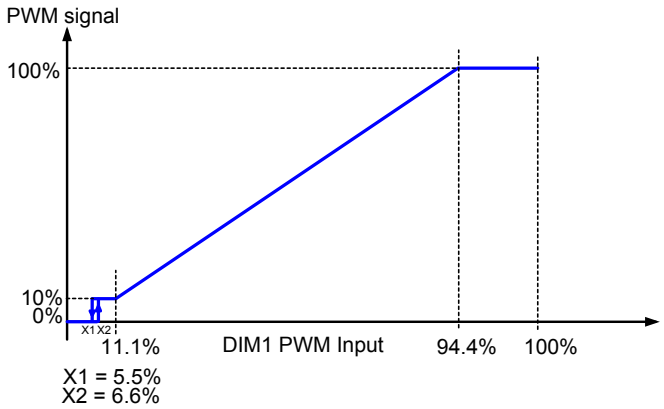



**Figure 9.3b: PWM Duty Cycle Remapping**
**$I_{SENSE}$ Configuration #8**

## 9.4 Understanding Primary Feedback

Figure 9.4 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance $L_M$. The rectifying diode D1 is reverse biased and the load current $I_O$ is supplied by the secondary capacitor $C_O$. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

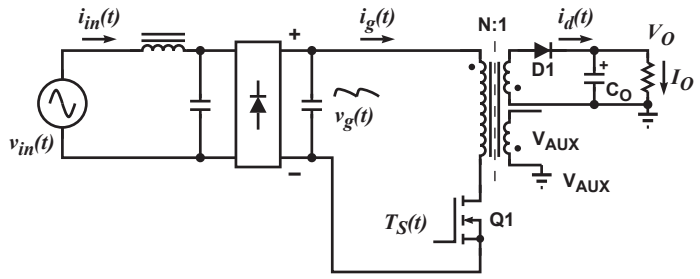



**Figure 9.4 : Simplified Flyback Converter**

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance ($L_M$). During the Q1 on-time, the load current is supplied from the output filter capacitor $C_O$. The voltage across $L_M$ is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1 turns off at $t_O$, $i_g(t)$ in $L_M$ forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance $L_K$ at the instant of turn-off $t_O$, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

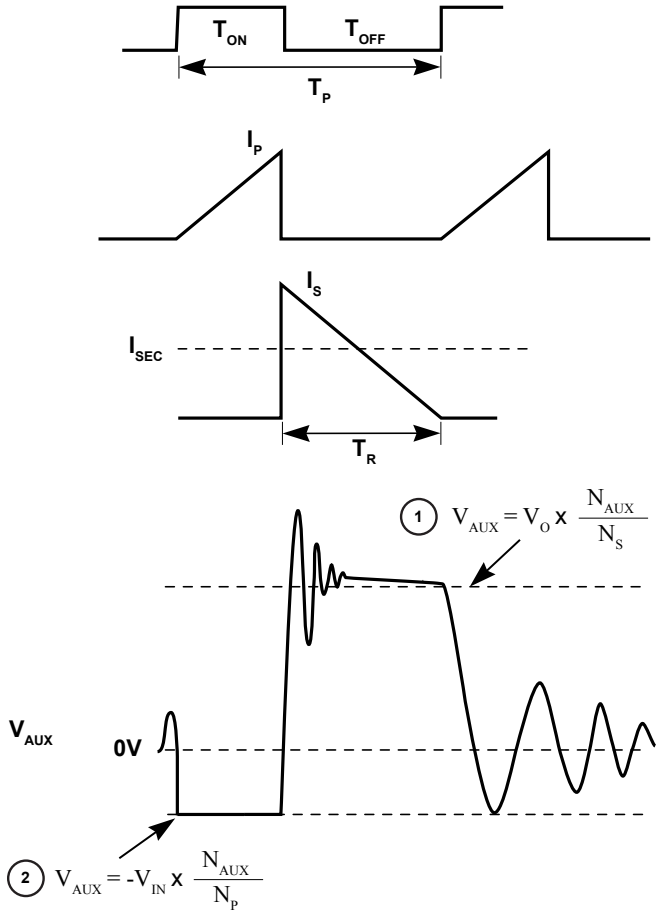



**Figure 9.5 : Drive, Primary and Secondary Currents and Auxiliary Voltage Waveforms**

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.5.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW3636, ΔV can be ignored.

## 9.5 LED Constant Current (CC) Operation

In the iW3636, peak current regulation is achieved by forcing the peak value of the primary-side current to follow the reference $V_{IPK}$ in every switching cycle. In the iW3636, the reference $V_{IPK}$ is designed to be proportional to the input voltage shape with a lower limit of 0.1V. When the main switch (Q1 in Figure 9.2) turns on, the transformer primary winding current ramps up linearly and energy builds up in the transformer. The iW3636 turns off the FET when the primary winding current reaches the peak current regulation level. At this moment, the transformer maintains the magnetic flux such that the energy in the transformer generates the secondary winding current equal to the peak winding current multiplied by the turns ratio (primary-secondary). Then the secondary winding current ramps down linearly until all the energy in transformer is discharged. After the energy in the transformer is discharged, the iW3636 starts the next switching cycle.

As shown in Figure 9.5, the averaged secondary current of the transformer can be expressed by an equation as shown below.

$$I_{SEC} = 0.5 \times N_{TR} \times I_{PK} \times T_R / T_P \qquad (9.6)$$

Where $I_{PK}$ is the peak value of primary winding current. $N_{TR}$ is the primary-secondary turns ratio. $T_R$ is the secondary winding current ramp-down time, or the transformer reset time. $T_P$ is the entire period.

The $I_{PK}$ is determined by the voltage generated on the current-sense resistor: $I_{PK} = V_{IPK} / R_{CS}$. Therefore, the equation can be written as:

$$I_{SEC} = 0.5 \times N_{TR} \times V_{IPK} / R_{CS} \times T_R / T_P \qquad (9.7)$$

In the steady state, the average output current is equal to the average transformer secondary current over one-half AC cycle. Therefore, the average output current can be obtained by averaging equation 9.7 over one-half AC cycle.

In the iW3636, the average output current $I_{OUT}$ can be determined by the equation 9.8.

$$I_{OUT} = 0.5 \times DIM \times N_{TR} / R_{CS} \times 0.4 \times \eta \qquad (9.8)$$

Where η is the transformer conversion efficiency, 0.4 is the reference voltage and DIM is the combination of the two dimming inputs.

## 9.6 Dimming Interface and Dimming Control

The iW3636 provides two dimming interface pins which can work separately or together to dim the output current from 100% to 1% with 1% resolution. The DIM1 pin accepts a standard square-wave PWM signal. By product options, the NTC/DIM2 pin can accept a standard square-wave PWM signal, or an analog signal from 0 to 1.8V to dim the output current. The dimming range for PWM dimming is still 1% to 100% with 1% resolution. For analog dimming, 1.8V or above corresponds to 100% dimming, and 0V corresponds to 0% dimming. The linearity is ensured over the voltage range.

When both dimming inputs are in play, the output current is determined by the multiplication of the two dimming inputs.

The iW3636 provides two types of dimming curves: linear and logarithmic, as shown in Figure 9.6.

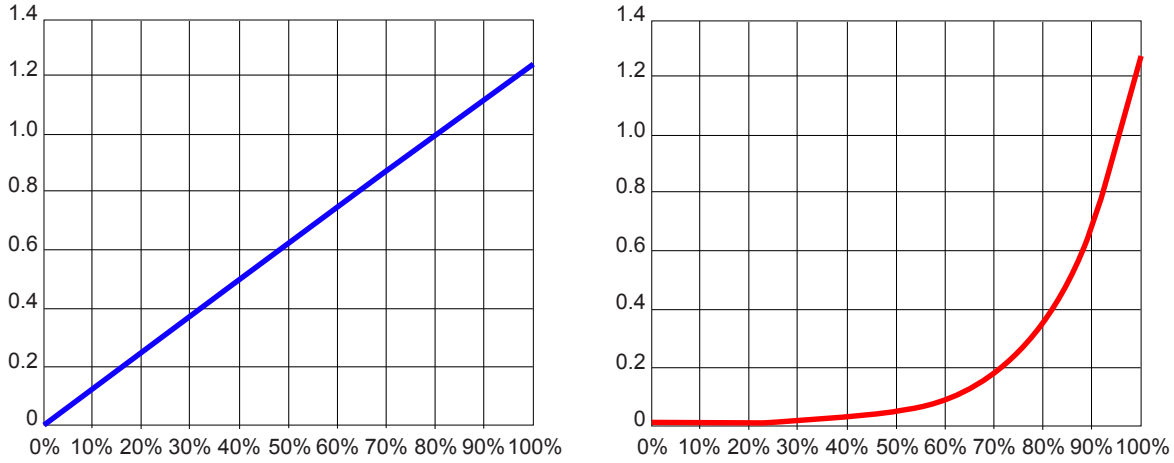



**Figure 9.6 : Linear and Log Dimming Curves**

## 9.7 LED Current Line Regulation

The iW3636 uses a unique technology to improve LED current regulation across line voltages by using a simple RC network ($R_{CMP}$/$C_{CMP}$) as shown in Figure 9.7 along with a proprietary internal circuitry. This allows LED drivers designed with the iW3636 to achieve excellent line regulation over a broad line voltage range.

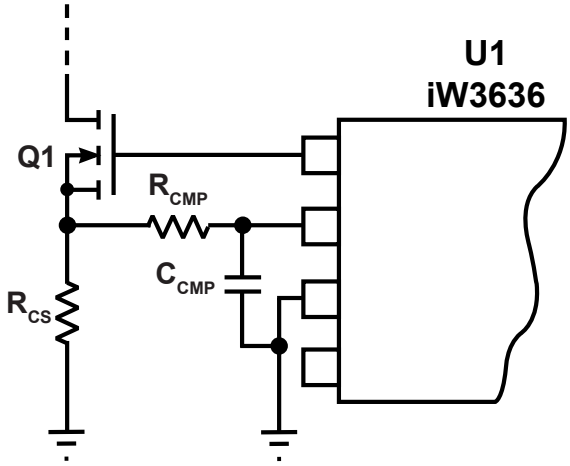



**Figure 9.7 : Compensation for LED current**

## 9.8 Dim_to_Off and Soft-Off

When the $I_{SENSE}$ pin configuration is set to levels 5 to 8, the iW3636 can respond to dimming commands and put the LED into “light-off” mode. When either of the dimming inputs is “0” (zero duty), the iW3636 gradually drops the output voltage to a level which is stipulated in the $V_{SENSE}$ configuration – it can put the output voltage to ½ or ⅓ of no-load CV voltage (Section 9.12) to keep the LED off. During start-up, the iW3636 checks the dimming input, and may enter into “light-off” mode if the dimming input is zero. Any dimming level larger than 1.2% can wake up the system and smoothly transition from this state to CC operation. During normal CC operation, the system can also enter into “light-off” mode if requested. During the transition, the iW3636 waits for the output voltage to drop to the predetermined value, which

can take some time due to the RC time constant associated with output capacitors and pre-load resistors. During this mode of operation, the iW3636 uses the active start-up device to maintain the $V_{CC}$ voltage between 10.0V-11.0V to ensure proper functionality. After the $V_{SENSE}$ signal detects that the output voltage is close to the predetermined value, the device disables the active start-up device and relies on the auxiliary winding to sustain $V_{CC}$, while the device switches in an attempt to keep the output voltage around its predetermined value.

Figure 9.8 shows the transition from normal CC operation to light-off state. As seen, $V_{IN}$ is pulled high and low to keep $V_{CC}$ in the small voltage band. For light-off steady-state, $V_{IN}$ is pulled low to disable the active device to save standby power consumption.

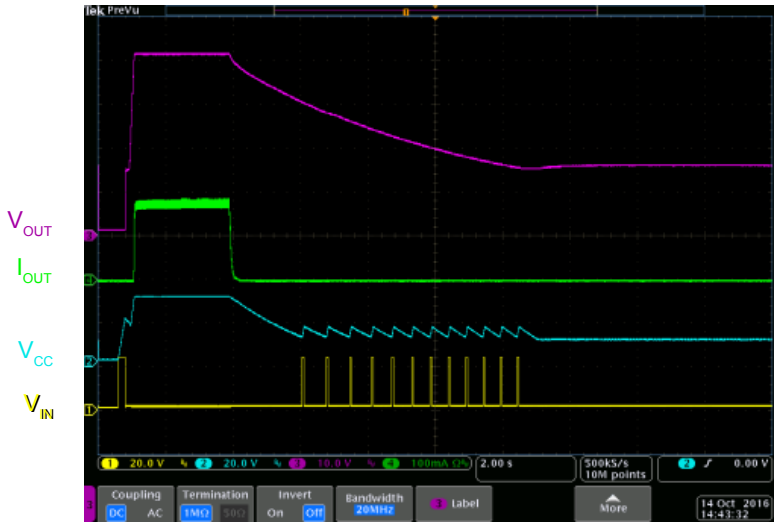



**Figure 9.8 : Dim-to-Off - Normal CC Operation to Light-Off State**

The iW3636 provides a “soft-off” feature when transitioning the output into the light-off state. When the device receives zero dimming command, it softly turns off light by gradually reducing the output current. When the dimming command is above zero but less than 0.4%, then device turns off the output current very quickly. Figure 9.9 shows the current waveforms for the two cases.

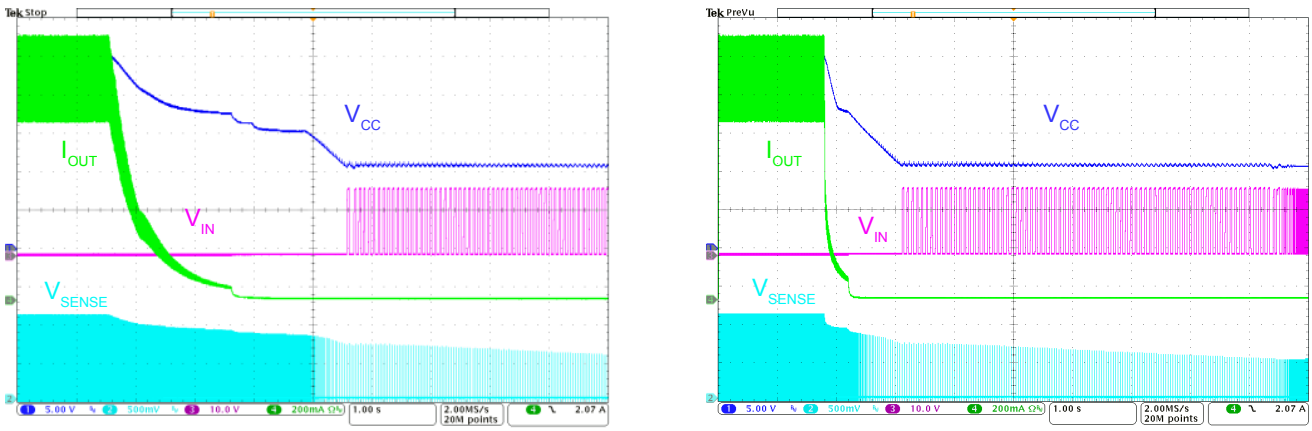



**Figure 9.9 : a) Soft-off ; b) Non-soft-off**

## 9.9 Quasi-Resonant Switching

The iW3636 incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn-on for every switching cycle. Note, a small ceramic capacitor may be required to connect from $V_{SENSE}$ to GND to generate a proper delay between $V_{SENSE}$ and $V_{DS}$ for valley-mode turn-on. In valley-mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.10). By switching at the lowest $V_{DS}$, the switching loss will be minimized.

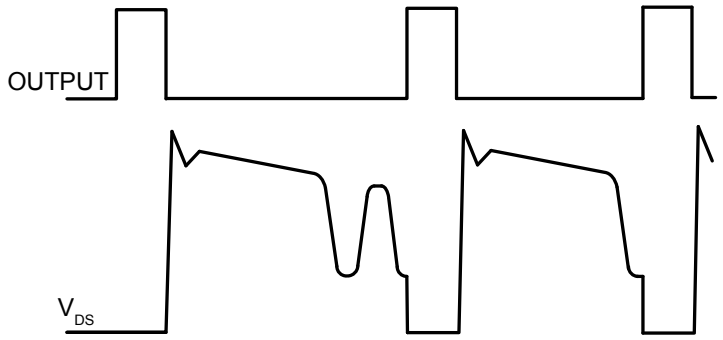
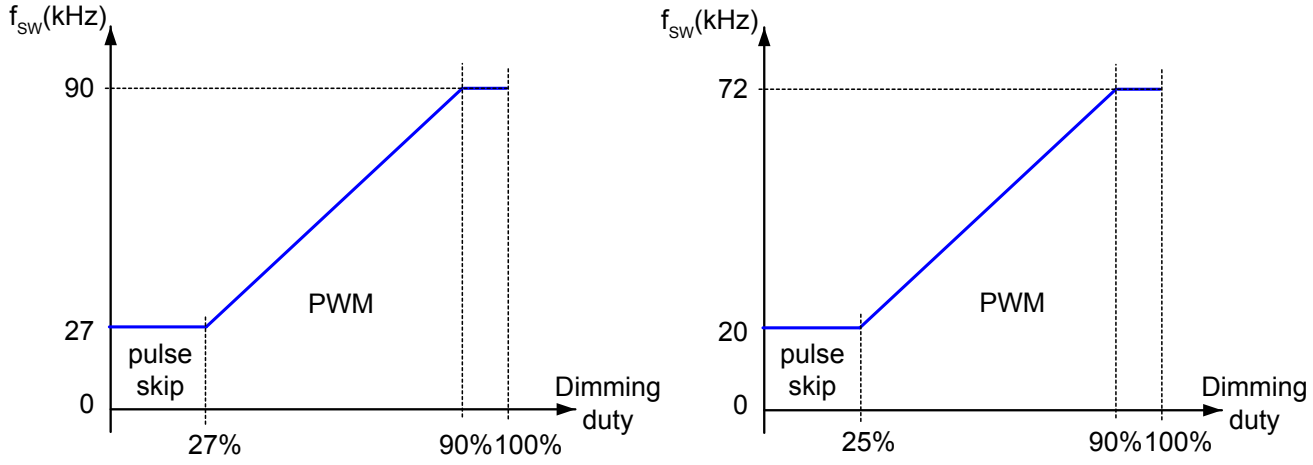



**Figure 9.10 : Valley Mode Switching**

Turning on at the lowest $V_{DS}$ generates lowest dV/dt, thus the valley mode switching can also reduce EMI. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI.

## 9.10 Variable Switching Frequency Control

The iW3636 has two main operating modes, i.e., pulse-width modulation (PWM) mode at high dimming levels and pulse-skip mode at low dimming levels. As a distinctive feature, the iW3636 varies the nominal switching frequencies at PWM mode according to the dimming inputs. Figure 9.11 shows the relationship between the switching frequency and dimming duty input.




(a) when maximum $f_{SW}$ is configured to 90kHz

(b) when maximum $f_{SW}$ is configured to 72kHz

**Figure 9.11 : Adaptive Switching Frequency Control**

Note, Figure 9.11 specifies the maximum switching frequency at a given dimming level. Since the iW3636 always attempts to achieve quasi-resonant switching, waiting for the valley to occur after the maximum switching period elapses, therefore in practice, the switching frequency is usually a little lower than the specified numbers.

As the output current dims down, the IC enters into pulse-skip mode. At this mode, the $I_{SENSE}$ current command $V_{IPK}$ is set to 0.35V and the switching-frequency is either 27kHz or 20kHz, depending upon the $V_{SENSE}$ frequency configuration. The output current is calculated on a cycle-by-cycle basis. When the output current is larger than the target value, the next switching pulse will be skipped; otherwise the next switching pulse occurs as normal at 27kHz or 20kHz.

## 9.11 Internal Loop Compensation

The iW3636 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

## 9.12 Output Open/Short and Output Over-voltage Protections

The iW3636 provides a loosely controlled constant voltage (CV) operation for LED open protection. In this state, the current command is fixed at 0.35V, with the switching period selected between 40µs and 40ms. When the knee point of $V_{SENSE}$ (corresponding to the point 1 of $V_{AUX}$ in Figure 9.5) is below the nominal voltage set by $V_{SENSE(NOM)}$, the switching period is set to 40µs. If the knee point is higher than or equal to $V_{SENSE(NOM)}$, then the switching period is set to 40ms. Depending on the output capacitor and its preload, the output voltage at no-load condition is regulated with the $V_{SENSE}$ knee voltage around $V_{SENSE(NOM)}$.

In normal CC mode, the iW3636 operates with the output voltage below $V_{SENSE(NOM)}$. After the LED opens, the output voltage rises higher momentarily. Depending on the output capacitor and LED operating current, the system may gradually settle down and stay regulated at constant voltage operation at the no-load condition. Under an extreme case, if the output voltage exceeds the output OVP threshold set by $V_{SENSE(OVP)}$ in Section 6, the iW3636 shuts down.

Output short fault is detected via $V_{SENSE}$ pin. When the knee point of $V_{SENSE}$ (corresponding to the point 1 of $V_{AUX}$ in Figure 9.5) is below 115mV for several consecutive cycles, the iW3636 shuts down.

When any fault condition is met, the IC remains biased to discharge the $V_{CC}$ supply. Once $V_{CC}$ drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

## 9.13 Brown-in and Brown-out Protection

The iW3636 provides input under-voltage protection. After the ENABLE signal becomes high, the $V_{IN}$ switch turns on and it is connected to $V_{IN\_A}$. The $V_{IN\_A}$ is determined by

$$V_{IN\_A} = R_{IN} / (R_{IN}+R_{EXT}) * V_{BUS} \qquad (9.9)$$

Where, the $R_{IN}$ is an internal resistor connected from $V_{IN\_A}$ to ground (15kΩ typical, see Figure 8.1); $R_{EXT}$ is the external resistor connected from the $V_{IN}$ pin to the rectified line voltage, which is denoted as $V_{BUS}$. After ENABLE is active, the control logic waits for 2ms or so to allow $V_{IN\_A}$ to settle from a voltage higher than $V_{CC}$ to its normal operating level before starting the input voltage brown-in check. Once the $V_{IN\_A}$ is detected higher than the $V_{BR\_IN}$ level, the iW3636 starts and begins a soft-start function. During normal operation, the iW3636 continues to monitor the line voltage via $V_{IN\_A}$. If $V_{IN\_A}$ is lower than $V_{BR\_OUT}$ for several consecutive line cycles, the brown-out fault is triggered and the iW3636 shuts down. When the fault occurs, the IC stays biased to discharge the $V_{CC}$ supply until it drops below the UVLO threshold, then the controller resets itself and initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

## 9.14 PCL, OCP, and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection ($S_{RSP}$) are features built into the iW3636. With the $I_{SENSE}$ pin the iW3636 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. During normal operation, the peak primary current multiplied by the $I_{SENSE}$ resistor ($R_{CS}$ in Figure 9.2) is limited to 1.38V. If under any abnormal case where the voltage is greater than 1.725V, over-current is detected and the IC immediately turns off the output driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW3636 shuts down.

If the $I_{SENSE}$ resistor is shorted there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault in the first two switching cycles during start-up and shut down the system immediately. Additionally, during normal operation, there is a $V_{IN}T_{ON}$ limit (defined as product of $V_{IN}$ and on-time in μs) which cannot go beyond 1500 v.μs (with $V_{IN}$ sense ratio of 0.0035). If the IC detects $V_{IN}T_{ON}$ limit is hit for consecutive 16 cycles, the system shuts down. Care needs to be taken during design to ensure $V_{IN}T_{ON}$ does not hit the limit during normal operation.

Like other protections, after shutdown, $V_{CC}$ is discharged since the IC remains biased. Once $V_{CC}$ drops below the UVLO threshold, the controller resets itself and then initiates a new start-up cycle. The controller continues attempting to start-up, but does not fully start-up until the fault condition is removed.

## 9.15 Internal OTP and Current-Derating

The iW3636 incorporates a distinctive internal over-temperature protection (OTP) with current-derating function. Before the soft-start process is initiated, the part first checks the junction temperature. If the junction temperature is above 130°C, then the system does not start up. Once the part starts up, the thermal shutdown temperature increases to 150°C. However, during normal operation, before the junction temperature reaches 150°C, the part first derates the output current in predetermined steps in an attempt to reach thermal equilibrium before thermal shutdown kicks in. This way, the part stays in a safe operation meanwhile maximizing output current.

Figure 9.12 shows the output current derating function. In this example, the LED current starts to derate the output current when the junction temperature hits 100°C and continues to derate the current as the temperature hits the next derating thresholds (110°C, 120°C, 130°C). For each derating, the output current drop is roughly 7.5% of the nominal operating current. In addition, each derating step consists of a couple of small steps taking place in a second or so. In this way, the output current drops gradually, so that there is no visual observation of any flicker during current derating process.

The over-temperature derating function operates in between 100% of rated output current and 70% rated output current set by DIM1. If the input to DIM1 is less than 70% and a thermal event occurs, the iW3636 does not derate the output current since 70% is the lowest derating level, relying upon the thermal shutdown threshold to protect the circuit. If a thermal event occurs at 70% dimming or below in normal ambient temperature conditions, an improved thermal design is recommended.

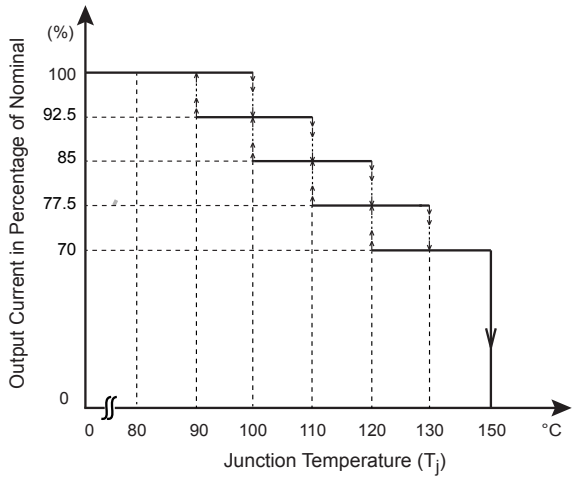



**Figure 9.12 : Internal OTP Thermal Derating**

## 9.16 External OTP and Current-Derating

Alternatively, the iW3636 also has a product option that uses an NTC resistor to sense external temperature and provide similar current-derating function, as shown in Figure 9.13. During normal operation, the internal current source of 100µA passes through the NTC resistor and generates a voltage proportional to the NTC resistance. As the NTC resistance varies as a function of temperature at which it is exposed to, the resulting voltages across the NTC resistor reflects different temperatures. In Figure 9.13, the numbers in the abscissa represent the voltages across the NTC resistor, via which, the external temperature information can be extracted for a given NTC resistor.

The operation of external OTP and current derating is similar to that of the internal OTP derating in Section 9.15. The iW3636 starts to derate the output current when the voltage across the NTC resistor hits corresponding thresholds. Similarly, the iW3636 retains hysteresis for each derating, with each derating step-size predetermined to 7.5%. Note the device shuts down when the NTC resistor voltage is below 0.374V, and it can only start up when the voltage is above 0.581V.

Similar to internal OTP current-derating, the external NTC-based derating is also related to DIM1 input. The output current is determined by the smaller between the currents set by DIM1 input or by the derating target. And, similar to the internal OTP functionality explained in Section 9.15, if the DIM1 pin sets the output current to 70% or below, no derating occurs when the temperature rises above the derating trip point. Improved thermal design needs to be done if this scenario arises under normal circumstances. The design will still be protected by the internal thermal shutdown.

For the product options with NTC derating function, the internal derating function is disabled. When the internal junction temperature reaches 150°C during normal operation, IC shuts down, and only recovers when the junction temperature drops below 130°C.

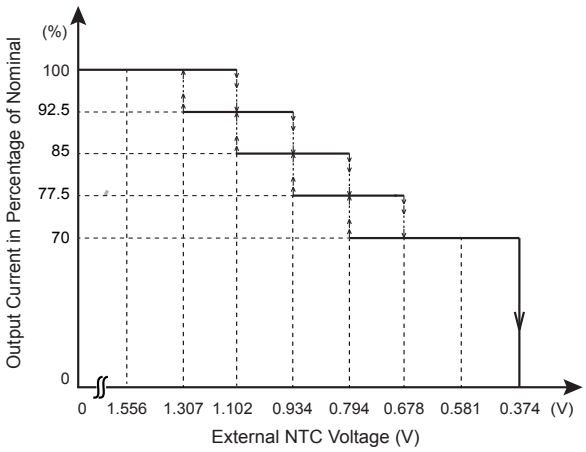
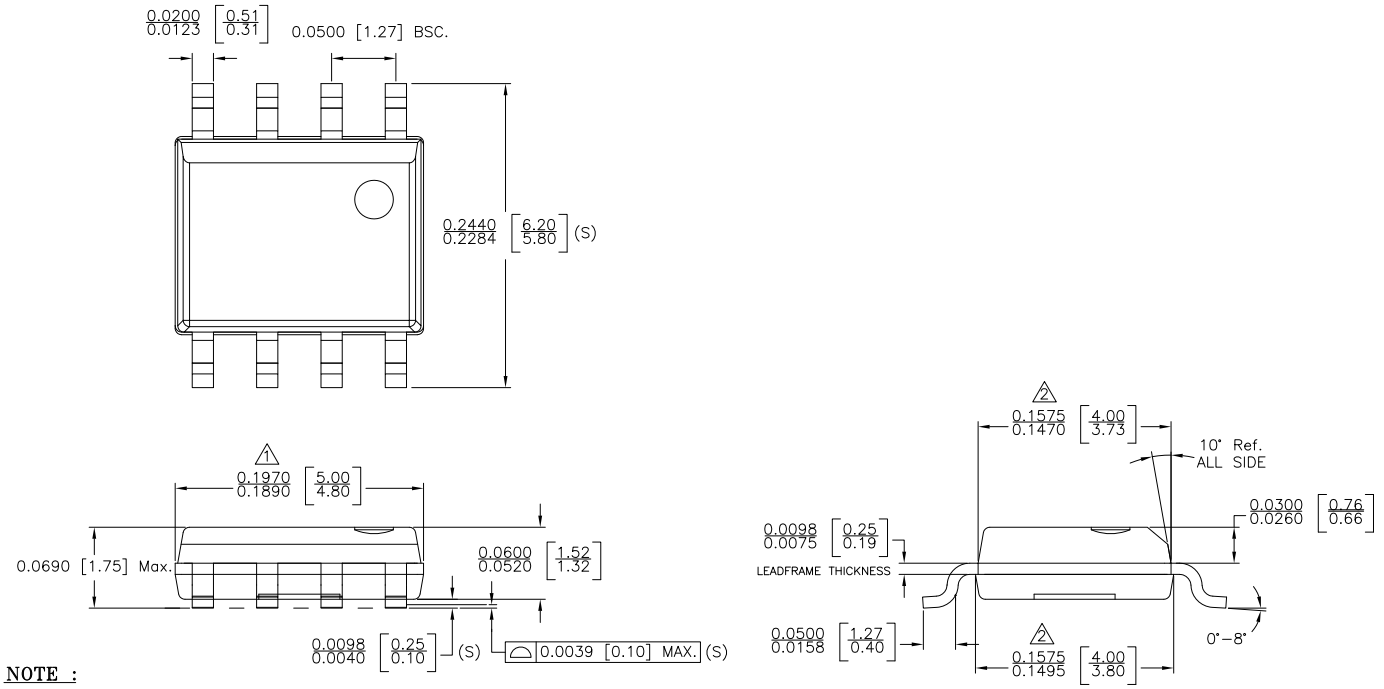



**Figure 9.13 : External OTP Thermal Derating**

## 10 Physical Dimensions




NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS–012.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROLLING DIMENSIONS IN INCHES. [mm]

| | |
|---|---|
| STATUS: RELEASED | SCALE: DO NOT SCALE |
| TERMINAL FINISH: 100% Sn or NiPdAu (PPF) | |
| TITLE: 8 SOIC PACKAGE OUTLINE | |
| REV: A | REVISION NOTE: NEW DRAWING — DATE: 02–MAR–2015 |

## 11 Ordering Information

| Part no. | Options | Package | Description |
|---|---|---|---|
| iW3636-01 | PWM DIM2 interface | SOIC-8 | Tape & Reel[1] |
| iW3636-02 | NTC DIM2 interface | SOIC-8 | Tape & Reel[1] |
| iW3636-03 | Analog DIM2 interface | SOIC-8 | Tape & Reel[1] |

**Note 1: Tape and reel packing quantity is 2,500/reel. Minimum ordering quantity is 2,500.**

# Single-Stage LED Driver with PFC
# Supports Wide Range of Dimming Interfaces

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## Revision History

| Revision | Date | Change |
|---|---|---|
| 0.1 | 08/17/2017 | • Initial datasheet created. |
| 0.11 | 08/24/2017 | • Changed the first feature, in section 2, from “Universal AC input (90VAC - 305VAC) or DC input up to 90W” to “Universal AC input (90VAC - 305VAC) or DC input with output power up to 90W”.<br>• Updated values in section 6, electrical characteristics:<br>» The zener breakdown voltage changed from 33.6V to 34.6V.<br>» The Test conditions of Pin 6, changed from $V_{SENSE}$ = 2V to $V_{SENSE}$ = 1V.<br>» Added a value to the blank test condition of Pin2: $I_{SENSE}$ = 1V.<br>» Changed most of the values in Pin 3: Added $V_{CC}$ = 18V~30V to the first test condition; changed the others from $C_L$ = 1,5nF to 5nF; the “Min” values changed from 12, 0,16 and 1.1 to 14.5, 0.2 and 0.4: the new “Typ” values are: 16.5, 180, 80, 0.6 and 1.2; and the “Max” values changed from 0,38 to 1.2 and from 2.5 to 1.7.<br>• Changed the voltage from 15V to 16.5V, in section 9, Pin 4 OUTPUT. |
| 0.12 | 08/31/2017 | • Deleted “PWM” from the title.<br>• Changed from “non-linear delay typical“ to “non-ideal characteristics” in the description section.<br>• Changed from ”Thermal resistance junction-to-PCB [GND lead]” to “Thermal resistance junction-to-ambient”, the symbol from “$\psi_{JB}$“ to “$\theta_{JA}$“ and the value from “75” to “170”, in section 5.<br>• In section 9:<br>» Changed the word “references” to “descriptions”.<br>» Changed tables 9.1 and 9.2.<br>» Updated the first part of the third paragraph (9.3.1): “For Figures 9.3a and 9.3b, please refer to Table 9.1 for the $I_{SENSE}$ configuration states explained here. In Figure 9.3a ($I_{SENSE}$ configuration state 4 - 10% minimum dimming level; 10% lowest dimming state), the minimum PWM duty cycle after remap is clamped to 10% when the input PWM signal at DIM1 pin drops to 11.1% or below; in Figure 9.3b ($I_{SENSE}$ configuration state 8 - 10% minimum dimming level; light-off mode - output current to zero at lowest dimming state),“.<br>» Changed “skip” to “pulse-skip” in figures 9.11. |
| 0.2 | 12/13/2017 | • Updated the Absolute Maximum Ratings table, changed the value “30” to “31”.<br>• Updated the package drawing.<br>• Updated the disclaimer page. |
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