iML8692

Phase-Cut Dimmable LED Current Controller

Preliminary Datasheet

General Description

The iML8692 is an LED current controller with line regulation compensation for operating over a wide alternative current (AC) voltage source range and with active load controller for phase cut dimmable function. It can drive an external N-channel power MOSFET to regulate the current flowing through a high voltage (HV) LED string and provide the holding current for the phase cut dimmer.

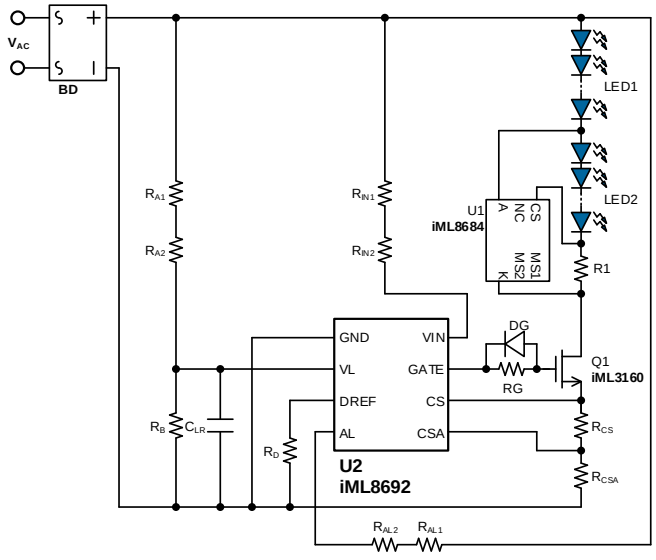
The application of the iML8692 is configured in series with an LED string, working as a constant current sink with over voltage protection (OVP), over temperature protection (OTP), and line regulation compensation. Active load function is included to improve the phase-cut dimming performance. It is suitable for applications with a rectified AC voltage source.

The PCB layout is also very flexible to meet various shape requirements. It is especially suitable for replacing incandescent light bulb and linear type fluorescent lamp.

Features

- **Device**
  - Active load current and LED string current control from single device.
  - Excellent system power regulation over AC line variation range.
  - 6V to 76V chip supply voltage range.
  - Over temperature protection.
  - Over voltage protection.
  - Single board LED lighting solution available.
- **System**
  - All solid state components.
  - No electrolytic capacitor required.
  - Scalable architecture allows optimization of performance vs. cost.
  - Driver-on-board and chip-on-board design solution available which minimize process flow and assembly cost.
  - High PF and Low THD performance.
  - Flexible PCB layout options.
  - Active load for phase-cut dimming operation

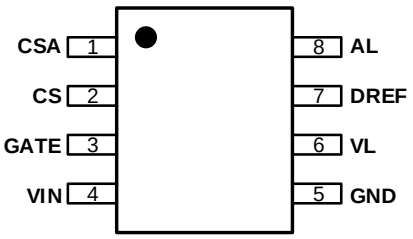
Typical Application Circuit



Applications

- A series LED bulbs
- Candelabra LED bulbs
- LED light tube
- LED down lights
- LED ceiling lamps
- AC LED lighting engines

Pin Diagram (Top View)



SOP - 8L

Ordering Information

Package	Part Number (Tape & Reel)
SOP–8L	iML8692CF-TR

Absolute Maximum Ratings

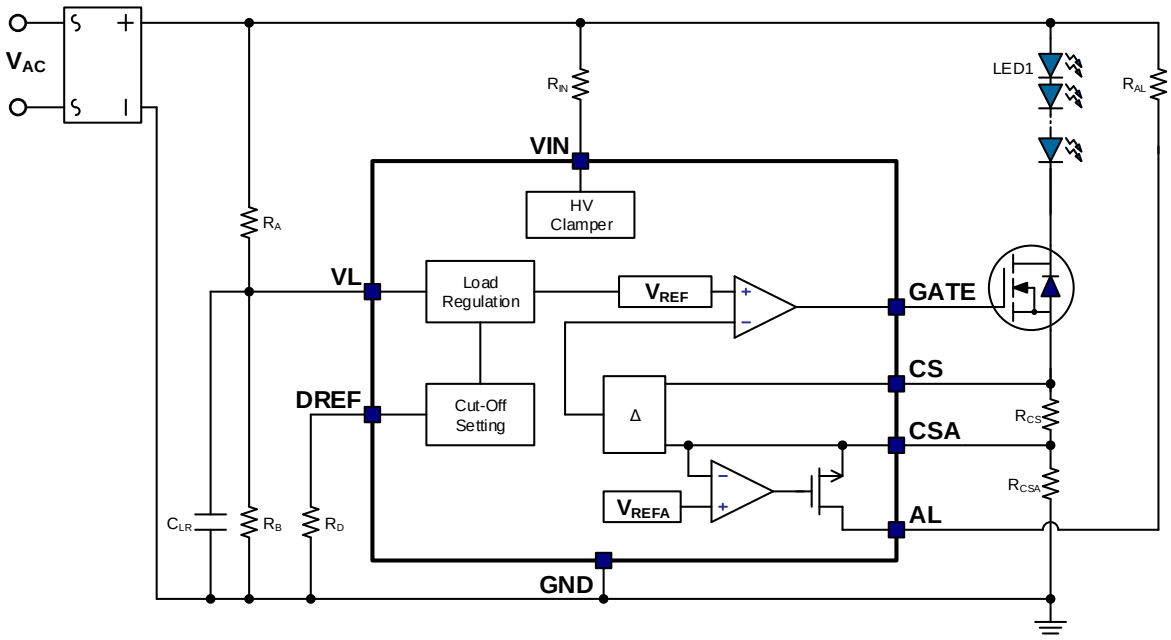
Caution: Values beyond absolute ratings can cause the device to be prematurely damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not guaranteed.

Sustaining Voltage	VIN, GATE to GND	-0.3V ~ +80V
	GATE to CS	-0.3V ~ +7V
	AL to GND	-0.3V ~ +500V
	VL to GND	-0.3V ~ +7V
	DREF to GND	-0.3V ~ +0.8V
	CS to GND	-0.3V ~ +2V
	CSA to GND	-0.3V ~ +1V
VIN Input Current		3mA
AL Input Current		40mA
ESD	HBM	2KV
	CDM	500V
Maximum Operating Junction Temperature, T_J		150°C
Operating Temperature, T_{opr}		-40°C to 85°C
Storage Temperature Range		-55°C to 150°C
Lead Temperature (Soldering, 10 seconds)		260°C

Note:

1). All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
2). All parameters having Min/Max specifications are guaranteed. Typical values are for reference purpose only.
3). Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.

Block Diagram



Pin Descriptions

Pin Name	Pin No.	Pin Function
CSA	1	Current Sense pin for active load circuit. Connect a sense resistor, R_{CSA}, between this pin and the GND pin. The current is set by $I_{AL} = \frac{V_{CSA}}{R_{CSA}}$
CS	2	Current Sense pin. Connect a sense resistor, R_{CS}, between this pin and the CSA pin. The current is set by $I_{OUT} = \frac{V_{CS-CSA}}{R_{CS}}$
GATE	3	External HV N-MOSFET Gate Driving pin.
VIN	4	Power supply pin.
GND	5	Ground pin.
VL	6	VAC Line Regulation Compensation Control pin. The VL voltage V_{VL} level is used to control the V_{CS} voltage to provide line regulation compensation and over voltage protection.
DREF	7	Reference voltage input pin for dimming cut-off setting.
ISINK	8	Active Load Current Sink pin.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VIN Input Voltage	V_{IN}	6		76	V
AL Input Current	I_{SINK}		20	30	mA

Electrical Characteristics

Unless otherwise noted, typical values are @ VIN=20V, T_A = 25ºC.

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VIN Supply Voltage	V_{IN}	VIN to GND		6		76	V
VIN Supply Current	I_{IN}	V_{IN}=6V~75V, R_{DREF} connected.		0.4	0.5	0.8	mA
VIN Over Voltage Clamping	VIN_{Clamp}	When V_{IN}>VIN_{CLAMP}, I_{IN} will increase to >1mA to clamp V_{IN} at VIN_{CLAMP}.		76	78	80	V
CS Voltage	V_{CS}	CS to CSA, V_{VL}=1.75V		488	500	512	mV
V_{CS} Line Regulation *Note 1	ΔV_{LR1}	CS to CSA	V_{VL}=1.57V~1.75V	-0.62	-0.56	-0.50	mV/mV
	ΔV_{LR2}		V_{VL}=1.75V~2.10V	-0.46	-0.40	-0.34	
	ΔV_{LR3}		V_{VL}=2.10V~2.28V	-0.60	-0.54	-0.48	
CSA Voltage	V_{CSA}	CSA to GND		240	250	260	mV
VL Over Voltage Protection	$V_{L,OVP}$	V_{VL} increasing			3.0		V
VL Over Voltage Protection Hysteresis for Recovery	$V_{L,HYS}$	V_{VL} decreasing			0.3		V
VL Over Voltage Protection Mode V_{CS}	$V_{CS,OVP}$	CS to CSA, V_{VL}>$V_{L,OVP}$			0		V
VL Over Voltage Protection Mode V_{CSA}	$V_{CSA,OVP}$	CSA to GND, V_{VL}>$V_{L,OVP}$		240	250	260	mV
Maximum V_{CS} Clamp	$V_{CS,Clamp}$	CS to CSA, V_{VL}=1.3V~1.5V		576	600	624	mV
V_{CS} Regulation under Dimming Operation *Note 2	ΔV_{DR}	V_{VL}=0.9V~1.2V		0.9	1.0	1.1	mV/mV
V_{CS} Low-Dim Clamp	V_{CS_LD}	CS to CSA, V_{DREF}=0V, V_{VL}<0.72V		185	200	215	mV
DREF Clamp Voltage	$V_{DREF,Clamp}$	DREF pin floating			0.76		V
DREF Source Current	i_{DREF}			9.3	10	10.7	uA
Cut-off Voltage*Note 3	V_{CUT}	V_{DREF} >0.76			0.76		V
		V_{DREF} <= 0.75			V_{DREF}		
GATE Voltage*Note 3	V_{GATE}	GATE to CS	V_{VL}>0.85V		6		V
			V_{VL}<V_{CUT}		1.4		
GATE Source Current *Note 4	I_{SOURCE}				30		uA
GATE Sink Current *Note 4	I_{SINK}				500		
AL Dropout Voltage *Note 5	V_{DROP}	R_{CSA}=25Ω				3	V
AL Leakage Current	$I_{Leakage}$	VIN=0V, V_{AL}=500V			0.03	1	uA

Parameter	Symbol	Test Conditions	Min	Typ	Max	UNIT
Thermal Protection Trip Temperature *Note 4	T_{TP}	When T_J is higher than T_{TP}, V_{CS} decreases linearly.	135	145		°C
Thermal Protection Mode V_{CS} Decreasing Slope *Note 4	$\Delta V_{CS}/\Delta T_J$	$T_J > T_{TP}$		-1.1		%/°C

Note 1: The CS voltage line regulation is defined as:

$$\Delta V_{LR1}=\frac{\Delta V_{CS}}{\Delta V_{VL}}=\frac{V_{CS(V_{VL}=1.75V)}-V_{CS(V_{VL}=1.57V)}}{1.75V-1.57V}$$

$$\Delta V_{LR2}=\frac{\Delta V_{CS}}{\Delta V_{VL}}=\frac{V_{CS(V_{VL}=2.10V)}-V_{CS(V_{VL}=1.75V)}}{2.10V-1.75V}$$

$$\Delta V_{LR3}=\frac{\Delta V_{CS}}{\Delta V_{VL}}=\frac{V_{CS(V_{VL}=2.28V)}-V_{CS(V_{VL}=2.10V)}}{2.28V-2.10V}$$

Note 2: V_{CS} Regulation under Dimming Operation ΔV_{DR} is defined as:

$$\Delta V_{DR}=\frac{\Delta V_{CS}}{\Delta V_{VL}}=\frac{V_{CS(V_{VL}=1.27V)}-V_{CS(V_{VL}=0.78V)}}{1.27V-0.78V}$$

Note 3: Cut-off voltage V_{CUT} is set by the input voltage V_{DREF} of DREF pin. When V_{DREF}<0.76V (clamp voltage for DREF pin), V_{CUT} is equal to V_{DREF}. Otherwise V_{CUT}=0.76V. When V_{VL}<V_{CUT}, which means the dimming duty is low, V_{GATE} is pulled low to turn off the system. When V_{VL} is increasing to >0.85, the system will start to regulate LED current.

Note 4: Guarantee by design, not by production test.

Note 5: Dropout voltage＝V_{AL} @ 90% × (I_{AL} @ V_{AL}＝5V)

Application Information

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Package Information

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Records of Revisions

Rev.	Date	Page	Description