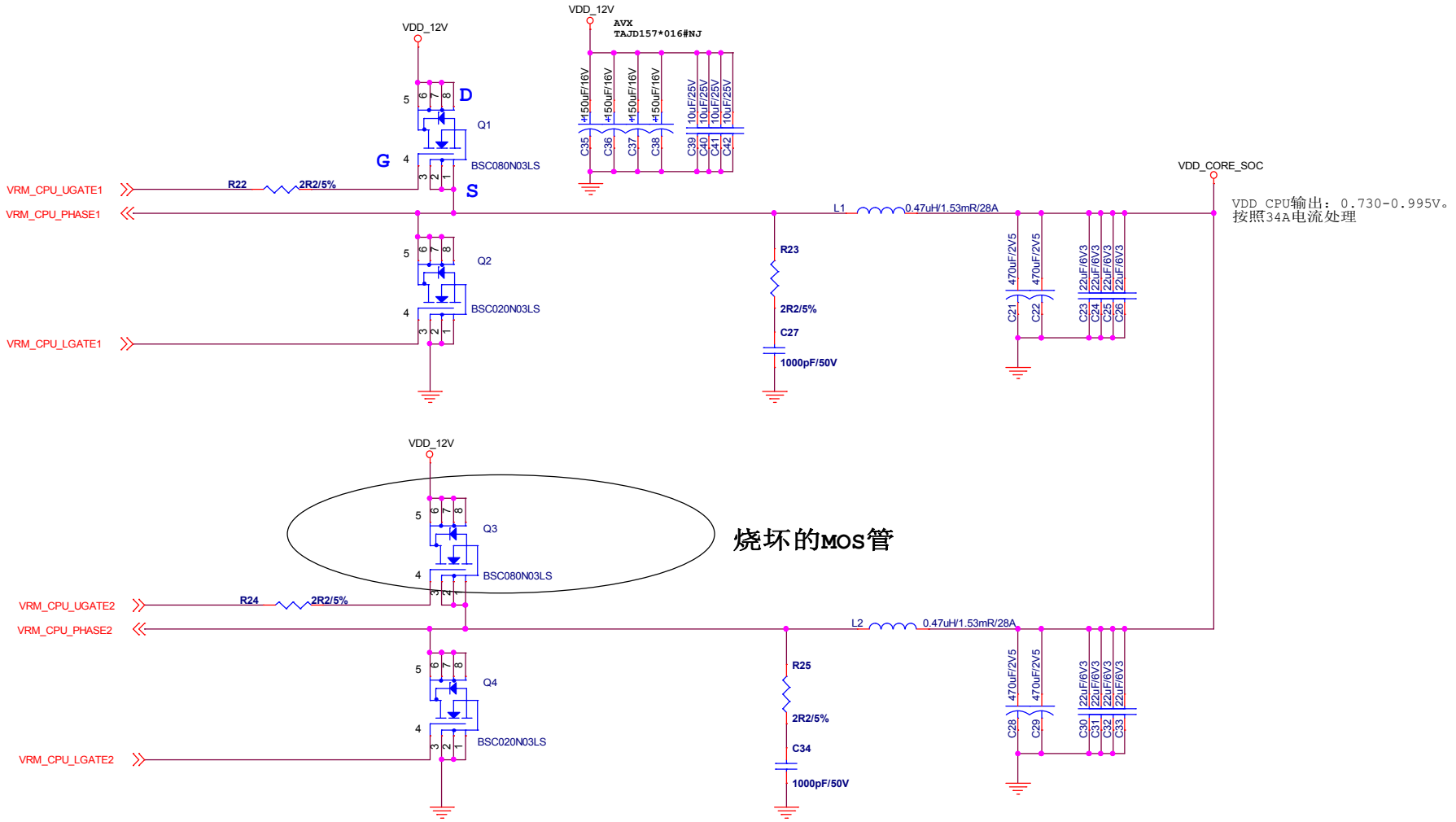
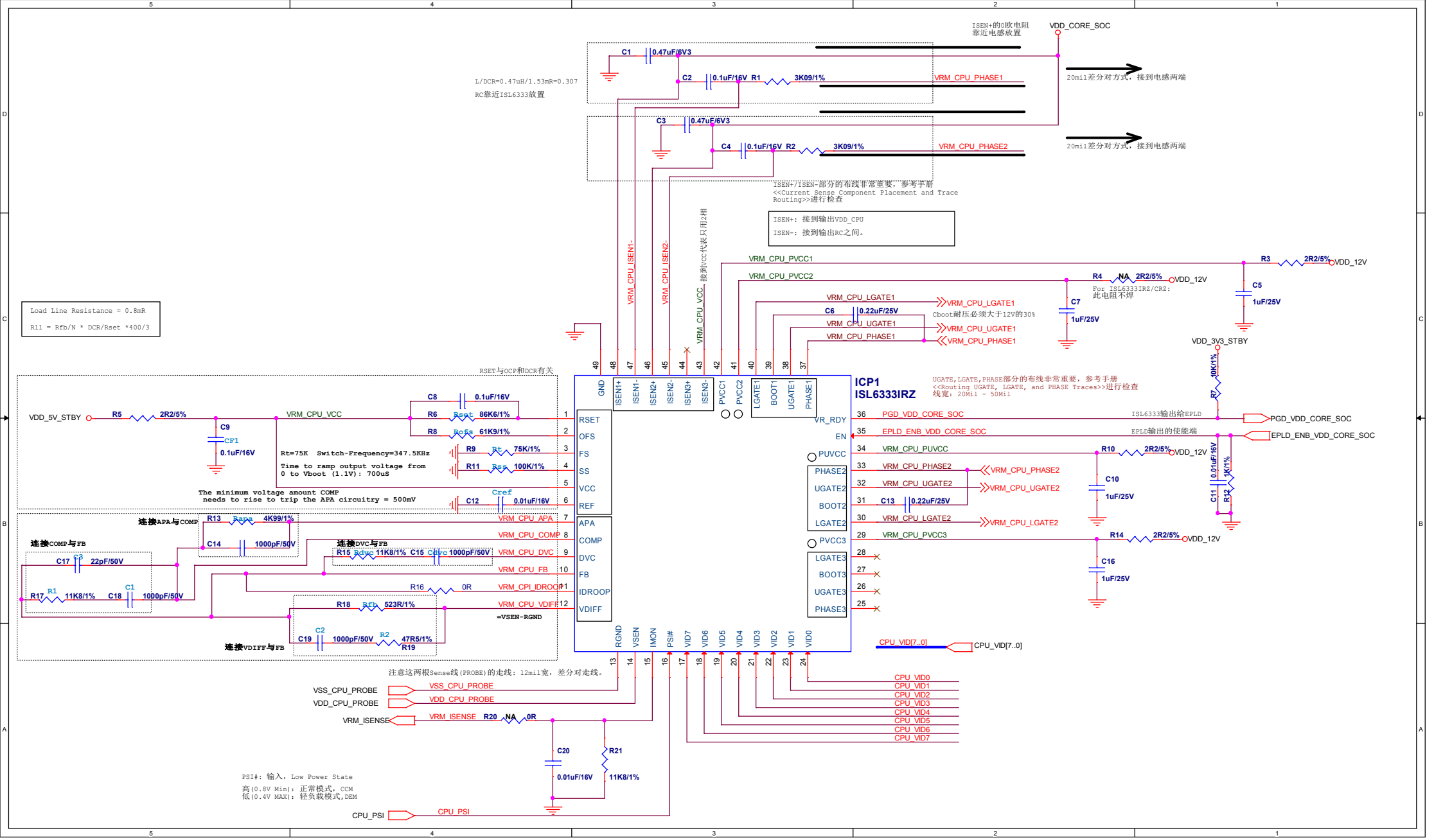

VDD_12V
AVX
TAJD157*016#NJ
#50uF/16V
10uF/25V
C35
C36
C37
C38
C39
C40
C41
C42
Q1
Q2
Q3
Q4
D
G
S
BSC080N03LS
BSC020N03LS
VRM_CPU_UGATE1
VRM_CPU_PHASE1
VRM_CPU_LGATE1
VRM_CPU_UGATE2
VRM_CPU_PHASE2
VRM_CPU_LGATE2
R22
R24
R23
R25
2R2/5%
C27
C34
1000pF/50V
L1
L2
0.47uH/1.53mR/28A
VDD_CORE_SOC
470uF/2V5
22uF/6V3
C21
C22
C23
C24
C25
C26
C28
C29
C30
C31
C32
C33
烧坏的MOS管
VDD_CPU输出：0.730-0.995V。
按照34A电流处理


ISEN+的0欧电阻
靠近电感放置
VDD_CORE_SOC
C1 0.47uF/6V3
C2 0.1uF/16V R1 3K09/1%
VRM_CPU_PHASE1
20mil差分对方式，接到电感两端
L/DCR=0.47uH/1.53mR=0.307
RC靠近ISL6333放置
C3 0.47uF/6V3
C4 0.1uF/16V R2 3K09/1%
VRM_CPU_PHASE2
20mil差分对方式，接到电感两端
ISEN+/ISEN-部分的布线非常重要，参考手册
<<Current Sense Component Placement and Trace Routing>>进行检查
ISEN+: 接到输出VDD_CPU
ISEN-: 接到输出RC之间。
VRM_CPU_ISEN1-
VRM_CPU_ISEN2-
VRM_CPU_VCC 接到VCC代表只用2相
VRM_CPU_PVCC1
VRM_CPU_PVCC2
R3 2R2/5% VDD_12V
R4 NA 2R2/5% VDD_12V
For ISL6333IRZ/CRZ:
此电阻不焊
C5 1uF/25V
C7 1uF/25V
VRM_CPU_LGATE1
C6 0.22uF/25V
Cboot耐压必须大于12V的30%
VRM_CPU_UGATE1
VRM_CPU_PHASE1
VDD_3V3_STBY
R7 10K/1%
Load Line Resistance = 0.8mR
Rll = Rfb/N * DCR/Rset *400/3
RSET与OCP和DCR有关
VDD_5V_STBY
R5 2R2/5%
C9 0.1uF/16V
CF1
VRM_CPU_VCC
C8 0.1uF/16V
R6 Rset 86K6/1%
R8 Rofs 61K9/1%
R9 Rt 75K/1%
R11 Rss 100K/1%
Rt=75K Switch-Frequency=347.5KHz
Time to ramp output voltage from 0 to Vboot (1.1V): 700uS
The minimum voltage amount COMP needs to rise to trip the APA circuitry = 500mV
C12 Cref 0.01uF/16V
ICP1
ISL6333IRZ
UGATE,LGATE,PHASE部分的布线非常重要，参考手册
<<Routing UGATE, LGATE, and PHASE Traces>>进行检查
线宽：20Mil - 50Mil
GND ISEN1+ ISEN1- ISEN2+ ISEN2- ISEN3+ ISEN3- PVCC1 PVCC2 LGATE1 BOOT1 UGATE1 PHASE1
RSET OFS FS SS VCC REF APA COMP DVC FB IDROOP VDIFF
VR_RDY PUVCC PHASE2 UGATE2 BOOT2 LGATE2 PVCC3 LGATE3 BOOT3 UGATE3 PHASE3
PGD_VDD_CORE_SOC
EPLD_ENB_VDD_CORE_SOC
ISL6333输出给EPLD
EPLD输出的使能端
VRM_CPU_PUVCC
VRM_CPU_PHASE2
VRM_CPU_UGATE2
VRM_CPU_LGATE2
VRM_CPU_PVCC3
R10 2R2/5% VDD_12V
C10 1uF/25V
C11 0.01uF/16V
R12 1K/1%
R14 2R2/5% VDD_12V
C16 1uF/25V
连接APA与COMP
R13 Rapa 4K99/1%
C14 1000pF/50V
连接COMP与FB
C17 C3 22pF/50V
R17 R1 11K8/1%
C18 C1 1000pF/50V
连接DVC与FB
R15 Rdvc 11K8/1% C15 Cdvc 1000pF/50V
R16 0R
R18 Rfb 523R/1%
=VSEN-RGND
连接VDIFF与FB
C19 C2 1000pF/50V
R2 47R5/1%
R19
VRM_CPU_APA
VRM_CPU_COMP
VRM_CPU_DVC
VRM_CPU_FB
VRM_CPI_IDROOP
VRM_CPU_VDIFF
RGND VSEN IMON PSI# VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0
CPU_VID[7..0]
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
CPU_VID7
注意这两根Sense线(PROBE)的走线：12mil宽，差分对走线。
VSS_CPU_PROBE
VDD_CPU_PROBE
VRM_ISENSE
R20 NA 0R
C20 0.01uF/16V
R21 11K8/1%
PSI#：输入，Low Power State
高(0.8V Min)：正常模式，CCM
低(0.4V MAX)：轻负载模式,DEM
CPU_PSI