MP5016

2.7V – 22V, 1A – 5A Current Limit Switch with Over Voltage Clamp and Reverse Block

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP5016 is a protection device designed to protect circuitry on the output from transients on input. It also protects input from undesired shorts and transients coming from the output.

At startup, inrush current is limited by limiting the slew rate at the output. The slew rate is controlled by DV/DT pin setting and MODE pin setting.

The maximum load at the output is current limited. The magnitude of the current limit is controlled by an external resistor from ILIMIT to GND. There is a fixed 2.5A current limit when floating ILIMIT pin.

The output voltage is limited by output OVP function, the clamp voltage can be set by MODE pin connection.

Offers a GATE drive signal connect to an external N-channel MOSFET gate to block current flows from output to input when IC is enable off, power shutdown or thermal shutdown.

The device is available in a QFN10 (1.5mm x 2mm) package.

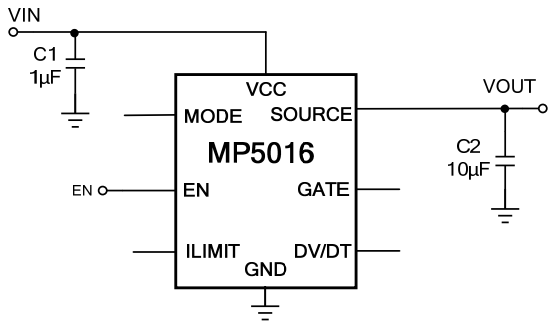
FEATURES

- Wide 2.7V to 22V Operating Input Range
- 50μA Typical Low Quiescent Current
- Selectable Over Voltage Clamp Threshold
- Fast Output OVP Response
- Integrated 43mΩ Power FET
- Adjustable Current-Limit or Fixed Current Limit when floating ILIMIT pin
- Reverse Blocking FET Driver
- Soft Start Time Programmable through DV/DT pin and MODE pin
- Fast Response for Hard Short Protection
- OCP Hiccup Protection
- Thermal Shutdown and Auto Retry
- Available in QFN10 (1.5mmx2mm) Package

APPLICATIONS

- HDD, SSD
- Hot Swap
- Wireless Modem Data Cards
- PC Cards
- USB Power Distribution
- USB Protection
- USB3.1 Power Delivery

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5016GQH	QFN-10 (1.5mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.MP5016GQH-Z);

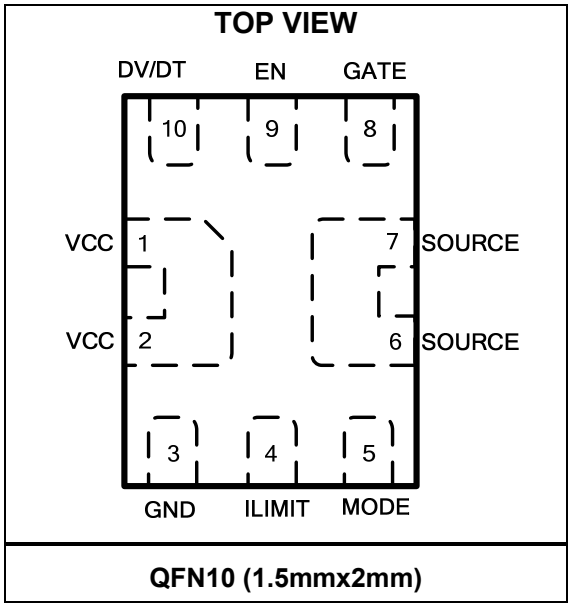
TOP MARKING

EK

LL

EK: product code of MP5016GQH;
LL: lot number;

PACKAGE REFERENCE



QFN10 (1.5mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

VCC, SOURCE .....-0.3V to 26V
MODE .....-0.3V to 26V
GATE .....SOURCE+5.5V
All Other Pins .....–0.3V to +5.5 V
Junction Temperature ..... -40°C to +150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A=+25°C)(2)
QFN10 (1.5mmx2mm) 0.96W

Recommended Operating Conditions (3)

Supply Voltage VCC .....2.7V to 22V
Output Voltage SOURCE.....2.7V to 22V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (1.5mmx2mm).....….130.....25 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, R_{LIMIT}=NS, C_{OUT}=10uF, T_J =-40°C + 125°C(5), typical value is tested at T_J=+25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	EN=HIGH		50		μA
		EN=GND		9		μA
Power FET						
ON Resistance	R_{DSon}	T_J=25°C		43		mΩ
Turn-on Delay	T_{delay}	DV/DT float, MODE=GND		450		μs
Off-State Leakage Current	I_{OFF}	V_{IN}=12V, EN=0V		0.1		μA
Under/Over Voltage Protection						
Under Voltage Lockout Rising Threshold	V_{UVLO}			2.5		V
UVLO Hysteresis	$V_{UVLOHYS}$			200		mV
Output Over Voltage Clamp Voltage	V_{CLAMP}	V_{MODE}=LOW		5.65		V
		V_{MODE}=HIGH		14.8		V
		R_{MODE}=115kΩ		5.55		V
		R_{MODE}=324kΩ		15		V
DV/DT						
DV/DT Slew Rate	dv/dt	DV/DT float, V_{MODE}=LOW		0.8		V/ms
		DV/DT float, V_{MODE}=HIGH		2.1		
		DV/DT float, V_{MODE}=FLOAT		3.88		
DV/DT Current	$I_{DV/DT}$	$V_{DV/DT}$=0.5V		6.5		μA
Current Limit						
Current Limit at Normal Operation	I_{Limit_NO}	Float ILIMIT pin		2.5		A
		R_{LIMIT}=604Ω		3.5		A
		R_{LIMIT}=3kΩ		0.8		A
Enable						
Enable Rising Threshold	V_{EN_RISING}			2		V
Enable Hysteresis	V_{EN_HYS}			400		mV
Enable Pull-Down Resistor	R_{EN_DOWN}			2.2		MΩ
Gate						
Gate Maximum Source Current	$I_{G\_SOURCE\_MAX}$			12		μA
Gate Maximum Sink Current	$I_{G\_SINK\_MAX}$	Vcc=5.5V		1.3		mA
Output Discharge						
Discharge Resistance	R_{DIS}	Vcc=5V		540		Ω
OTP						
Thermal shutdown(6)	T_{SD}			175		°C
Thermal Hysteresis(6)	T_{SD_HYS}			50		°C

Notes:

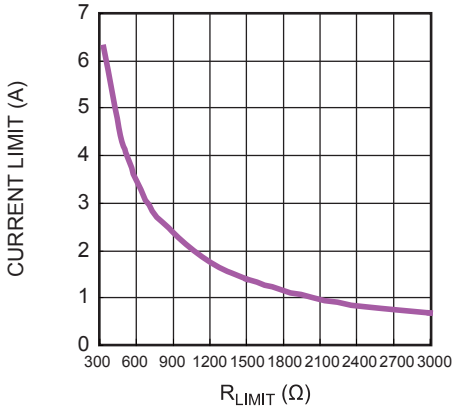
5) Not tested in production. Guaranteed by over-temperature correlation.

6) Guarantee by engineering sample characterization.

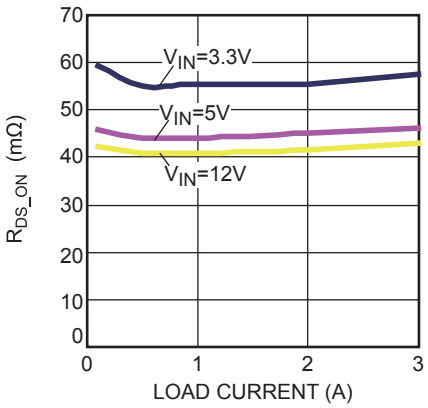
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, V_{EN}=5V, R_{LIMIT} =604Ω, C_{OUT}=10μF, T_A=25°C, unless otherwise noted.

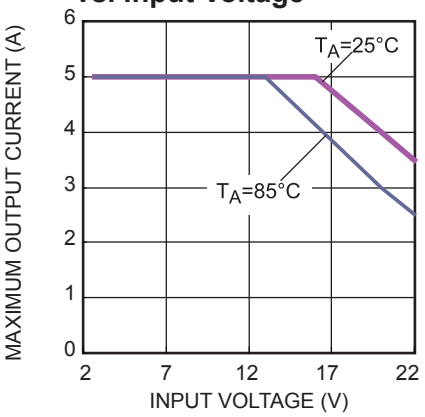
Current Limit vs. R_{LIMIT}



R_{DS_ON} vs. Load Current

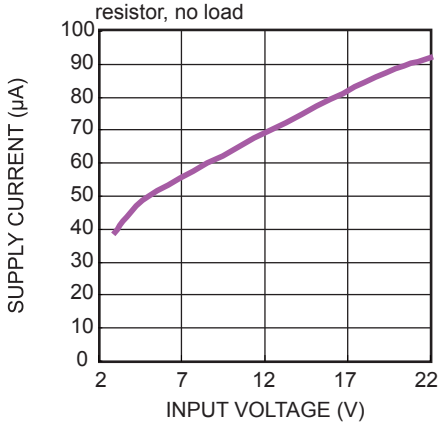


Maximum Output Current vs. Input Voltage



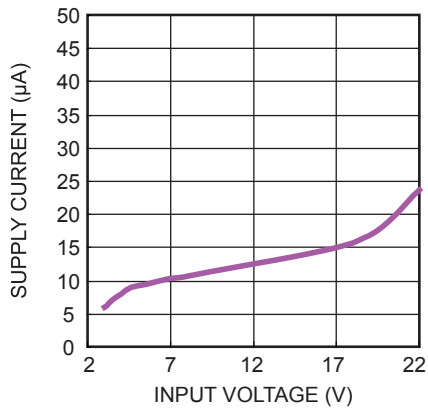
Supply Current, Output Enabled vs. Input Voltage

EN=3V, Remove the EN pull-up resistor, no load

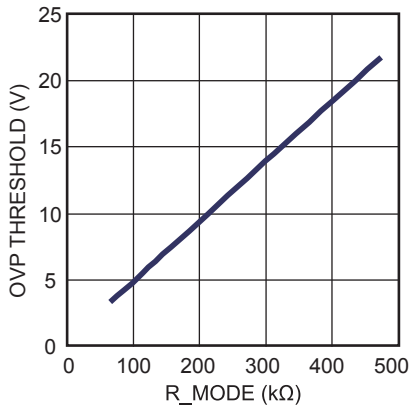


Supply Current, Output Disabled vs. Input Voltage

V_{EN}=0



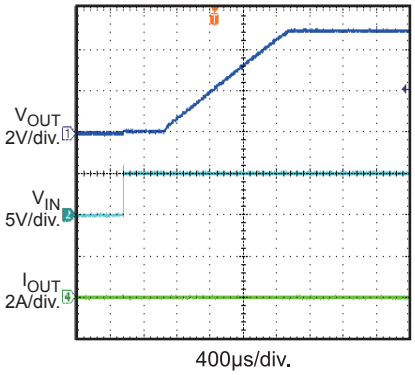
Output OVP threshold vs. R_MODE



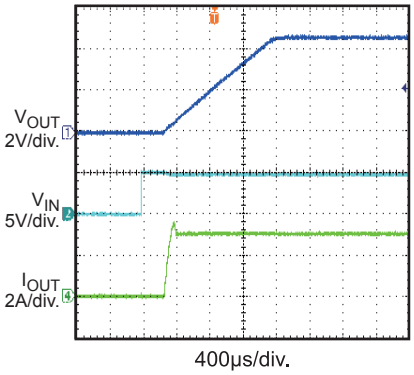
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{EN}=5V, R_{LIMIT} =604Ω, MODE pin float, DV/DT pin float, C_{OUT}=10μF, T_A=25°C, unless otherwise noted.

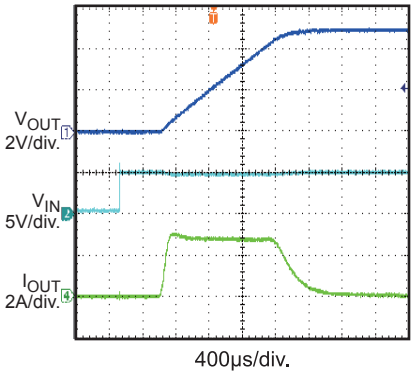
Start-Up through Input Voltage
No Load



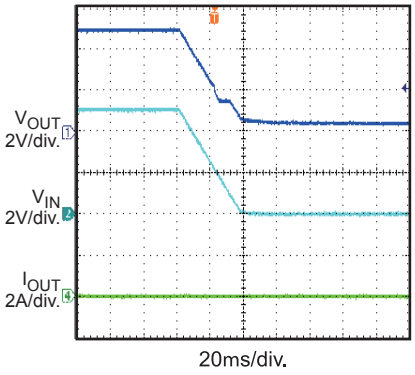
Start-Up through Input Voltage
CC Load =3A



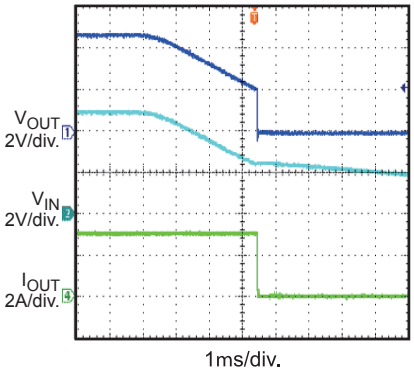
Start-Up through Input Voltage
No Load, C_{OUT} = 1000μF



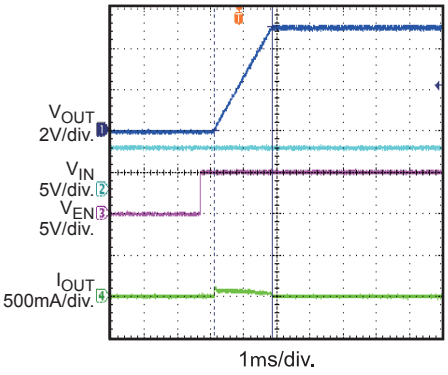
Shutdown through Input Voltage
No Load



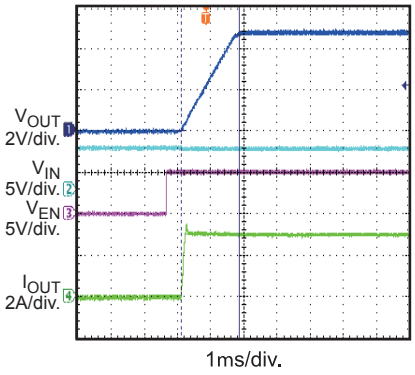
Shutdown through Input Voltage
CC Load =3A



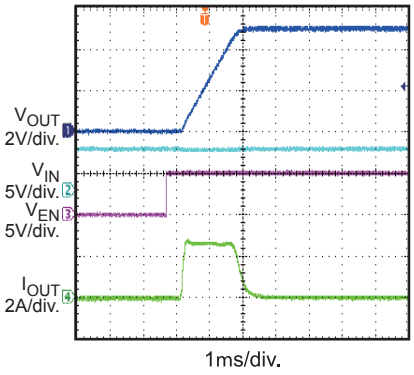
Start-Up through Enable
No Load



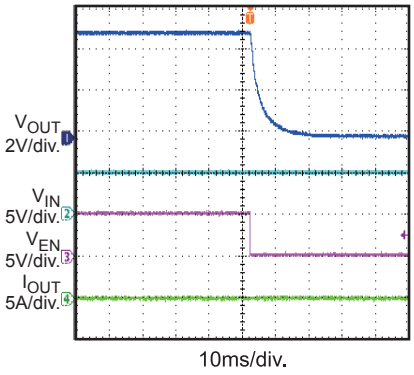
Start-Up through Enable
CC Load =3A



Start-Up through Enable
No Load, C_{OUT} =1000μF



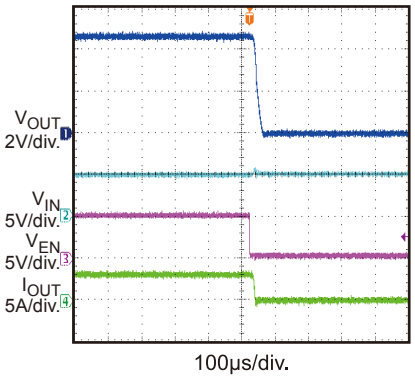
Shutdown through Enable
No Load



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{EN}=5V, R_{LIMIT} =604Ω, MODE pin float, DV/DT pin float, C_{OUT}=10μF, T_A=25°C, unless otherwise noted.

Shutdown through Enable
CC Load = 3A



PIN FUNCTIONS

Pin #	Name	Description
1,2	VCC	Supply Voltage. The MP5016 operates from a 2.7V-to-22V input rail. Requires ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
3	GND	System Ground.
4	ILIMIT	Current Limit Set pin. Place a resistor between this pin and ground to set the value of the current limit. Float this pin gets 2.5A fixed current limit.
5	MODE	Output OVP Clamp Voltage Select pin. Output OVP clamp voltage range selected by MODE pin voltage. A resistor is connected from MODE pin to ground to set OVP threshold voltage. Also three digital inputs are provided for MODE pin. Drive MODE pin High to VCC, output OVP clamp voltage will be set at 14.8V. Drive MODE pin Low to GND, output OVP clamp voltage will be set at 5.65V. Float MODE pin, there is no OVP clamp protection.
6,7	SOURCE	This pin is the source of the internal power FET and the output terminal of the IC.
8	GATE	Gate driver for reverse current block MOSFET. An 100pF capacitor is required on Gate pin if not use the reverse current block MOSFET.
9	EN	Force EN high to enable MP5016. Float EN pin or pull it to ground can disable the IC. For quickly startup, pull EN up to VCC through a 300kΩ resistor.
10	DV/DT	DV/DT pin. Connect a capacitor from DV/DT to ground can set the dv/dt slew rate.

FUNCTIONAL BLOCK DIAGRAM

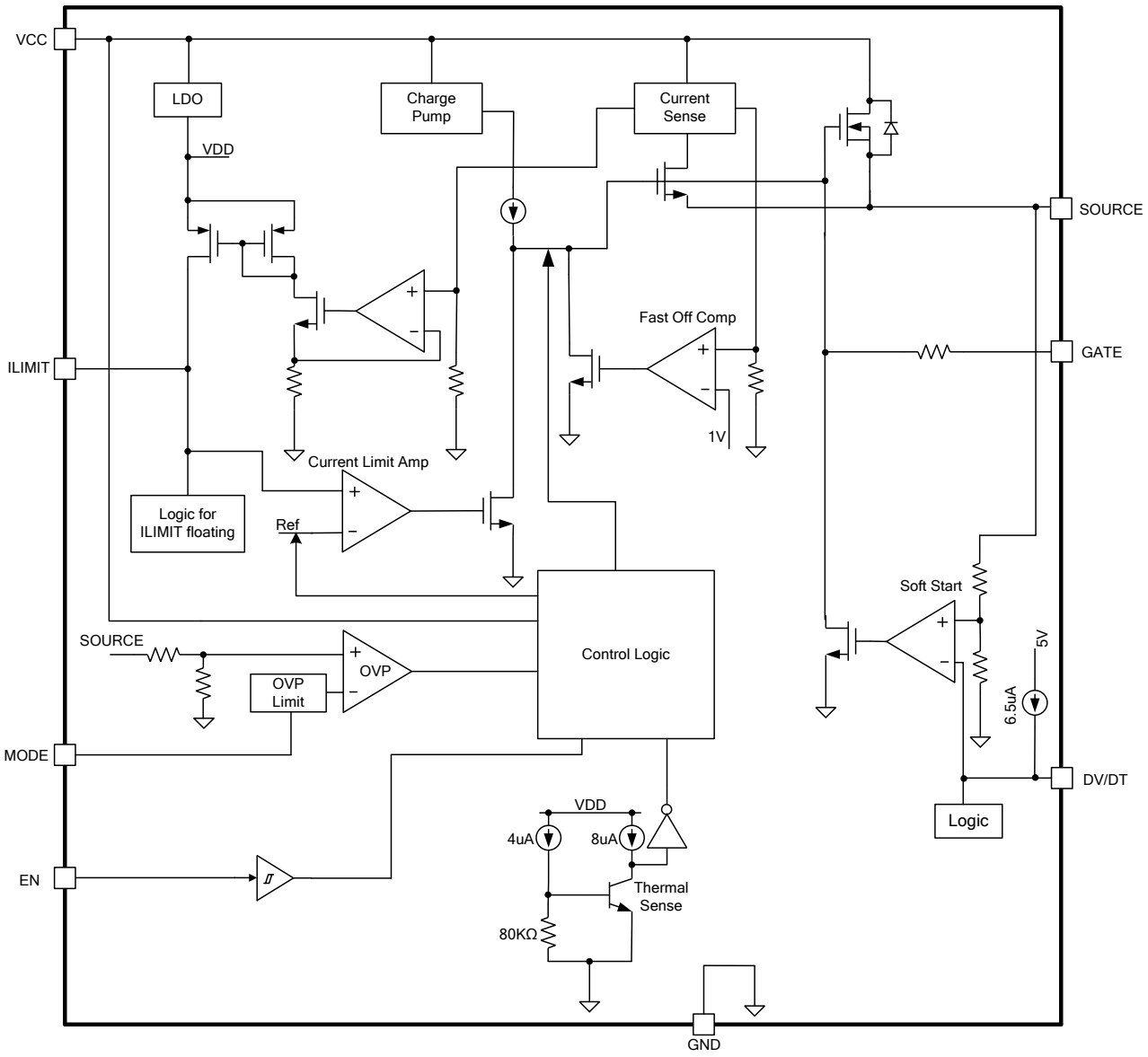


Figure 1: Functional Block Diagram

OPERATION

The MP5016 is designed to limit the in-rush current to the load when a circuit card inserts into a live backplane power source, thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load as well. It offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature which eliminates the requirement of external current sense power resistor, power MOSFET and thermal sense device.

Under-Voltage Lockout (UVLO)

The MP5016 can be used in the 2.7V to 22V input supply system. And there is high energy transients during normal operation or during hot swap. Those transients depend on the parasitic inductance and resistance of the wire along with capacitor at VCC node. If power clamp (TVS, Tranzorb) diode is not used, E-Fuse must be able to withstand this transient voltage. MP5016 integrates high voltage MOSFET up to 26V and also uses high voltage circuit for VCC node to guarantee safe operation.

MODE

The MODE pin is used to select the output OVP threshold.

Three digital inputs are provided for MODE pin. Drive MODE pin High to VCC, output OVP clamp voltage will be set at 14.8V. Drive MODE pin Low to GND, output OVP clamp voltage will be set at 5.65V. Float MODE pin, there is no OVP clamp protection.

Also, the OVP threshold can be set by connecting a resistor from MODE pin to ground. For more detail, please refer to APPLICATION INFORMATION section.

Soft-Start

The soft start time is related to the dv/dt slew rate and input voltage.

$$t\_ss(ms) = \frac{Vin(V)}{dv/dt\ (V/ms)}$$

The dv/dt slew rate is controlled by external DV/DT capacitor setting and MODE pin setting. For more details, please refer to APPLICATION INFORMATION section.

Fast Output and Input over Voltage Protection (OVP)

To protect the downstream loading when there is a surge voltage at input, MP5016 provides output OVP function. An accurate and fast comparator will monitor the over voltage condition of output. If the output voltage rises above the threshold which is set by MODE pin, the gate of internal MOSFETs is quickly pulled down and it's regulated to a certain value to maintain the output voltage clamped at OVP threshold. The fast loop response speed keeps the over voltage overshoot small.

Current Limit

The MP5016 provides a constant current limit and the current limit can be programmed by external resistor. Once the current limit threshold is reached, the internal circuit will regulate gate voltage to hold the current in power FET constantly. In order to limit the current, the gate to source voltage needs to be regulated from 5V to around 1V. The typical response time is about 15μs, during this period the output current may have a small overshoot.

The desired current limit is a function of the external current limit resistor. It's given by:

$$I_{LIMIT}(A) = \frac{0.6(V)}{R_{LIMIT}(\Omega)} \times 3450$$

Where, 3450 is the current sense ratio.

MP5016 allows ILIMIT pin floating operation. If ILIMIT pin is floating, the current limit will be set as fixed 2.5A internally.

When the over current limit condition lasts more than 2ms the chip enters the hiccup mode with 2ms on time and 700ms off time.

When short MP5016 ILIMIT pin to GND, the normal current limit will be disabled but the secondary current limit still works. The secondary current limit is set internally to 8A. When the secondary current limit is triggered, IC will shutdown the power MOSFET.

Reverse Blocking FET Driver

MP5016 has a GATE pin to provide external N-channel MOSFET gate drive signal for reverse current protection. Three events will pull low GATE voltage. Vin below UVLO, Enable voltage lower than high level threshold or thermal shutdown. When Vin below UVLO, Enable voltage lower than high level threshold or thermal shutdown happens, GATE will sink current immediately from the gate of external MOSFET to initiate fast turn off.

A 100pF capacitor is required on GATE pin if not connect the external MOSFET.

Short Circuit Protection (SCP)

If the load current increases rapidly due to short circuit event, the current may exceed the current limit threshold before control loop able to respond. If the current reaches 8A secondary current limit level, there is a fast turn off circuit active to turn off the power FET, as shown in Figure 1. This can help to limit the peak current through the switch, thus keep the input voltage not drop too much. The total short circuit response time is about 1μs. After the FET is switched off, the part will restart. During the restart process, if the short still exist, MP5016 will regulate the gate voltage to hold the current at normal current limit level.

To avoid large input voltage spike to damage the IC during SCP entry, recommend use large input capacitor at high Vin application.

Output Discharge

The part involves a discharge function that provides a resistive discharge path for the external output capacitor. The function will be active when the part is disabled (Vin UVLO, EN shutdown) and it will be done in a very limited time. When use external reverse current block MOSFET, the output discharge path will be block by the reverse current block MOSFET. So output can't be discharged when reverse current block MOSFET is used.

EN

The EN enables the part when high and disables the part when low. Floating the EN pin will set the part shutdown because there is an internal 2.2MΩ resistor pull EN down to ground. For auto startup, connect a pull-up resistor from VCC to EN. When use pull-up resistor to set the power on threshold, need avoid using too small pull-up resistor to increase the operation quiescent current.

Thermal Shutdown – Auto Retry

Thermal shutdown prevents the chip from operating at exceedingly high temperature. When the silicon die reaches temperature that exceeds 175°C, it shuts down the whole chip, and EN will report a fail mode. When the temperature drops below its lower threshold, typically 125°C, chip is enable again after a 700ms delay typically.

APPLICATION INFORMATION

Setting the Current Limit

The MP5016 current limit value should exceed the normal maximum load current, allowing the tolerances in the current sense value. The current limit is a function of the external current limit resistor. Table 1 and Figure 2 list examples of typical current limit values as a function of the resistor value.

Table 1: Typical Current Limit vs. Current Limit Resistor (7)

R_{LIMIT} (Ω)	2000	820	604	470	422
I_{LIMIT} (A)	1	2.5	3.5	4.5	5

Note:
7) The current limit in table 1 is a typical value for reference design.

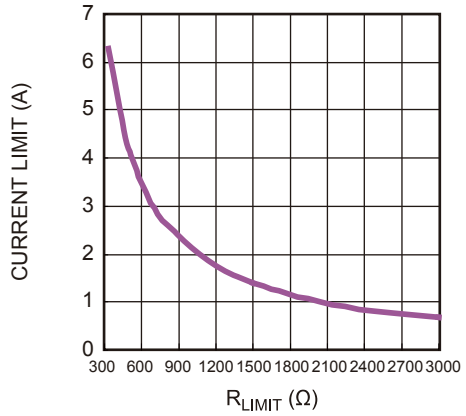


Figure 2: Current Limit vs. Current Limit Resistor

MP5016 Current limit can be programmed from 0.8A to 5A by connecting correct R_{LIMIT} resistor. Current limit cannot be set too low, because MP5016 works in sleep mode when the load is lower than 0.38A and current limit logic will be disabled in sleep mode.

Recommend to set current limit within the Maximum Output Current vs. Input Voltage curve in TPC section.

Setting the Over Voltage Clamp Threshold

Drive MODE pin High to VCC, output OVP clamp voltage will be set at 14.8V. Drive MODE pin Low to GND, output OVP clamp voltage will be set at 5.65V.

When connect MODE pin to HIGH/LOW digital voltage, Please refer to Table 2 to set the MODE HIGH/LOW digital voltage.

Table 2. MODE HIGH/LOW Digital Voltage

	Min.	Max.
V_{MODE}_HIGH	VCC-0.3V	
V_{MODE}_LOW		0.4V

Also, the OVP threshold can be set by connecting a resistor from MODE pin to ground. In this case, the OVP clamp threshold is given by:

$$V_{clamp}(V) = 0.04522(A) \times R_{MODE}(K\Omega) + 0.3502(V)$$

Recommend R_{MODE} value should be above 68kΩ. For example, 115kΩ R_{MODE} can set the OVP clamp threshold to 5.55V.

Setting the Soft Start Time

The soft start time is related to the dv/dt slew rate and input voltage.

$$t\_ss(ms) = \frac{Vin(V)}{dv/dt\ (V/ms)}$$

The dv/dt slew rate is controlled by external DV/DT capacitor setting and MODE pin setting.

For DV/DT pin float case, the dv/dt slew rate value is refer to Table 3.

Table 3. dv/dt slew rate value at DV/DT pin float

MODE pin connection	dv/dt slew rate (V/ms)
LOW	0.8
HIGH	2.1
FLOAT	3.88
Rmode	$\frac{V_{clamp}(V)}{7ms}$

Where Vclmap is set by resistor in MODE pin, it is the output OVP clamp voltage.

For the case with external DV/DT capacitor, the dv/dt slew rate is calculated by:

$$dv/dt\ (V/ms) = \frac{6.5\mu A \times K}{1V \times C_{DV/DT}(nF)}$$

Where K factor value is refer to table 4:

Table 4. K factor value at external DV/DT capacitor

MODE pin connection	K(V)
LOW	5.65
HIGH	14.8
FLOAT	27
R_{MODE}	Vclamp

Large Output Capacitor

With large output capacitor, if the charge current during soft start triggers the current limit, MP5016 will enter hiccup when current limit is triggered for 2ms.To avoid startup failure with large output capacitor, need set proper dv/dt slew rate during soft start not to trigger current limit during soft start.

PCB Layout Guide

PCB layout is benefit for better performance. Please follow these guidelines and use Figure 3 as reference.

1. Place the high-current paths (VCC and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VCC and GND pins.
3. Connect the VCC and VOUT pads to large copper to achieve better thermal performance.
4. Place current limit resistor close to the ILIMIT pin.
5. Place DV/DT capacitor close to DV/DT pin.

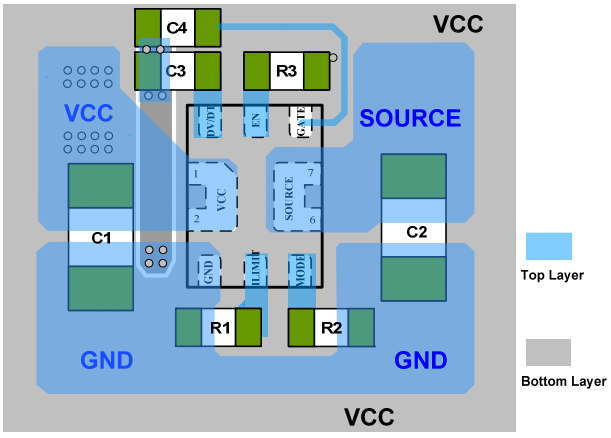


Figure 3: PCB Layout Example

Design Example

Below is a design example following the application guidelines for the given specifications:

Table 5: Design Example

Vin(V)	2.7 to 22
Current Limit (A)	3.5
DV/DT slew rate (V/ms)	3.88

The detailed application circuits are shown in Figure 4 and Figure 5. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related Evaluation Board Datasheets of MP5016.

TYPICAL APPLICATION CIRCUITS

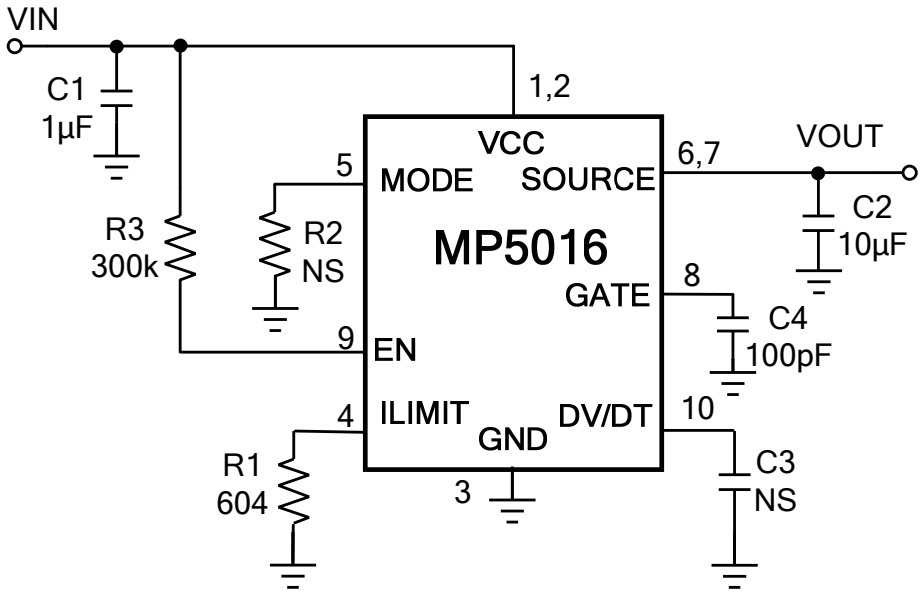


Figure 4: Typical Application Circuit without Reverse Current Blocking MOSFET (8)

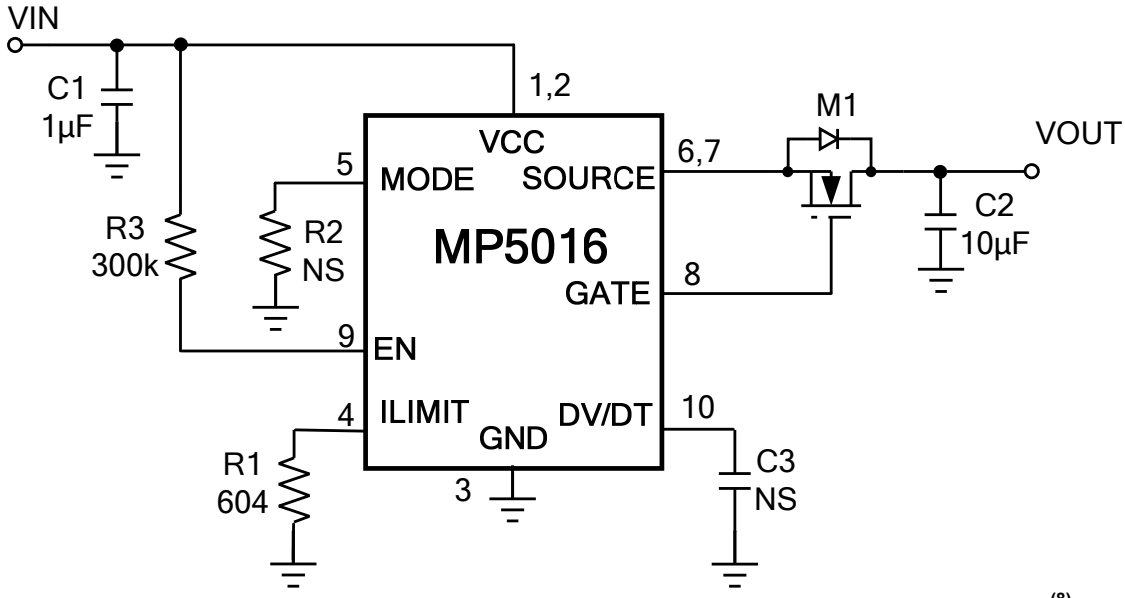


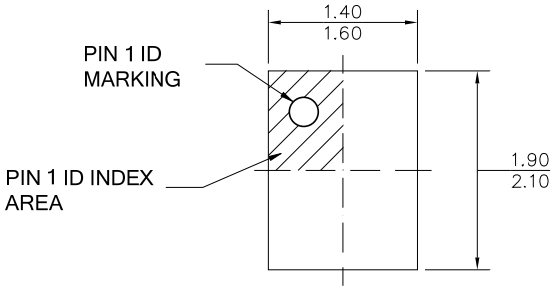
Figure 5: Typical Application Circuit with Reverse Current Blocking MOSFET (8)

Note :

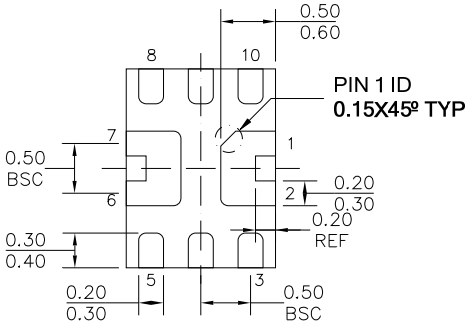
8) To avoid large input voltage spike to damage the IC during SCP entry, recommend use larger input capacitor C1 at high Vin application.

PACKAGE INFORMATION

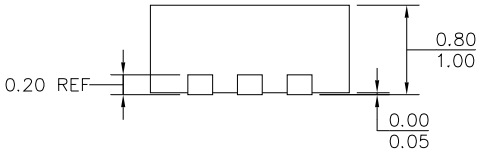
QFN-10 (1.5mmx2mm)



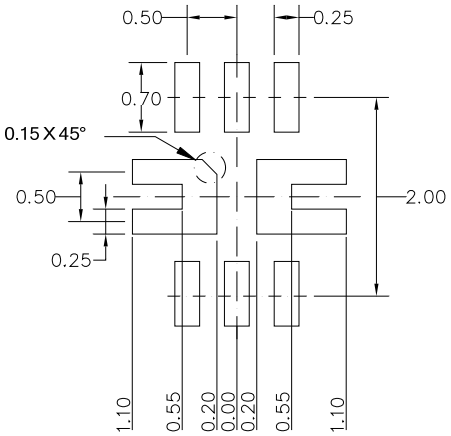
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLI
MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.