2.5A 和 5A，35V$_{MAX}$ VDD 场效应晶体管 (FET) 和绝缘栅双极晶体管 (IGBT) 单栅极驱动器

查询样片: UCC27531 , UCC27533, UCC27536 , UCC27537, UCC27538

特性

- 低成本栅极驱动器（为驱动 **FET** 和 **IGBT** 的最佳解决方案）
- 离散晶体管对驱动的出色替代产品（提供与控制器的简便对接）
- **TTL** 和 **CMOS** 兼容输入逻辑阀值，（与电源电压无关）
- 分离输出选项实现打开和关闭电流调节
- 反向和非反向输入配置
- 由固定 **TTL** 兼容阀值启用
- **18V VDD** 时的高 **2.5A** 拉电流和 **2.5A** 或 **5A** 灌峰值驱动电流
- 从 **10V** 到高达 **35V** 的宽 **VDD** 范围
- 能够耐受比接地最多低 **5V** 的直流电压的输入和使能引脚
- 当输入悬空或 **VDD** 欠压闭锁 **(UVLO)** 期间，输出保持低电平
- 快速传播延迟（典型值 **17ns**）
- 快速上升和下降时间（**1800pF** 负载时的典型值分别为 **15ns** 和 **7ns**）
- 欠压闭锁 **(UVLO)**
- 被用作高侧或低侧驱动器（如果采用适当的偏置和信号隔离设计）
- 低成本、节省空间的 **5** 引脚或 **6** 引脚 **DBV**（小外形尺寸晶体管 **(SOT)-23**）封装选项
- **UCC27536** 和 **UCC27537** 与 **TPS2828** 和 **TPS2829** 引脚到引脚兼容
- 运行温度范围 **-40°C** 至 **140°C**

应用范围

- 开关模式电源
- 直流到直流转换器
- 太阳能逆变器、电机控制、不间断电源 **(UPS)**
- 混合动力车 **(HEV)** 和电动车辆 **(EV)** 充电器
- 家用电器
- 可再生能源功率转换
- **SiC FET** 转换器

说明

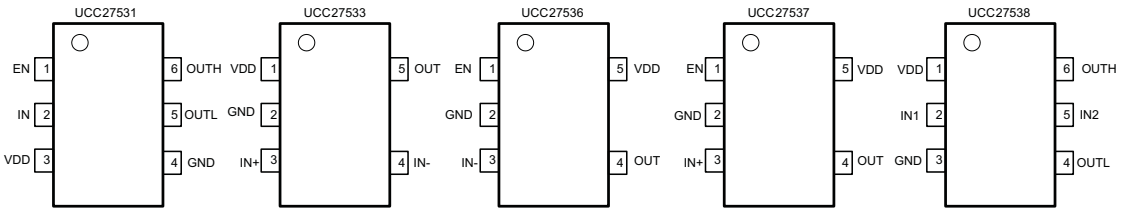
UCC2753x 是一款单通道、高速、栅极驱动器，此驱动器可借助于高达 2.5A 拉电流和 5A 灌电流（非对称驱动）峰值电流来有效驱动金属氧化物半导体场效应晶体管 (MOSFET) 和 IGBT 电源开关。 强劲的非对称驱动中的吸收能力提升了寄生米勒 (Miller) 接通效应抗扰度。 UCC2753x 器件还特有一个分离输出配置，在此配置中栅极驱动电流从 OUTH 引脚拉出并从 OUTL 引脚被灌入。 这个引脚安排使得用户能够分别在 OUTH 和 OUTL 引脚上采用独立的接通和关闭电阻器并且能很轻易地控制开关的转换率。

此驱动器具有轨到轨驱动能力和典型值为 17ns 的极小传播延迟。

UCC2753xDBV 的输入阀值基于与 TTL 和 COMS 兼容的低压逻辑电路，此逻辑电路是固定的且与 VDD 电源电压无关。 1V 滞后典型值提供出色的抗扰度。

此驱动器具有支持固定 TTL 兼容阀值的 EN 引脚。 EN 被内部上拉；将 EN 下拉为低电平禁用驱动器，而将其保持打开可提供正常运行。 此 EN 引脚可被用作额外输入，具有与 IN，IN+，IN1 和 IN2 引脚相同的性能 引脚。

UCC2753x（顶视图）



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION(CONT.)

离开驱动器的输入引脚使输出为低电平。 驱动程序的逻辑行为如应用图，时序图和输入输出逻辑真值表所示。
VDD引脚上的内部电路提供欠压锁定功能，可将输出保持低电平，直到VDD电源电压在工作范围内。
UCC2753x驱动器采用5引脚或6引脚标准SOT-23（DBV）封装。 该器件工作在-40°C至140°C的宽温度范围

Internal circuitry on VDD pin provides an under voltage lockout function that holds output low until VDD supply voltage is within operating range.

The UCC2753x driver is offered in a 5-pin or 6-pin standard SOT-23 (DBV) package. The device operates over wide temperature range of -40°C to 140°C.

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE(2)	PEAK CURRENT (SOURCE AND SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE T_A
UCC27531DBV	SOT-23, 6-PIN	2.5 A and 5 A	TTL/CMOS –Compatible (low-voltage, independent of VDD bias voltage)	-40°C to +140°C
UCC27533DBV	SOT-23, 5-PIN	2.5-A/5-A		
UCC27536DBV	SOT-23, 5-PIN	2.5-A/2.5-A		
UCC27537DBV	SOT-23, 5-PIN	2.5-A/5-A		
UCC27538DBV	SOT-23, 6-PIN	2.5-A/5-A		

TTL / CMOS兼容（低电压，独立于VDD偏置电压）

(1) DBV package uses Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) For the most up-to-date packaging information see the TI web site.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range,	VDD	-0.3	35	V
Continuous	OUTH, OUTL, OUT	-0.3	VDD +0.3	
Pulse	OUTH, OUTL, OUT (200 ns)	-2	VDD +0.3	
Continuous IN, EN, IN+, IN-, IN1, IN2		-5	27	V
Pulse IN, EN, IN+, IN-, IN1, IN2 (1.5 µs)		-6.5	27	
Human body model, HBM (ESD)			4000	
Charged device model, CDM (ESD)			1000	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

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THERMAL INFORMATION

THERMAL METRIC		UCC27533, UCC27536, UCC27537	UCC27531, UCC27538	UNITS
		DBV	DBV(1)	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	178.3	178.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	109.7	109.7	
θ_{JB}	Junction-to-board thermal resistance(4)	28.3	28.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.7	14.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	27.8	27.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	-40		140	°C
Input voltage, IN, IN+, IN-, IN1, IN2	-5		25	V
Enable, EN	-5		25	

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Bias Currents						
I_{DDoff}	Startup current (UCC25731)	VDD = 7.0, IN, EN=VDD	100	200	300	µA
		IN, EN = GND	100	217	300	
I_{DDoff}	Startup current (UCC27533)	VDD = 7.0, IN+ = GND, IN- = VDD	100	200	300	
		IN+ = VDD, IN- = GND	100	217	300	
I_{DDoff}	Startup current (UCC27536)	VDD = 7.0, IN- = GND, EN = VDD	100	217	300	
		IN- = VDD, EN = GND	100	217	300	
I_{DDoff}	Startup current (UCC27537)	VDD =7.0, IN+, EN = VDD	100	200	300	
		IN+, EN = GND	100	217	300	
I_{DDoff}	Startup Current (UCC27538)	VDD = 7.0, IN1, IN2=VDD	100	200	300	
		IN1, IN2=GND	100	200	300	
Under Voltage Lockout (UVLO)						
V_{ON}	Supply start threshold		8.0	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	
V_{DD_H}	Supply voltage hysteresis			0.7		
Input (IN, IN+, IN1, IN2)						
V_{IN_H}	Input signal high threshold, output high	Output High, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	1.8	2.0	2.2	V
V_{IN_L}	Input signal low threshold, output low	Output Low, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	0.8	1.0	1.2	
V_{IN_HYS}	Input signal hysteresis			1.0		
Input (IN-)						
V_{IN_H}	Input signal high threshold, output low	Output low, IN+ = HIGH, EN = High	1.7	1.9	2.1	V
V_{IN_L}	Input signal low threshold, output high	Output high,, IN+ = HIGH, EN = High	0.8	1.0	1.2	
V_{IN_HYS}	Input signal hysteresis			0.9		
Enable (EN)						
V_{EN_H}	Enable signal high threshold	Output High	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output Low	0.8	1.0	1.2	
V_{EN_HYS}	Enable signal hysteresis			0.9		

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Outputs (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(13)	CLOAD = 0.22 µF, f = 1 kHz		-2.5/+5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = -10 mA	VDD -0.2	VDD - 0.12	VDD - 0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	V
V_{OL}	OUTL, Low Voltage UCC27536	I_{OUTL} = 100 mA		0.130	0.23	V
R_{OH}	OUTH, pull-up resistance (15)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = -40°C to 140°C, I_{OUT} = -10 mA	7	12	20	Ω
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	Ω
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	Ω
R_{OL}	OUTL, pull-down resistance UCC27536	T_A = 25°C, I_{OUT} = 100 mA	0.9	1.3	1.7	Ω
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.6	1.3	2.3	Ω
Switching Time						
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		ns
t_F	Fall Time UCC27536DBV	CLOAD = 1.8 nF		10		ns
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 0 V to 5 V		17	26	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 5 V to 0 V		17	26	ns
t_{D3}	Inverting turn-off propagation delay	C_{LOAD} = 1.8 nF, IN- = 0 V to 5 V		17	28	ns
t_{D4}	Inverting turn-on propagation delay	C_{LOAD} = 1.8 nF, IN- = 5 V to 0 V		20	28	ns

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Timing Diagram

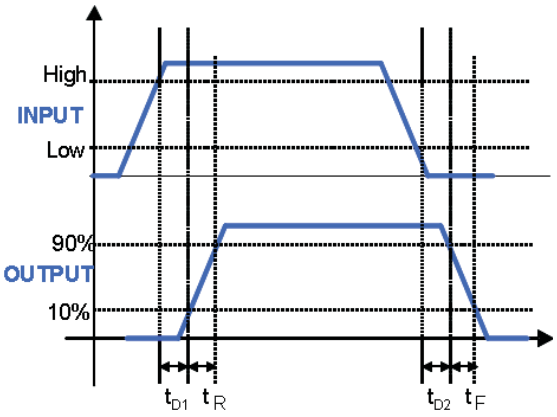

Figure 1.
UCC27531: (OUTPUT = OUTH tied to OUTL) INPUT = IN, (EN = VDD), or INPUT = EN, (IN = VDD)
UCC27537: (OUTPUT = OUT) INPUT = IN+, (EN = VDD), or INPUT = EN, (IN+ = VDD)
UCC27538: (OUTPUT = OUTH tied to OUTL) INPUT = IN1, (IN2 = VDD), or INPUT = IN2, (IN1 = VDD)

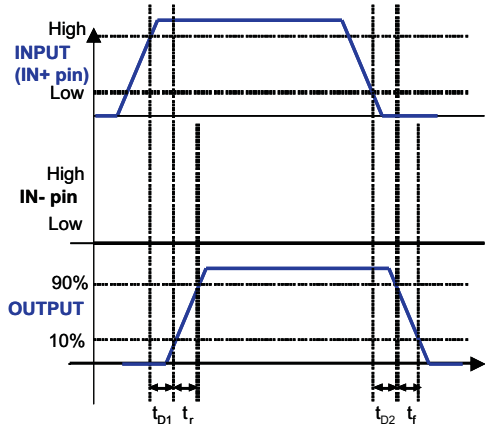

Figure 2. UCC27533: (OUTPUT = OUT) INPUT = IN+
UCC27536: (OUTPUT = OUT) INPUT = EN

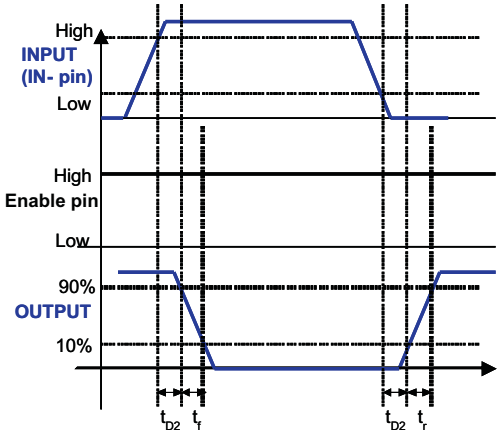

Figure 3. UCC27533: (OUTPUT = OUT) ENABLE = IN+
UCC27536: (OUTPUT = OUT) ENABLE = EN

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DEVICE INFORMATION
设备信息

Block Diagram
框图

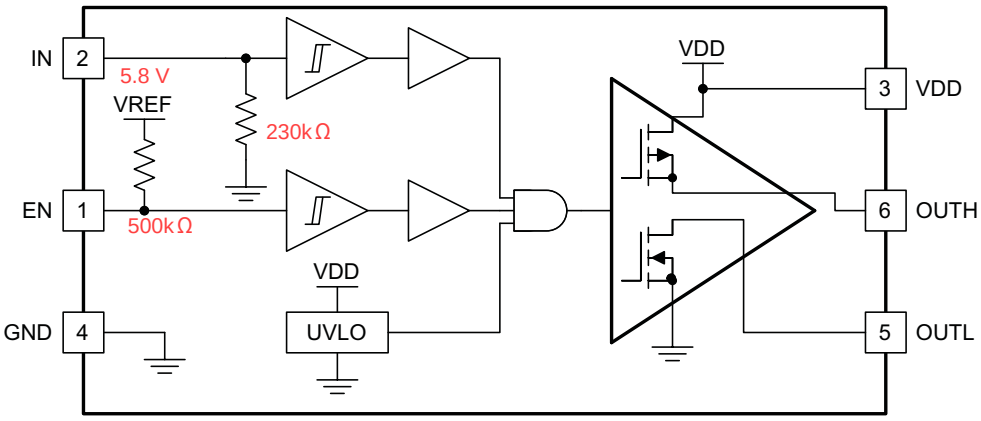

Figure 4. UCC27531
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, in pull-down resistance to GND = 230 kΩ)
（EN的上拉电阻= 500kΩ，VREF = 5.8 V，下拉电阻为GND = 230kΩ）

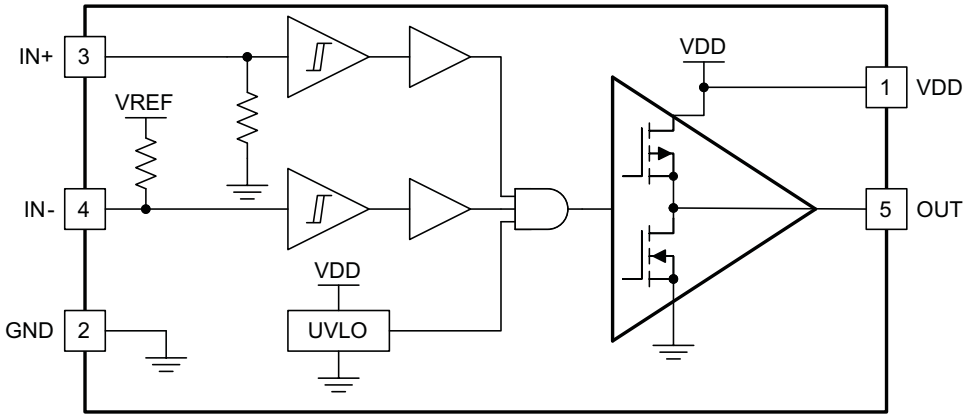

Figure 5. UCC27533
(IN- pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ pull-down resistance to GND = 230 kΩ)

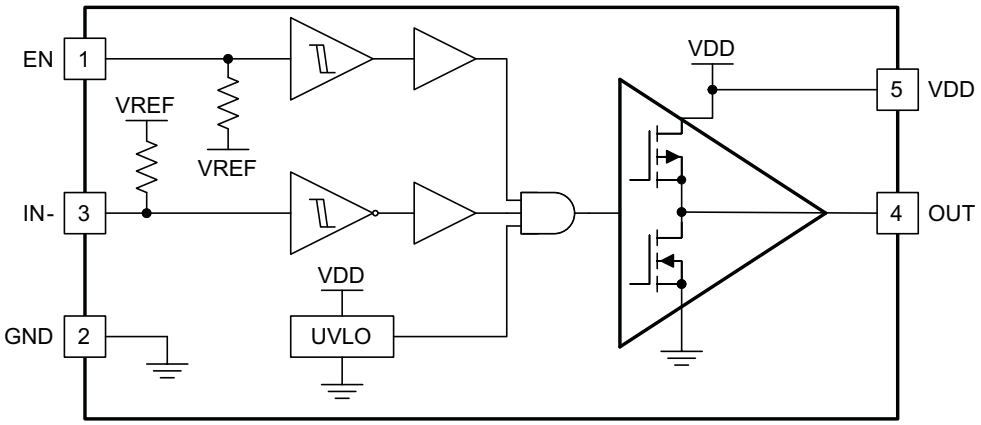

Figure 6. UCC27536
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN- pull-up resistance to VREF = 500 kΩ)

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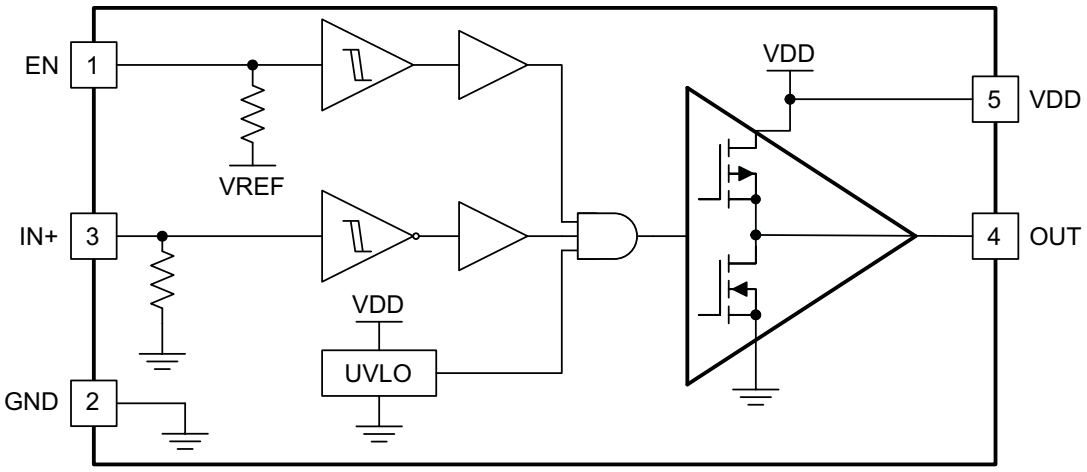

Figure 7. UCC27537
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ pull-down resistance to GND = 230 kΩ)

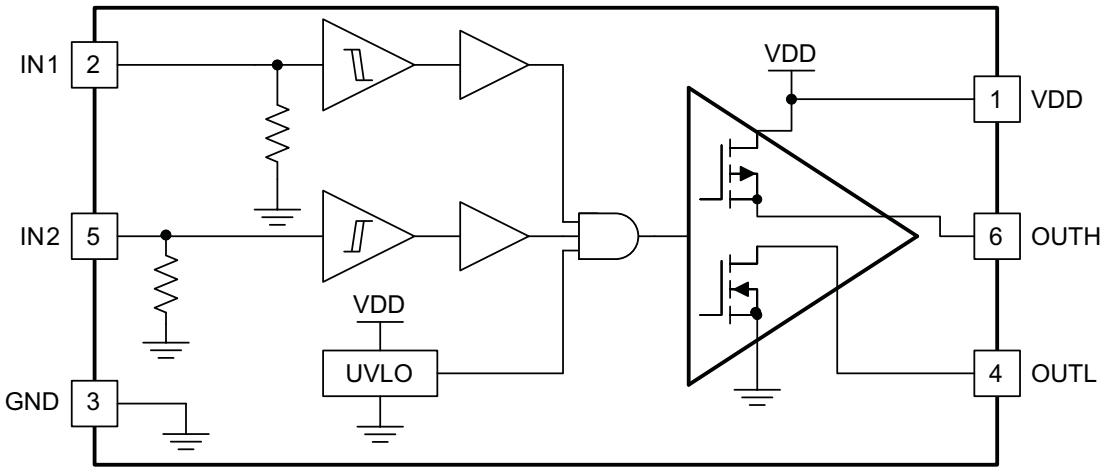

Figure 8. UCC27538
(IN1 pull-down resistance to GND = 230 kΩ, IN2 pull-down resistance to GND = 230 kΩ)

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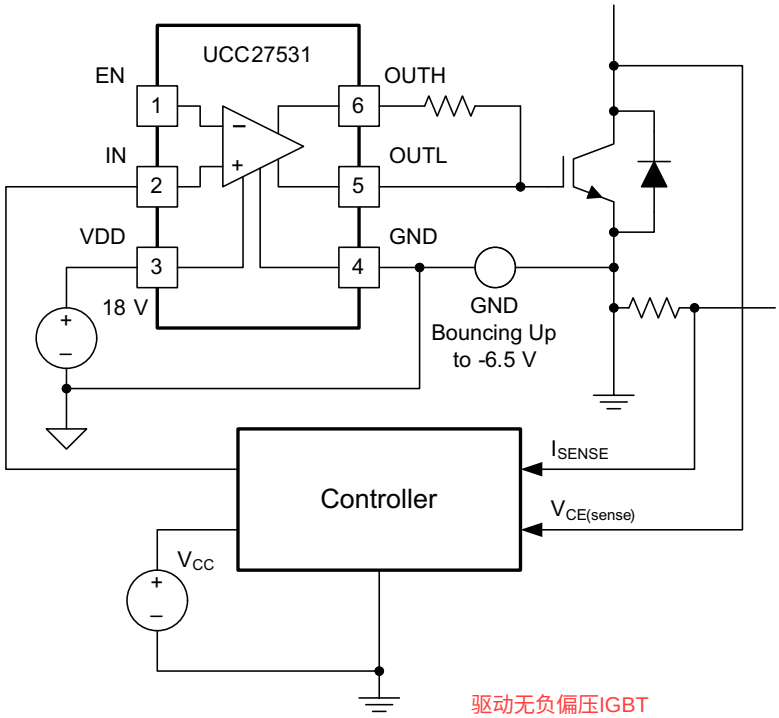
DEVICE INFORMATION

设备信息

Typical Application Diagrams

典型应用图



驱动无负偏压IGBT

Figure 9. Driving IGBT Without Negative Bias

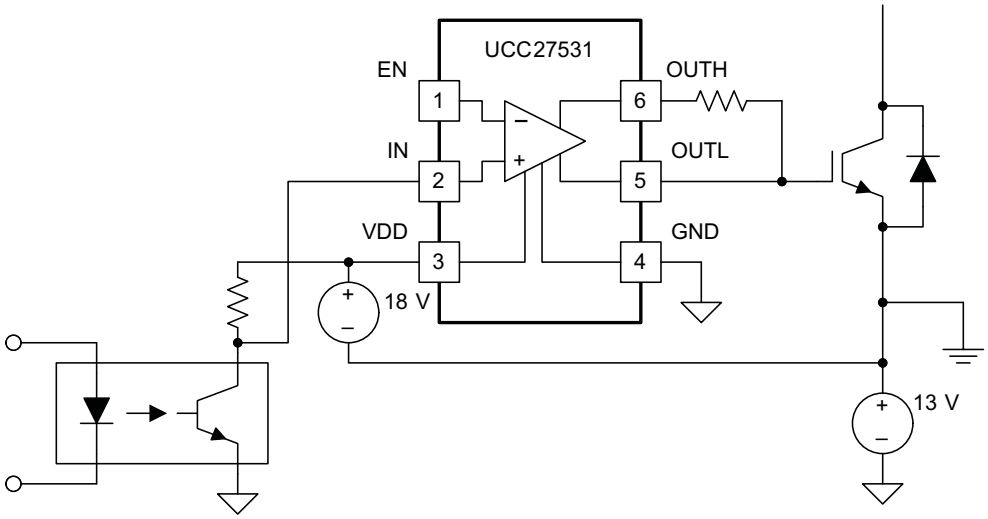


Figure 10. Driving IGBT With 13-V Negative Turn-Off Bias

驱动具有13 V负极关断偏置的IGBT

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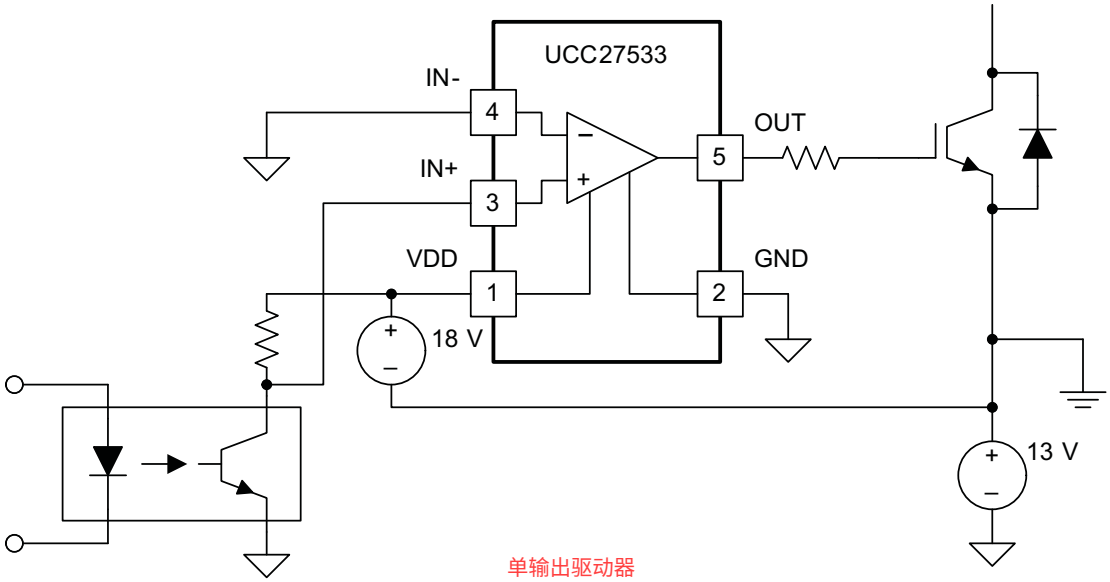

单输出驱动器

Figure 11. Single Output Driver

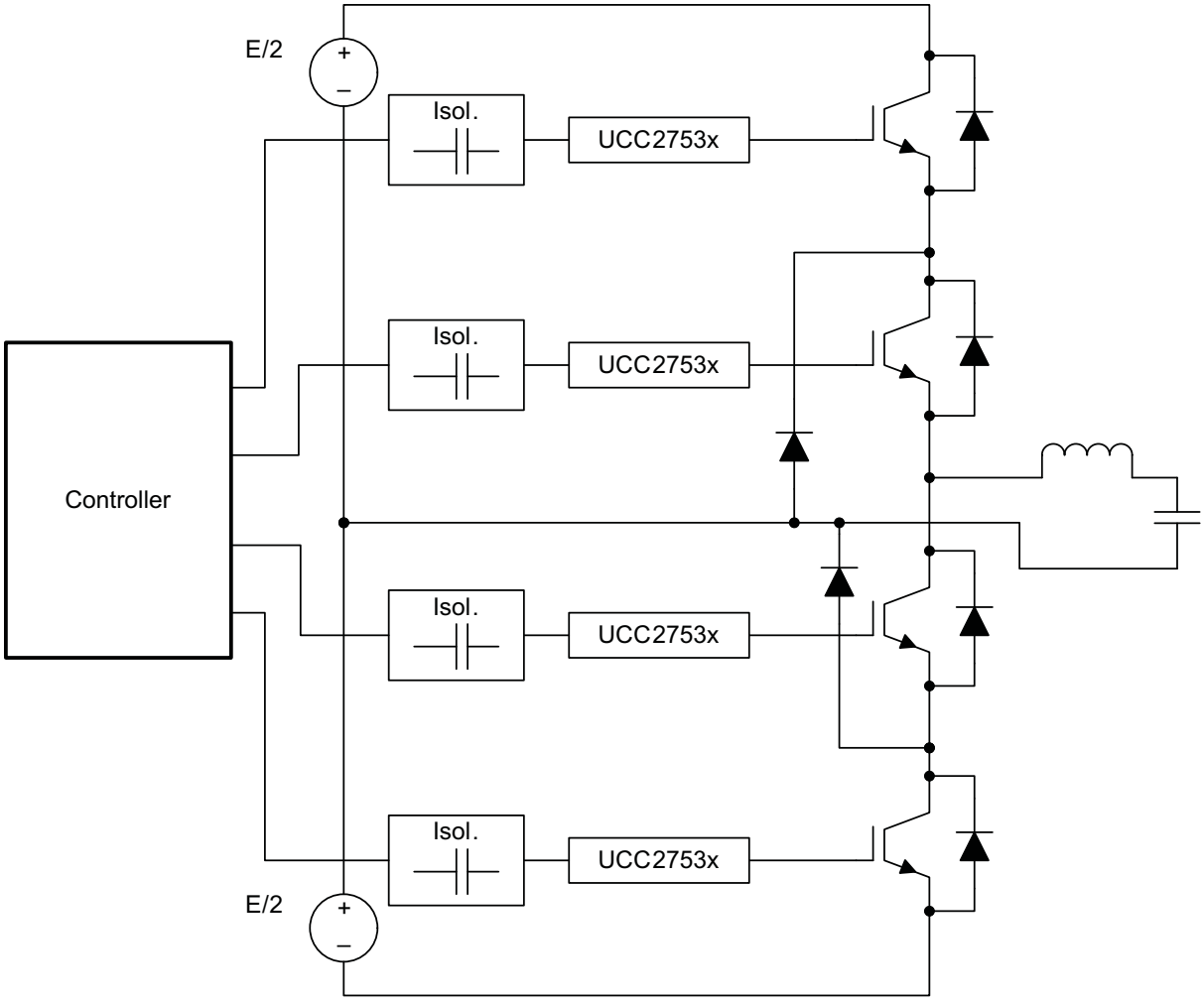

Figure 12. Using UCC2753x Drivers in an Inverter 在变频器中使用UCC2753x驱动器

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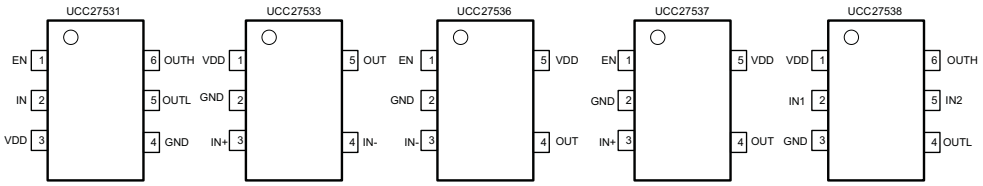
DEVICE INFORMATION

UCC2753x Product Matrix

Table 1. UCC2753x Product Matrix

	UCC27531	UCC27533	UCC27536	UCC27537	UCC27538
I_{ON} PEAK	2.5 A	2.5 A	2.5 A	2.5 A	2.5 A
I_{OFF} PEAK	5 A	5 A	2.5 A	5 A	5 A
PACKAGE	SOT-23-6	SOT-23-5	SOT-23-5	SOT-23-5	SOT-23-6
IN	Single 单	Dual 双	Single	Single	Dual
IN LOGIC	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS
EN	Yes	No	Yes	Yes	No
OUTPUT	Split 分裂	Single 单	Single	Single	Split
INVERTING 颠倒	No	Inverting/Non-Inverting 反相/非反相	Yes	No	No
MAX VDD	35 V	35 V	35 V	35 V	35 V
PIN OUT					

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TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
UCC27531DBV			
1	EN	I	Enable (Pull EN to GND in order to disable output, pull it high or leave open to enable output) 启用（将EN拉至GND以禁用输出，将其拉高或保持开路以使能输出）
2	IN	I	Driver non-inverting input 驱动器非反相输入
3	VDD	I	Bias supply input 偏置电源输入
4	GND	-	Ground (all signals are referenced to this node) 接地（所有信号都参考此节点
5	OUTL	O	5-A sink current output of driver 驱动器的5-A电流输出
6	OUTH	O	2.5-A Source Current Output of driver 驱动器的2.5-A源电流输出
UCC27533DBV			
1	VDD	I	Bias supply input
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input 驱动器非反相输入
4	IN-	I	Driver inverting input 驱动器反相输入
5	OUT	O	2.5-A source and 5-A sink current output of driver
UCC27536DBV			
1	EN	I	Enable (pull EN to GND in order to disable output, pull it high or leave open to enable output)
2	GND	-	Ground (all signals are referenced to this node)
3	IN-	I	Driver inverting input
4	OUT	O	2.5-A source and 2.5-A sink current output of driver
5	VDD	I	Bias supply input
UCC27537DBV			
1	EN	I	Enable (Pull EN to GND in order to disable Output, Pull it high or leave open to enable Output)
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input
4	OUT	O	2.5-A source and 5-A sink current output of driver
5	VDD	I	Bias supply input
UCC27538DBV			
1	VDD	I	Bias supply input
2	IN1	I	Driver non-inverting input
3	GND	-	Ground (all signals are referenced to this node)
4	OUTL	O	5-A sink current output of driver
5	IN2	I	Driver non-inverting input
6	OUTH	O	2.5-A source current output of driver

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INPUT/OUTPUT LOGIC TRUTH TABLE (for single output driver)

输入/输出逻辑真值表（单输出驱动器）

UCC27531DBV				
IN PIN	**EN PIN**	**OUTH PIN**	**OUTL PIN**	**OUT (OUTH and OUTL pins tied together)**
L	L	High-impedance高阻抗	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H
H	FLOAT浮动	H	High-impedance	H
FLOAT	H	High-impedance	L	L

OUTH和OUTL引脚连在一起

INPUT/OUTPUT LOGIC TRUTH TABLE

UCC27533DBV		
IN+ PIN	**IN- PIN**	**OUT PIN**
L	L	L
L	H	L
H	L	H
H	H	L
FLOAT	X	L
X	FLOAT	L
UCC27536DBV		
IN- PIN	**EN PIN**	**OUT PIN**
L	L	L
L	H	H
H	L	L
H	H	L
FLOAT	X	L
L	FLOAT	H
UCC27537DBV		
IN+ PIN	**EN PIN**	**OUT PIN**
L	L	L
L	H	L
H	L	L
H	H	H
FLOAT	X	L
H	FLOAT	H

INPUT/OUTPUT LOGIC TRUTH TABLE (for single output driver)

UCC27538DBV				
IN1 PIN	**IN2 PIN**	**OUTH PIN**	**OUTL PIN**	**OUT (OUTH and OUTL pins tied together)**
L	L	High-Impedance	L	L
L	H	High-Impedance	L	L
H	L	High-Impedance	L	L
H	H	H	High-Impedance	H
X	FLOAT	High-Impedance	L	L
FLOAT	X	High-Impedance	L	L

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TYPICAL CHARACTERISTICS

If not specified, INPUT refers to non-inverting input

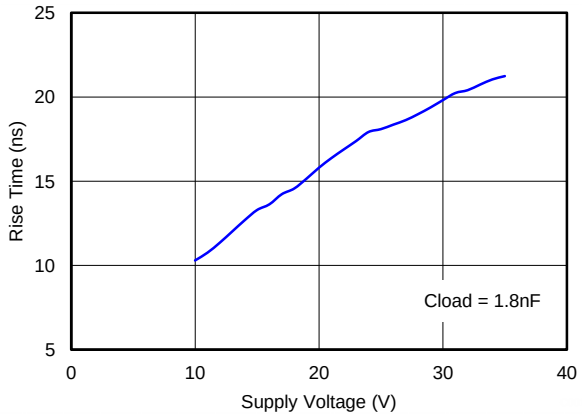

Figure 13. Rise Time vs. Supply Voltage

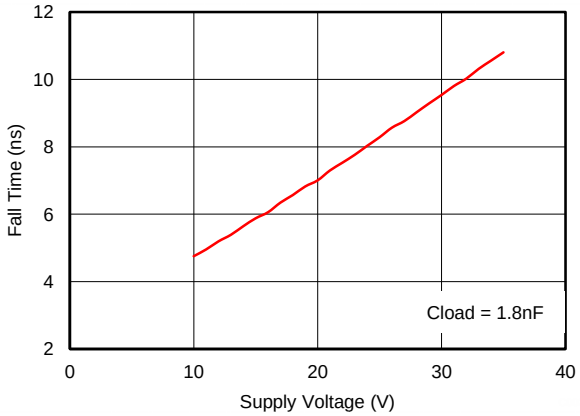

Figure 14. Fall Time vs. Supply Voltage

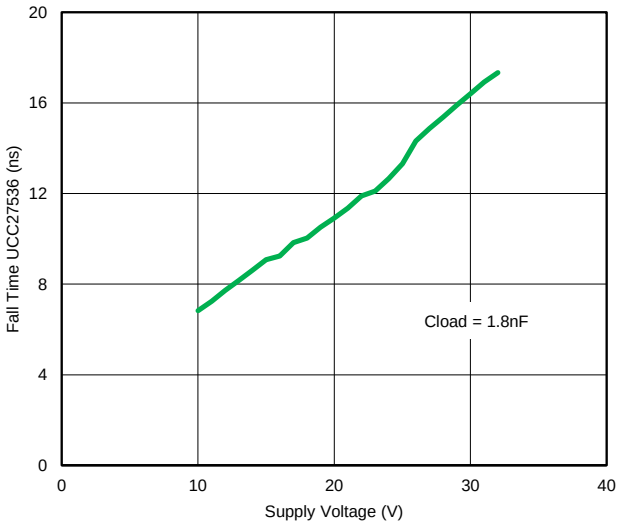

Figure 15. UCC27536 Fall Time vs. Supply Voltage

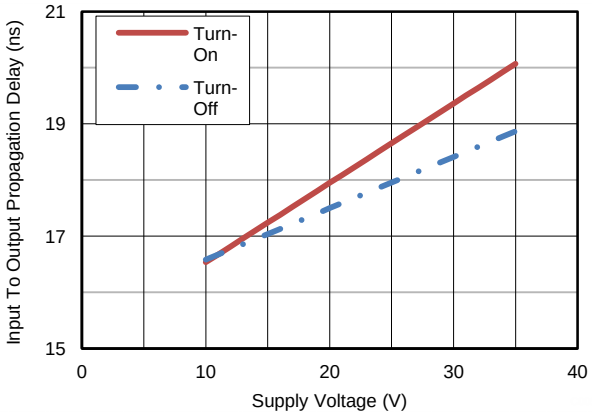

Figure 16. Propagation Delay vs. Supply Voltage

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

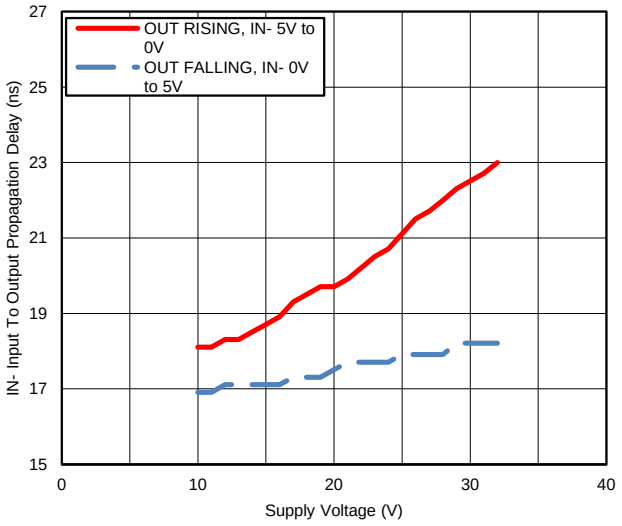

Figure 17. IN- Propagation Delay vs. Supply

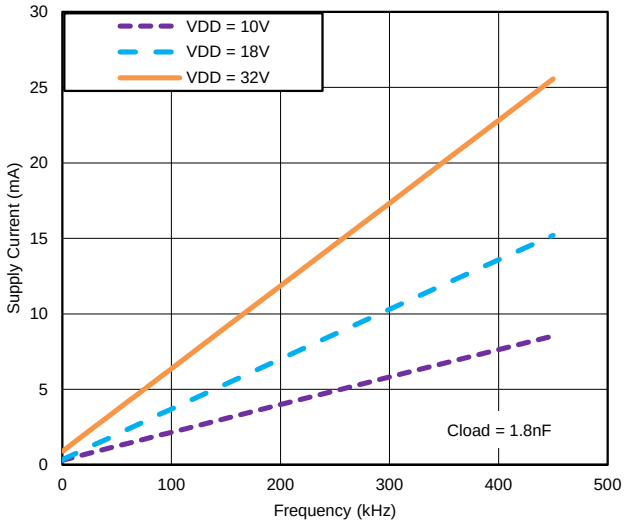

Figure 18. Operating Supply Current vs. Frequency

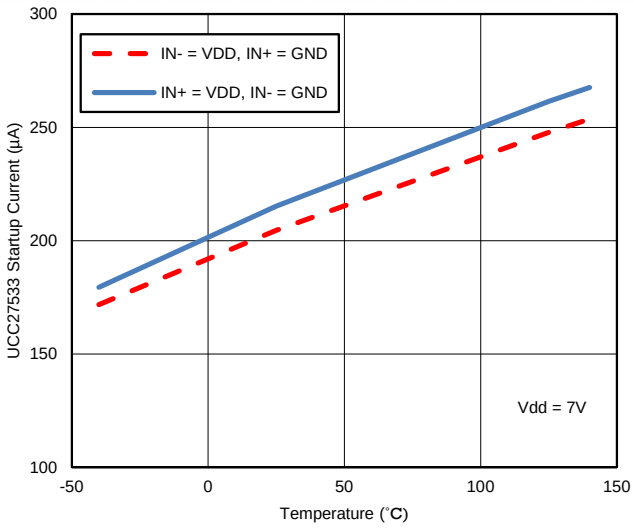

Figure 19. UCC27533 Start-Up Current vs. Temperature

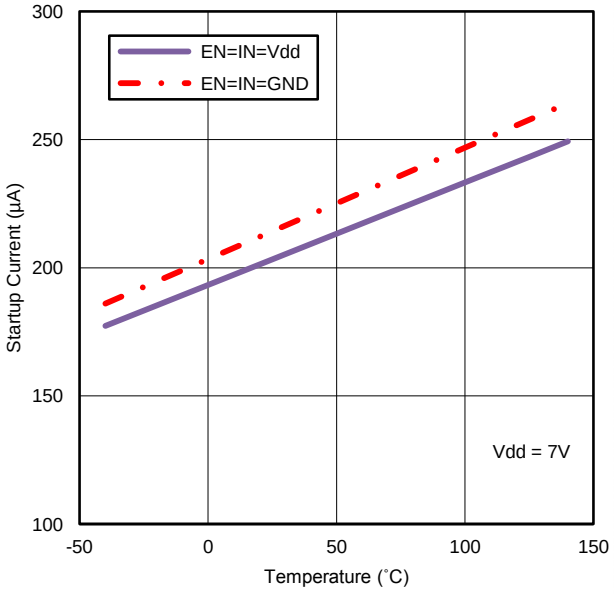

Figure 20. UCC27531 Start-Up Current vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

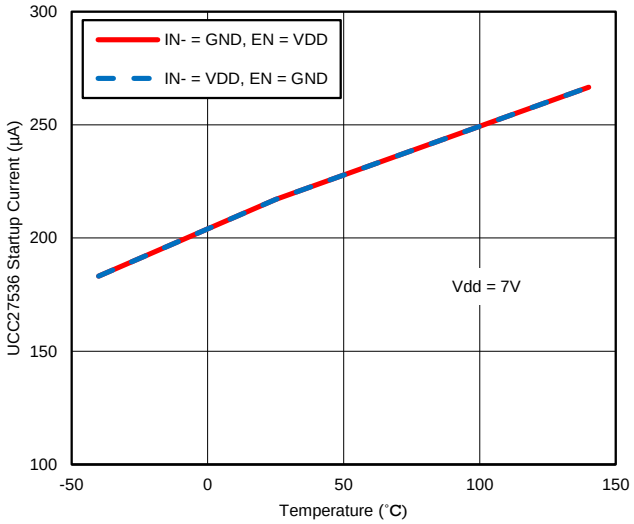

Figure 21. UCC27536 Start-Up Current vs. Temperature

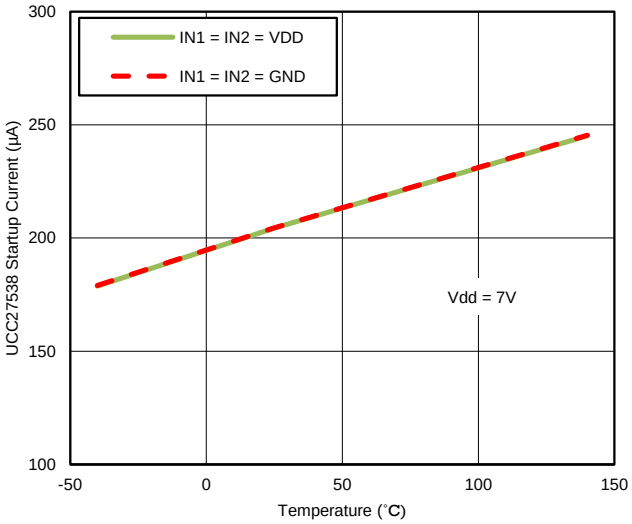

Figure 22. UCC27538 Start-Up Current vs. Temperature

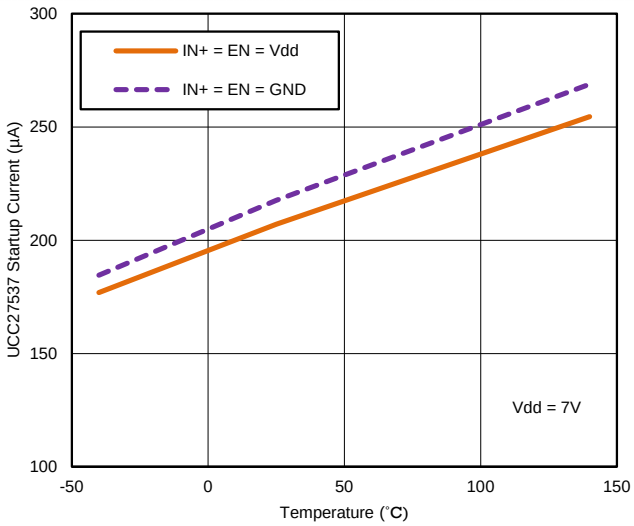

Figure 23. UCC27537 Start-Up Current vs. Temperature

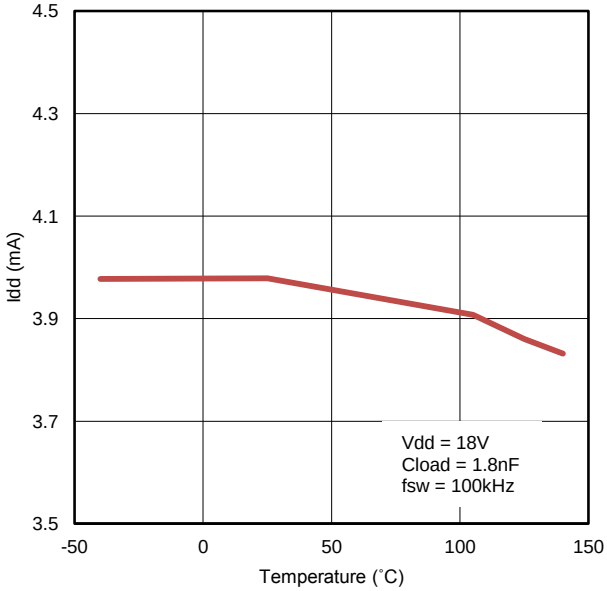

Figure 24. Operating Supply Current vs. Temperature (output switching)

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

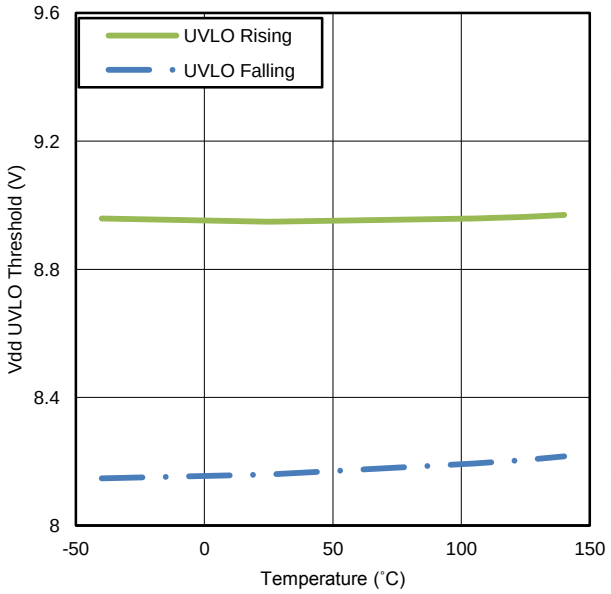

Figure 25. UVLO Threshold Voltage vs. Temperature

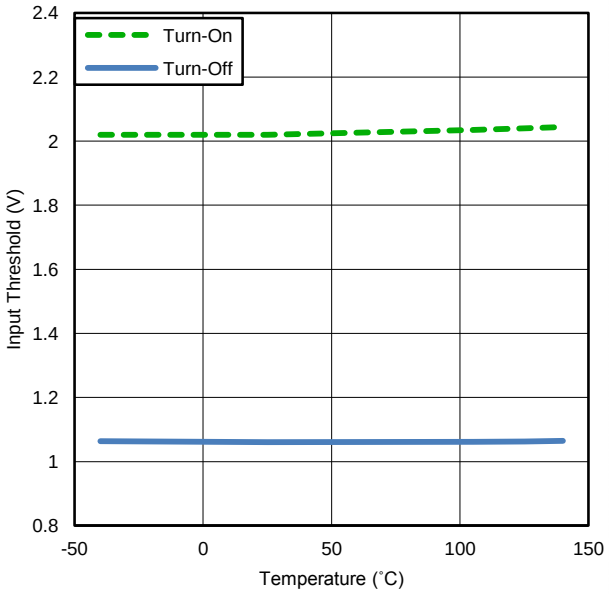

Figure 26. Input Threshold vs. Temperature

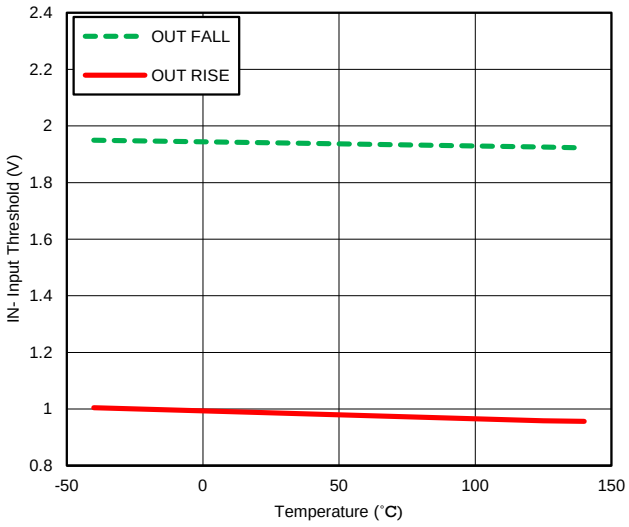

Figure 27. IN- Input Threshold vs. Temperature

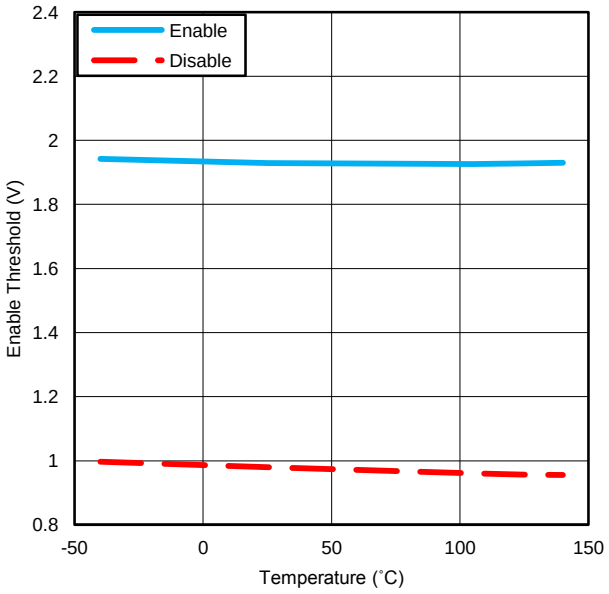

Figure 28. Enable Threshold vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

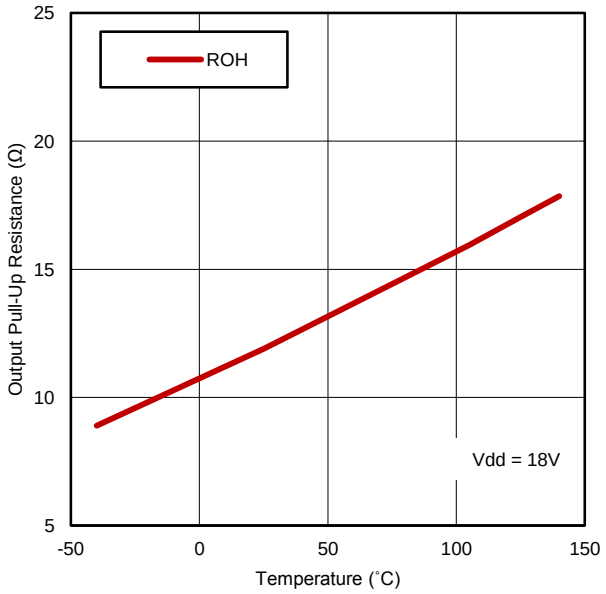

Figure 29. Output Pull-Up Resistance vs. Temperature

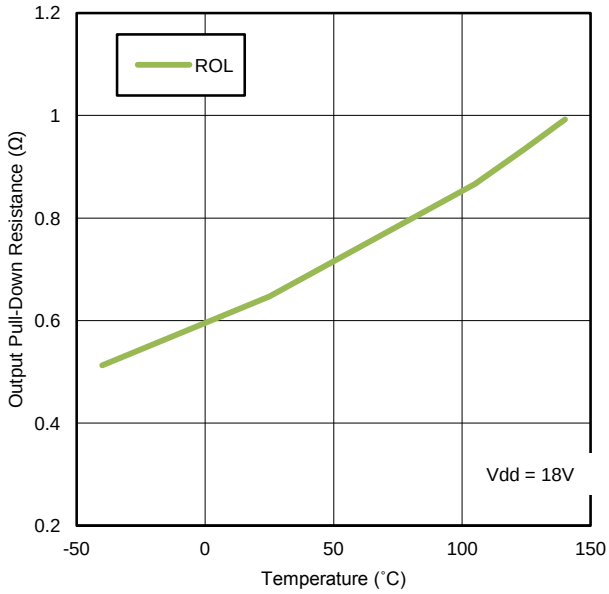

Figure 30. Output Pull-Down Resistance vs. Temperature

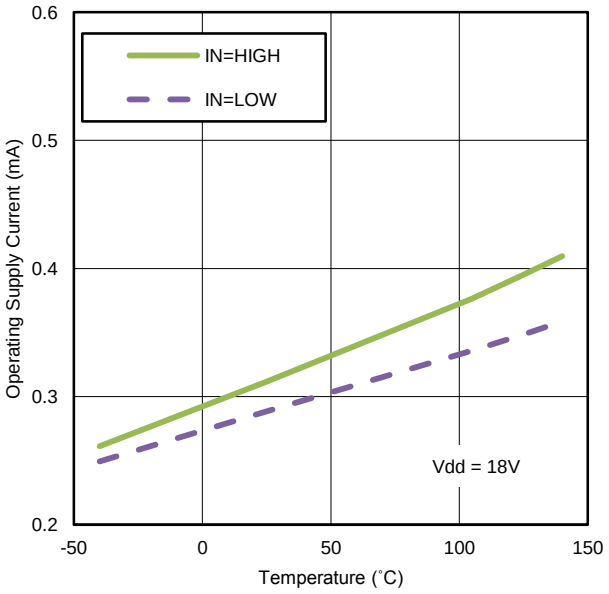

Figure 31. Operating Supply Current vs. Temperature (output in DC on/off condition)

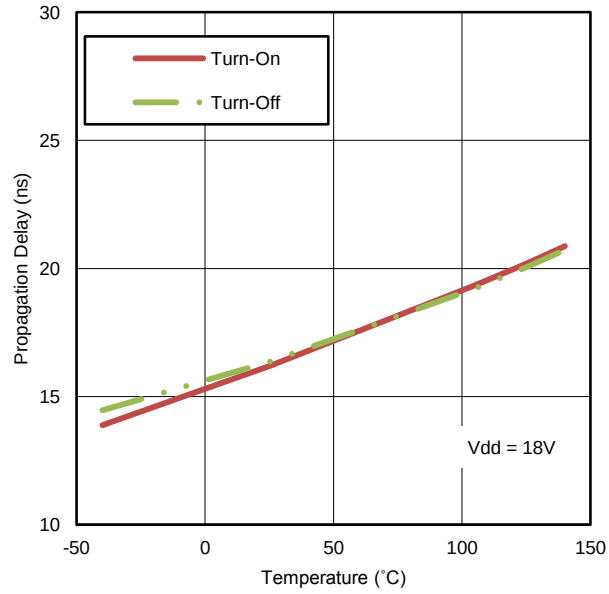

Figure 32. Input-to-Output Propagation Delay vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

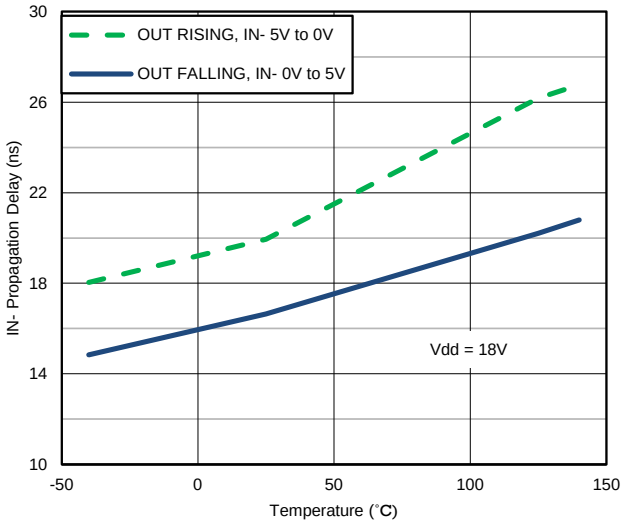

Figure 33. IN- Input-to-Output Propagation Delay vs. Temperature

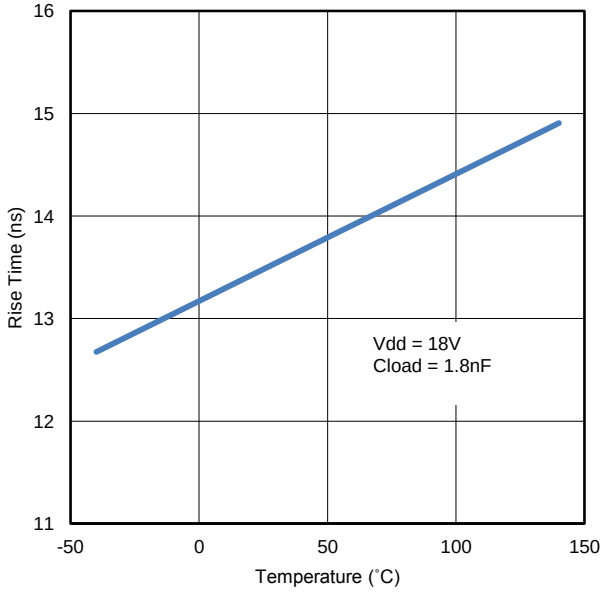

Figure 34. Rise Time vs. Temperature

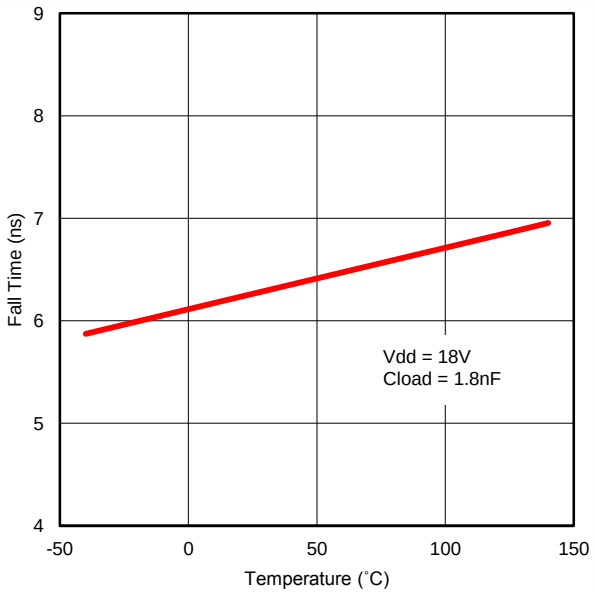

Figure 35. Fall Time vs. Temperature

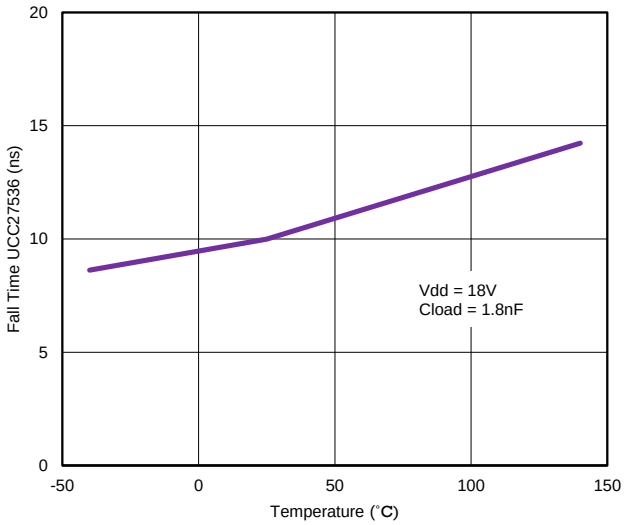

Figure 36. UCC27536 Fall Time vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

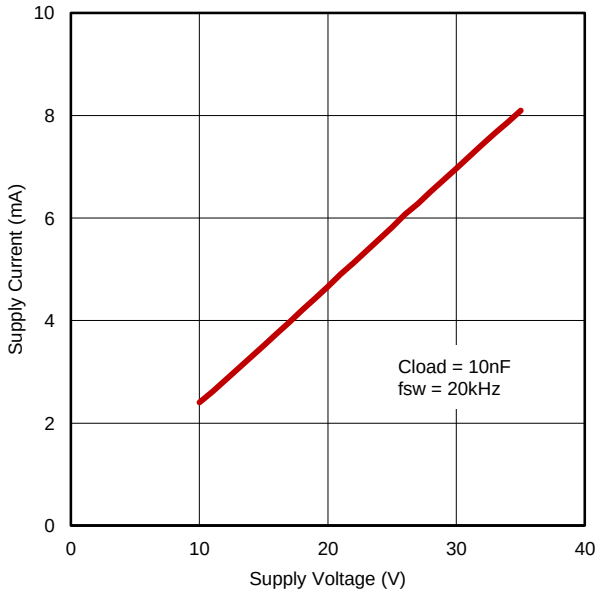

Figure 37. Operating Supply Current vs. Supply Voltage (output switching)

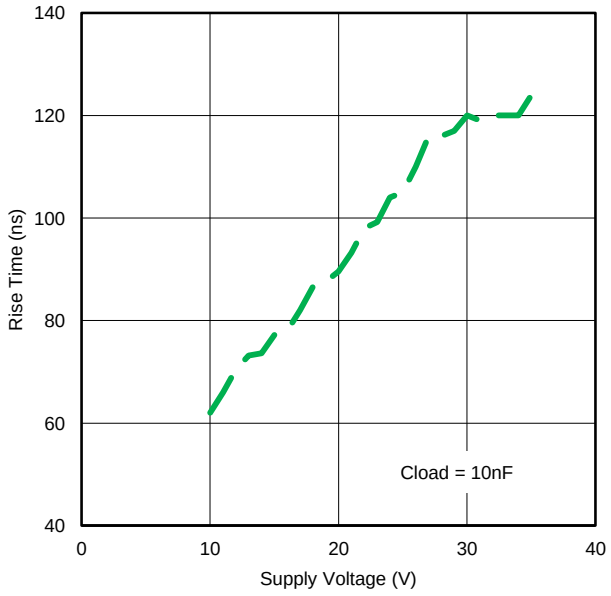

Figure 38. Rise Time vs. Supply Voltage

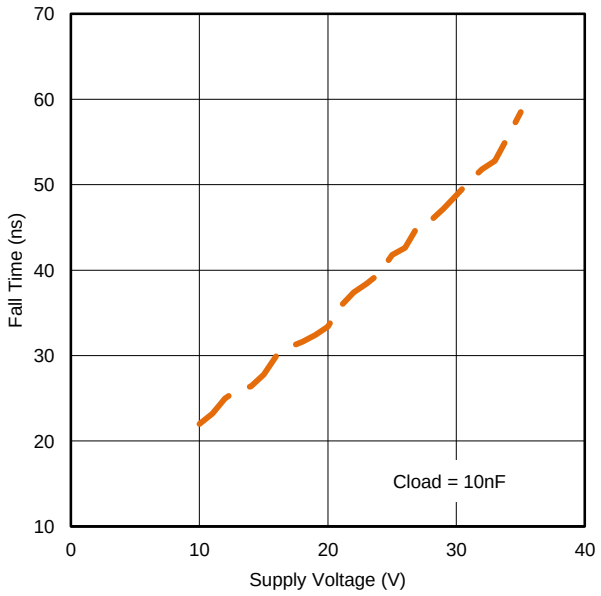

Figure 39. Fall Time vs. Supply Voltage

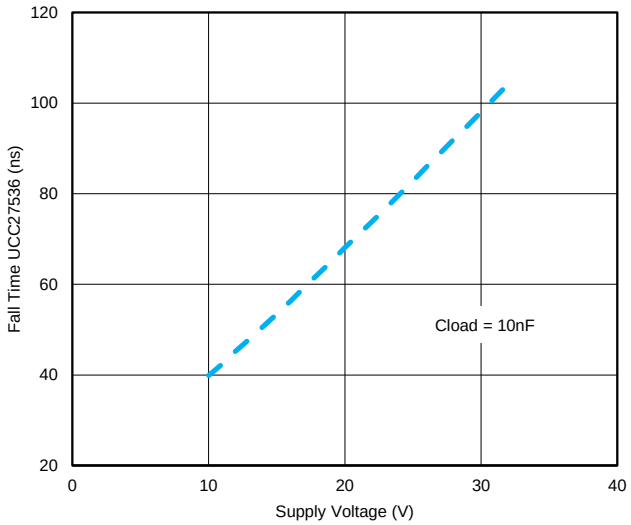

Figure 40. UCC27536 Fall Time vs. Supply Voltage

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APPLICATION INFORMATION

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered since the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or p- n-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this since they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC2753x is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V(relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC2753x can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC2753x. Alternatively, in a high-side drive configuration the UCC2753x can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC2753x need to drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC2753x extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

由于各种原因，开关电源应用中需要大电流栅极驱动器件。 为了实现功率器件的快速切换并降低相关的开关功率损耗，可以在控制器或信号隔离器件的PWM输出与功率半导体器件的栅极之间采用强大的栅极驱动器。 此外，当有时PWM控制器直接驱动开关器件的栅极是不可行的，栅极驱动器是不可或缺的。 由于来自数字控制器或信号隔离装置的PWM信号通常是不能有效打开电源开关的3.3 V或5 V逻辑信号，所以会经常遇到这种情况。 需要电平移位电路来将逻辑电平信号提升到栅极驱动电压，以便完全打开功率器件并最小化传导损耗。 基于NPN / PNP双极性（或p- n沟道MOSFET）的传统缓冲驱动电路，图腾柱晶体管是发射极跟随器配置，由于它们缺乏电平移动能力和低驱动电压保护，因此证明不足 。 门驱动器有效地结合了电平转换，缓冲驱动和UVLO功能。 栅极驱动器还可以通过将大电流驱动器物理靠近功率开关，驱动栅极驱动变压器和控制浮动功率器件栅极来最小化开关噪声的影响，从而通过移动来减少控制器中的功耗和热应力 栅极自身的电荷损耗。 UCC2753x在这个角色中非常灵活，具有强大的电流驱动能力和高达32 V的宽电源电压范围。这允许驱动器用于12 V Si MOSFET应用，20 V和-5 V（相对于 源）SiC FET应用，15 V和-15 V（相对于发射极）IGBT应用等等。 作为单通道驱动器，UCC2753x可以用作低端或高端驱动器。 作为低端驱动器，开关地通常是系统接地，因此可以直接连接到门驱动器。 然而，要使用具有浮动返回节点的高边驱动器，则需要控制器进行信号隔离以及与UCC2753x的隔离偏置。 或者，在高侧驱动配置中，UCC2753x可以直接连接到控制器信号，并通过非隔离电源进行偏置。 然而，在这种配置中，UCC2753x的输出需要驱动脉冲变压器，然后驱动电源开关与电源开关的浮动源和发射极正常工作。 此外，具有独立的OUTH和OUTL引脚控制导通和关断速度的能力确保最佳效率，同时保持系统的可靠性。 这些要求加上需要具有良好散热能力的紧凑型低电感封装中的低传播延迟和可用性，使得诸如UCC2753x之类的栅极驱动器器件在开关电源中极为重要的部件组合了高性能，低成本，元件数量和 减少电路板空间并简化系统设计。

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Table 2. UCC2753x Features and Benefits

FEATURE特征	BENEFIT 效益
High ... 5 A (asymmetrical). 2.5A和5（不对称）高源和灌电流能力。	High ... 采用UCC2753x器件，以高速度驱动各种电源开关器件，具有高电流能力。
Low 17 ns (typ) propa... 低17 ns（典型值）传播延迟。	Extremely low pulse transmission distortion. 极低的脉冲传输失真。
Wide VDD operating range of 10 V to 32 V. 宽VDD工作范围为10 V至32 V.	Flexibility in system design. 灵活的系统设计。
Ca... neg...	可用于分体轨系统，例如驱动具有正负极（相对于发射极）电源的IGBT。
	Optimal for many SiC FETs. 适用于许多SiC FET。
VDD UVLO protection. VDD UVLO保护。	输出在UVLO条件下保持低电平，可确保在上电和掉电时可预测的无毛刺操作。
	8.9V典型的高UVLO可确保电源开关在高阻态下不导通，这可能导致高功耗或甚至故障。
当输入引脚（INx）处于浮置状态时，输出保持低电平。	安全特性，特别适用于在安全认证过程中通过异常情况测试
分割输出结构选项（OUTH，OUTL）。	允许使用串联栅极电阻独立优化开启和关闭速度。
强电流（5A）和低下拉电流阻抗（0.65Ω）。	High immunity to high dV/dt Miller turn-on events. 对高dV / dt米勒开启事件的高度免疫力。
CMOS和TTL兼容输入阈值逻辑，具有较大的滞后...	同时保持与微控制器逻辑电平输入信号（3.3 V，5 V）的兼容性，优化数字电源。
Input capable of withstanding -6.5 V. 输入能承受-6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver. 在嘈杂的环境中增强信号的可靠性，在门驱动器上经历地面反弹。

VDD Under Voltage Lockout VDD欠压锁定

The UCC2753x device has internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power-up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

UCC2753x器件在VDD引脚电源电路块上具有内部欠压锁定（UVLO）保护功能。 为了确保电源开关中可接受的功耗，该UVLO可防止栅极驱动器在低电源电压下工作。 每当驱动器处于UVLO状态（当上电时VDD电压小于VON，掉电期间VDD电压小于VOFF时），无论输入状态如何，该电路均保持所有输出为低电平。 UVLO通常为8.9 V，典型值为700 mV。 这种滞后有助于防止低VDD电源电压从电源产生噪声并且当系统开始切换并且IDD突然增加时VDD偏置电压下降时产生颤动。 在10 V至32 V的电压电平下工作的能力可以灵活地驱动Si MOSFET，IGBT和新兴的SiC FET。

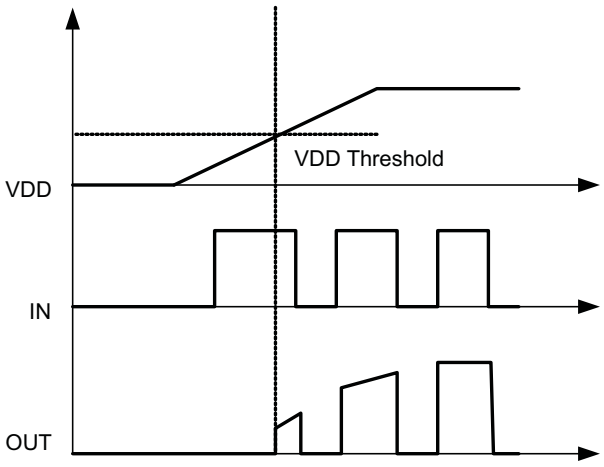

Figure 41. Power Up

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Input Stage 输入阶段

The input pins of UCC2753x device are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 2 V and typical low threshold = 1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and guarantees stable operation across temperature. The very low input capacitance , typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pull-up or pull-down resistors on the input pins as shown in the block diagrams.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switching to amplitude > 15 V
- Input or Enable pins are switched at dV/dt > 2 V/ns

If both of these conditions occur, it is advised to add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

Enable Function

The Enable (EN) pin of the UCC2753x has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

ucc2753x装置的输入引脚基于TTL和CMOS兼容的输入阈值逻辑是独立的电源电压VDD。典型的高门槛= 2 V，典型的低阈值= 1 V，逻辑电平阈值可以方便地驱动PWM控制信号从3.3V或5V逻辑。宽滞后（通常为1 V）提供了增强的噪声免疫力相比传统的TTL逻辑的实现，其中的滞后是通常小于0.5 V.该装置还具有输入引脚的阈值电压水平，简化系统的设计，保证稳定运行在严格控制温度，非常低的输入电容，通常为20 pF，这些减少加载和切换速度，增加销。
该装置具有重要的安全功能，其中每当输入引脚处于浮动状态时，输出保持在低状态。这是通过输入引脚上的下拉或下拉电阻来实现的，如方框图所示。
驱动程序的输入级最好由短上升或下降时间信号驱动。当司机使用缓慢变化的输入信号时，必须小心，尤其是在设备位于独立的子板或PCB布局有长输入连接痕迹的情况下：
?高di/dt电流驱动器输出耦合板布局寄生效应会引起接地反弹。由于该设备的功能只有一个GND引脚，可参考电源地，这可能干扰输入引脚和GND之间的差分电压，并触发输出状态的意外变化。
由于快速的17 ns的传播延迟，这可能最终导致高频振荡，这增加了功耗，并造成损害的风险。
?V输入阈值迟滞增强抗噪声比大多数其他行业标准的驱动程序。
如果限制功率器件的上升或下降时间以减少电磁干扰，则在驱动器和电源设备的输出之间强烈推荐外部电阻，而不是在输入信号上增加延迟。这种外部电阻器有一个额外的好处，就是减少栅极驱动装置封装中与栅极电荷有关的部分损耗，并将其转移到外部电阻器本身。
最后，由于允许输入和启用引脚负电压能力的独特输入结构，在下列应用中必须谨慎使用：
输入或使能引脚切换到幅度> 15 V
?输入或使能引脚切换到dt / dt > 2伏/纳秒
如果这些情况发生，建议添加一系列150的销Ω电阻（S）被切换到限制通过输入结构的电流。
启用功能
启用（EN）的ucc2753x引脚具有内部上拉电阻的内部参考电压将使浮动打开驱动器和允许它发送输出信号正常。如果需要，启用也可以由低电压逻辑来驱动和禁用驱动程序。

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Output Stage

The output stage of the UCC2753x device is illustrated in Figure 42. The UCC2753x device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

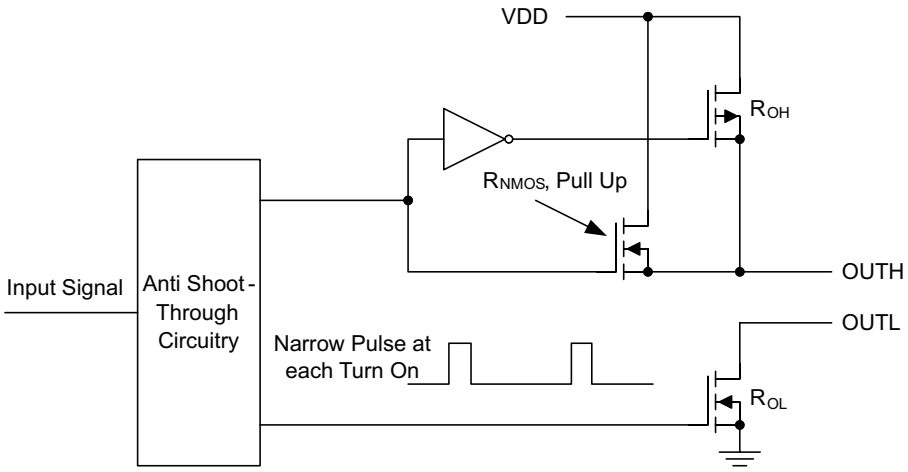

Figure 42. UCC27531 Gate Driver Output Stage 栅极驱动器输出级

Split output depicted in Figure 42. For devices with single OUT pin, OUTH and OUTL are connected internally and then connected to OUT.

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by ROH parameter. The pull-down structure is composed of a N-Channel MOSFET only. The ROL parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC2753x, the effective resistance of the hybrid pull-up structure is approximately 3 x R_{OL}.

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The UCC2753x is capable of delivering 2.5-A source, and up to 5-A sink at VDD = 18 V. Strong sink capability results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in Off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in Figure 43.

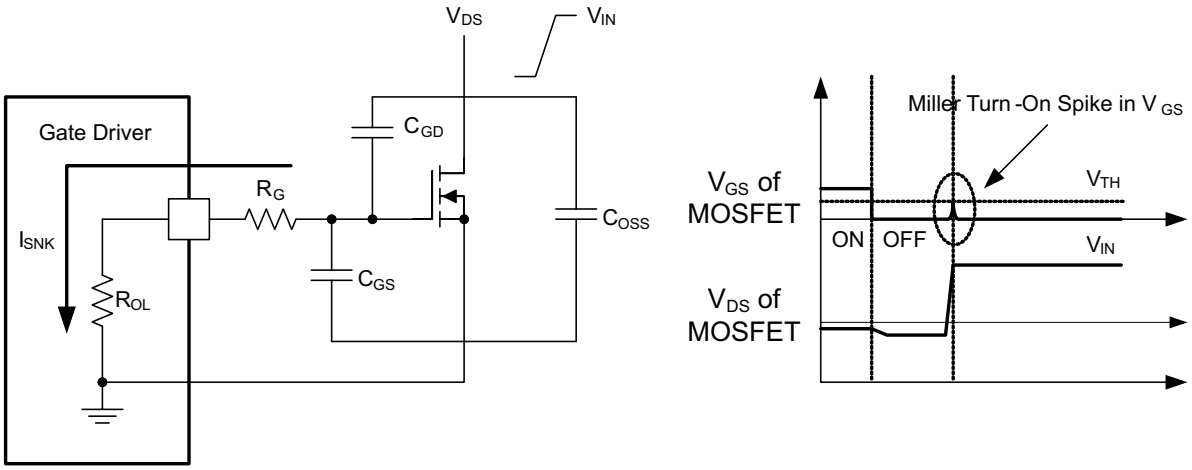

Figure 43. Low Pull-Down Impedance in UCC2753x (output stage mitigates Miller turn-on effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated.

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Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC2753x features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is discharged. During turn off the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 3 x R_{OL} (5)

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Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the 'Thermal Information' section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled "IC Package Thermal Metrics" (SPRA953A).

PCB Layout

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC2753x gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the driver Output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Changed Block Diagram. 7

Changes from Revision A (December 2012) to Revision B **Page**

- Added UCC27533, UCC27536, UCC27537 and UCC27538 parts to the datasheet. 1

Changes from Revision B (April 2013) to Revision C **Page**

- Added 额外说明信息。 1

Changes from Revision C (April, 2013) to Revision D **Page**

- Added Startup Current UCC27537 Bias Current Parameters to the ELECTRICAL CHARACTERISTICS. 4
- Added UCC27531 Start-Up Current vs. Temperature TYPICAL CHARACTERISTICS diagram. 15
- Added UCC27537 Start-Up Current vs. Temperature TYPICAL CHARACTERISTICS diagram. 16

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27531D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27531D	Samples
UCC27531DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27531DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27531DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27531D	Samples
UCC27533DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples
UCC27533DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples
UCC27536DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7536	Samples
UCC27536DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7536	Samples
UCC27537DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7537	Samples
UCC27537DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7537	Samples
UCC27538DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7538	Samples
UCC27538DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7538	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC27531 :

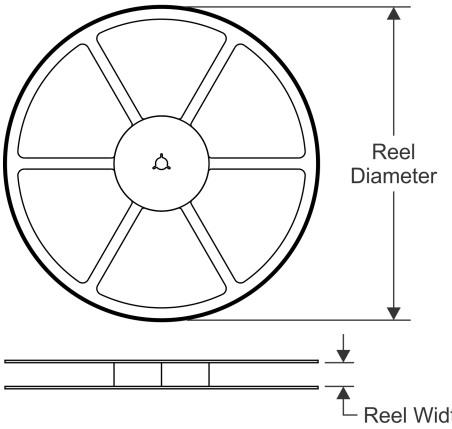
- Automotive: UCC27531-Q1

NOTE: Qualified Version Definitions:

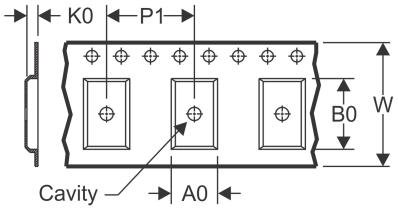
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

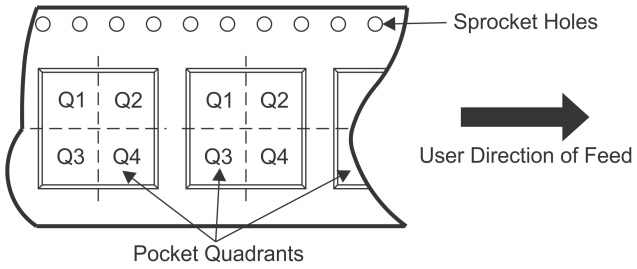


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

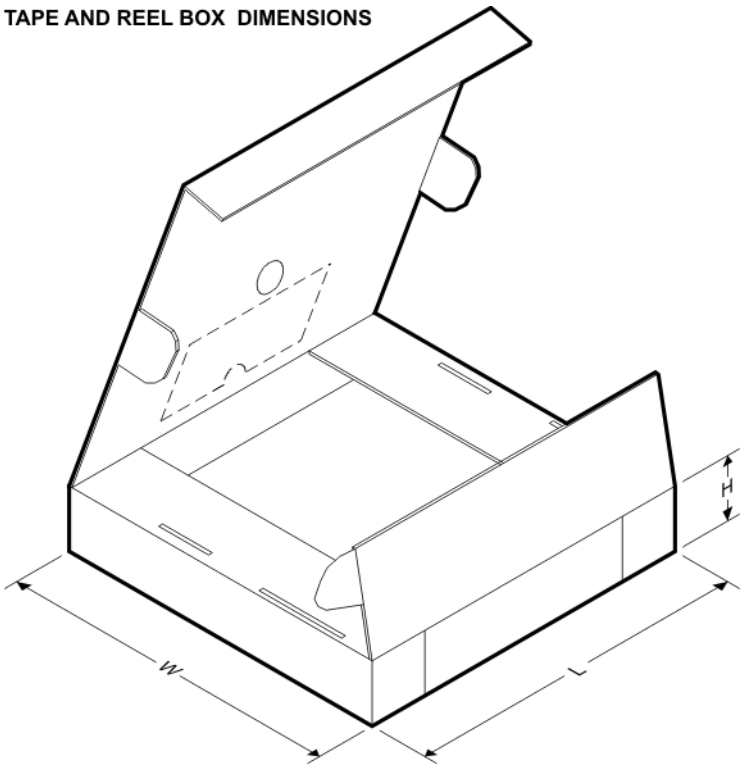
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27531DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27531DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27531DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27531DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27531DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27533DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27533DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27536DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27536DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27537DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27537DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27538DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27538DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

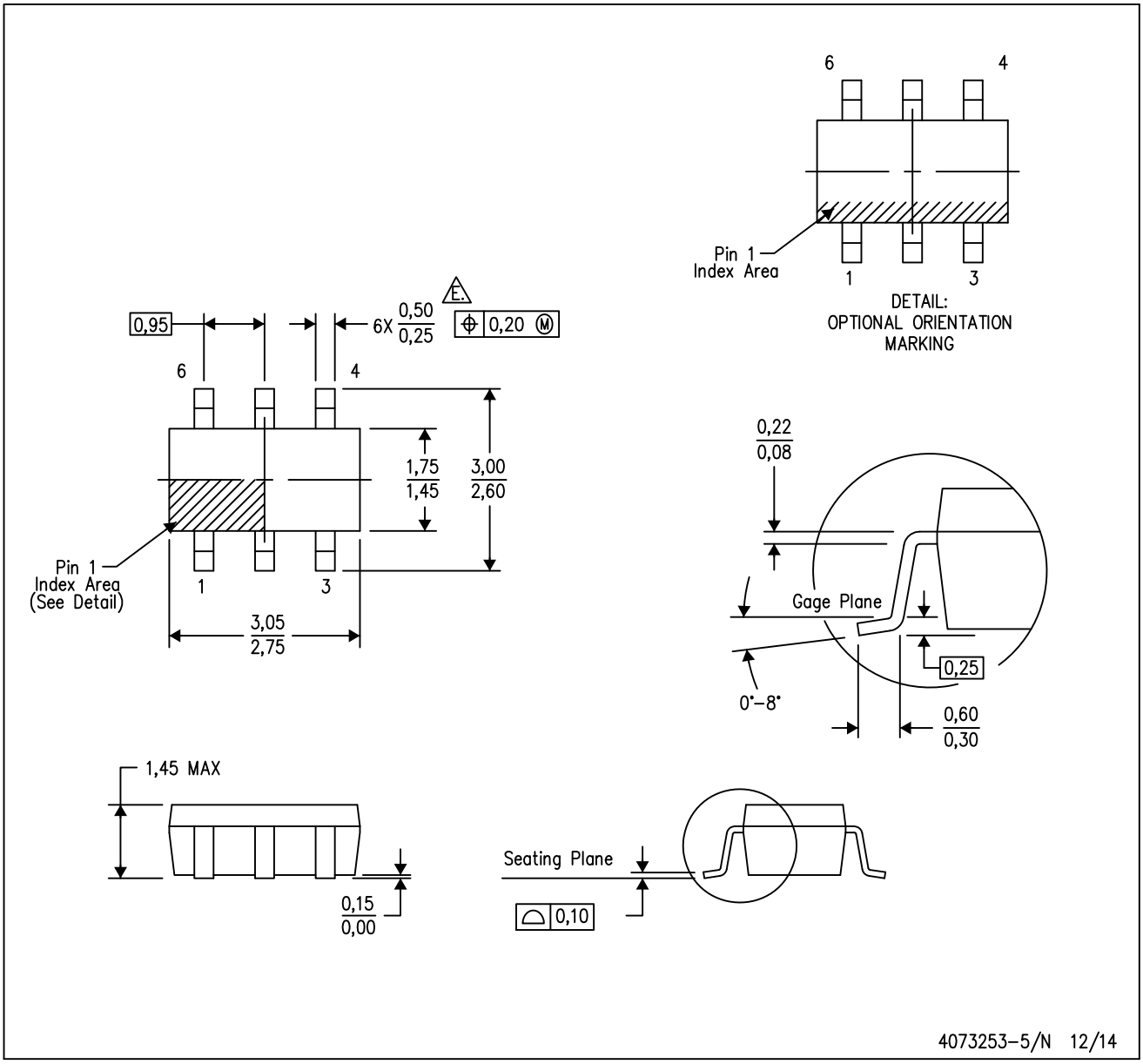
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

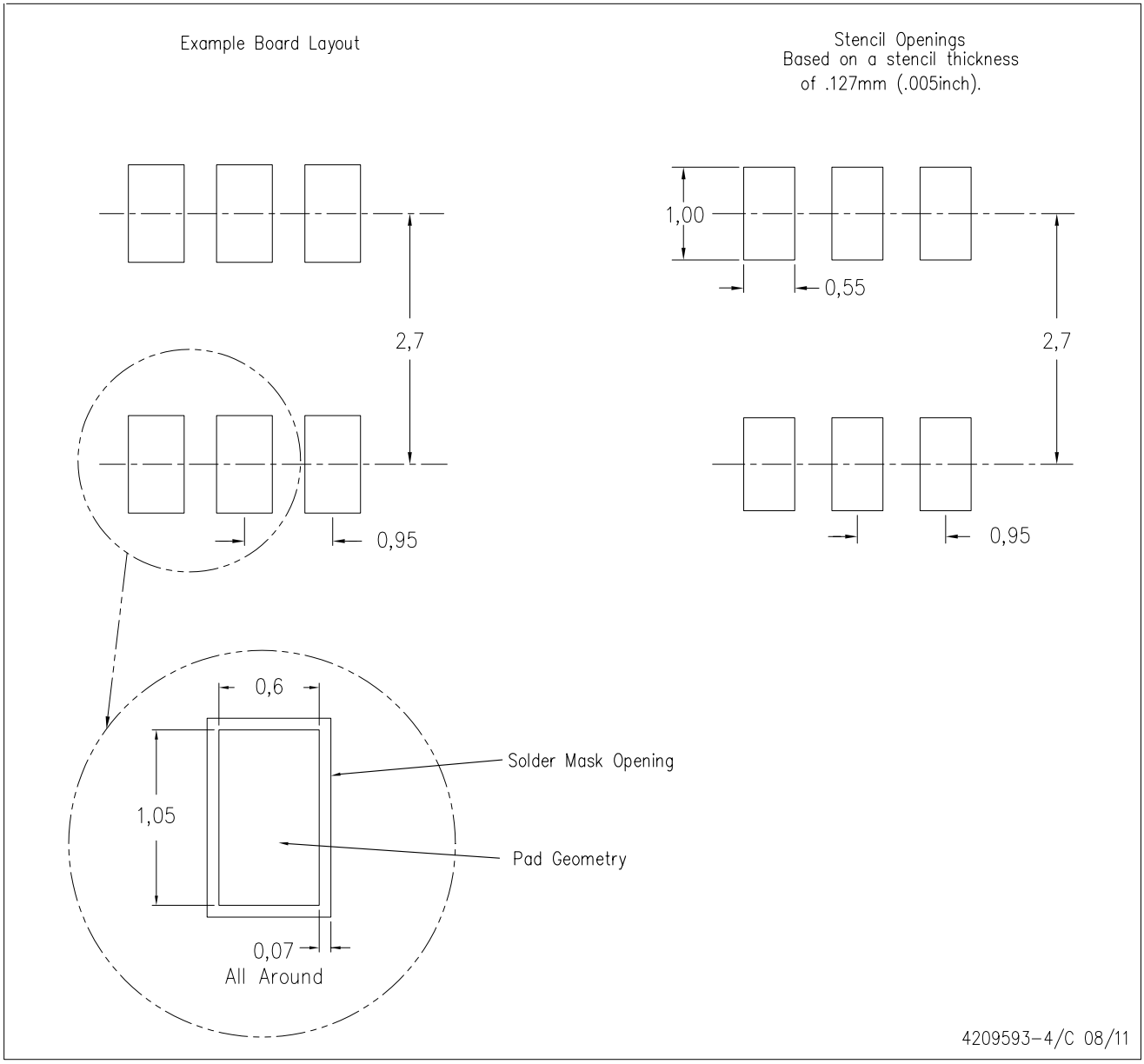
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27531DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC27531DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27531DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
UCC27531DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
UCC27531DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC27533DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27533DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27536DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27536DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27537DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27537DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27538DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27538DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



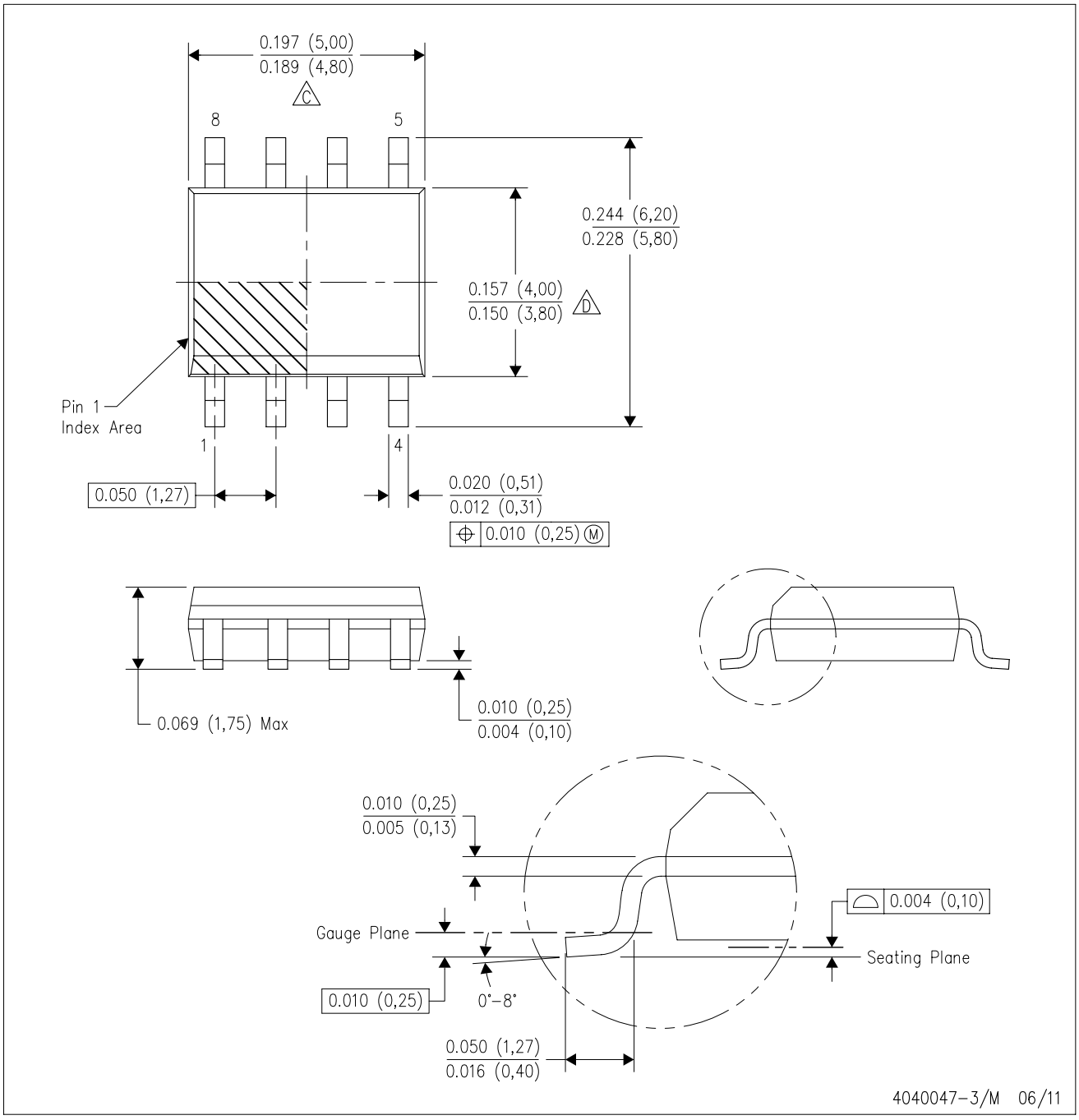
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



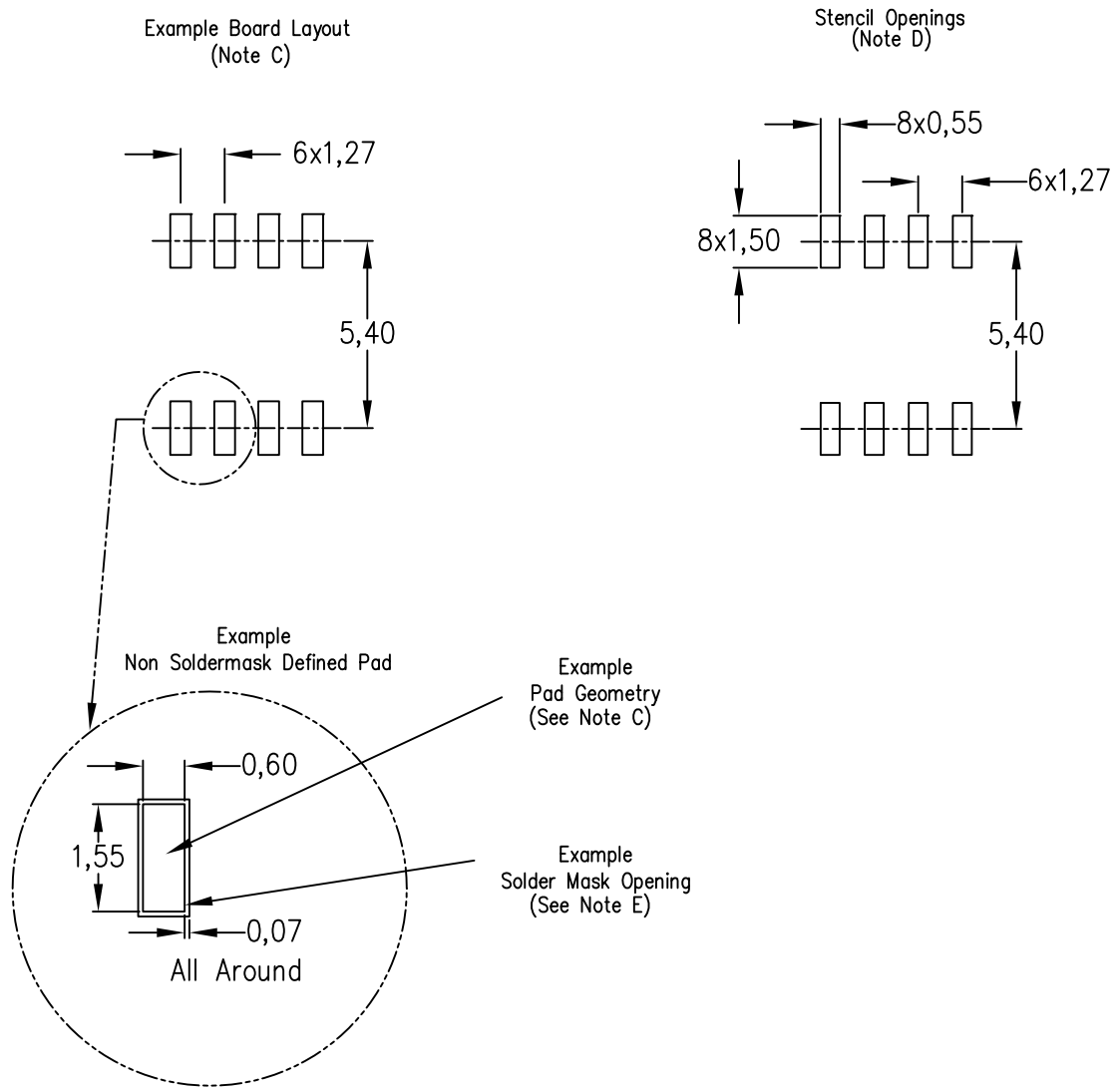
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



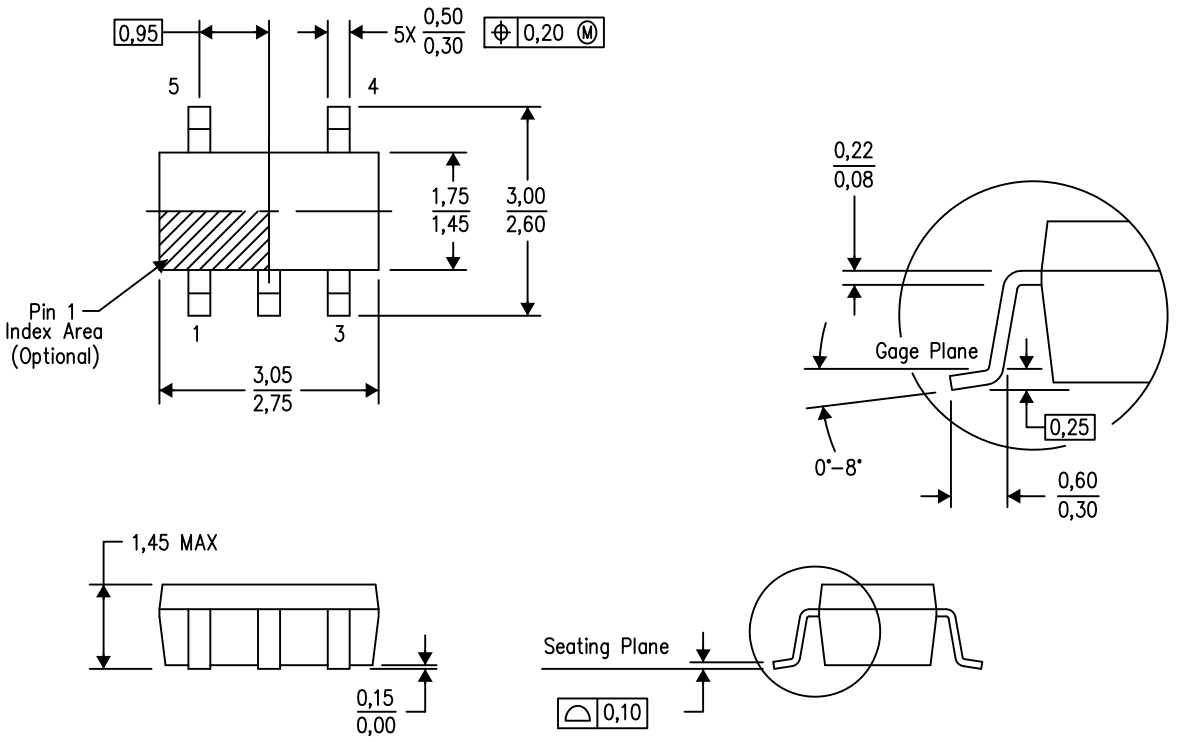
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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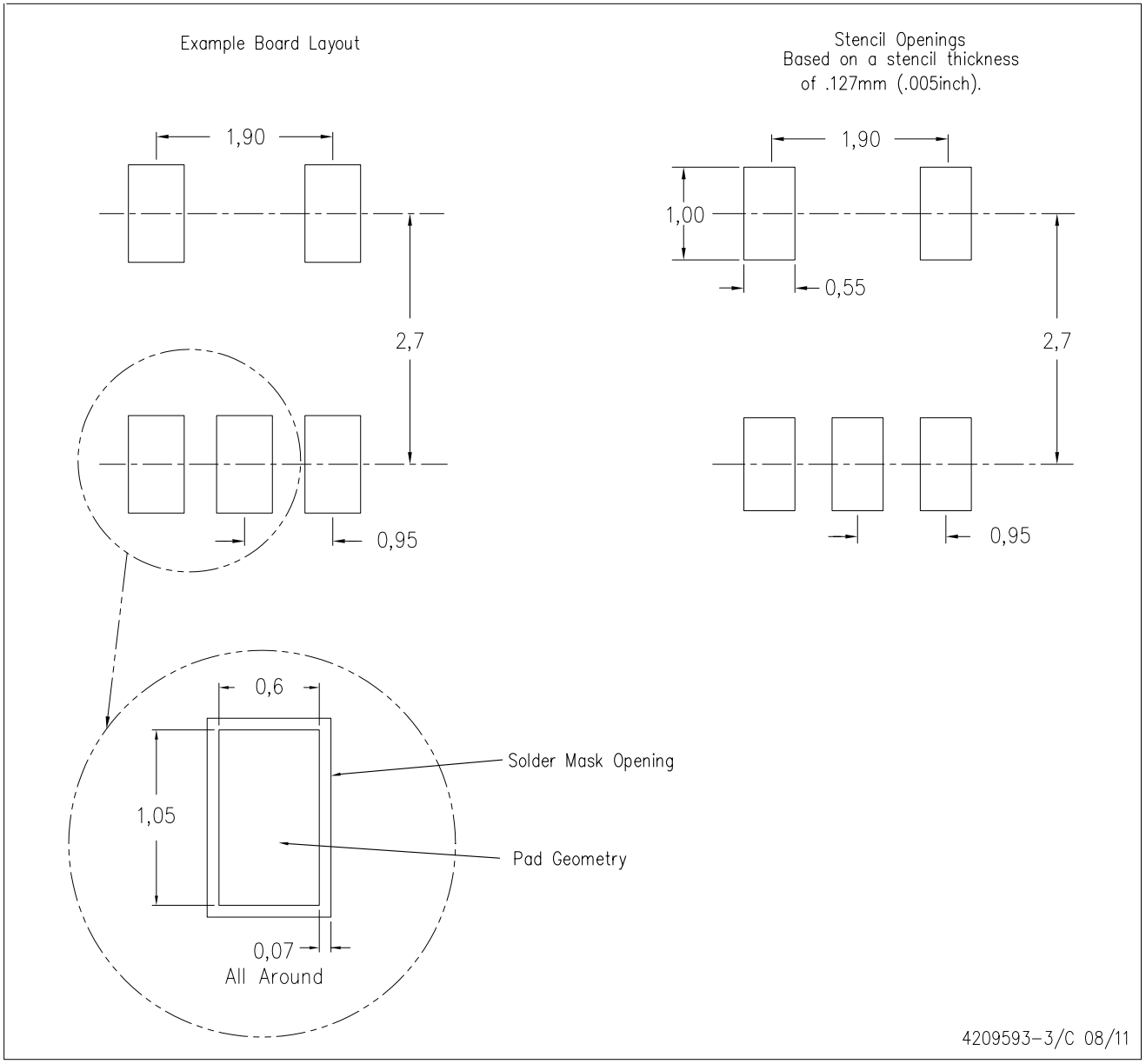
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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