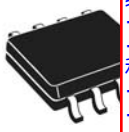
life.augmented

SRK2000A

Synchronous rectifier smart driver for LLC resonant converters

Datasheet - production data



SO-8

特征
·为LLC谐振变换器优化的次级侧同步整流控制器
·防止电流反转
·安全管理负载瞬态，轻负载和启动条件
·匹配关闭阈值
·轻负载智能自动睡眠模式
·具有1 A电源和3.5 A吸收驱动电流的N沟道MOSFET的双栅极驱动器
·工作电压范围4.5?32V
·具有迟滞的可编程UVLO
·250 µ A静态消耗
·工作频率高达500 kHz
·可用于SO-8封装

Features

- Secondary side synchronous rectifier controller optimized for LLC resonant converters
- Protection against current reversal
- Safe management of load transient, light load and startup condition
- Matched turn-off thresholds
- Intelligent automatic sleep mode at light load
- Dual gate driver for N-channel MOSFETs with 1 A source and 3.5 A sink drive current
- Operating voltage range 4.5 to 32 V
- Programmable UVLO with hysteresis
- 250 µA quiescent consumption
- Operating frequency up to 500 kHz
- Available in SO-8 package

Applications

- All-in-one PC
- High-power AC-DC adapters
- 80+/85+ compliant ATX SMPS
- 90+/92+ compliant server SMPS
- Industrial SMPS

应用
·一体机
·大功率AC-DC适配器
·80/85兼容ATX SMPS
·符合90/92标准的服务器SMPS
·工业SMPS

描述
SRK2000A智能驱动器在LLC谐振变换器中实现专用于二次侧同步整流的控制方案，该谐振变换器使用带中心抽头次级绕组的变压器进行全波整流。
它提供两个高电流栅极驱动输出，每个驱动一个或多个N沟道功率MOSFET。 每个栅极驱动器分别被控制，并且互锁逻辑电路防止两个同步整流MOSFET同时导通。
该IC中的控制方案允许每个同步整流器随着相应的半绕组开始导通而导通，并在其电流变为零时关断。 SRK2000A器件实现了匹配的关断MOSFET阈值。 该IC的独特功能是其智能自动睡眠模式。 它允许检测转换器的低功耗工作状态，并将IC置于低功耗睡眠模式，其中门驱动停止，静态消耗降低。 这样，在轻载时转换器的效率得到改善，同步整流不再有益。 IC自动退出睡眠模式，并重新开始切换，因为它识别出转换器的负载已经增加。
一个显着的特征是所需的非常低的外部元件数量。

prevents the two synchronous rectifier MOSFETs from conducting simultaneously.

The control scheme in this IC allows for each synchronous rectifier to be switched on as the corresponding half-winding starts conducting and switched off as its current goes to zero. The SRK2000A device implements matched turn-off MOSFET thresholds. A unique feature of this IC is its intelligent automatic sleep mode. It allows the detection of a low-power operating condition for the converter and puts the IC into a low consumption sleep mode where gate driving is stopped and quiescent consumption is reduced. In this way, converter efficiency improves at light load, where synchronous rectification is no longer beneficial. The IC automatically exits sleep mode and restarts switching as it recognizes that the load for the converter has increased.

A noticeable feature is the very low external component count required.

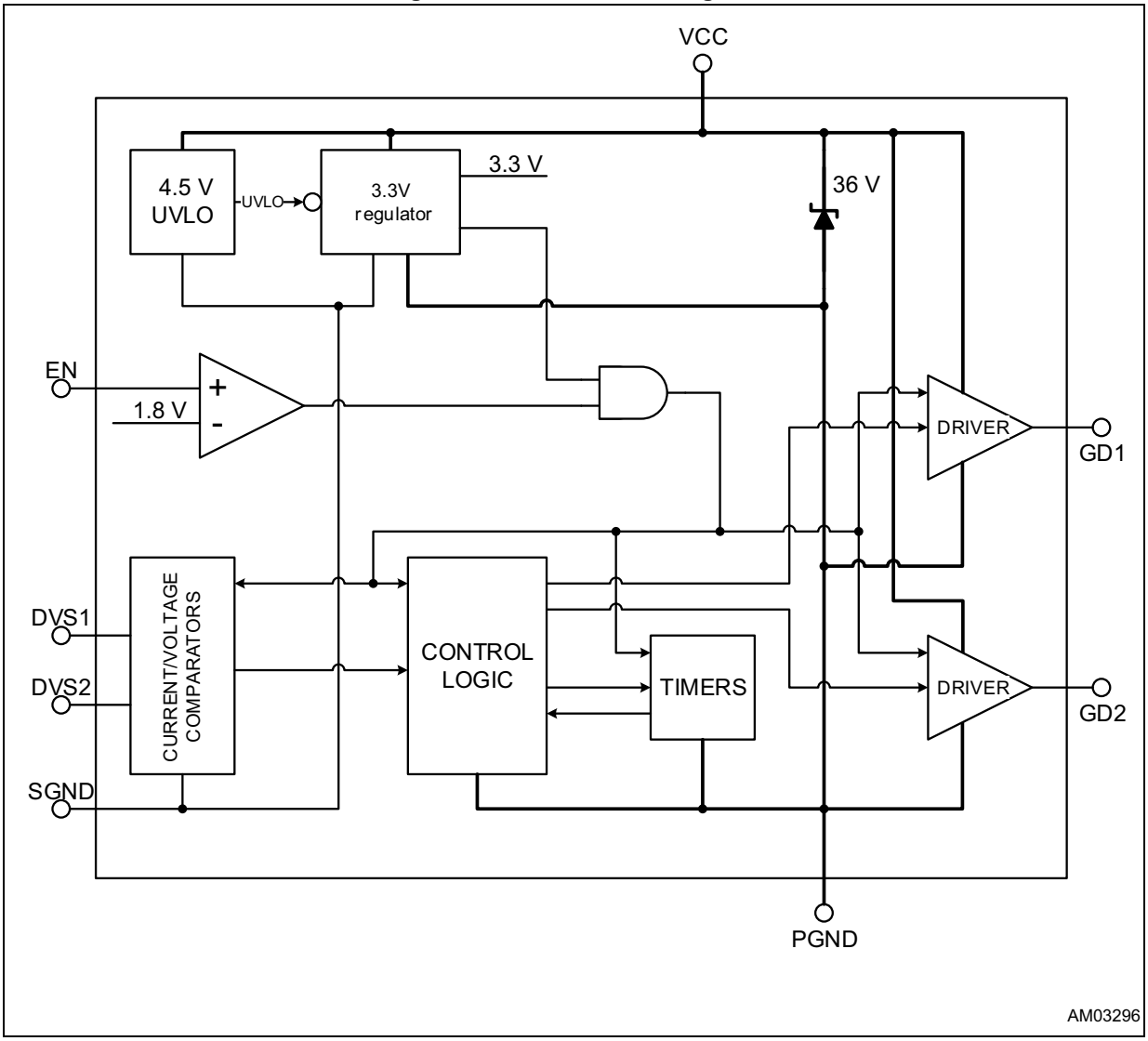
Table 1. Device summary

Order code	Package	Packing
SRK2000A	SO-8	Tube
SRK2000ATR		Tape and reel

Contents

1 Internal block diagram

Figure 1. Internal block diagram



2 Pin description

Figure 2. Pin configuration

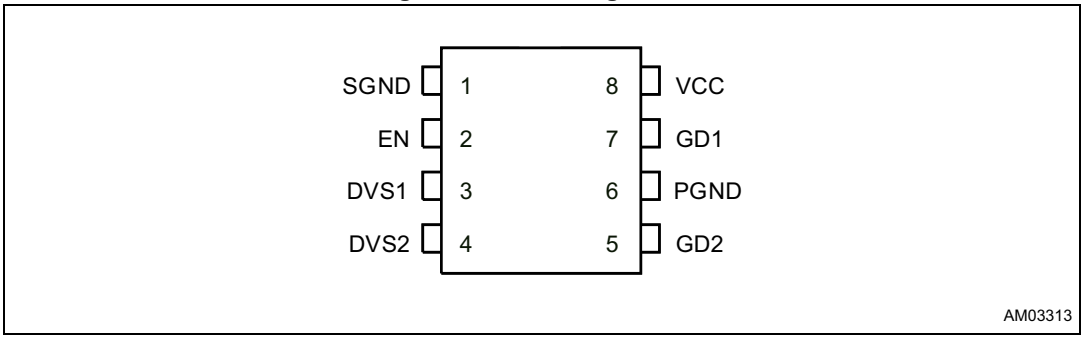
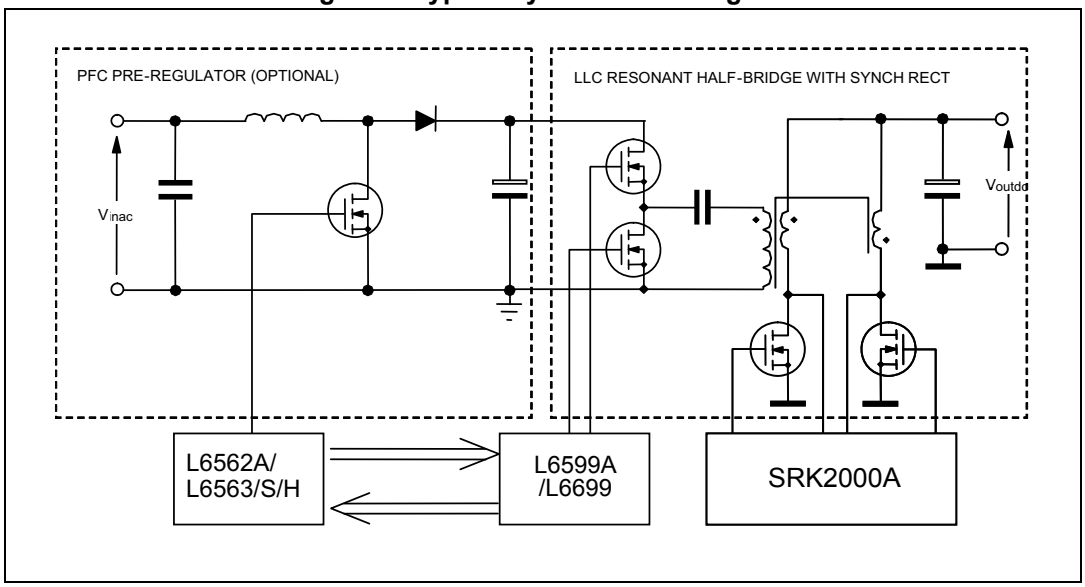


Table 2. Pin description

No.	Name	Function
1	SGND	信号地。 返回器件的偏置电流和两段的漏极 - 源极电压监视器的0 V参考电压。 将此引脚直接连接到PGND PGND.
2	EN	同步整流MOSFET关断的漏极电压阈值设定。 UVLO阈值编程。 该引脚通常由连接到VCC的上拉电阻或感测VCC的电阻分压器偏置。 将引脚拉到地可禁用栅极驱动器输出GD1和GD2，因此也可以用作使能输入。 to ground disables the gate driver outputs GD1 and GD2 and can therefore be used also as Enable input.
3 4	DVS1 DVS2	第1部分和第2部分的漏极电压检测。这些引脚将通过限流电阻连接到相应的同步整流器MOSFET的各个漏极端子。 当任一引脚上的电压为负时，对应的同步整流MOSFET导通; 由于其（负极）电压超过由EN引脚定义的阈值，所以MOSFET被关断。 内部逻辑拒绝开关噪声，但是建议在排水连接的正确布线时要特别注意。 (negative) voltage exceeds a threshold defined by the EN pin, the MOSFET is switched off. An internal logic rejects switching noise, however, extreme care in the proper routing of the drain connection is recommended.
5 7	GD2 GD1	每个图腾柱输出级可以驱动功率MOSFET，峰值电流为1A和3.5A电流。 这些引脚的高电平电压钳位在12 V左右，以避免在器件被提供高VCC时出现过大的栅极电压。 voltages in case the device is supplied with a high V_{CC}.
6	PGND	电源地。 返回门驱动电流。 将该引脚连接到两个同步整流MOSFET的源极端子连接的公共点。 connected.
8	V_{CC}	Supply voltage of the device. A small bypass capacitor (0.1 µF typ.) to SGND, located as close to the IC's pins as possible, may be useful to obtain a clean supply voltage for the internal control circuitry. A similar bypass capacitor to PGND, again located as close to the IC's pins as possible, may be an effective energy buffer for the pulsed gate drive currents.

设备的电源电压。 位于靠近IC引脚的SGND的小型旁路电容（0.1 µ F，典型值）可能对于内部控制电路获得干净的电源电压是有用的。 与PGND类似的旁路电容，再次位于尽可能靠近IC引脚的位置，可能是脉冲栅极驱动电流的有效能量缓冲器。

Figure 3. Typical system block diagram



3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	DC supply voltage 直流电源电压	-0.3 to V_{CCZ}	V
I_{CCZ}	8	Internal Zener maximum current 内部齐纳最大电流	25	mA
---	2, 3, 4	Analog inputs voltage rating模拟输入电压额定值	-0.3 to V_{CCZ}	V
$I_{DVS1,2\_sk}$	3, 4	Analog inputs max. sink current (single pin) 模拟输入最大吸电流（单针）	2	mA
$I_{DVS1,2\_sr}$	3, 4	Analog inputs max. source current (single pin)	-5	mA

模拟输入最大 源电流（单引脚）

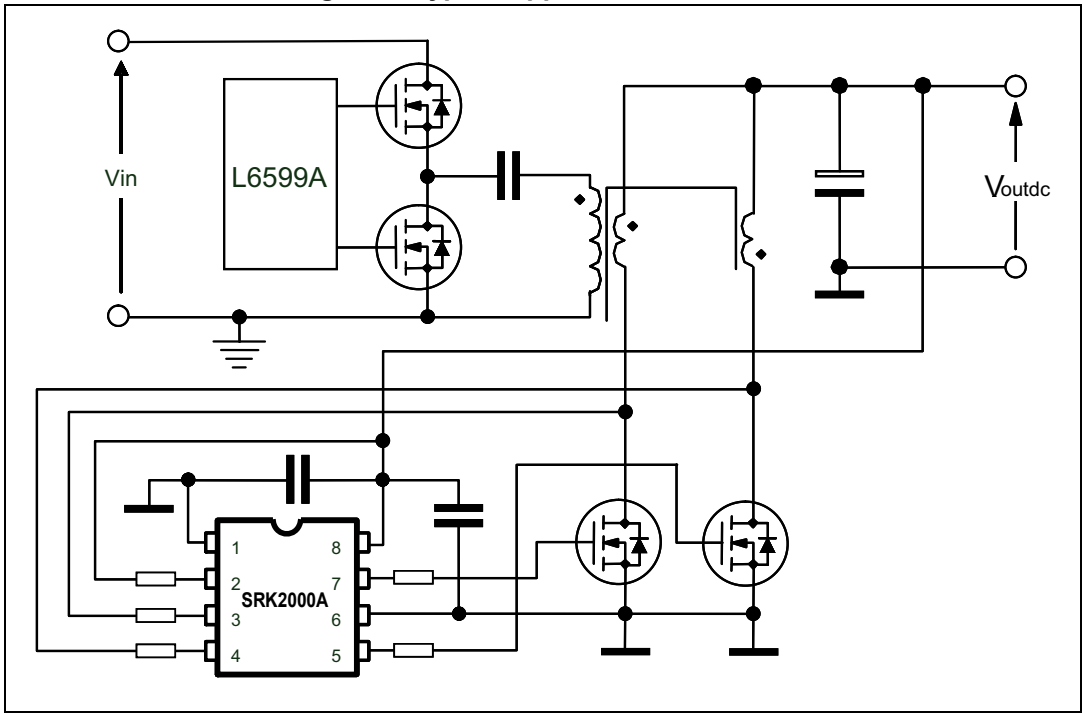
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction to ambient	150	°C/W
Ptot	Power dissipation at T_A = 50 °C	0.65	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

4 Typical application schematic

典型应用原理图

Figure 4. Typical application schematic



5 Electrical characteristics

T_J = -25 to 125 °C, V_{CC} = 12 V, C_{GD1} = C_{GD2} = 4.7 nF, EN = V_{CC}; unless otherwise specified; typical values refer to T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	4.5	-	32	V
V_{CCOn}	Turn-on threshold	See(1)	4.25	4.5	4.75	V
V_{CCOff}	Turn-off threshold	See(1)	4	4.25	4.5	V
Hys	Hysteresis	-	-	0.25	-	V
V_{CCZ}	Zener voltage齐纳电压	I_{CCZ} = 20 mA	33	36	39	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, V_{CC} = 4 V	-	45	70	µA
Iq	Quiescent current	After turn-on	-	250	500	µA
I_{CC}	Operating supply current	At 300 kHz	-	35	-	mA
Iq	Quiescent current	EN = SGND	-	150	250	µA
Drain sensing inputs and synch functions						
$V_{DVS1,2\_H}$	Upper clamp voltage	$I_{DVS1,2}$ = 20 mA	-	V_{CCZ}	-	V
$I_{DVS1,2\_b}$	Input bias current	$V_{DVS1,2}$ = 0 to V_{CC}(2)	-1		1	µA
$V_{DVS1,2\_A}$	Arming voltage (positive-going edge)	-	-	1.4	-	V
$V_{DVS1,2\_PT}$	Pre-triggering voltage (negative-going edge)	-	-	0.7	-	V
$V_{DVS1,2\_TH}$	Turn-on threshold	-	-250	-200	-180	mV
$I_{DVS1,2\_On}$	Turn-on source current	$V_{DVS1,2}$ = -250 mV	-	-50	-	µA
$V_{DVS1,2\_Off}$	Turn-off threshold (positive-going edge)	R = 680 kΩ from EN to V_{CC}	-18	-25	-32	mV
		R = 270 kΩ from EN to V_{CC}	-9	-12.5	-16	
$V_{DVS1,2\_Off\_match}$	Matching between the two turn-off thresholds	-	-	1	-	mV
T_{PD_On}	Turn-on debounce delay	After sourcing $I_{DS1,2\_On}$	-	250	-	ns
T_{PD_Off}	Turn-off propagation delay	After crossing $V_{DS1,2\_Off}$	-	-	60	ns
T_{ON_min}	Minimum on-time	-	-	150	-	ns
D_{OFF}	Min. operating duty-cycle	- 最小工作周期	-	40	-	%
D_{ON}	Restart duty-cycle	- 重启占空比	-	60	-	%

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Gate drive enable function						
V_{EN_On}	Enable threshold	Positive-going edge(1)	1.7	1.8	1.9	V
Hyst	Hysteresis	Below V_{EN_On}	-	45	-	mV
I_{EN}	Bias current	$V_{EN} = V_{EN\_On}$	-	-	1	µA
Turn-off threshold selection						
V_{EN-Th}	Selection threshold	$V_{CC} = V_{CCOn}$	0.32	0.36	0.40	V
I_{EN}	Pull-down current	$V_{EN} = V_{EN\_Th}$, $V_{CC} = V_{CCOn}$	7	10	13	µA
Gate drivers						
V_{GDH}	Output high voltage	$I_{GDsource}$ = 5 mA	11.75	11.9	-	V
		$I_{GDsource}$ = 5 mA, V_{CC} = 5 V	4.75	4.9	-	
V_{GDL}	Output low voltage	I_{GDsink} = 200 mA	-	0.2	-	V
		I_{GDsink} = 200 mA, V_{CC} = 5 V	-	0.2	-	
$I_{sourcepk}$	Output source peak current	-	-	-1	-	A
I_{sinkpk}	Output sink peak current	-	-	3.5	-	A
t_f	Fall time	-	-	18	-	ns
t_r	Rise time	-	-	40	-	ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; V_{CC} = 20 V	12	13	15	V
V_{GDL_UVLO}	UVLO saturation	V_{CC} = 0 to V_{CCon} Isink = 5 mA	-	1	1.3	V

1. Parameters tracking each other.
2. For V_{CC} > 30 V $I_{DVS1,2\_b}$ may be greater than 1 µA because of the possible current contribution of the internal clamp Zener (few tens of µA).

6 Application information

EN 引脚引脚功能和用途
该引脚可以执行三种不同的功能：它为同步整流器（SR）功率MOSFET的漏极到源极电压设置阈值VDVS1,2_Off，以确定其在每个导通周期中的关断; 它允许用户对栅极驱动器的UVLO阈值进行编程，并可用作启用（远程开/关控制）

6.1 EN pin - pin function and usage

This pin can perform three different functions: it sets the threshold $V_{DVS1,2\_Off}$ for the drain-to-source voltage of either synchronous rectifier (SR) Power MOSFET to determine their turn-off in each conduction cycle; it allows the user to program the UVLO thresholds of the gate drivers and can be used as Enable (remote on/off control).

6.1.1 Pull-up resistor configuration 上拉电阻配置

启动时，只要器件电源电压VCC低于启动阈值VCCOn，内部10 µ A电流吸收器（IEN）就会被激活。 当VCC等于VCCOn（4.5 V典型值）时，EN引脚上的电压VEN决定了两个同步整流器在逐周期运行时的漏极电压的关断阈值VDVS1,2_Off：如果VEN <VEN_Th = 0.36 V），阈值设置为-25 mV，否则为-12 mV。 一旦做出决定，只要VCC大于关断电平VCCOff（4.25 V，典型值），设置就会被冻结，一个简单的上拉电阻R1到VCC可以用于设置VDVS1,2_Off关断 阈。 器件打开时EN引脚上的电压由下式给出

the setting is frozen as long as V_{CC} is greater than the turn-off level V_{CCOff} (4.25 V typ.).

A simple pull-up resistor R_1 to V_{CC} can be used to set $V_{DVS1,2\_Off}$ turn-off threshold. The voltage on the EN pin as the device turns on is given by:

Equation 1

$$V_{EN} = V_{CCOn} - I_{EN} R1$$

Then, considering worst-case scenarios, we have:
那么，考虑到最坏的情况，我们有：

Equation 2

$$R1 > 633\ k\Omega \rightarrow V_{DVS1,2\_Off} = -25\ mV$$

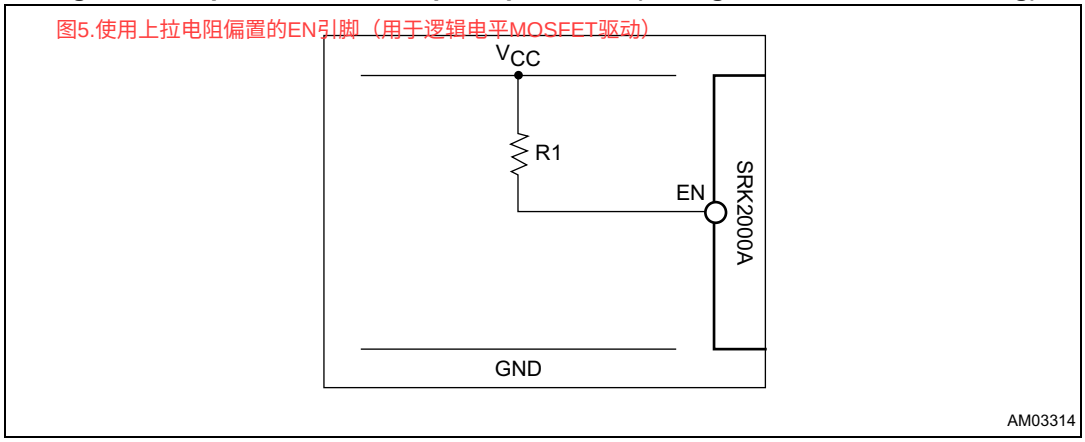
$$R1 < 296\ k\Omega \rightarrow V_{DVS1,2\_Off} = -12\ mV$$

需要考虑一些额外的余量（等于电阻容差） 假设5%容差，在第一种情况下使用标准值R1 = 680 kR，在第二种情况下使用R1 = 270 kR

Some additional margin (equal to the resistor's tolerance) needs to be considered; assuming 5% tolerance, the use of the standard values R_1 = 680 kΩ in the first case and R_1 = 270 kΩ in the second case, is suggested.

Figure 5. EN pin biased with a pull-up resistor (for logic level MOSFET driving)

图5.使用上拉电阻偏置的EN引脚（用于逻辑电平MOSFET驱动）



当VCC超过VCCOn时，内部电流吸收器IEN被关闭，使能功能被激活。 然后将引脚上的电压与设置为1.8 V的内部参考VEN_On进行比较：如果超过该阈值，则启用栅极驱动器GD1和GD2，并且操作SR MOSFET; 否则，器件处于空闲状态，而SR MOSFET处于关断状态。
使用上拉电阻RP，EN引脚上的电压随着IEN关断而上升，趋于VCC，因此超过VEN_On并使两个SR MOSFET工作。 从本质上讲，这导致了门极驱动使得VCC超过VCCOn，并且当VCC下降到VCCOn以下时，禁止它。 因此，当SR MOSFET为逻辑电平类型时，建议使用此配置。

Using the pull-up resistor R_P, the voltage on the EN pin rises as I_{EN} is switched off and tends to V_{CC}, therefore exceeding V_{EN_On} and enabling the operation of both SR MOSFETs. Essentially, this results in enabling the gate-driving as V_{CC} exceeds V_{CCOn} and disabling it as V_{CC} falls below V_{CCOn}. This configuration is thereby recommended when SR MOSFETs are logic level types.

6.1.2 Resistor divider configuration

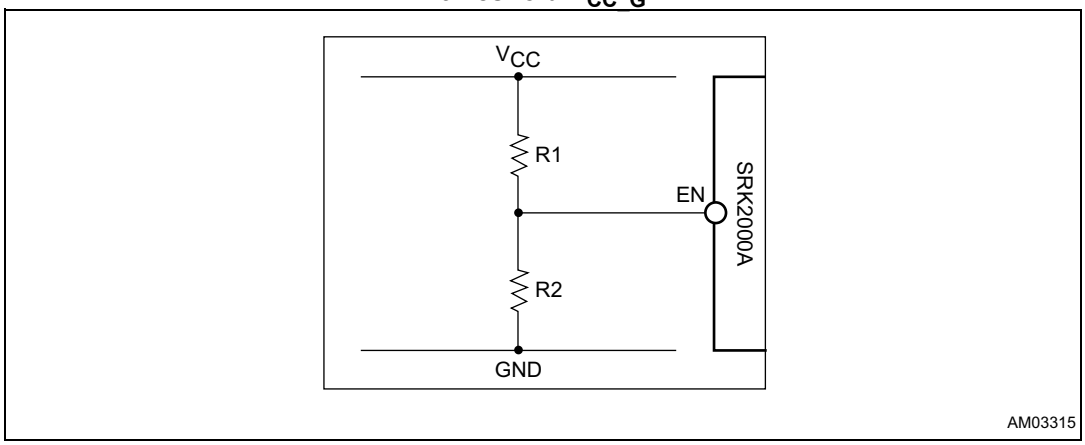
电阻分压器配置
为了使VCC电压高于预定值VCC_G的栅极驱动，为了适当地驱动标准SR MOSFET，EN引脚被选择为超过的值的电阻分压器（R1上电阻R2下电阻）偏置 VCC = VCC_G时VEN_On，并设置所需的VDVS1,2_Off电平。 注意，随着VCC下降，由于比较器的45 mV滞后，栅极驱动在VCC电平约为VCC_G低约2.5%时被禁止。
描述两个关键条件VCC = VCCOn（当VDVS1,2_Off电平决定时）和VCC = VCC_G（当门驱动被使能时）的电路分别为：

disabled at a V_{CC} level about 2.5% lower than V_{CC_G}, because of the 45 mV hysteresis of the comparator.

The equations that describe the circuit in the two crucial conditions $V_{CC} = V_{CCOn}$ (when the decision of the $V_{DVS1,2\_Off}$ level is made) and $V_{CC} = V_{CC\_G}$ (when gate-driving is to be enabled) are respectively:

EN引脚用电阻分压器偏置来编程栅极驱动器UVLO阈值VCC_G

Figure 6. EN pin biased with a resistor divider to program the gate drive UVLO threshold V_{CC_G}



Equation 3

$$\begin{cases} \dfrac{V_{CCOn} - V_{EN}}{R1} = I_{EN} + \dfrac{V_{EN}}{R2} \\ V_{CC\_G}\dfrac{R2}{R1+R2} = V_{EN\_On} \end{cases}$$

Solving these equations for R_1 and R_2 we get:

为R1和R2求解这些方程

Equation 4

$$\begin{cases} R1 = \dfrac{V_{CCOn} - V_{EN}\dfrac{V_{CC\_G}}{V_{EN\_On}}}{I_{EN}} \\ R2 = R1\dfrac{V_{EN\_On}}{V_{CC\_G} - V_{EN\_On}} \end{cases}$$

If [illegible] at
o
T d
is concerned: in fact, the large spread of I_{EN} considerably affects the voltage on the EN pin as the device turns on, a value that can be found by solving the first of (1) for V_{EN}:

VCC_G不是太低（<8÷9 V），它的容差并不重要，因为它只与VEN_On（±5.6%）和外部电阻R1，R2（推荐为±1%）相关。 然后，只要选择-12 / -25 mV阈值就需要注意：事实上，IEN的大幅扩展在器件导通时大大影响EN引脚上的电压，值 可以通过解决VEN中的（1）中的第一个来找到

Equation 5

$$V_{EN} = \frac{V_{CCOn} - I_{EN}R1}{1 + \dfrac{R1}{R2}}$$

A couple of examples clarify the suggested calculation methodology.

几个例子说明了建议的计算方法。

Example 1 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 25 mV.

I
I g
t
s e

在这种情况下，VEN肯定要低于VEN_Th（= 0.32 V）的最小值。 从（2）的第二个，R1到R2的标称比例为（10 - 1.8）/ 1.8 = 4.555。 在（3）中代入适当的极值，必须是（4.75 - 7·10-6·R1）/（1 + 4.555）<0.32; R1的求解产生R1>425kR; 让我们考虑额外的4%的余量来考虑R1和R2值的容限和粒度，因此：R1> 425·1.04 = 442k?。 选择R1 = 442kR（E48标准值），从（2）的第二个，R2 = 442 / 4.555 = 97kR; 使用97.6k?（E48标准值）。

tolerance and the granularity of the R1 and R2 values into account, so that:
R1 > 425·1.04 = 442 kΩ. Choose R1 = 442 kΩ (E48 standard value) and, from the second of (2), R2 = 442/4.555 = 97 kΩ; use 97.6 kΩ (E48 standard value).

Example 2 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 12 mV.

In this case, V_{EN} must definitely be higher than the maximum value of V_{EN_Th} (= 0.40 V).
I g
t
s
C
I

在这种情况下，VEN肯定要高于VEN_Th（= 0.40 V）的最大值。 从（2）的第二个，R1到R2的标称比例为（10 - 1.8）/ 1.8 = 4.555。 在（3）中代入适当的极值必须是（4.25 - 13·10-6·R1）/（1 + 4.555）> 0.4; R1的求解产生R1 <156kR; 其中4%的附加额度为R1 <156 / 1.04 = 150 kR。 选择R1 = 147 kR（E48标准值），从（2）的第二个，
R2 = 147 / 4.555 = 32.3kR; 使用32.4 kR（E48标准值）。
? 在这两个例子中，由于VCC低于9.75 V（标称值），所以门驱动器被禁止，因为EN引脚上的电压低于VEN_On 45 mV。

Note: In both examples the gate drivers are disabled as V_{CC} falls below 9.75 V (nominal value), as the voltage on the EN pin falls 45 mV below V_{EN_On}.

6.1.3 Remote on/off control 远程开/关控制

W [illegible]
d in
and force the gate drivers into an off state.

无论使用哪种配置，由于EN引脚上的电压低于VEN_On的45 mV电压会禁用栅极驱动器，因此可以使用任何小信号晶体管来下拉EN引脚并强制栅极驱动器处于关断状态

Finally, it should be noted that during power-up, power-down, and under overload or short-circuit conditions, the gate drivers are shut down if the V_{CC} voltage is insufficient: < V_{CCOff} in

最后，应该注意的是，在上电，掉电和过载或短路条件下，如果VCC电压不足，则栅极驱动器关闭：在上拉电阻器配置的情况下，VCCOff < 0.975·VCC_G在电阻分压器配置的情况下（系数0.975取决于使能引脚阈值的滞后）

configuration (the coefficient 0.975 depends on the hysteresis on the Enable pin threshold).

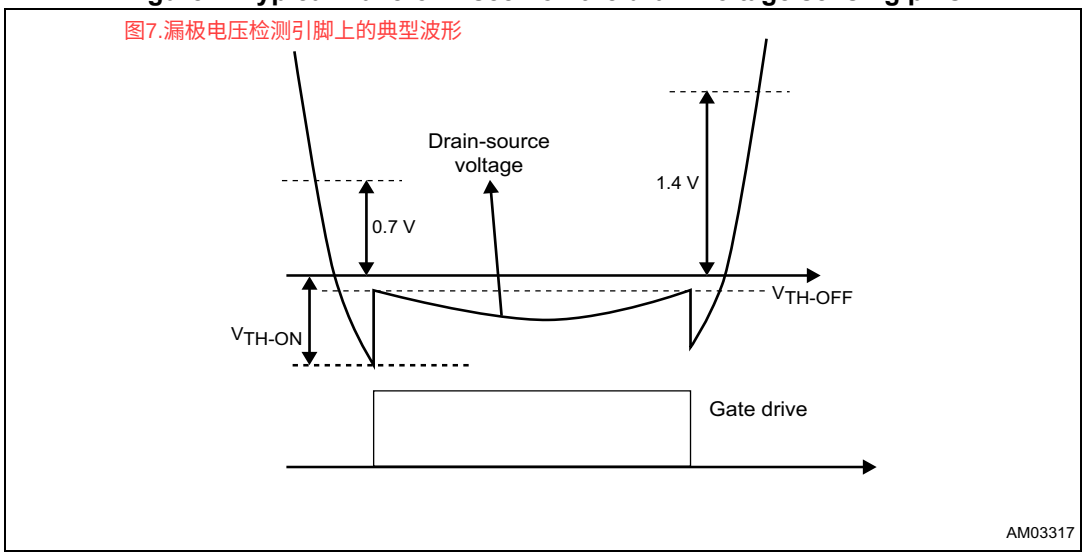
6.2 Drain voltage sensing 漏极电压检测

在以下说明中，假设读者熟悉LLC谐振半桥拓扑及其波形，特别是二次侧采用中心抽头变压器绕组进行全波整流的波形。
为了了解在SR MOSFET（或其体二极管或与MOSFET并联的二极管）中流动的电流的极性和电平，IC提供了两个引脚DVS1-2，能够感测MOSFET的电压电平水渠。

To understand the polarity and the level of the current flowing in the SR MOSFETs (or their body diodes, or diodes in parallel to the MOSFETs) the IC is provided with two pins, DVS1-2, able to sense the voltage level of the MOSFET drains.

Figure 7. Typical waveform seen on the drain voltage sensing pins

图7.漏极电压检测引脚上的典型波形



控制两个SR MOSFET的驱动的逻辑是基于两个门驱动状态机以并联方式并联工作，以避免两个门驱动器同时接通。

on at the same time.

有四个重要的漏极电压阈值：第一个，VDVS1,2_A（= 1.4 V），对正向沿敏感，臂对着栅极驱动器（互锁功能）；第二，对负向边缘敏感的VDVS1,2_PT（= 0.7V）提供了栅极驱动器的预触发; 第三个是当SR MOSFET的体二极管开始导通时触发栅极驱动器的（负）阈值VTH-ON; 第四个是内部（负）阈值VDVS1,2_Off ? 其中SR MOSFET关闭（通过适当偏置EN引脚，可在-12 mV或-25 mV之间选择）。
匹配VDVS1_Off和VDVS2_Off阈值，以便在两个SR MOSFET中具有相同的电流关断电平。

threshold $V_{DVS1,2\_Off}$ where the SR MOSFET is switched off (selectable between -12 mV or -25 mV by properly biasing the EN pin).

The V_{DVS1_Off} and V_{DVS2_Off} thresholds are matched in order to have the same current turn-off level in both SR MOSFETs.

The value of the ON threshold V_{TH-ON} is affected by the external resistor in series to each

导通阈值VTH-ON的值受到每个DVS1-2引脚串联的外部电阻的影响，基本上要限制当一个SR MOSFET关断而另一个SR MOSFET导通时可能注入到引脚的电流。事实上，一方面，当一个MOSFET关断（另一个导通）时，其漏极 - 源极电压略高于输出电压的两倍;如果超过内部钳位电压（VCCZ = 36 V，典型值），串联电阻RD必须将注入电流限制在低于最大额定值（25 mA）的适当值，并考虑相关的功耗。另一方面，当电流开始流入一个MOSFET（或与MOSFET并联的二极管）的体二极管时，漏极 - 源极电压为负（?-0.7V）;当引脚DVS1,2上的电压达到阈值VDVS1,2_TH（-0.2 V，典型值）时，内部电流源IDVS1,2_On被激活;当该电流超过50 µ A时，MOSFET的栅极导通。因此，实际触发阈值可以由等式6确定

appropriate value, lower than the maximum rating (25 mA) and taking the related power

dissipation into account. On the other hand, when current starts flowing into the body diode of one MOSFET (or in the diode in parallel with the MOSFET), the drain-to-source voltage is negative (≅ -0.7 V); when the voltage on pins DVS1,2 reaches the threshold $V_{DVS1,2\_TH}$ (-0.2 V typ.), an internal current source $I_{DVS1,2\_On}$ is activated; as this current exceeds 50 µA, the gate of the MOSFET is turned on. Therefore, the actual triggering threshold can be determined by *Equation 6*.

Equation 6

$$V_{TH-ON} = R_D \cdot I_{DVS1,2On} + V_{DVS1,2\_TH}$$

例如，对于RD = 2kR，触发阈值位于

For instance, with R_D = 2 kΩ, the triggering threshold is located at - (2 kΩ · 50 µA) - 0.2 V = -0.3 V.

为了避免栅极驱动器的错误触发，在采样IDS1,2_On之后使用去抖动延迟TPD_On（= 250 ns）（即，在栅极驱动器接通之前，引脚的电流必须超过50 µ A超过250 ns）。这个延迟对于转换器的效率来说并不重要，因为初始电流接近零或者甚至远低于峰值。
一旦SR MOSFET被接通，其漏极 - 源极电压就下降到流过电流的时间（MOSFET）RDS（on）的值。再次，由于初始电流低，RDS（导通）两端的电压降可能超过关断阈值VDVS1,2_Off
，并确定不正当的关闭。为了防止这种情况，状态机基于上一个周期的持续时间的信息，使得仅在导通周期的后半部分中关闭的比较器参考VDVS1,2_Off。在导通周期的前半部分，只有一个参考零的附加比较器才有效，以防止SR MOSFET的电流反向，这将损害LLC转换器的工作。
一旦阈值VDVS1,2_Off超过（在导通周期的后半段）并且GATE被关断，电流再次流过体二极管，导致漏极 - 源极电压具有负跳变，再次低于VTH-ON。然而，互锁逻辑防止了假启动。值得指出的是，由于每个MOSFET在体二极管开始导通之后导通，因此漏极 - 源极电压等于体二极管正向压降时导通ON;因此在MOSFET导通时既不存在米勒效应也不具有开关损耗。关断时也不存在开关损耗，实际上电流总是从源极流向漏极，当MOSFET关断时，它将流过体二极管（或者外部二极管平行于MOSFET）。
与导通时不同，关断速度对于避免次级侧的电流反向至关重要，特别是当转换器工作在谐振频率以上时，流过MOSFET的电流呈现非常陡峭的边缘同时减小到零：关断传播TPD_Off
?延迟的最大值为60 ns。
互锁逻辑，除了检查一致的二次电压波形（一个MOSFET只能在另一个具有正的漏极 - 源极电压> VDVS1,2_A）导通，以防止同时导通，每个周期只允许一次开关：在一个门驱动器关闭之后，在另一个驱动器有自己的开/关循环之前，不能重新打开。
IC逻辑还防止两个SR MOSFET中的不平衡电流：如果一个SR MOSFET在一个周期内不能导通，则另一个SR MOSFET在下一个周期中也不会导通。

MOSFET is turned on after its body diode starts conducting, the ON transition happens with the drain-source voltage equal to the body diode forward drop; therefore there is neither a Miller effect nor switching losses at MOSFET turn-on. Also at turn-off the switching losses are not present, in fact, the current is always flowing from source to drain and, when the MOSFET is switched off, it goes on flowing through the body diode (or the external diode in parallel to the MOSFET).

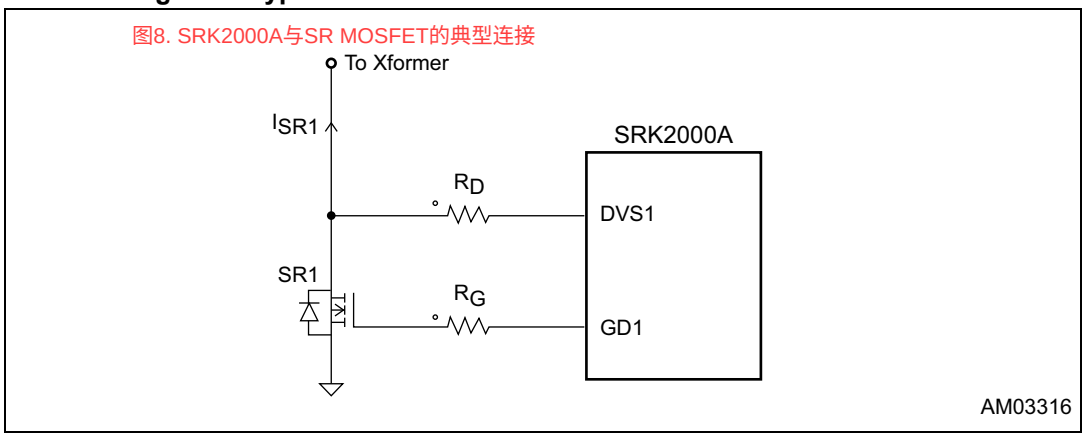
Unlike at turn-on, the turn-off speed is critical to avoid current reversal on the secondary side, especially when the converter operates above the resonance frequency, where the current flowing through the MOSFET exhibits a very steep edge while decreasing down to zero: the turn-off propagation T_{PD_Off} delay has a maximum value of 60 ns.

The interlock logic, in addition to checking for consistent secondary voltage waveforms (one MOSFET can be turned on only if the other one has a positive drain-to-source voltage > $V_{DVS1,2\_A}$) to prevent simultaneous conduction, allows only one switching per cycle: after one gate driver has been turned off, it cannot be turned on again before the other gate drive has had its own on/off cycle.

The IC logic also prevents unbalanced current in the two SR MOSFETs: if one SR MOSFET fails to turn on in one cycle, the other SR MOSFET is also not turned on in the next cycle.

Figure 8. Typical connection of the SRK2000A to the SR MOSFET

图8. SRK2000A与SR MOSFET的典型连接



6.3 Gate driving

该IC具有两个高电流栅极驱动输出（1A源和3.5A接收器），每个能够驱动一个或多个N沟道功率MOSFET。 由于可编程栅极驱动器UVLO，可以驱动标准MOSFET和逻辑电平MOSFET。
驱动器提供的高电平电压被钳位在VGDclamp（= 12 V），以避免在器件被提供高电压VCC时栅极上的过高的电压电平。
两个栅极驱动器具有下拉功能，可确保即使在低VCC时也不会使MOSFET MOSFET发生伪负载：事实上，驱动器在VCC低于导通阈值时具有1 V（典型值）的UVLO饱和电平

The high-level voltage provided by the driver is clamped at $V_{GDclamp}$ (= 12 V) to avoid excessive voltage levels on the gate in case the device is supplied with a high V_{CC}.

The two gate drivers have a pull-down capability that ensures the SR MOSFETs cannot be spuriously turned on even at low V_{CC}: in fact, the drivers have a 1 V (typ.) UVLO saturation level at V_{CC} below the turn-on threshold.

6.4 Intelligent automatic sleep mode 智能自动睡眠模式

该IC的独特功能是其智能自动睡眠模式。逻辑电路能够检测转换器的轻负载条件和停止门驱动，也降低了IC的静态消耗。这提高了轻负载下的转换器效率，其中整流体二极管（或与MOSFET并联的外部二极管）的功率损耗低于MOSFET中的功率损耗以及与驱动相关的功率损耗。
IC还能够检测到转换器负载的增加并自动重启
门开车。
智能自动睡眠模式使用的算法是基于双时间测量系统。 SR MOSFET的开关周期（即谐振变换器开关周期的一半）的持续时间是使用下降到VDVS1.2_PT以下的漏极 - 源极电压的负向边缘的组合来测量的，超越VDVS1,2_A; SR MOSFET导通的持续时间是从其体二极管开始导通（漏极到源极电压低于VTH-ON）的瞬间到栅极驱动器关闭的时刻（器件工作时）或瞬间体二极管停止导通（漏极 - 源极电压超过VTH-ON）。在满载时，SR MOSFET导通时间几乎占开关周期的100%，负载减小时，导通时间减少，并且随着SR MOSFET开关周期降低到40%以下（DOFF），器件进入睡眠模式。为了防止错误的决定，必须在谐振转换器的16个连续开关周期的两个部分中的至少一个上确认睡眠模式条件

A unique feature of this IC is its intelligent automatic sleep mode. The logic circuitry is able t IC's c er l go r half

of the resonant converter switching period) is measured using a combination of the negative-going edge of the drain-to-source voltage falling below $V_{DVS1,2\_PT}$ and the positive-going edge exceeding $V_{DVS1,2\_A}$; the duration of the SR MOSFET conduction is measured from the moment its body diode starts conducting (drain-to-source voltage falling below V_{TH-ON}) to the moment the gate drive is turned off (in case the device is operating) or the moment the body diode ceases to conduct (drain-to-source voltage going over V_{TH-ON}). While at full load the SR MOSFET conduction time occupies almost 100% of the switching cycle, as the load is reduced, the conduction time is reduced and as it falls below 40% (D_{OFF}) of the SR MOSFET switching cycle the device enters sleep mode. To prevent

erroneous decisions, the sleep mode condition must be confirmed on at least one of the two sections for 16 consecutive switching cycles of the resonant converter.

Once in sleep mode, SR MOSFET gate driving is re-enabled when the conduction time of

一旦处于睡眠模式，当体二极管（或与MOSFET并联的外部二极管）的导通时间超过开关周期的60%（DON）时，SR MOSFET栅极驱动被重新使能。 同样在这种情况下，考虑在8个连续的开关周期（即中心抽头的每个SR MOSFET的8个连续周期）中进行测量。 此外，在每个睡眠模式进入/退出转换之后，在一定数量的周期内忽略定时，以使输出电流中产生的瞬态衰减。 忽略谐振转换器切换周期数进入休眠模式后为128，退出休眠模式后为256。 如果在忽略的周期结束时，进入或退出休眠模式的条件已经满足所需的周期数，状态将立即更改; 否则控制器（忽略周期之后）将等到该条件满足

a certain number of cycles, to let the resulting transient in the output current fade out. The number of ignored resonant converter switching cycles is 128 after entering the sleep mode and 256 after exiting the sleep mode. If by the end of the ignored cycles the condition to enter or exit the sleep mode is already met for the required number of cycles, the state will be changed immediately; otherwise the controller (after the ignored cycles) will wait until that condition is satisfied.

6.5 Protection against current reversal 防止电流逆转

该IC提供了针对SR MOSFET电流反向的保护。 如果在两个连续的开关周期中检测到电流反转条件，则IC进入睡眠模式，避免SR MOSFET的导通，直至恢复安全状态。

avoiding the turn-on of the SR MOSFETs until a safe condition is restored.

6.6 Layout guidelines 布局指南

The IC is designed with two grounds, SGND and PGND.

IC设计有两个地面SGND和PGND。
SGND用作所有内部高精度模拟模块的接地参考，而PGND是所有噪声数字模块的接地参考以及栅极驱动器的当前返回值。此外，它也是ESD保护电路的基础。 SGND通过两个反并联二极管由ESD事件与PGND保护。
布线PCB时，请确保两个SR MOSFET的源极端子彼此尽可能靠近，并将与PGND分开的走线与负载电流返回路径分开。该跟踪应尽可能短，尽可能靠近物理源终端。尽可能几何对称的布局有助于电路尽可能以最对称的方式运行。 SGND应使用尽可能短的路径（在设备主体下）直接连接到PGND。
漏极电压检测应尽可能物理地靠近漏极端子进行，漏极 - 源极电压检测电路中的负载电流所跨越的任何杂散电感可能会显着改变电流读数，关闭SR MOSFET。值得一提的是，特别是在高功率应用或更高的工作频率下，即使内部引线接合的杂散电感也可能是有害的。在这种情况下，需要谨慎选择SR MOSFET封装。
建议在VCC与SGND和PGND之间使用旁路电容。它们应该是低ESR，低ESL类型，并且尽可能靠近IC引脚。有时，转换器的输出电压和VCC引脚之间的串联电阻（几十）与旁路电容一起形成RC滤波器，以便获得更清洁的VCC电压。

possible helps the circuit to operate in the most electrically symmetrical way as possible. SGND should be directly connected to PGND using a path as short as possible (under the device body).

Also drain voltage sensing should be performed as physically close to the drain terminals as possible: any stray inductance crossed by the load current that is in the drain-to-source voltage sensing circuit may significantly alter the current reading, leading to a premature turn-off of the SR MOSFET. It is worth mentioning that, especially in higher power applications or at higher operating frequencies, even the stray inductance of the internal wire bonding can be detrimental. In this case, a cautious selection of the SR MOSFET package is required.

The use of bypass capacitors between V_{CC} and both SGND and PGND is recommended. They should be low-ESR, low-ESL types and located as close to the IC pins as possible. Sometimes a series resistor (in the tens) between the converter's output voltage and the V_{CC} pin, forming an RC filter along with the bypass capacitor, is useful in order to get a cleaner V_{CC} voltage.

7 Package information 包装信息

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

为了满足环保要求，ST根据其环保要求水平，为不同等级的ECOPACK?包装提供这些设备。 ECOPACK规格，等级定义和产品状态可从以下网址获取：www.st.com。 ECOPACK是ST商标。

7.1 SO-8 package information

Figure 9. SO-8 package outline

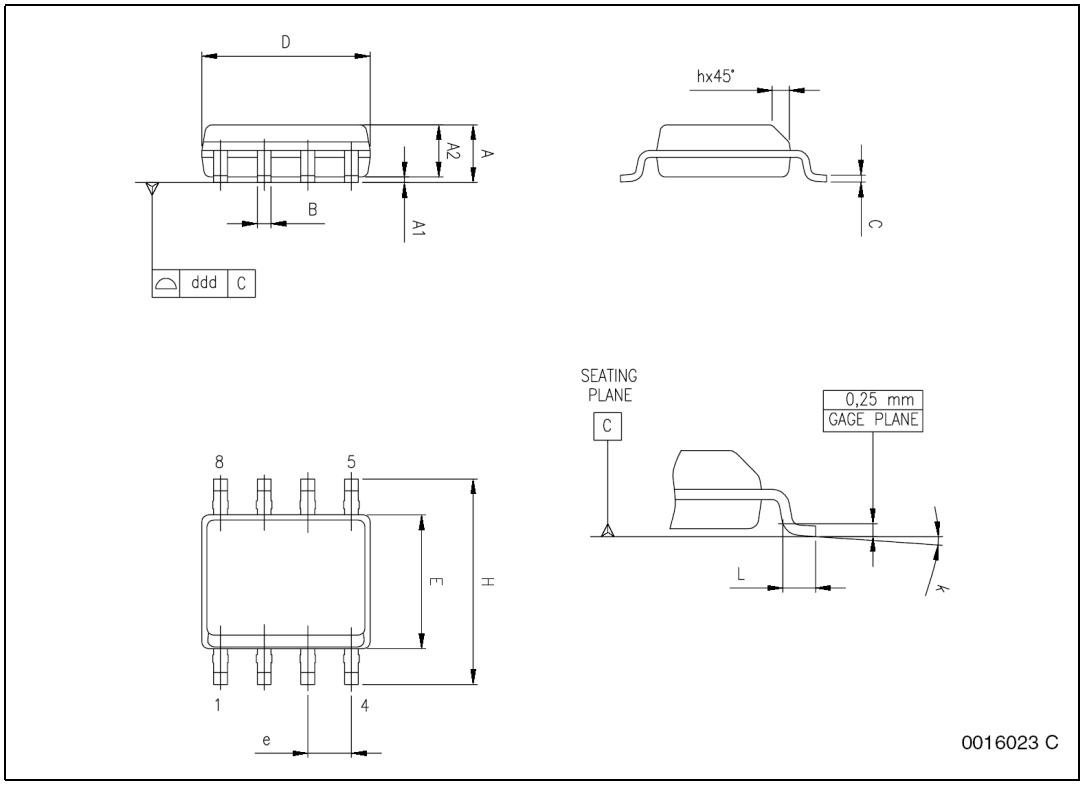


Table 6. SO-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.10	-	1.65	0.043	-	0.065
B	0.33	-	0.51	0.013	-	0.020
C	0.19	-	0.25	0.007	-	0.010
D (1)	4.80	-	5.00	0.189	-	0.197
E	3.80	-	4.00	0.15	-	0.157
e	-	1.27	-	-	0.050	-
H	5.80	-	6.20	0.228	-	0.244
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
k	0° (min.), 8° (max.)					
ddd	-	-	0.10	-	-	0.004

1. D dimensions do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs should not exceed 0.15 mm (0.006 inch) in total (both sides).

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
18-Oct-2013	1	Initial release.
13-Dec-2013	2	Updated *Table 1 on page 1* (removed “D” from order codes). Minor modifications throughout document.
04-May-2017	3	Updated text in *Section 6.4 on page 14*. Minor modifications throughout document.