High voltage CoolMOS™ P7 in SOT-223 package

SOT-223 as DPAK replacement

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About this document

Scope and purpose

Nowadays, the package cost of high voltage (HV) and high-ohmic MOSFETs is the dominant part of the overall product price, therefore it is necessary to find alternative packaging solutions that meet the same requirements and provide the same benefits. This application note (AN) will provide an explanation of how to use an HV CoolMOS™ in a SOT-223 package.

In 2016, Infineon introduced the first HV MOSFET portfolio in a SOT-223 package without a middle pin, with the CoolMOS™ CE portfolio. Today an extended portfolio is being released, offering the benefits of Infineon's latest superjunction (SJ) technology, the CoolMOS™ P7 series, in combination with the benefits of the SOT-223 package. This cost-effective package offers direct pin-to-pin compatibility to DPAK without suffering any large thermal limitations when using the DPAK footprint for SOT-223. It features the smallest geometry per $R_{DS(on)}$ (drain source on-state resistance) and reduces the overall bill of materials (BOM) cost of an application as much as possible. The biggest challenge when using a surface-mount device (SMD) package is the thermal behavior. Therefore this document compares the CoolMOS™ P7 against previous technologies in DPAK and the SOT-223 package with respect to package dimensions, footprint, efficiency and most importantly, the thermal behavior.

Intended audience

This application note is written to give an application engineer or SMPS designer the ability to overcome thermal boundaries related to SOT-223 package through simulations and real application measurements based on CoolMOS™ P7 and previous CoolMOS™ technologies.

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1 SOT-223 versus DPAK package outlines

A SOT-223 package can be a direct pin-to-pin replacement for a DPAK package with the outer dimensions and lead spacing shown in Figure 1.

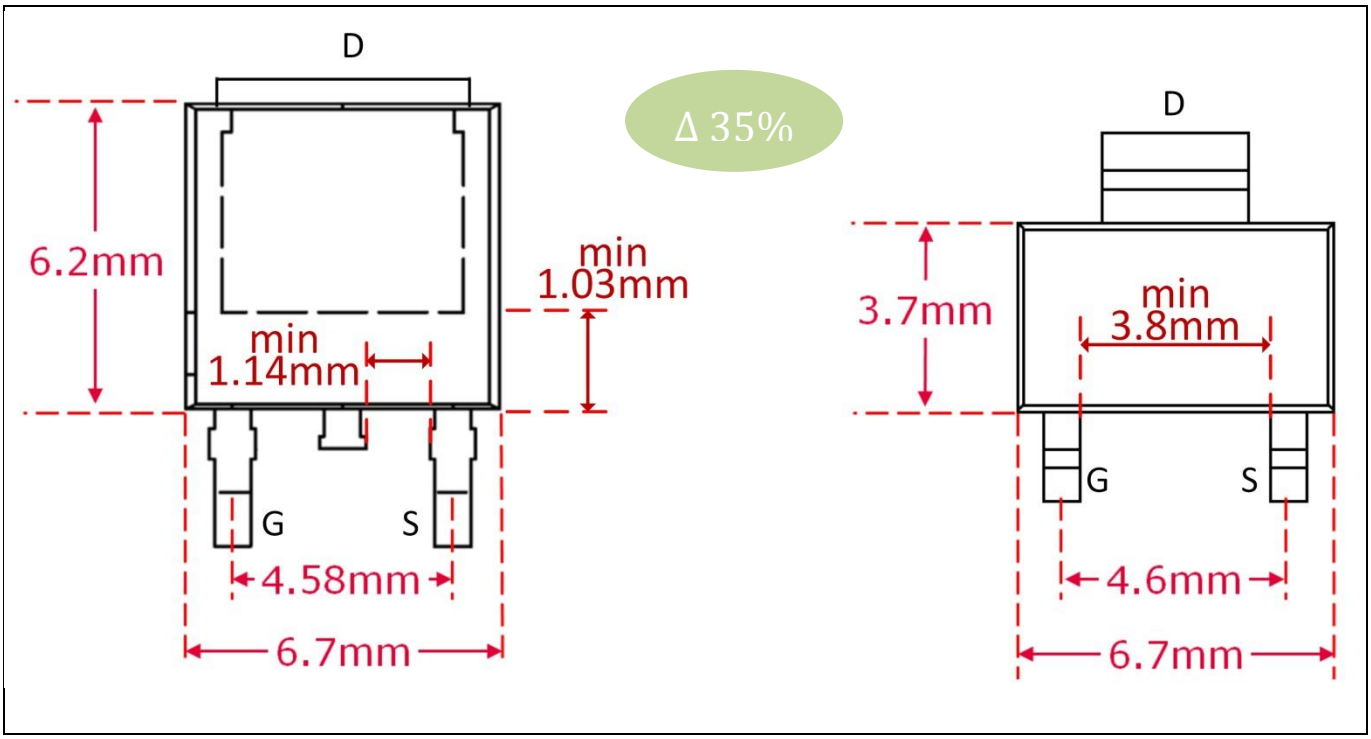


Figure 1 Package comparison: SOT-223 (48.9 mm² PCB area) and DPAK (74.7 mm² PCB area)

It can be seen that the middle pin of a standard SOT-223 is removed, which allows HV MOSFETs in the SOT-223 package and increases the creepage between the gate and source pins when compared to a DPAK. This version of SOT-223 is even safer with respect to soldering processes (reflow or especially wave soldering), as there is a lower possibility of having solder residue between the leads. Additionally, optical inspection after the soldering process benefits from greater visibility than with DPAK.

As already anticipated in the scope and purpose section of this document, the greatest challenge with SOT-223 is the thermal behavior. This application note will discuss the general structure and thermal resistance (R_{th}) during steady-state conditions in the next section.

2 Thermal behavior in steady-state

A SOT-223 package does not offer an exposed leadframe like a DPAK does. Therefore, the overall $R_{th,JC}$ (thermal resistance from the junction to the back of the leadframe) is not a useful parameter and a SOT-223 package instead uses an $R_{th,JS}$ (thermal resistance from the junction to the solder point), which is typically higher than the $R_{th,JC}$ from a DPAK (see Figure 2).

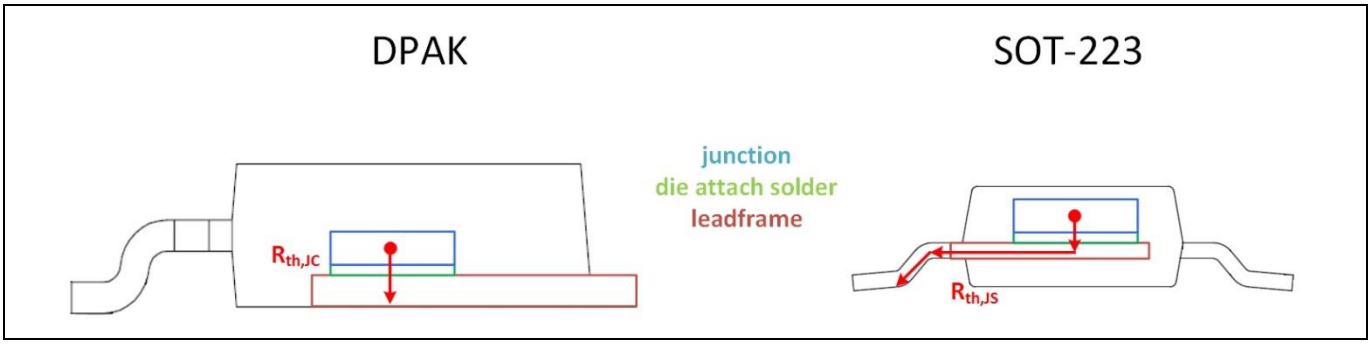


Figure 2 Simplified $R_{th,JC}$ (DPAK) versus $R_{th,JS}$ (SOT-223)

This leads to the conclusion that a SOT-223 package can only be used as a plug-and-play replacement, if the overall power losses (switching losses and conduction losses) of the MOSFET are not too high. The allowable power dissipation will be influenced by the ambient temperature, PCB temperature and PCB copper area. With a minimal copper footprint a typical power limit for the SOT-223 would be 250 mW, as shown in the graph below. If the power losses exceed this value, an additional copper area (connected to the drain pin, D) needs to be included on the PCB. Figure 3, below, shows the thermal dependency of the DPAK and SOT-223 packages on the copper area around the drain connection.

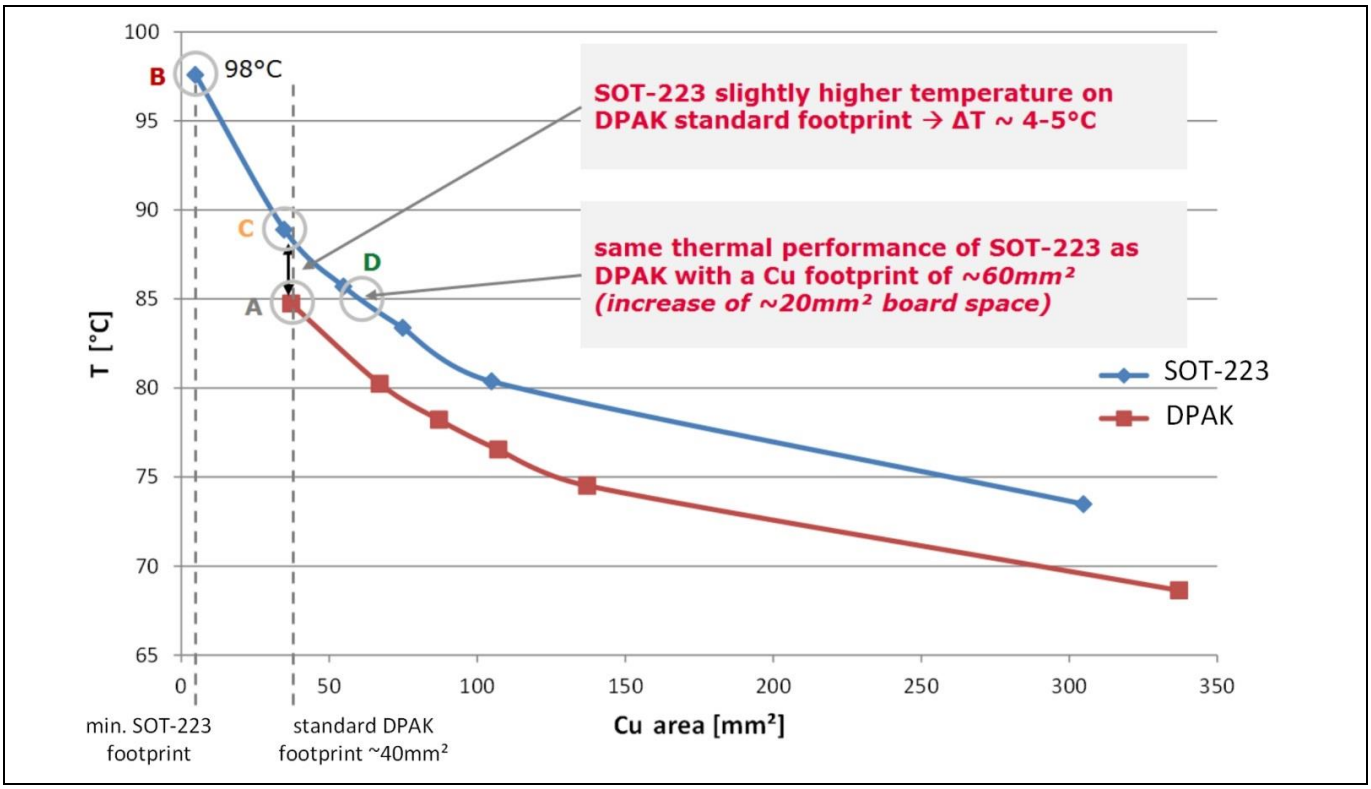


Figure 3 Thermal simulation of junction temperature at 250 mW and ambient temperature of 70°C

This thermal behavior can be demonstrated by using a constant current measurement set-up in which the DPAK device is mounted on a minimum footprint (~40 mm^2) and the SOT-223 is placed on various copper area

Thermal behavior in steady-state

PCB footprints with up to 800 mW losses within the MOSFET. The test PCBs are single layer with 35 µm copper thickness, FR4 material and 1.5 mm thick.

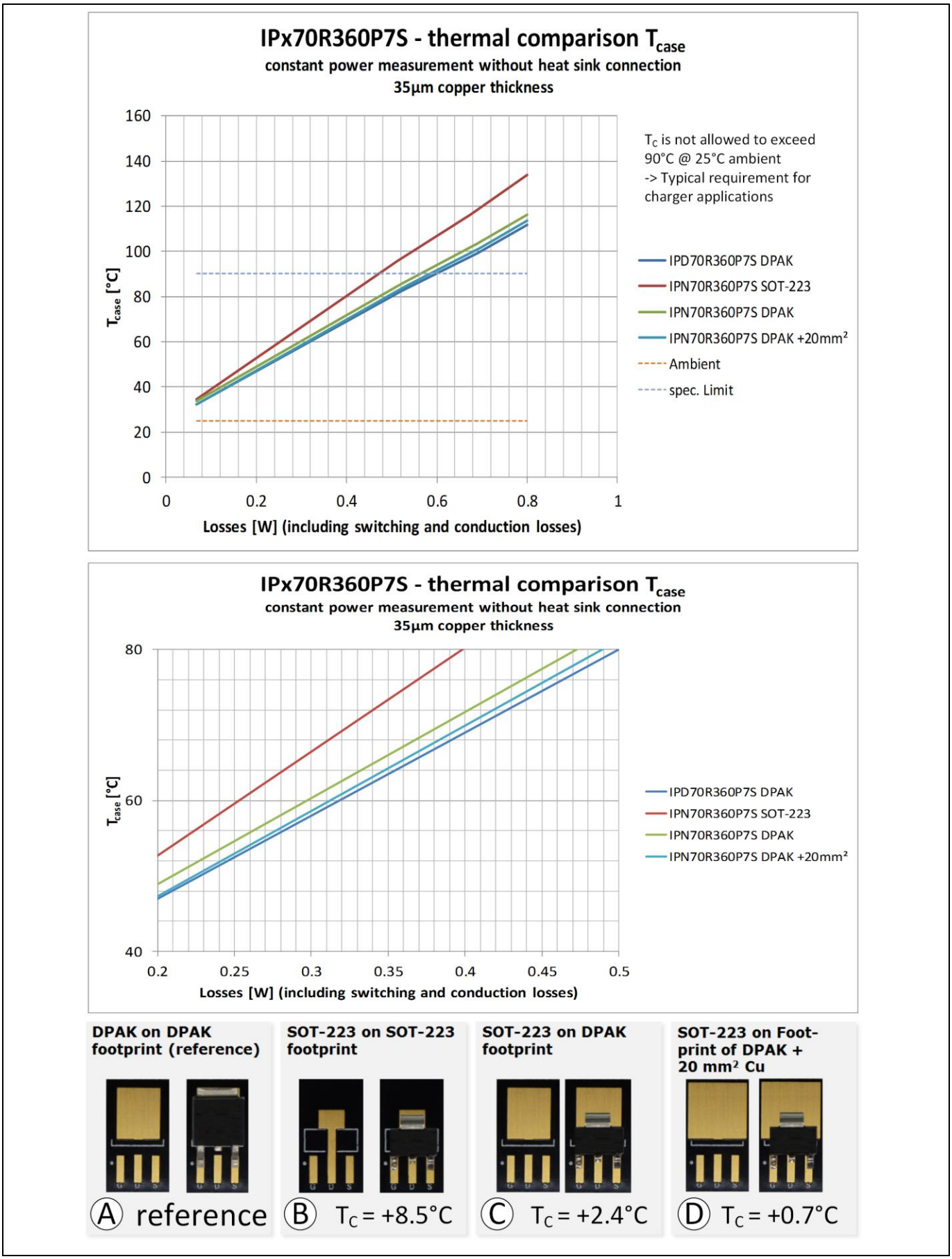


Figure 4 Thermal measurement with different adapter PCBs for SOT-223

Thermal behavior in steady-state

A	DPAK on DPAK footprint:	This adapter board uses the minimum DPAK footprint with a DPAK package in order to have a reference measurement. The thermal image was acquired by a thermal camera after thermal saturation with a thermal gradient (ΔT_C) < 0.1 °C/min.
B	SOT-223 on SOT-223 footprint: ~10 mm² copper area	The use of a SOT-223 package on the minimum SOT-223 footprint adds an additional 10°C to the mold compound temperature when compared to the DPAK, which makes this set-up suitable for very low power levels – making possible board space savings. Nevertheless, as a direct DPAK replacement it can only be implemented if the design has enough thermal margin.
C	SOT-223 on DPAK footprint: ~40 mm² copper area	With this set-up it is possible to use a SOT-223 package as a direct drop-in replacement for DPAK by accepting a ~5°C higher mold compound temperature. However, the DPAK design should have some thermal margin before reaching specification limits.
D	SOT-223 on DPAK + 20 mm² Cu: ~60 mm² copper area	The Infineon recommended usage is represented by this configuration. With an additional copper area on the drain lead of around 20 mm² in comparison to the DPAK minimum footprint, it is possible to achieve nearly the same thermal performance as with a DPAK.

It is clear that when using a SOT-223 package on the minimum footprint as a replacement for DPAK, a very high thermal margin would be needed, and this is not typically available in customer designs. The best chance of achieving a similar performance to the DPAK is by increasing the copper area. This is especially true in lighting applications, and this is discussed in the next section of this AN, where we will cover some thermal measurements in real customer designs with open and closed frames.

3 Thermal behavior in end customer designs

By reviewing end customer designs, especially in the lighting segment, it becomes clear that there is a general availability of additional copper, in the range of >150 mm^2, as can be seen below, in section 3.2. This would allow for a plug-and-play replacement by accepting a 2°C higher case temperature. All the results shown were gathered after 30 minutes of burn-in time in order to heat up the whole application.

Attention: ***For a reliable and correct comparison between different packages, even with the same internal technology, it is necessary to have characterized and matched devices with respect to the chip inside the package.***

3.1 18 W mobile charger

3.1.1 Set-up description

To demonstrate the interchangeability of DPAK and the new SOT-223, a customer phone charger board already on the market was taken to carry out some measurements.

The objective was to first make a plug-and-play comparison with the original 700 V CoolMOS™ CE in the SOT-223 package, by comparing this with a 700 V CoolMOS™ P7 device. Then a comparison was made between a 650 V CoolMOS™ C6 device in the DPAK and the 700 V CoolMOS™ P7 in the SOT-223 to show how changing an old technology in the DPAK for a new technology in the SOT-223 would affect the system performance.

The table below shows the specifications of the 18 W phone charger tested:

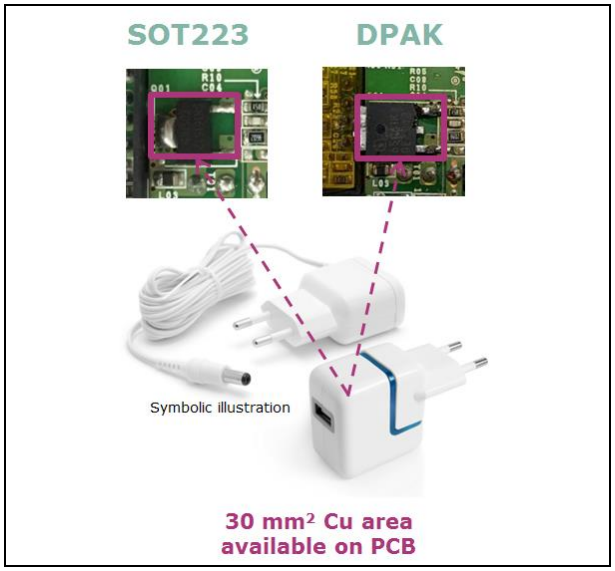


Figure 5 **18 W charger – both SOT-223 and DPAK package were compared with a 30 mm^2 copper area**

Table 1 **18 W phone charger details**

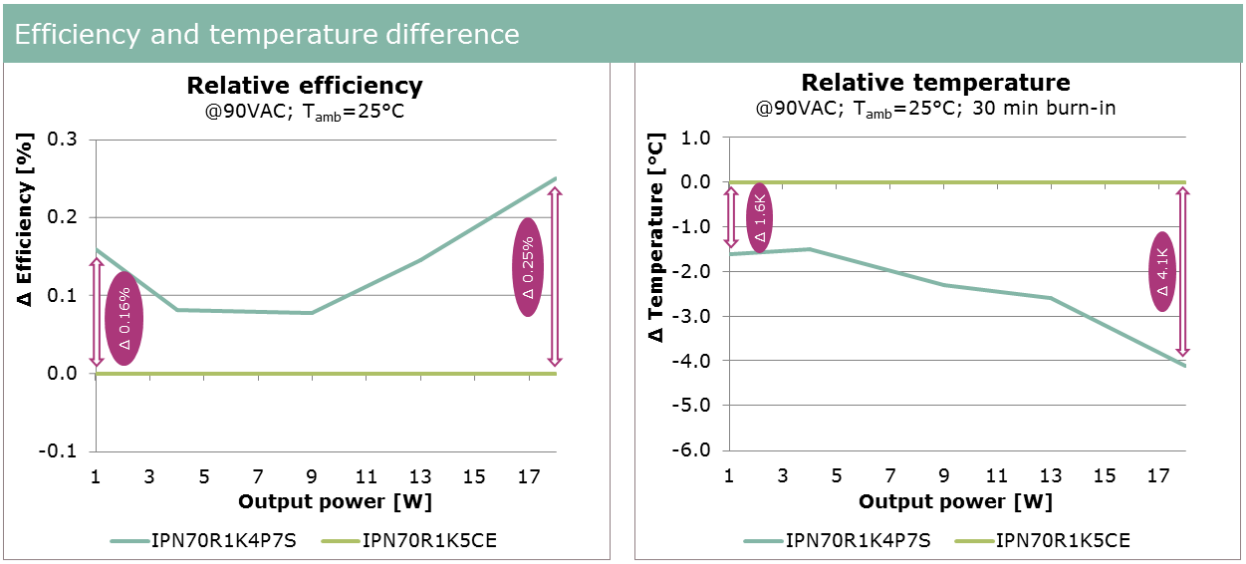
Description	Specification
Input	90–265 V_{AC}
Output	9.0 V_{DC} 2.0 A at 18 W
Topology	Flyback
Original device	IPN70R1K5CE
Switching frequency	25–76 kHz 76 kHz @90 V_{AC}, FL 57 kHz @230 V_{AC}, FL
PCB dimensions – L x W x H	45 mm x 35 mm x 13.5 mm

In this example we want to show two different possible scenarios. The first shows the performance delta when using a 700 V CoolMOS™ P7 and a 700 V CoolMOS™ CE in SOT-223 package to demonstrate the improvement in performance made possible by switching to the new P7 technology. The second shows a DPAK CoolMOS™ C6 device versus a CoolMOS™ P7 SOT-223, to demonstrate that changing from an old technology in the DPAK to a new technology in the SOT-223 enables a similar thermal performance to be met.

Around 30 mm^2 of copper is used to get rid of the heat in the SOT-223 package. When using this small copper area with the same $R_{DS(ON)}$ technology, and switching from DPAK to SOT-223, there will be a slight increase in

temperature. In the absolute worst case scenario, at 90 V_{AC} input and full-load output, we see an increase in temperature of 4.1°C as a result of switching to the smaller SOT-223 package.

3.1.2 Results

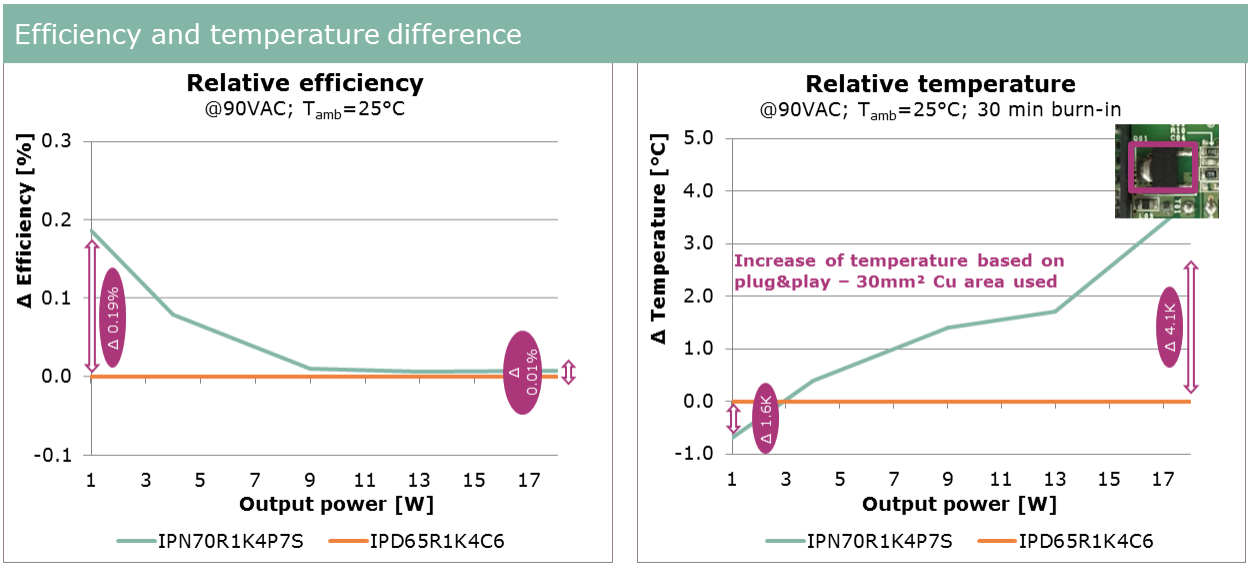


Note: 90VAC – worst case thermal condition

Figure 6 Thermal comparison of IPN70R1K4P7S vs IPN70R1K5CE in an 18 W phone charger. The MOSFET temperature is 69.8°C and efficiency is 82.5% at full load with IPN70R1K5CE.

The graphs shown in Figure 6 are taken at 90 V_{AC} input, which is going to be the limiting thermal point for the design due to the system having the lowest efficiency at this point. The left-hand image is a differential chart in which the MOSFET IPN70R1K5CE is shown as the baseline in green.

When switching to the new CoolMOS™ P7 technology in the same package (SOT-223), an efficiency improvement at the full-load point (in the range of 0.25%) can be realized. This translates to a 4.1°C cooler MOSFET, as shown in the right-hand chart.



Note: 90VAC – worst case thermal condition

Figure 7 Thermal comparison of IPN70R1K4P7S vs IPD65R1K4C6 in an 18 W phone charger. The MOSFET temperature is 61.9°C and efficiency is 82.7% at full load with IPN70R1K5CE.

The left-hand image in Figure 7 a differential chart in which the baseline MOSFET IPD65R1K4C6 is the reference shown in orange.

When a customer switches to the new CoolMOS™ P7 technology in the SOT-223, it can be seen that the efficiency at full load will be comparable due to similar conduction losses, but the SOT-223 package means that the temperature will increase by 4.1°C due to the 30 mm² copper drain pad area. With a larger copper area, as shown previously, this temperature increase can be overcome.

By combining the new SOT-223 and the new CoolMOS™ P7 technology as a drop-in replacement for a DPAK device, a designer can achieve an overall package cost reduction with only a slight decrease in thermal performance. The thermal performance can be matched by increasing the MOSFET drain pad copper area.

3.2 52 W LED driver

3.2.1 Set-up description

To demonstrate the interchangeability of DPAK and the new SOT-223 a board already on the market was taken to carry out some measurements. In LED drivers there tends to be space available for PCB heatsinking due to the low power-density requirements of LED drivers. This makes substituting a DPAK device with a SOT-223 a good fit in lighting applications.

The original device used in the product was an 800 V CoolMOS™ C3 in the DPAK. A plug-and-play comparison was made by changing from the DPAK to a SOT-223 in both CoolMOS™ P7 and CoolMOS™ CE technologies to show the difference between packages and technological performance.

The table below shows the technical LED driver specification:

Table 2 LED driver details

Description	Specification
Input	220 V / 50 Hz
Output	55–150 V / 0.35 A / 52 W
Topology	SEPIC
Original device	SPD04N80C3
Switching frequency	40–60 kHz
PCB dimensions – L x W x H	210 mm x 30 mm x 21 mm
Lifetime requirement	100,000 h

When discussing a new package, topics such as footprint, thermal performance and ease-of-use are important. In this example we want to show two different possible settings:
Introducing a new technology in a known package, which means 800 V CoolMOS™ C3 to 800 V CoolMOS™ P7 in DPAK; and secondly, the combination of a new technology (P7) and a totally new package (SOT-223).
Looking at the footprint, it is clear that the customer uses a large copper pad around the DPAK to lower the effort of external cooling and improve heat spreading over a larger area, and this is illustrated in Figure 8.

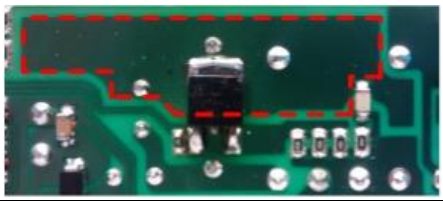


Figure 8 52 W LED driver MOSFET heatsinking copper 530 mm²

Around 530 mm² is used to get rid of the heat from the DPAK package, which immediately suggests the switch to a SOT-223 package. To emphasize this, efficiency and temperature measurements have been taken, and these results are shown on the graph that follows.

The following conditions must be observed: Input of 230 V_{AC}, ambient temperature stabilized to 25°C, and the inside of the enclosure consistent with normal operating conditions.

3.2.2 Results

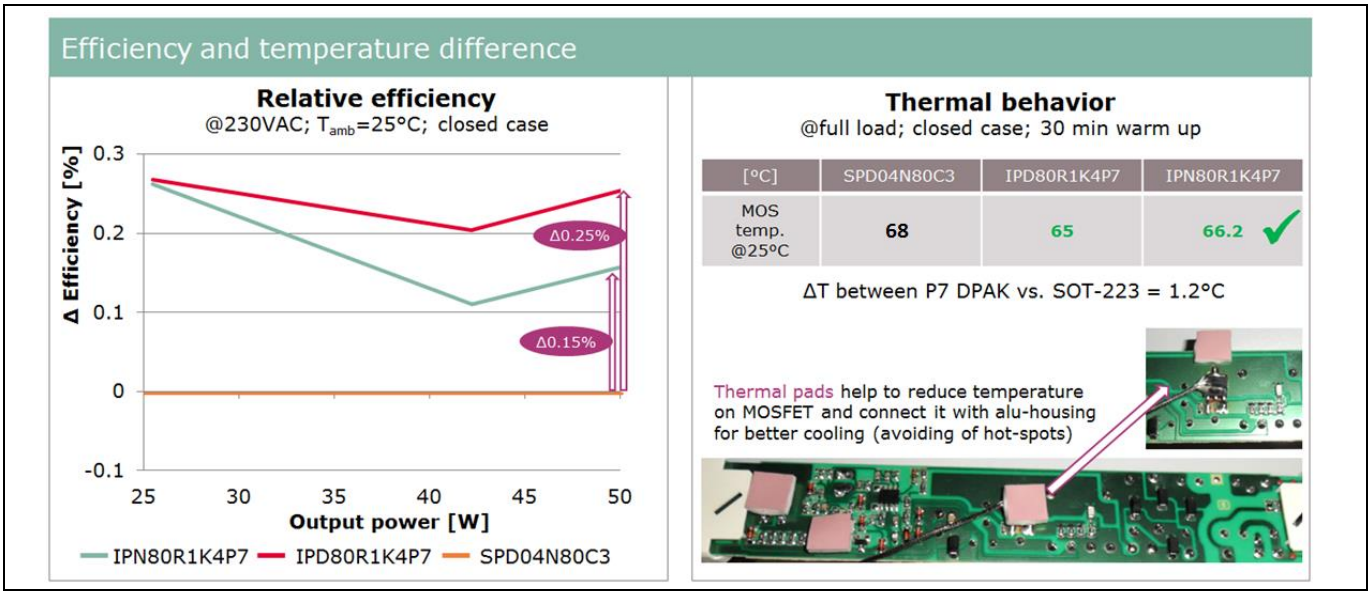


Figure 9 Thermal comparison of IPN80R1K4P7, IPD80R1K4P7 and SPD04N80C3 in a 50 W LED driver. The full-load efficiency with SPD04N80C3 is 90.9%.

The left-hand image is a differential chart in which the original MOSFET SPD04N80C3 is shown as the reference in orange.

When the customer switches to the new CoolMOS™ P7 technology in the same package (DPAK), an efficiency improvement at the full-load point (the most interesting point from a thermal limitation standpoint) in the range of 0.25% can be realized. This translates to a 3°C cooler MOSFET, as shown in the table on the right.

In combination with the new SOT-223 and the new CoolMOS™ P7 technology, the customer can even realize an improvement of 0.15% and a lower MOSFET temperature of 1–2°C while enabling a potential cost reduction with a much smaller package.

It is important to note that in this case the customer is using additional thermal pads to compensate for different heights of SMD packages mounted on the back of the PCB. These thermal pads also improve the thermal performance by providing the best possible connection between the MOSFET and diodes and the LED driver housing to spread the overall system heat.

To summarize this evaluation, the new CoolMOS™ P7 in SOT-223 offers:

1. Potential cost reduction with the new package
2. Improved efficiency and thermal behavior compared to the CoolMOS™ C3
3. Similar efficiency and thermal behavior as the CoolMOS™ P7 in a DPAK

3.3 Application test summary

All of the applications analyzed above have shown that the mold compound temperature is heavily dependent on the additional cooling from the copper area connected to the drain pad. With an additional copper area of ~20 mm² or more when compared to the DPAK minimum footprint, it is possible for a SOT-223 package to have

nearly the same thermal performance as a DPAK by accepting a 2–3°C (approx.) higher case temperature. This gives the SMPS designer the opportunity to reduce the overall BOM costs significantly, as an additional copper area of 20mm^2, if not already in place, does not increase the production costs of the application PCB. The additional performance of the CoolMOS™ P7 technology can help to further reduce the difference between using SOT-223 and DPAK devices on the same copper area.

The last section of this document will show the available range of CoolMOS™ HV MOSFETs in SOT-223.

4 Portfolio

Figure 10 shows the portfolio of the CoolMOS™ P7 in SOT-223, offering products in three different voltage classes: 600 V, 700 V and 800 V. While 600 V and 700 V devices are standard-grade products, the 800 V family is qualified for industrial grade. Once fully released by end of 2017, the portfolio will cover an $R_{DS(on)}$ range from 360 mΩ up to 4500 mΩ.

$R_{DS(on)}$ [mΩ]	Standard grade		Industrial grade
	600 V	700 V	800 V
4500			IPN80R4K5P7
3300			IPN80R3K3P7
2400			IPN80R2K4P7
2000		IPN70R2K0P7S	IPN80R2K0P7
1400		IPN70R1K4P7S	IPN80R1K4P7
1200		IPN70R1K2P7S	IPN80R1K2P7
900		IPN70R900P7S	IPN80R900P7
750		IPN70R750P7S	IPN80R750P7
600	IPN60R600P7S	IPN70R600P7S	IPN80R600P7
450		IPN70R450P7S	
360	IPN60R360P7S	IPN70R360P7S	

In production Release by end of 2017

Figure 10 Portfolio for SOT-223

Revision history

Major changes since the last revision

Page or reference	Description of change

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