PRELIMINARY

INN2214-2215
InnoSwitch-CP Family

Off-Line CV/CC Flyback Switcher IC with Integrated 650 V MOSFET, Sync-Rect, Feedback and Constant Power Profile for USB-PD and QC 3.0

Product Highlights

Highly Integrated, Compact Footprint
- Incorporates flyback controller, 650 V MOSFET, secondary-side sensing and synchronous rectification driver
- Delivers constant power to simplify USB-PD and QC 3.0 designs
- FluxLink™ integrated, HIPOT-isolated, feedback link
- Exceptional CV accuracy, independent of transformer design or external components

EcoSmart™– Energy Efficient
- <10 mW no-load at 230 VAC when supplied by transformer bias winding
- Easily meets all global energy efficiency regulations

Advanced Protection / Safety Features
- Primary sensed output OVP
- Secondary sensed output overshoot clamp
- Secondary sensed output OCP to zero output voltage
- Hysteretic thermal shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

Full Safety and Regulatory Compliance
- 100% production HIPOT compliance testing equivalent to 6 kV DC/1 sec
- Reinforced insulation
- Isolation voltage >3,500 VAC
- UL1577 and TUV (EN60950) safety approved
- EN61000-4-8 (100 A/m) and EN61000-4-9 (1000 A/m) compliant

Green Package
- Halogen free and RoHS compliant

Applications
- QC 3.0 and USB PD chargers

Description

The InnoSwitch™-CP family of ICs dramatically simplify the development and manufacturing of low-voltage, high current power supplies, particularly those in compact enclosures or with high efficiency requirements. The InnoSwitch-CP architecture is revolutionary in that the devices incorporate both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link permit accurate control of a secondary-side synchronous rectification MOSFET and optimization of primary-side switching to maintain high efficiency across the entire load range. Additionally, the minimal DC bias requirements of the link, enable the system to achieve less than 10 mW no-load.

Figure 3. High Creepage, Safety-Compliant eSOP Package.

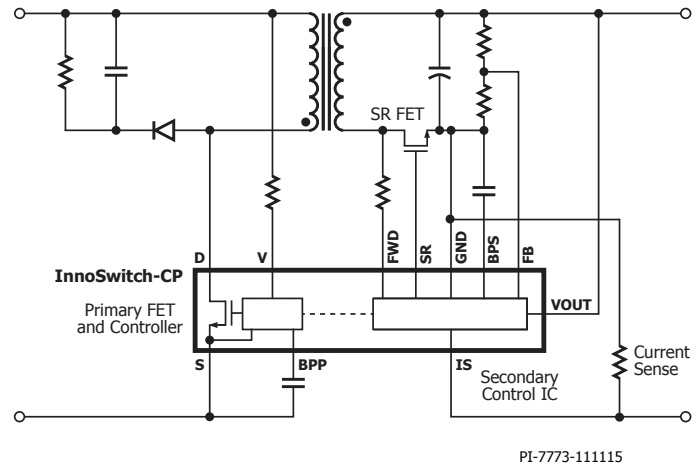

Figure 1. Typical Application/Performance.

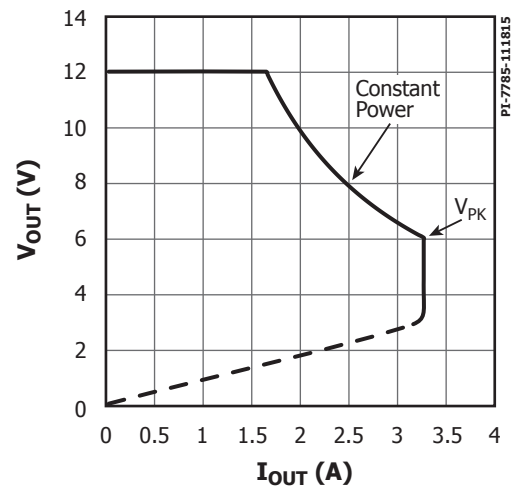

Figure 2 Output Characteristics.

Output Power Table

Product[3]	230 VAC ±15%	85-265 VAC
	Adapter[1]	Peak or Open Frame[1,2]
INN2214K	15 W	20 W
INN2215K	22 W	22 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < = 125 °C.
2. Minimum peak power capability.
3. Package: K: eSOP-R16B.

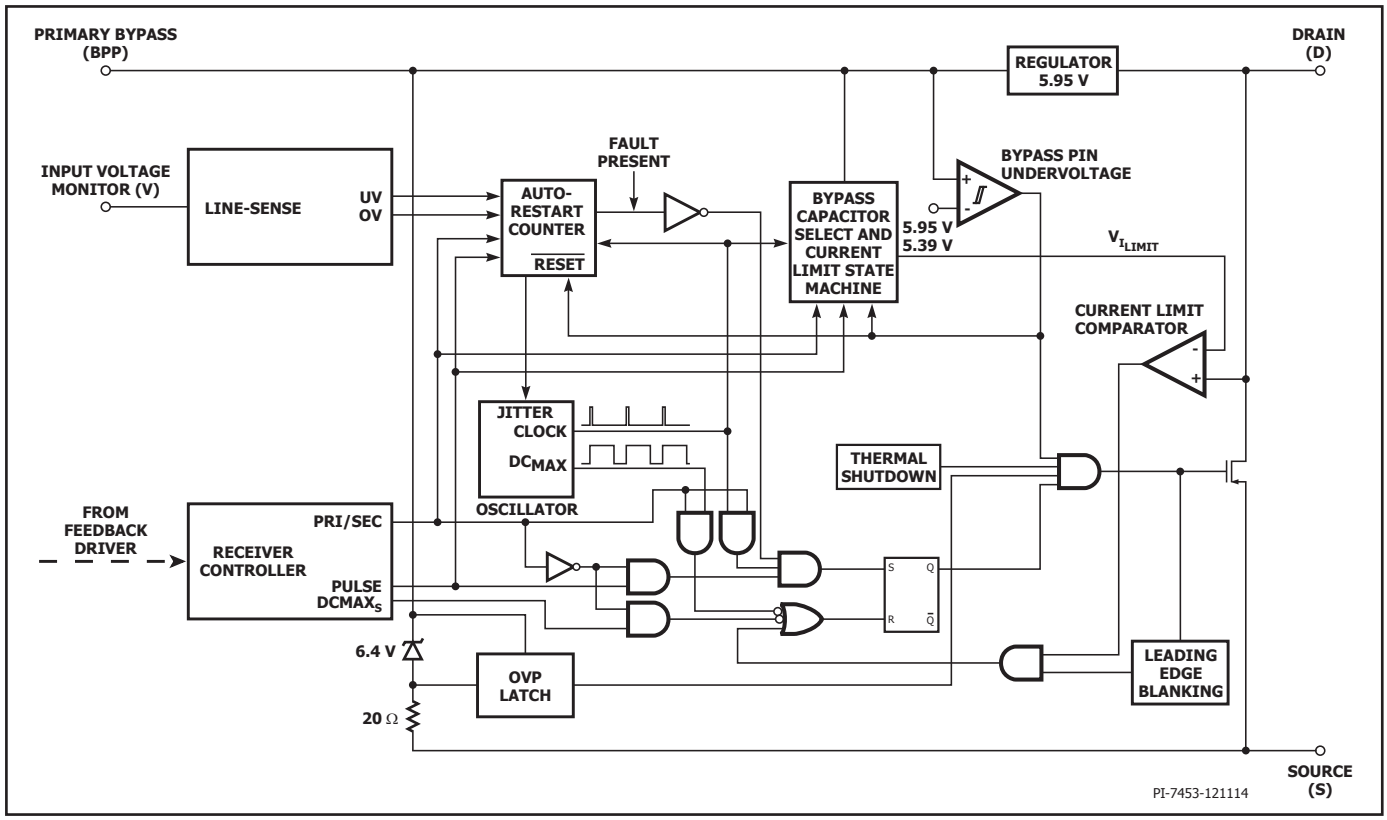

Figure 3. Primary-Side Controller Block Diagram.

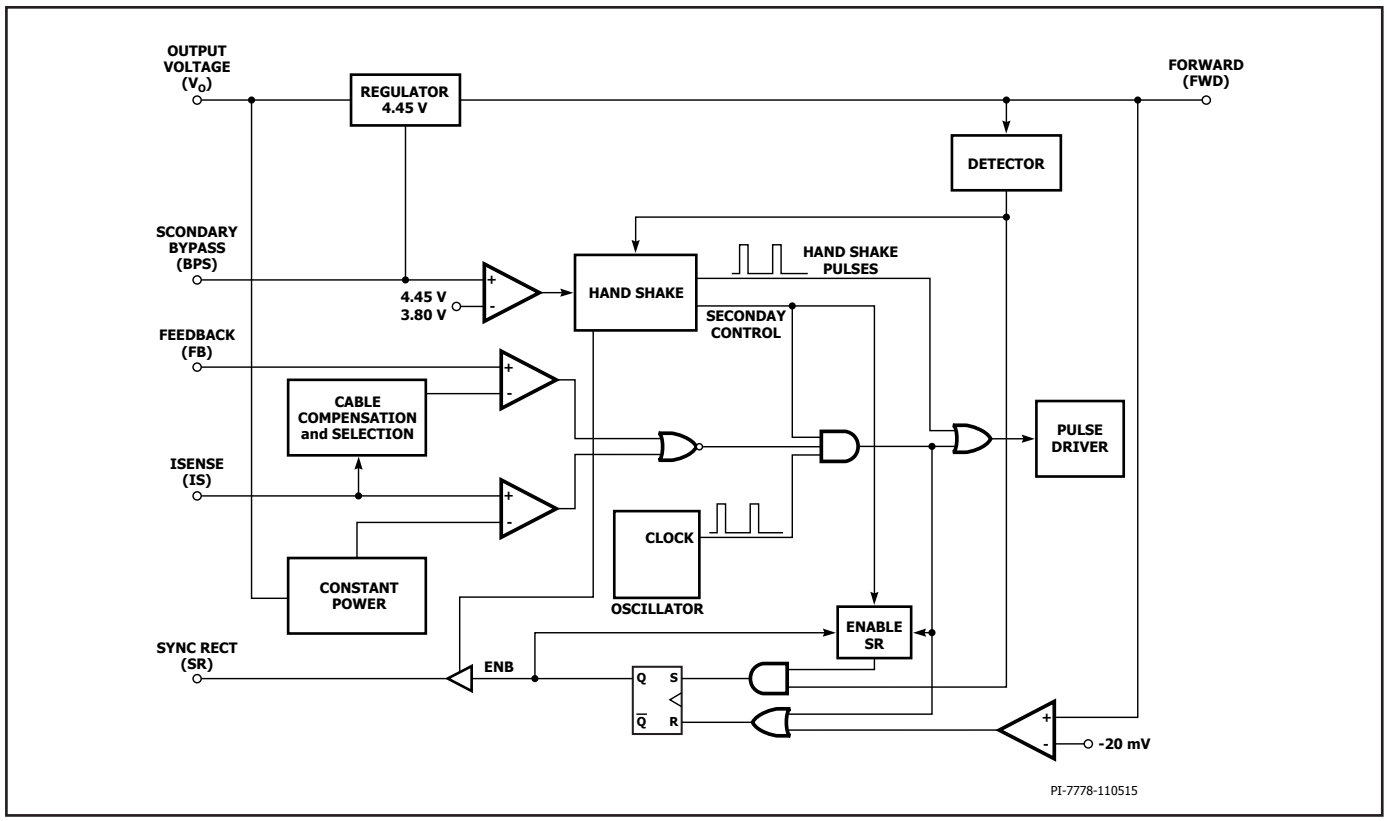

Figure 4. Secondary-Side Controller Block Diagram.

PRELIMINARY

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Pin Functional Description

DRAIN (D) Pin (Pin 1)
This pin is the power MOSFET drain connection.

SOURCE (S) Pin (Pin 3-6)
This pin is the power MOSFET source connection. It is also the ground reference for the PRIMARY BYPASS pin.

PRIMARY BYPASS (BPP) Pin (Pin 7)
It is the connection point for an external bypass capacitor for the primary-side controller IC supply.

INPUT VOLTAGE MONITOR (V) Pin (Pin 8)
A 8 MΩ resistor is tied between the pin and the input bulk capacitor to provide input under and overvoltage protection.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding for sensing and other functions.

OUTPUT VOLTAGE (VOUT) Pin (Pin 11)
This pin is connected directly to the output voltage of the power supply to provide bias to the secondary IC.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 12)
Connection to external SR FET gate terminal.

SECONDARY BYPASS (BPS) Pin (Pin 13)
It is the connection point for an external bypass capacitor for the secondary-side controller supply.

FEEDBACK (FB) Pin (Pin 14)
This pin connects to an external resistor divider to set the power supply CV voltage regulation threshold.

SECONDARY GROUND (GND) (Pin 15)
Ground connection for the secondary IC.

ISENSE (IS) Pin (Pin 16)
Connection to the power supply output terminals. An external current sense resistor is connected between this pin and the SECONDARY GROUND pin.

If secondary current sense is not required, the ISENSE pin should be connected to the SECONDARY GROUND pin.

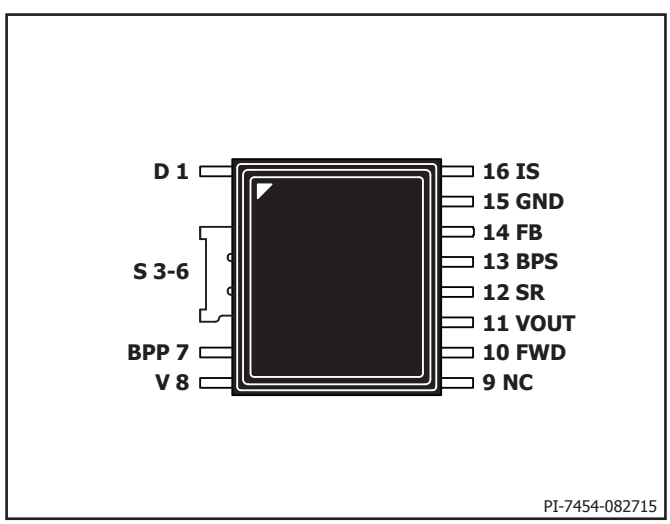

Figure 5. Pin Configuration.

InnoSwitch-CP Functional Description

The InnoSwitch-CP combines a high-voltage power MOSFET switch, along with both primary-side and secondary-side controllers in one device. It has a novel inductive coupling feedback scheme using the package leadframe and bond wires to provide a reliable and low-cost means to provide accurate direct sensing of the output voltage and output current on the secondary to communicate information to the primary IC. Unlike conventional PWM (pulse width modulated) controllers, it uses a simple ON/OFF control to regulate the output voltage and current. The primary controller consists of an oscillator, a receiver circuit magnetically coupled to the secondary controller, current limit state machine, 5.95 V regulator on the PRIMARY BYPASS pin, overvoltage circuit, current limit selection circuitry, over temperature protection, leading edge blanking and a 650 V power MOSFET. The InnoSwitch-CP secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, constant voltage (CV) and constant current (CC) control circuitry, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier MOSFET driver, frequency jitter oscillator and a host of integrated protection features. Figures 3 and 4 show the functional block diagrams of the primary and secondary controllers with the most important features.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor. Extremely low power consumption of the internal circuitry allows the InnoSwitch-CP to operate continuously from current it takes from the DRAIN pin.

In addition, there is a shunt regulator clamping the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This facilitates powering the InnoSwitch-CP externally through a bias winding to decrease the no-load consumption to less than 10 mW (5V output design).

PRIMARY BYPASS Pin Capacitor Selection
The PRIMARY BYPASS pin can use a ceramic capacitor as small as 0.1 μF for decoupling the internal power supply of the device. A larger capacitor size can be used to adjust the current limit. A 1 μF capacitor on the PRIMARY BYPASS pin will select a higher current limit equal to the standard current of the next larger device. A 10 μF capacitor on the PRIMARY BYPASS pin selects a lower current limit equal to the standard current limit of the next smaller device.

PRIMARY BYPASS Pin Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below V_{BPP}-$V_{BPP(H)}$ in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise back to V_{BPP} to enable (turn-on) the power MOSFET.

PRIMARY BYPASS Pin Output Overvoltage Latching Function
The PRIMARY BYPASS pin has an OV protection latching feature. A Zener diode in parallel to the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding to activate this protection mechanism. In the event the current into the PRIMARY BYPASS pin exceeds (I_{SD}) the device will disable the power MOSFET switching. The latching condition is reset by bringing the primary bypass below the reset threshold voltage ($V_{BPP(RESET)}$).

Over-Temperature Protection

The thermal shutdown circuitry senses the primary die temperature. This threshold is typically set to 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C is provided to prevent over-heating of the PC board due to continuous fault condition.

Current Limit Operation

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that switch cycle. The current limit state-machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned-on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse. Each switching cycle is terminated when the Drain current of the primary power MOSFET reaches the current limit of the device.

Auto-Restart

In the event of a fault condition such as output overload, output short-circuit or external component/pin fault, the InnoSwitch-CP enters into auto-restart (AR) operation. In auto-restart operation the power MOSFET switching is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous switching requests from the secondary for time period exceeding t_{AR}.
2. No requests for switching cycles from the secondary for a time period exceeding $t_{AR(SK)}$.

The first condition corresponds to a condition wherein the secondary controller makes continuous cycle requests without a skipped-cycle for more than t_{AR} time period. The second method was included to ensure that if communication is lost, the primary tries to restart again. Although this should never be the case in normal operation, this can be useful in the case of system ESD events for example where a loss of communication due to noise disturbing the secondary controller, is resolved when the primary restarts after an auto-restart off time.

The auto-restart alternately enables and disables the switching of the power MOSFET until the fault is removed. The auto-restart counter is gated by the switch oscillator in SOA mode the auto-restart off timer may appear to be longer.

The auto-restart counter is reset once the primary PRIMARY BYPASS pin falls below the undervoltage threshold V_{BPP}-$V_{BPP(HYS)}$.

Safe-Operating-Area (SOA) Protection

In the event there are two consecutive cycles where the primary power MOSFET switch current reaches current limit (I_{LIM}) within the blanking (t_{LEB}) and current limit (t_{ILD}) delay time, the controller will skip approximately 2.5 cycles or ~25 μsec. This provides sufficient time for reset of the transformer without sacrificing start-up time into large capacitive load. Auto-restart timing is increased when the device is operating in SOA-mode.

Primary-Secondary Handshake Protocol

At start-up, the primary initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers). If no feedback signals are received during the auto-restart on-time, the primary goes into auto-restart and repeats. However under normal conditions, the secondary chip will power-up through the FORWARD pin or directly from VOUT and then take over control. From then onwards the secondary is in control of demanding switching cycles when required.

The handshake flowchart is shown in Figure 6 below.

In the event the primary stops switching or does not respond to cycle requests from the secondary during normal operation when the secondary has control, the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins switching again. This protocol for an additional handshake is also invoked in the event the secondary detects that the primary is providing more cycles than were requested.

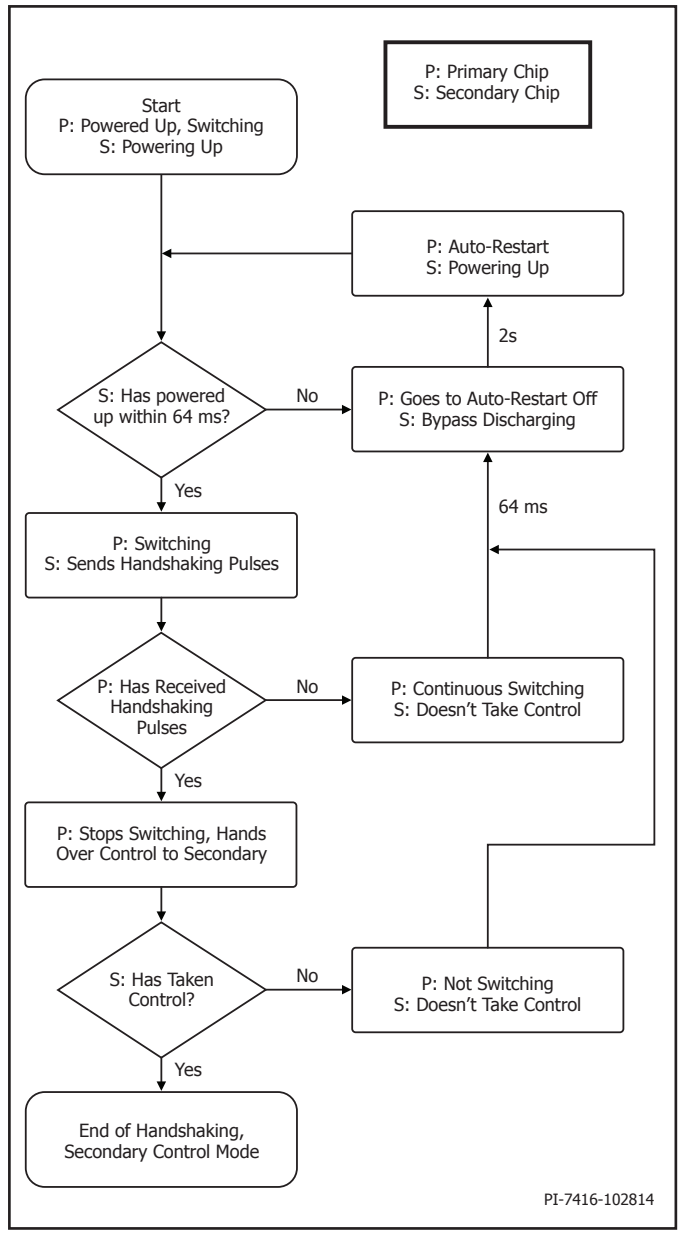

Figure 6. Primary –Secondary Handshake Flowchart.

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The most likely event that could require an additional handshake is when the primary stops switching resulting from a momentary line drop-out or brown-out event. When the primary resumes operation, it will default into a start-up condition and attempt to detect hand-shake pulses from the secondary.

In the event the secondary does not detect that the primary responds to requests for 6 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 6 or more consecutive cycles, the secondary controller will initiate a second handshake sequence.

This protection mode also provides additional protection against cross-conduction of the SR MOSFET while the primary is switching. This protection mode also prevents output overvoltage in the event the primary is reset while the secondary is still in control and light/medium load conditions exist.

Line Voltage Monitor

The VOLTAGE MONITOR pin is used for input under and overvoltage sensing and protection function.

A 8 MΩ resistor is tied between the high voltage bulk DC capacitor after the bridge or connected through a set of diodes from the AC side of bridge and small high-voltage capacitor and bleed resistor (for fast AC reset) and VOLTAGE MONITOR pin to enable this function. To disable this function the VOLTAGE MONITOR pin should be tied to the PRIMARY BYPASS pin.

At power-up after the BPP is charged and the I_{LIM} is latched, prior to switching the state of VOLTAGE MONITOR pin current is checked to determine that it is above brown-in (I_{UV+}) And below the overvoltage shutdown threshold (I_{OV+}) To proceed with start-up.

If during normal operation the VOLTAGE MONITOR pin current falls below the brown-out (I_{UV-}) threshold and remains below brown-in (I_{UV+}) for longer than t_{UV-} the controller enters into auto-restart with a short auto-restart off-time (~200 ms). Switching will only resume once the VOLTAGE MONITOR pin current is above the brown-in threshold (I_{UV+}) for a time period exceeding ~150 ms.

In the event during normal operation the VOLTAGE MONITOR pin current is above the overvoltage threshold (I_{OV+}) for longer than t_{OV}, the controller will enter auto-restart with a short auto-restart off-time (~200 ms). Switching will only resume once the VOLTAGE MONITOR pin current fall below (I_{OV-}) for a time period exceeding ~150 ms.

Secondary Controller

Once the device enters the short auto-restart OFF-time, the PRIMARY BYPASS pin will activate an internal bleed to discharge the input bulk capacitor. The feedback driver block is the drive to the FluxLink communication loop transferring switching pulse requests to the primary IC.

As shown in the block diagram in Figure 4, the secondary controller is powered through a 4.45 V Regulator block by either VOUT or FORWARD pin connections to the SECONDARY BYPASS pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the synchronous rectifier MOSFET (SR FET) connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is also used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below $V_{SR(TH)}$.

In continuous mode operation the SR FET is turned off when the pulse request is sent to demand the next switching cycle, providing excellent synchronization free of any overlap for the FET turn-off while operating in continuous mode.

The mid-point of an external resistor divider network between the VOUT and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{REF} (1.265V).

The external current sense resistor connected between IS and SECONDARY GROUND pins is used to regulate the output current in constant current regulator mode. The internal current sense comparator threshold is IS_{VTH} used to determine the value at which the power supply output current is regulated.

Secondary Controller Oscillator

The typical oscillator frequency is internally set to an average frequency of 100 kHz.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 6 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions.

Output Overvoltage Protection

In the event the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~10 mA is applied on the VOUT pin. This bleed current increases to ~140 mA in the event the FEEDBACK pin voltage is raised to beyond ~20% of the internal FEEDBACK pin reference voltage. The current sink on the VOUT pin is intended to discharge the output voltage for momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

FEEDBACK Pin Short Detection

In the event the FEEDBACK pin voltage is below the $V_{FB(OFF)}$ threshold at start-up, the secondary will complete the primary/secondary hand-shake and will stop requesting pulses to initiate an auto-restart. The secondary will stop requesting cycles for $t_{AR(SK)}$, to begin primary-side auto-restart of $t_{AR(OFF)SH}$. In this condition, the total apparent AR off-time is $t_{AR(SK)} + t_{AR(OFF)SH}$. During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below $V_{FB(OFF)}$ threshold. The deglitch filter on the $V_{FB(OFF)}$ is less than 10 µsec. The secondary will relinquish control after detecting the FEEDBACK pin is shorted to ground.

Cable Drop Compensation (CDC)

The amount of cable drop compensation is a function of the load with respect to the constant current regulation threshold as illustrated in Figure 7.

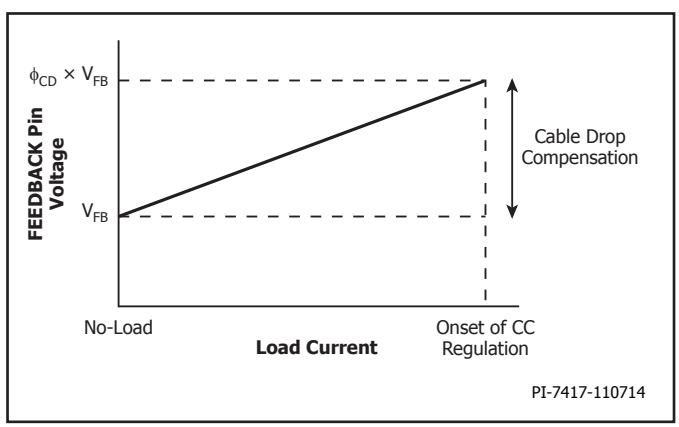

Figure 7. Cable Drop Compensation Characteristics.

The lower feedback pin resistor must be tied to the SECONDARY GROUND pin (not ISENSE pin) to have output cable drop compensation enabled.

OUTPUT VOLTAGE Pin Auto-Restart Threshold

The VOUT pin also includes a comparator to detect when the output voltage falls below the $V_{OUT(AR)}$ threshold for a duration exceeding $t_{VOUT(AR)}$. The secondary controller will relinquish control when it detects the FEEDBACK pin has fallen below $V_{OUT(AR)}$ for a time duration longer than $t_{VOUT(AR)}$. This threshold is meant to limit the range of constant current (CC) operation.

Output Constant-Current and Constant Power Regulation

The InnoSwitch-CP regulates the output current through a resistor between the ISENSE and SECONDARY GROUND pins as well controls the output power in conjunction with ouput voltage sensed on the VOUT pin. If constant current regulation or constant power is not required, this pin must be tied to the GROUND pin.

SR Disable Protection

On a cycle by cycle basis the SR is only engaged in the event a cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event the voltage on the ISENSE pin exceeds approximately 3 times the IS_{VTH} threshold, the SR MOSFET drive is disabled until the surge current has diminished to nominal levels.

InnoSwitch-CP Operation

InnoSwitch-CP devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the

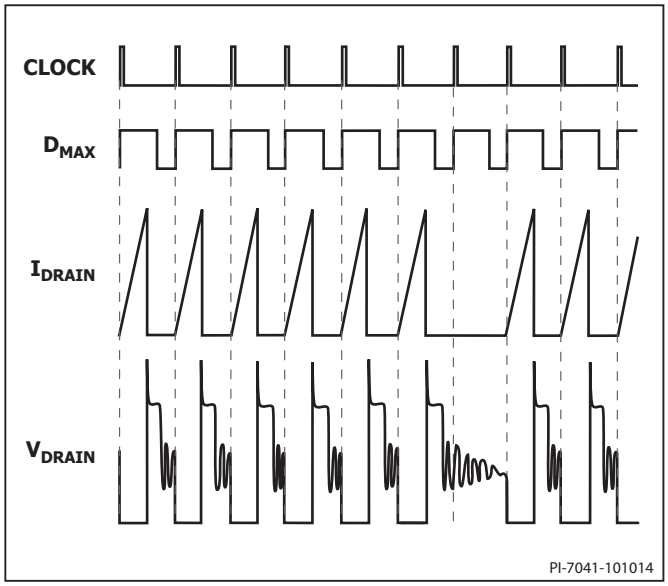

Figure 8. Operation at Near Maximum Loading.

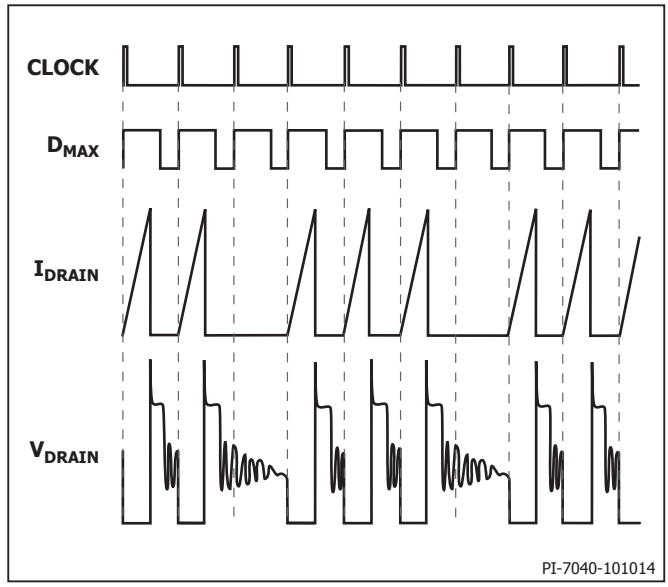

Figure 9. Operation at Moderately Heavy Loading.

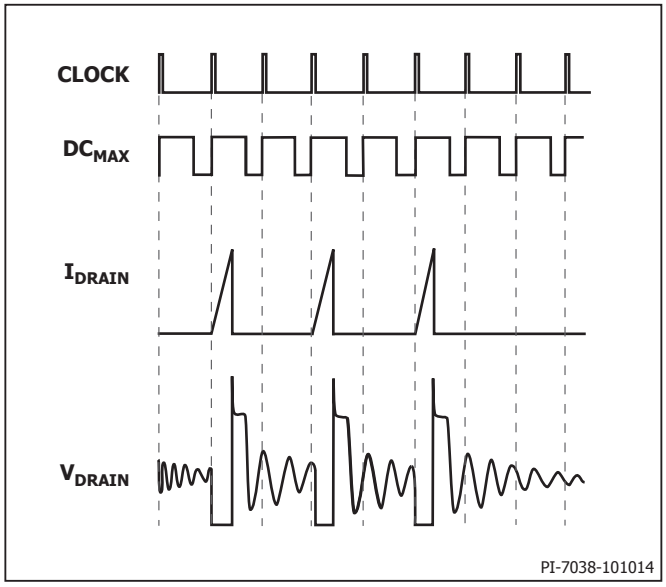

Figure 10. Operation at Medium Loading.

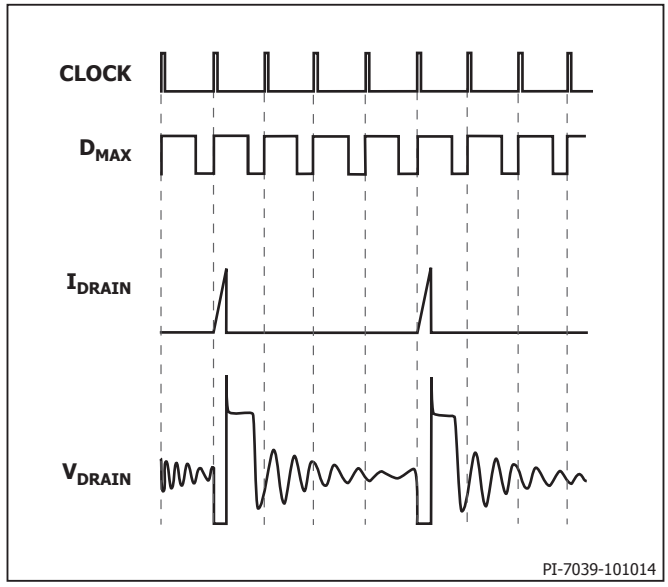

Figure 11. Operation at Very Light Load.

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highest current limit level and frequency of a InnoSwitch-CP design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the InnoSwitch-CP is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

InnoSwitch-CP senses the output voltage on the FEEDBACK pin using a resistive voltage divider to determine whether or not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle. This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, and the amount of energy per switch cycle.

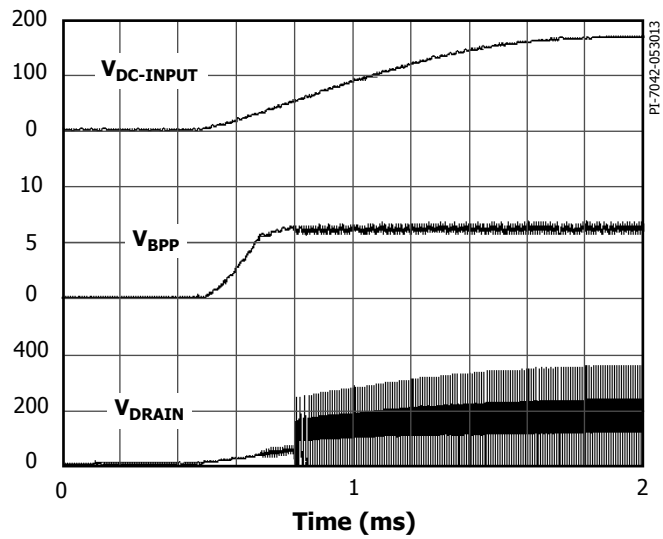

Figure 12. Power-Up.

ON/OFF Operation with Current Limit State Machine

The internal clock of the InnoSwitch-CP runs all the time. At the beginning of each clock cycle, the voltage comparator on the FEEDBACK pin decides whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.

At near maximum load, InnoSwitch-CP will conduct during nearly all of its clock cycles (Figure 8). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 9). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 10). At very light loads, the current limit will be reduced even further (Figure 11). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides accurate regulation and excellent transient response.

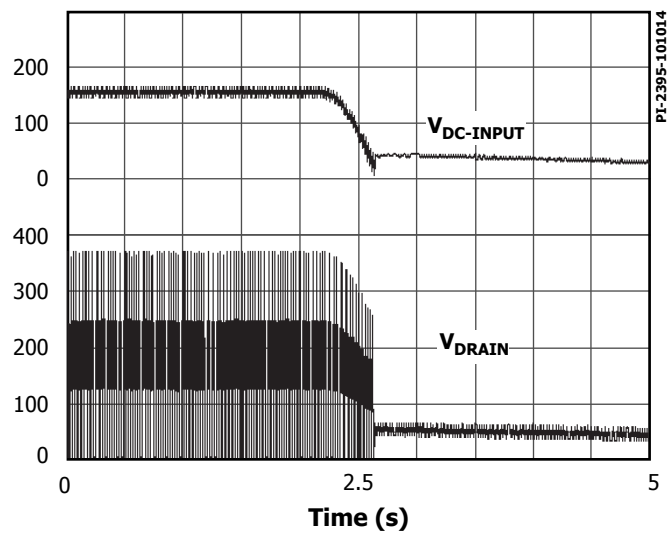

Figure 13. Normal Power-Down Timing.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage ..... -0.3 V to 650 V
DRAIN Pin Peak Current[3] INN2214 ..... 1360 (2550) mA
INN2215 ..... 1680 (3150) mA
PRIMARY BYPASS/SECONDARY BYPASS Pin Voltage ..... -0.3 V to 9 V
PRIMARY BYPASS/SECONDARY BYPASS Pin Current ..... 100 mA
FORWARD Pin Voltage ..... -1.5 V to 150[7] V
FEEDBACK/CURRENT SENSE Pin Voltage ..... -0.3 to 9 V
SR/P Pin Voltage ..... -0.3 to 9 V[6]
OUTPUT VOLTAGE Pin Voltage ..... -0.3 to 15[8] V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to Source and Secondary Ground, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Higher peak Drain current is allowed while the Drain voltage is simultaneously less than 400 V.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. -1.8 V for a duration of ≤500 nsec. See Figure 23.
7. The maximum current out of the FORWARD pin when the FORWARD pin is below Ground is -40 mA.
8. Maximum current into VOUT pin at 15 V should not exceed 10 mA.

Thermal Resistance

Thermal Resistance: K Package:
(θ_{JA}) ..... 65 °C/W[2], 69 °C/W[1]
(θ_{JC}) ..... 12 °C/W[3]

Notes:
1. Solder to 0.36 sq. in (232 mm²), 2 oz. (610 g/m²) copper clad.
2. Solder to 1 sq. in (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured at the plastic surface at the top of the package.

Parameter	Conditions	Rating	Units
Ratings for UL1577 (Adapter power rating is derated power capability)			
Primary-Side Current Rating	Current from pin (3-6) to pin 1	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency Applies to Both Primary and Secondary Controllers	f_{OSC}	T_J = 25 °C	Average	93	100	107	kHz
			Peak-to-Peak Jitter		6		
Maximum Duty Cycle	DC_{MAX}	T_J = 0 °C to 125 °C		60			%
PRIMARY BYPASS Pin Supply Current	I_{S1}	T_J = 25 °C, V_{BPP} + 0.1 V (MOSFET not Switching) See Note B			260		µA
	I_{S2}	T_J = 25 °C, V_{BPP} + 0.1 V (MOSFET Switching at f_{OSC}) See Note A, C	INN2214		790		
			INN2215		930		

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Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
PRIMARY BYPASS Pin Charge Current	I_{CH1}	T_J = 25 °C, V_{BP} = 0 V See Notes D, E			-6.8		mA
	I_{CH2}	T_J = 25 °C, V_{BP} = 4 V See Notes D, E			-4.4		
PRIMARY BYPASS Pin Voltage	V_{BPP}	See Note D		5.70	5.95	6.15	V
PRIMARY BYPASS Pin Voltage Hysteresis	$V_{BPP(H)}$			0.40	0.56	0.70	V
PRIMARY BYPASS Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		6.15	6.45	6.75	V
Line Fault Protection							
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C See Note F			12.3		µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C See Note A, F, G, H			0.87 × I_{UV+}		
Brown-Out Delay Time	t_{UV-}	See Note F, H			32		ms
UV/OV Pin Line Over-voltage Threshold	I_{OV+}	T_J = 25 °C			55.75		µA
UV/OV Pin Line Ovevolt-age Recovery Threshold	I_{OV-}				0.95 × I_{OV+}		
UV/OV Pin Overvoltage Deglitch Filter	t_{OV+}				5		µs
VOLTAGE MONITOR Pin Threshold Voltage	V_V				3.7		V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.1 µF	I_{LIMIT} See Note E	di/dt = 168 mA/µs T_J = 25 °C	INN2214	799	850	901	mA
		di/dt = 213 mA/µs T_J = 25 °C	INN2215	893	950	1007	
Reduced Current Limit (BPP) Capacitor = 10 µF	$I_{LIMIT-1}$ See Note E	di/dt = 168 mA/µs T_J = 25 °C	INN2214	682	750	818	mA
		di/dt = 213 mA/µs T_J = 25 °C	INN2215	773	850	927	
Increased Current Limit (BPP) Capacitor = 1 µF	$I_{LIMIT+1}$ See Note E	di/dt = 168 mA/µs T_J = 25 °C	INN2214	864	950	1036	mA
		di/dt = 213 mA/µs T_J = 25 °C	INN2215	955	1050	1145	

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Power Coefficient	I^2f	Standard Current Limit, $I^2f = I_{LIMIT(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN2214-2215	0.87 × I^2f	I^2f	1.15 × I^2f	A^2Hz
		Reduced Current Limit, $I^2f = I_{LIMITred(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN2214-2215	0.84 × I^2f	I^2f	1.18 × I^2f	
		Increased Current Limit, $I^2f = I_{LIMITinc(TYP)}^2 \times f_{OSC(TYP)}$ See Note A	INN2214-2215	0.84 × I^2f	I^2f	1.18 × I^2f	
Initial Current Limit	I_{INIT}	T_J = 25 °C See Note A		0.75 × $I_{LIMIT(TYP)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note A		170	250		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note A, F			170		ns
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			75		°C
PRIMARY BYPASS Pin Shutdown Threshold Current	I_{SD}			5.6	7.6	9.6	mA
Primary Bypass Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.0	3.3	V
Auto-Restart On-Time at f_{osc}	t_{AR}	T_J = 25 °C See Note G		64	77	90	ms
Auto-Restart Trigger-Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A, G			1		s
Auto-Restart Off-Time at f_{osc}	$t_{AR(OFF)}$	T_J = 25 °C See Note G				2	s
Short Auto-Restart Off-Time at f_{osc}	$t_{AR(OFF)SH}$	T_J = 25 °C See Note A, G			0.5		s

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN2214 I_D = 850 mA	T_J = 25 °C		2.30	2.70	Ω
			T_J = 100 °C See Note A		3.60	4.20	
		INN2215 I_D = 1050 mA	T_J = 25 °C		1.70	2.00	
			T_J = 100 °C See Note A		2.70	3.10	
OFF-State Drain Leakage Current	I_{DSS1}	V_{BPP} = 6.2 V, V_{DS} = 560 V, T_J = 125 °C See Note H				200	µA
OFF-State Drain Leakage Current	I_{DSS2}	V_{BPP} = 6.2 V, V_{DS} = 325 V, T_J = 25 °C See Note A, H			15		µA
Breakdown Voltage	BV_{DSS}	V_{BPP} = 6.2 V, T_J = 25 °C See Note I		725			V
Drain Supply Voltage				50			V
Secondary							
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C		1.250	1.265	1.280	V
OUTPUT VOLTAGE Pin Auto-Restart Threshold	$V_{OUT(AR)}$				3.15		V
SECONDARY BYPASS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			300		µA
Cable Drop Compensation Factor	ϕ_{CD}	T_J = 25 °C See Note J	INN2214	250	300	350	mV
			INN2215	290	300	390	
SECONDARY BYPASS Pin Voltage	V_{BPS}			4.25	4.45	4.65	V
SECONDARY BYPASS Pin Undervoltage Threshold	$V_{BPS(UVLO)}$			3.45	3.8	4.15	V
SECONDARY BYPASS Pin Undervoltage Hysteresis	$V_{BPS(HYS)}$			0.10	0.65	1.2	V
Output (IS Pin) Current Limit Voltage Threshold	IS_{VTH}	T_J = 25 °C			52		mV
VOUT Pin Auto-Restart Timer	$t_{VOUT(AR)}$			50			ms
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$				0.1		V
Constant Power Threshold	V_{PK}	T_J = 25 °C	INN2214	5.35			V
			INN2215	6.35			

Parameter	Symbol	Conditions SOURCE = 0 V T_{JI} = -40 °C to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Synchronous Rectifier[1]							
SYNCHRONOUS RECTIFIER Pin Threshold	V_{SRTH}	T_J = 25 °C		-19	-24	-29	mV
SYNCHRONOUS RECTIFIER Pin Pull-Up Current	I_{SRPU}	T_J = 25 °C C_{LOAD} = 2 nF, f_S = 100 kHz			162		mA
SYNCHRONOUS RECTIFIER Pin Pull-Down Current	I_{SRPD}	T_J = 25 °C C_{LOAD} = 2 nF, f_S = 100 kHz			280		mA
SYNCHRONOUS RECTIFIER Pin Drive Voltage	V_{SR}	See Note A		4.2	4.4	4.6	V
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF See Note A	0-100%		71		ns
			10-90%		40		
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF See Note A	0-100%		32		ns
			10-90%		15		
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C, V_{SPS} = 4.4 V I_{SR} = 10 mA, See Note A			11.5		Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C, V_{SPS} = 4.4 V I_{SR} = 10 mA, See Note A			3.5		Ω

NOTES:

A. This parameter is derived from characterization.

B. I_{S1} is an estimate of device current consumption at no-load, since the operating frequency is so low under these conditions. Total device consumption at no-load is sum of I_{S1} and I_{DSS2} (this does not include secondary losses)

C. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the Drain. An alternative is to measure the PRIMARY BYPASS pin current at 6.2 V.

D. The PRIMARY BYPASS pin is not intended for sourcing supply current to external circuitry.

E. To ensure correct current limit it is recommended that nominal 0.1 µF/1 µF/10 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal PRIMARY BYPASS Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.1 µF	-60%	+100%
1 µF	-50%	+100%
10 µF	-50%	N/A

F. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

G. Auto-restart on-time has same temperature characteristics as the oscillator (inversely proportional to frequency).

H. I_{DSS1} is the worst-case OFF-state leakage specification at 80% of BV_{DSS} and the maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 230 VAC) for no-load consumption calculations.

I. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping Drain voltage up to but not exceeding minimum BV_{DSS}.

J. When used with current source/xx circuit (like CHY103), it is 6% of secondary output voltage if adjusted by changing feedback divider (like CHY100/101).

Typical Performance Characteristics

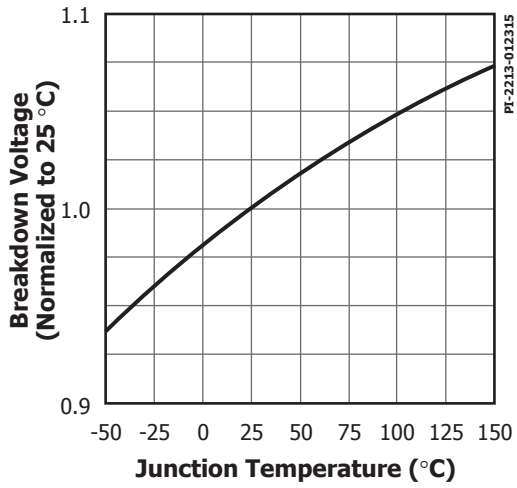

Figure 20. Breakdown vs. Temperature.

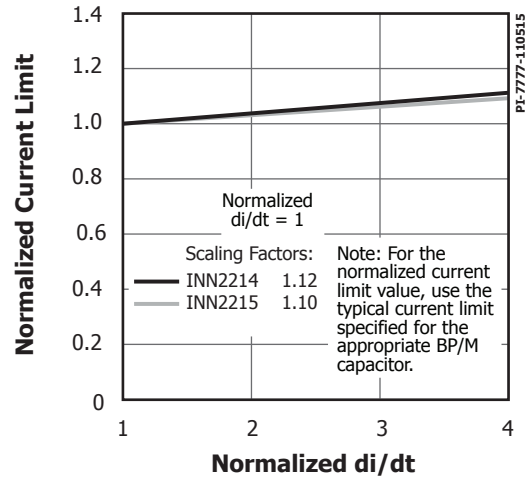

Figure 21. Standard Current Limit Vs. di/dt.

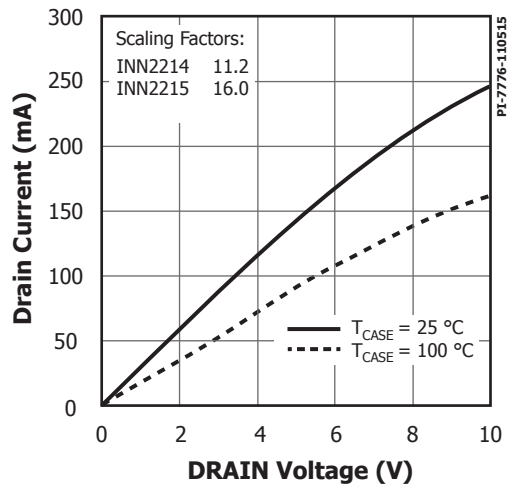

Figure 22. Output Characteristic.

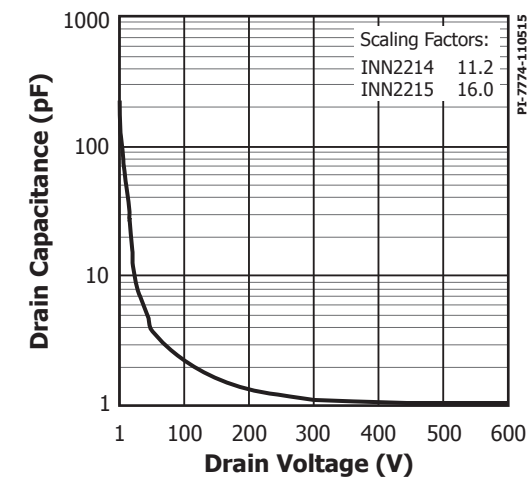

Figure 23. C_{OSS} vs. Drain Voltage.

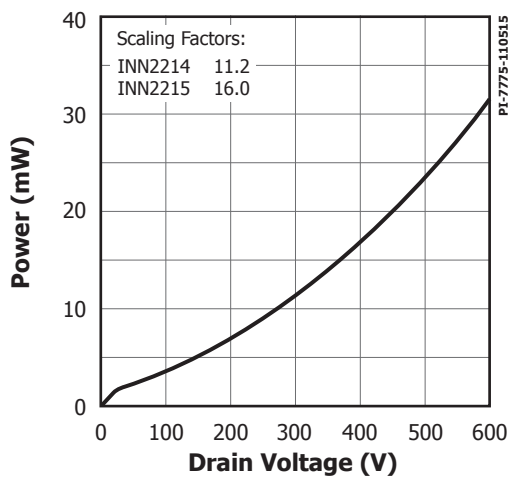

Figure 24. Drain Capacitance Power.

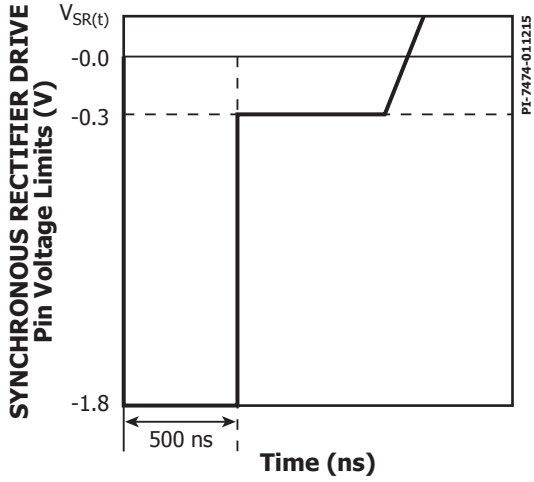

Figure 25. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

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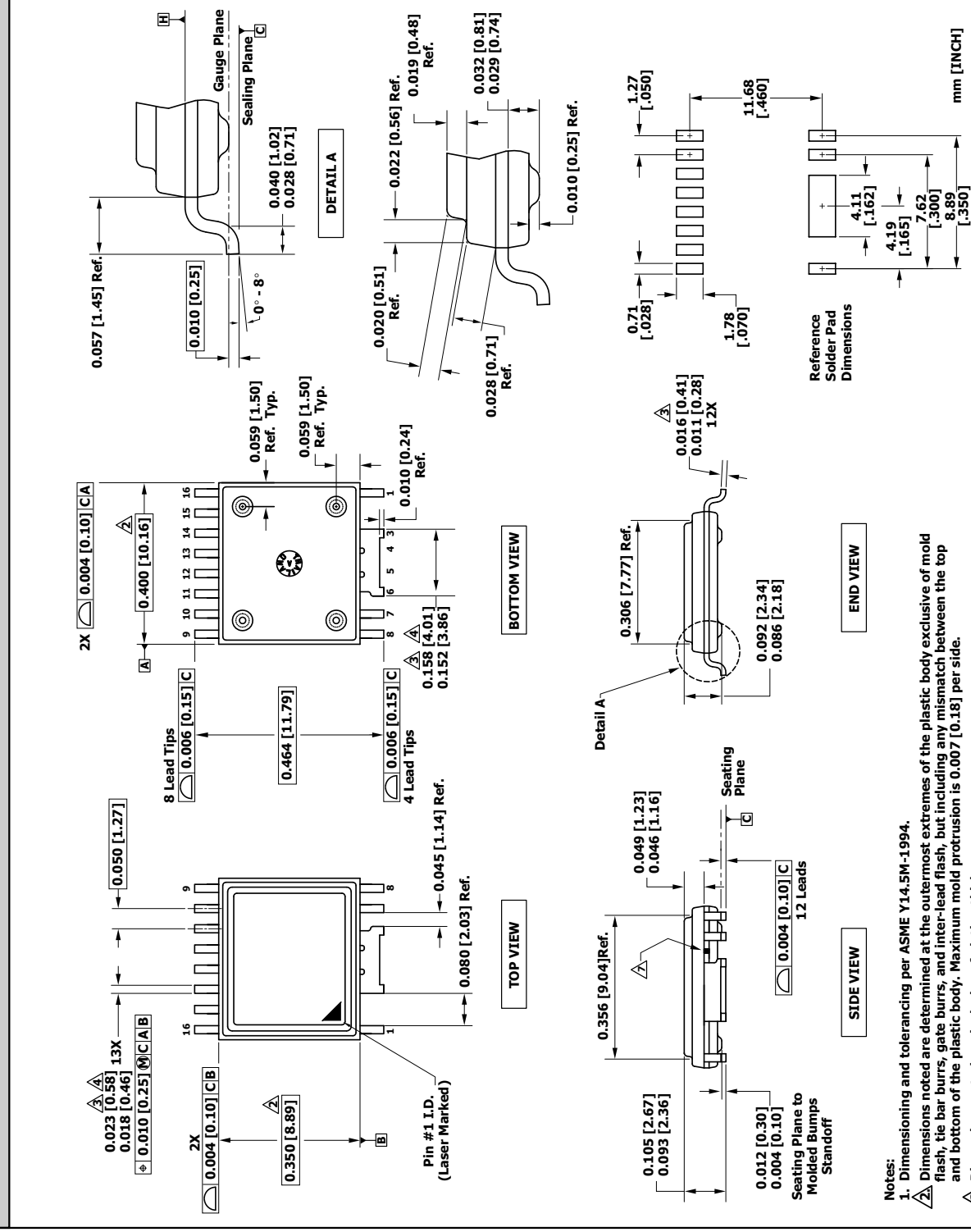

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

PI-6995-111214
POD-eSOP-R16B Rev B

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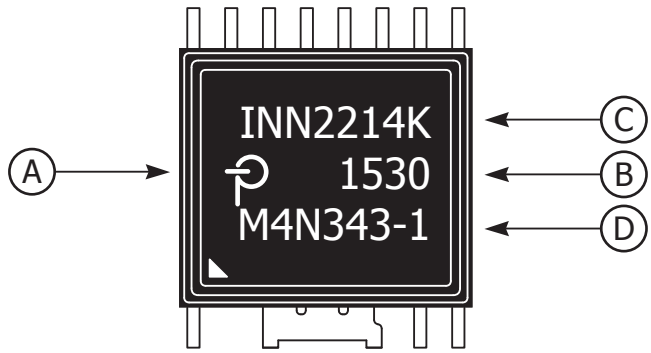
PACKAGE MARKING

eSOP-R16B



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-7786-111015

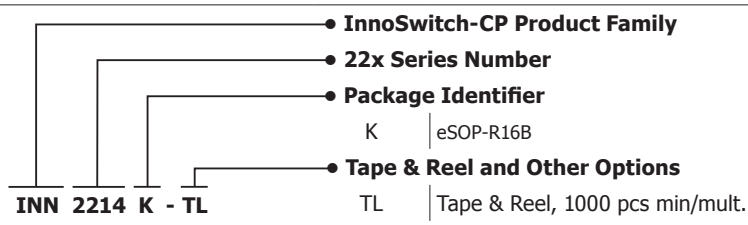
MSL Table

Part Number	MSL Rating
INN2214	3
INN2215	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 V (max) on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Machine Model ESD	JESD22-A115C	> ±200 V on all pins

Part Ordering Information



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Notes

Revision	Notes	Date
A	Code S.	11/15

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

Germany
Lindwurmstrasse 114
80337 Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokohama,
Kohoku-ku
Yokohama-shi, Kanagawa
222-0033 Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@power.com

UK
Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5, 2nd Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com