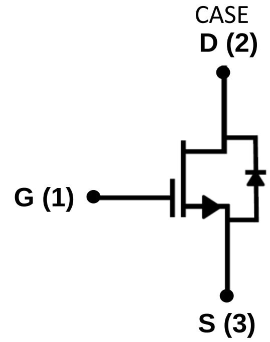
Description

United Silicon Carbide's cascode products co-package its xJ series high-performance SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.



Part Number	Package	Marking
UJC1206K	TO-247-3L	UJC1206K

Features

- Max. on-resistance $R_{DS(on)max}$ of 60mΩ
- Standard 12V gate drive
- Maximum operating temperature of 150°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
Continuous drain current	I_D	T_C = 25°C	38	A
		T_C = 100°C	24.5	A
Pulsed drain current [1]	I_{DM}	T_j = 25°C	138	A
		T_j = 150°C	88	
Short-circuit withstand time [2]	t_{SC}	V_{GS}=15V, V_{CC}<600V	4	µs
Single pulsed avalanche energy [2]	E_{AS}	L=15mH, I_{AS} =4.2A	143	mJ
Power dissipation	P_{tot}	T_C = 25°C	192	W
Maximum junction temperature	$T_{J,max}$		150	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 150	°C
Max. lead temperature for soldering, 1/8" from case for 5 Seconds	T_L		250	°C

1 Pulse width t_p limited by $T_{j,max}$

2 Starting T_J = 25°C

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS} = 1200V, V_{GS} = 0V, T_J = 25°C		110	800	μA
		V_{DS} = 1200V, V_{GS} = 0V, T_J = 150°C		230		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_j=25°C, V_{GS} = -20V / +20V		5	100	nA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=20A, T_J = 25°C		42	60	mΩ
		V_{GS}=12V, I_D=20A, T_J = 150°C		98		
Gate threshold voltage	$V_{G(th)}$	V_{DS} = 5V, I_D = 10mA	4	4.9	6	V
Gate resistance	R_G	f = 1MHz, open drain		1.1		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current	I_S	T_C = 25°C			38	A
Diode pulse current [1]	$I_{S,pulse}$	T_C = 25°C			138	A
Forward voltage	V_{FSD}	V_{GS} = 0V, I_F =20A, T_J = 25°C		1.45	2	V
		V_{GS} = 0V, I_F = 20A, T_J =150°C		2.1		
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=24.5A, V_{GS} =0V, R_{G_EXT} = 22Ω di/dt=1300A/μs, T_J = 25°C		190		nC
Reverse recovery time	t_{rr}			34		ns
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=24.5A, V_{GS} =0V, R_{G_EXT} = 22Ω di/dt=1300A/μs, T_J = 150°C		227		nC
Reverse recovery time	t_{rr}			36		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Input capacitance	C_{iss}	V_{DS} = 100V, V_{GS} = 0V, f = 100kHz		2214		pF
Output capacitance	C_{oss}			178		
Reverse transfer capacitance	C_{rss}			3.5		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS} = 0V to 800V, V_{GS} = 0V		98		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS} = 0V to 800V, V_{GS} = 0V		174		pF
C_{OSS} stored energy	E_{oss}	V_{DS} = 800V, V_{GS} = 0V		31		μJ
Total gate charge	Q_G	V_{DS}=800V, I_D = 24.5A, V_{GS}=0V to 12V		47.5		nC
Gate-drain charge	Q_{GD}			15		
Gate-source charge	Q_{GS}			15		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=24.5A, Gate Driver =0V to +12V, Turn-on $R_{G,EXT}$ = 2Ω, Turn-off $R_{G,EXT}$ = 22Ω Inductive Load, FWD: UJ2D1215T T_J = 25°C		41		ns
Rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			94		
Fall time	t_f			21		
Turn-on energy	E_{ON}			657		μJ
Turn-off energy	E_{OFF}			147		
Total switching energy	E_{TOTAL}			804		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=24.5A, Gate Driver =0V to +12V, Turn-on $R_{G,EXT}$ = 2Ω, Turn-off $R_{G,EXT}$ = 22Ω Inductive Load, FWD: UJ2D1215T T_J = 150°C		41		ns
Rise time	t_r			33		
Turn-off delay time	$t_{d(off)}$			102		
Fall time	t_f			22		
Turn-on energy	E_{ON}			735		μJ
Turn-off energy	E_{OFF}			186		
Total switching energy	E_{TOTAL}			921		

Thermal Characteristics

Parameter	symbol	Test Conditions	Value Min	Value Typ	Value Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.5	0.65	°C/W

Typical Performance Diagrams

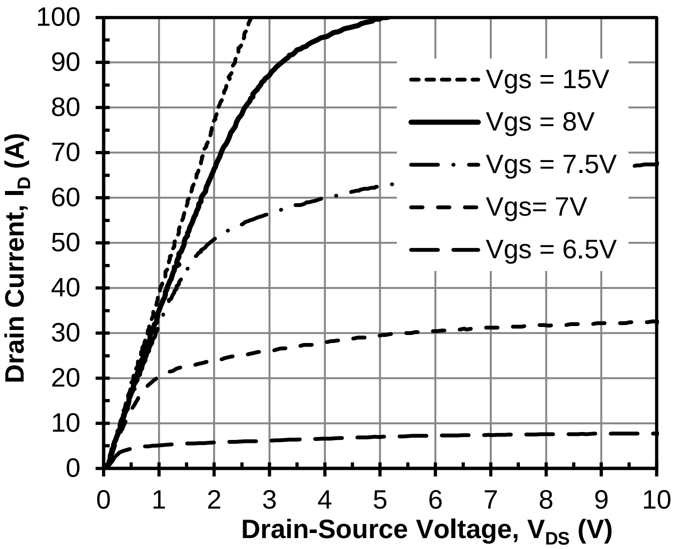


Figure 1 Typical output characteristics at T_j = - 55°C, tp < 250 μs

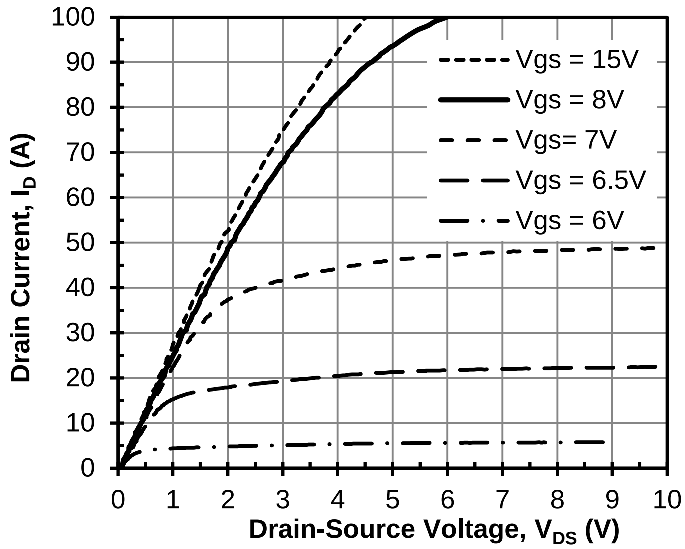


Figure 2 Typical output characteristics at T_j = 25°C, tp < 250 μs

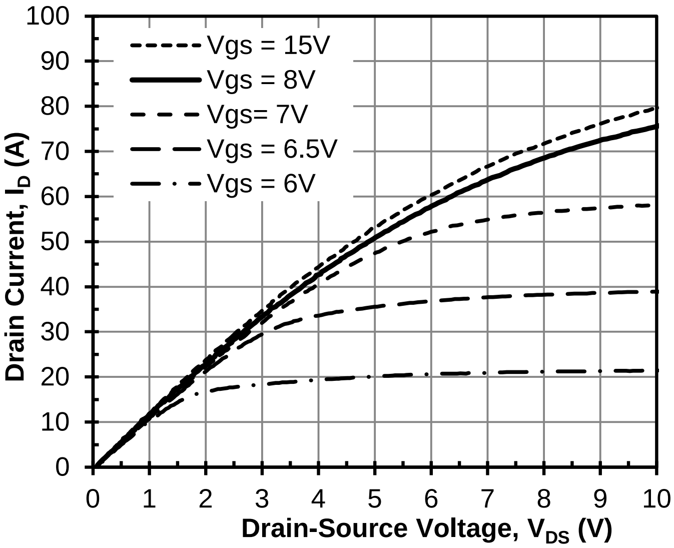


Figure 3 Typical output characteristics at T_j = 150°C, tp < 250 μs

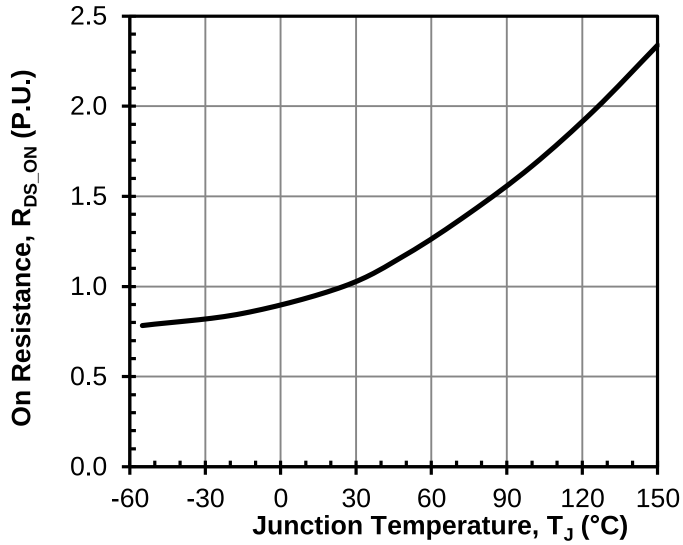


Figure 4 Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 20A

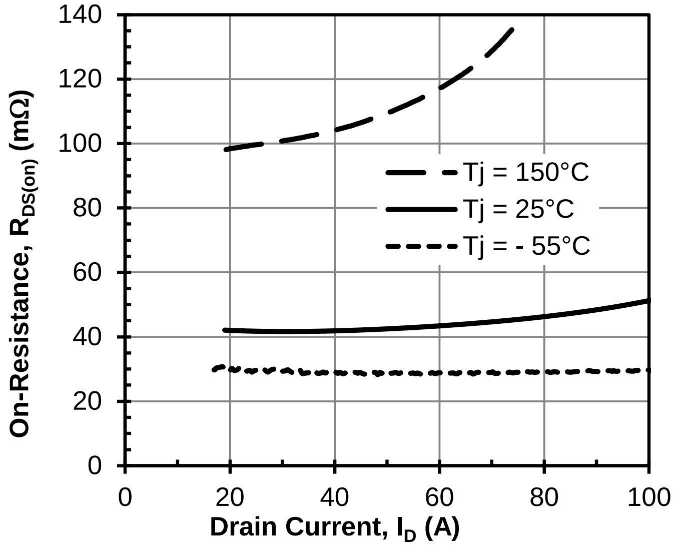


Figure 5 Typical drain-source on-resistance at V_{GS} = 12V

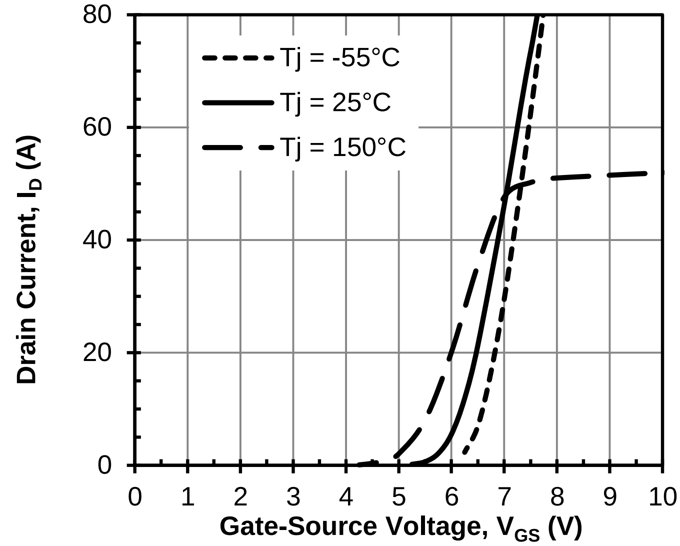


Figure 6 Typical transfer characteristics at V_{DS} = 5V

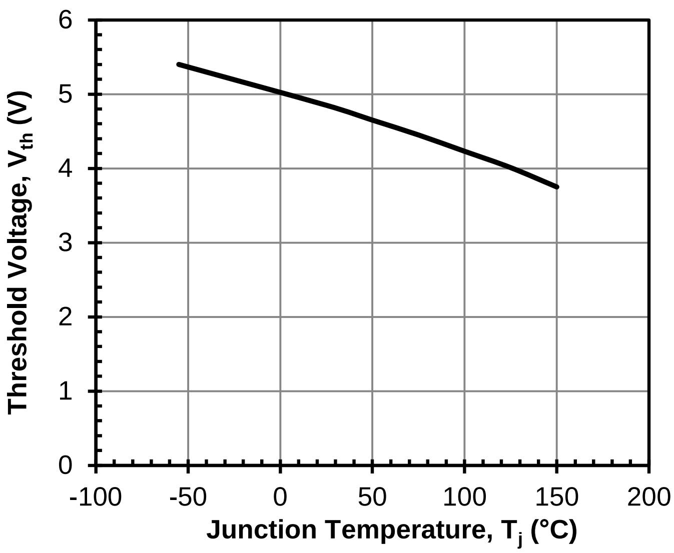


Figure 7 Threshold voltage vs. Tj at V_{DS} = 5V and I_D = 10mA

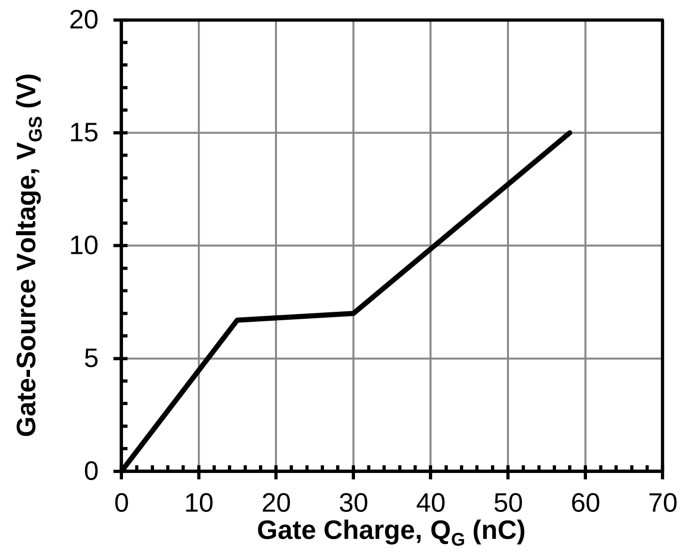


Figure 8 Typical gate charge at V_{DS} = 800V and I_D = 24.5A

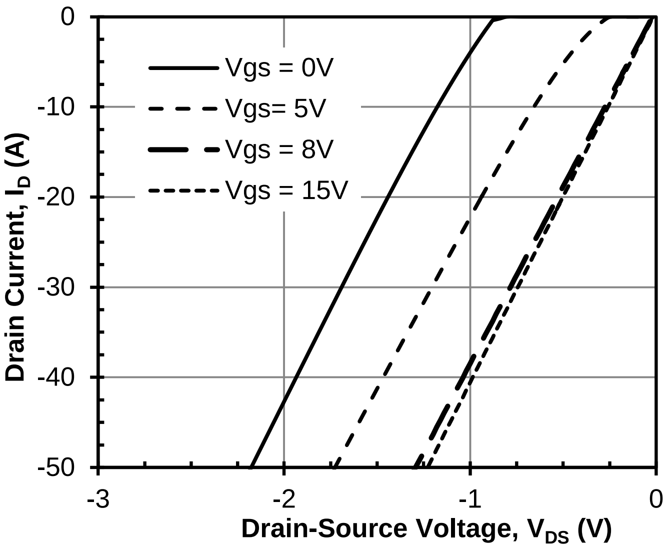


Figure 9 3rd quadrant characteristics at T_J = - 55°C

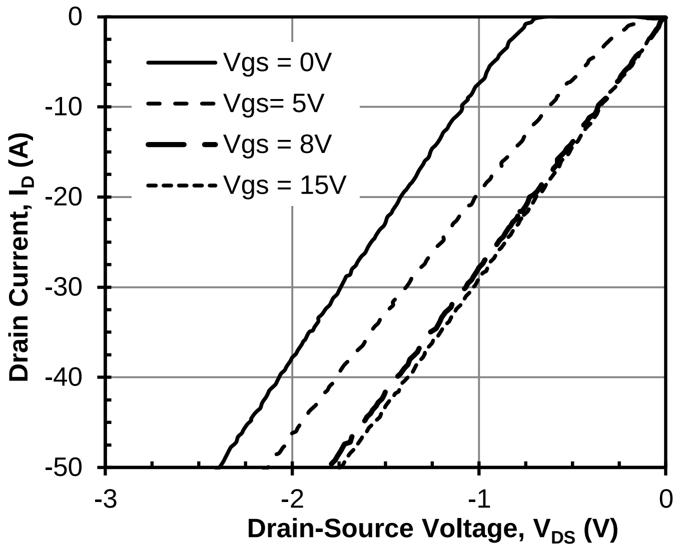


Figure 10 3rd quadrant characteristics at T_J = 25°C

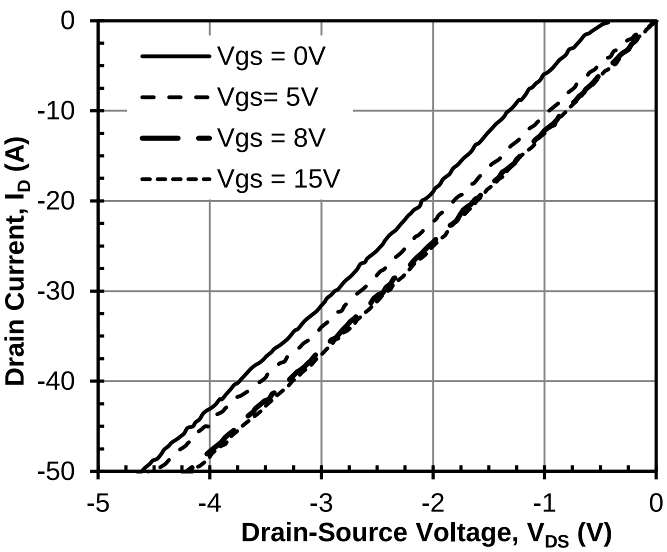


Figure 11 3rd quadrant characteristics at T_J = 150°C

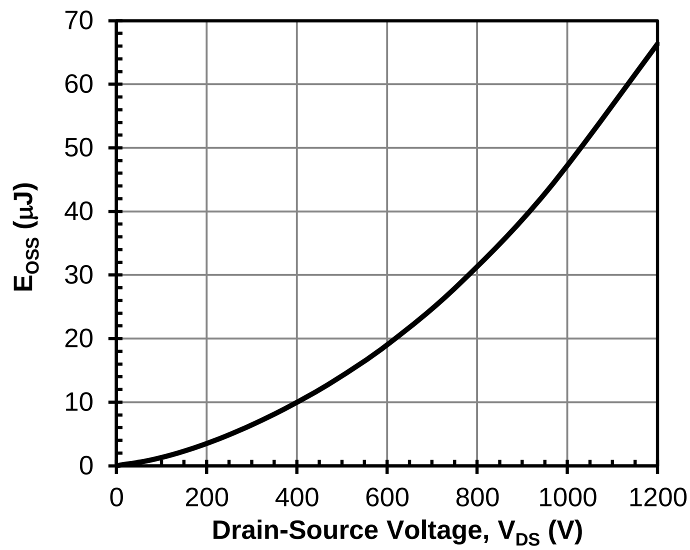


Figure 12 Typical stored energy in C_{OSS} at V_{GS} = 0V

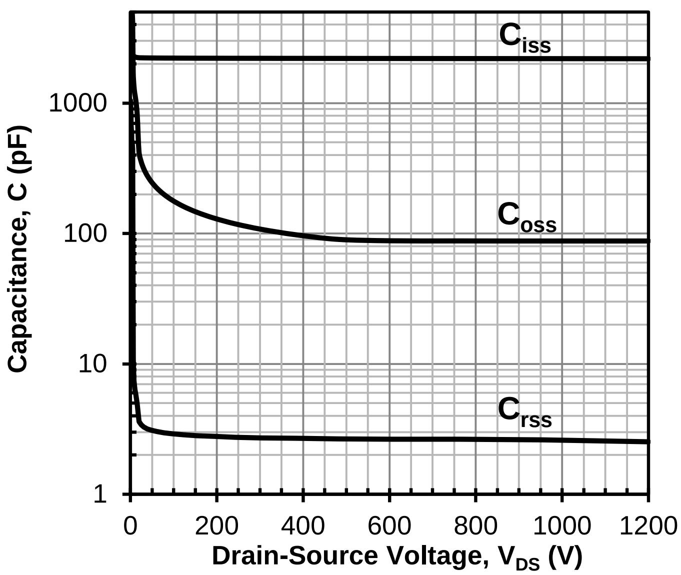


Figure 13 Typical capacitances at 100kHz and V_{GS} = 0V

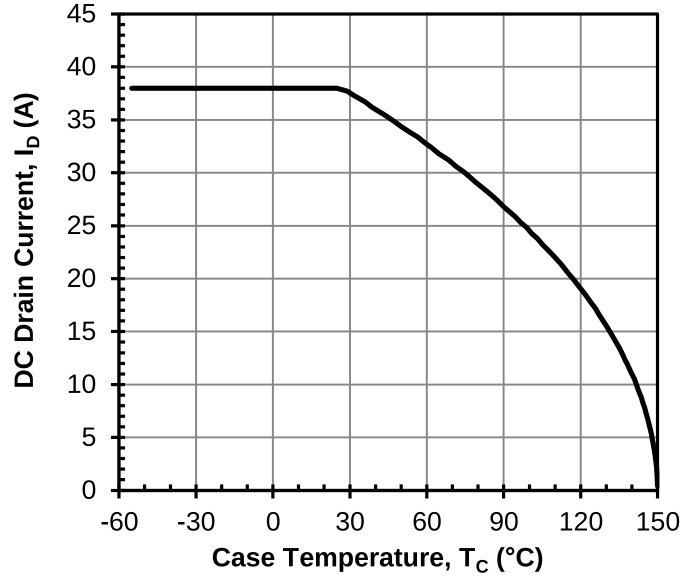


Figure 14 DC drain current derating

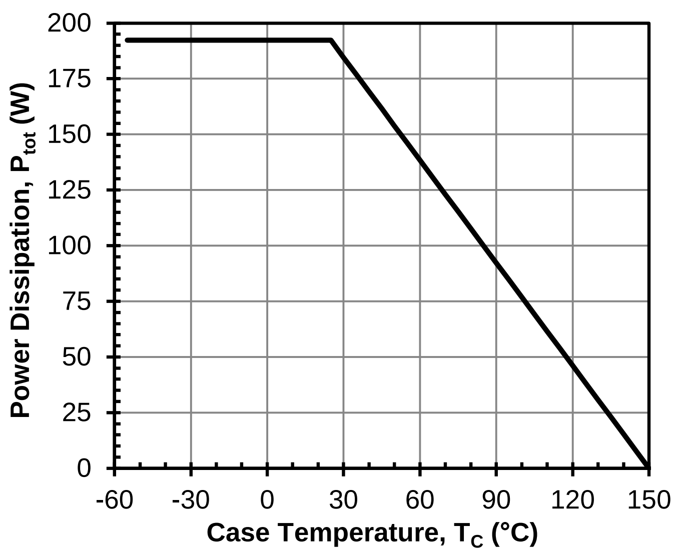


Figure 15 Total power dissipation

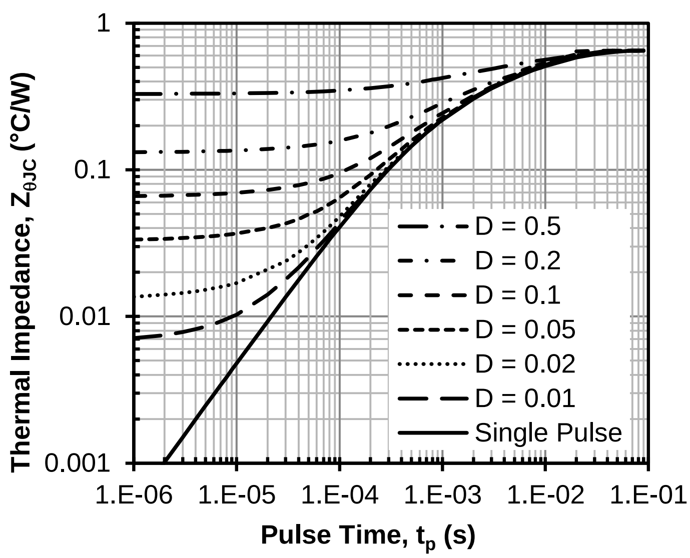


Figure 16 Maximum transient thermal impedance

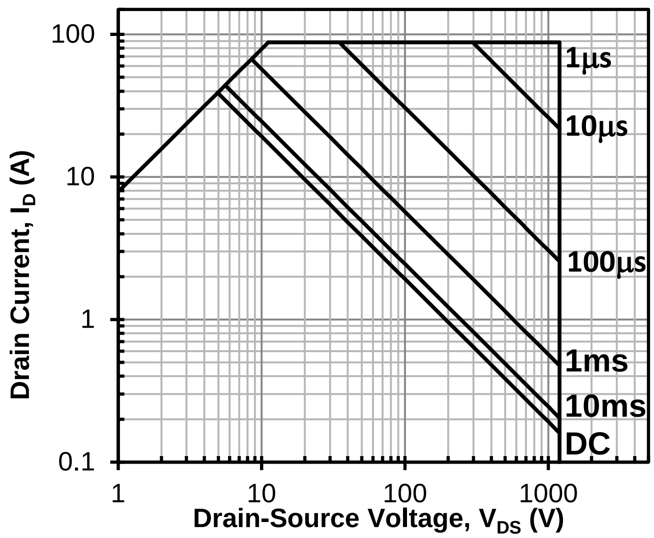


Figure 17 Safe operation area
T_c = 25°C, D = 0, Parameter t_p

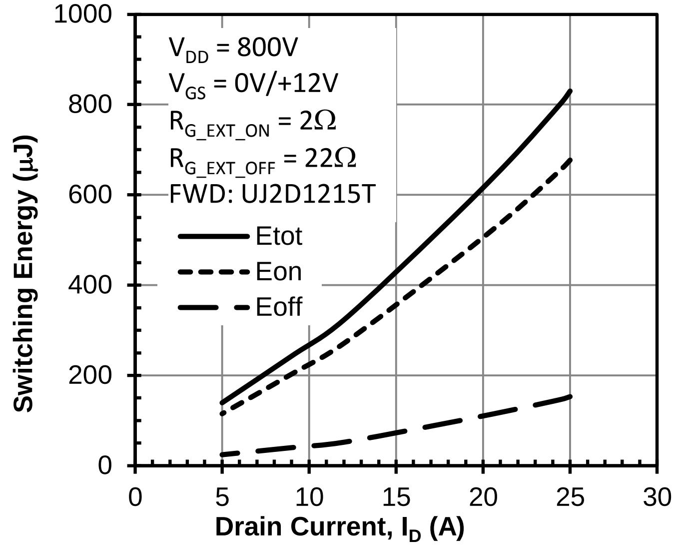


Figure 18 Clamped inductive switching energy
vs. drain current at T_J = 25°C

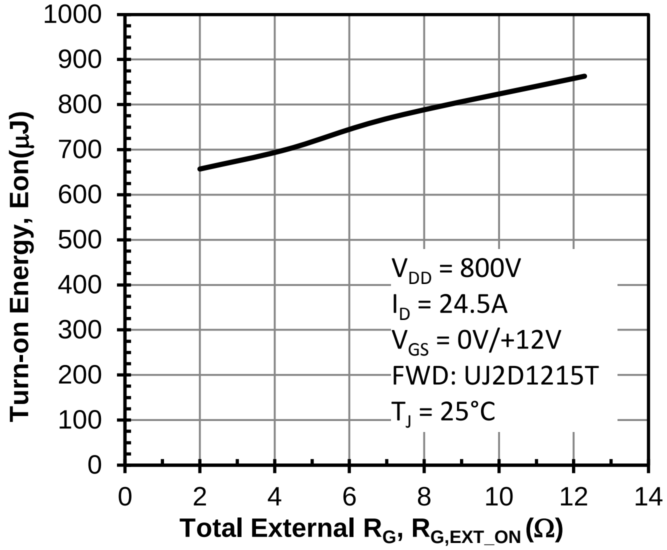


Figure 19 Clamped inductive switching
turn-on energy vs. R_{G,EXT_ON}

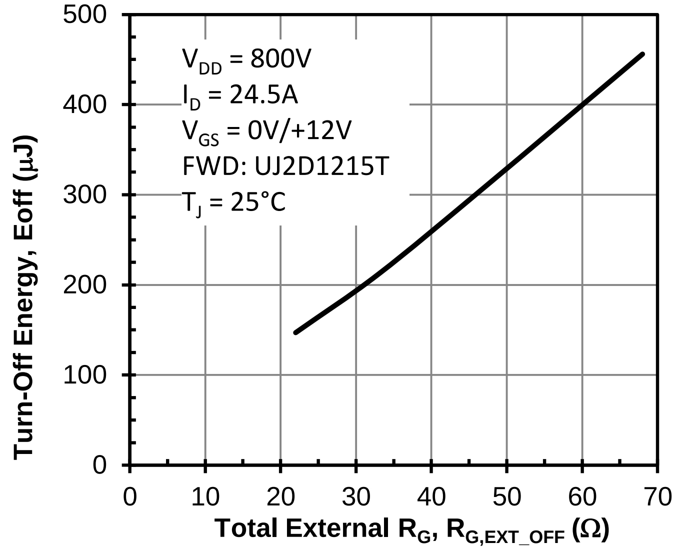


Figure 20 Clamped inductive switching
turn-off energy vs. R_{G,EXT_OFF}

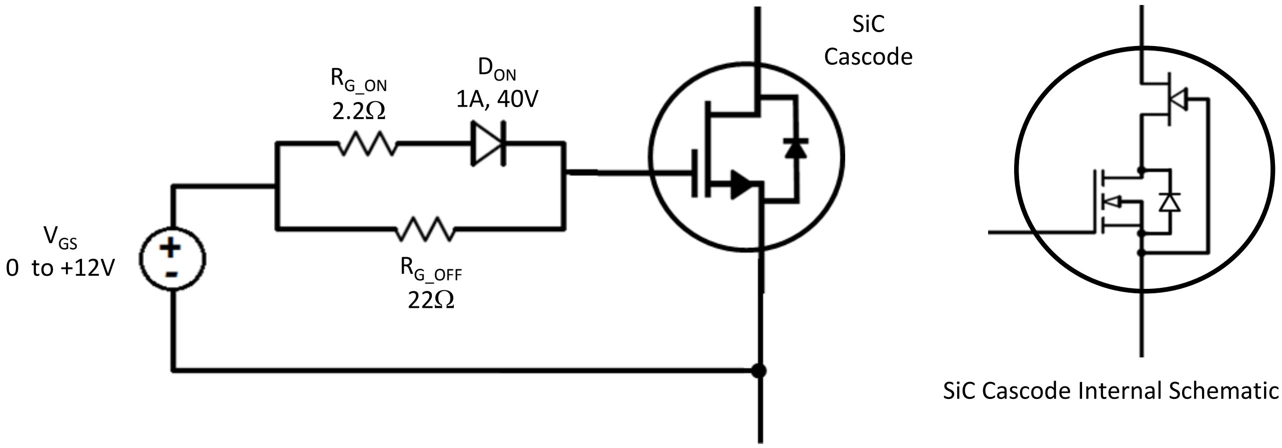


Figure 21 Recommended gate drive and internal circuit schematic of SiC cascode

Applications Information

SiC cascodes are enhancement-mode power siwtches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series as shown in Figure 21. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (Coss), gate charge (Qg), and reverse recovery charge (Qrr) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. In particular, separate turn-on and turn-off gate resistors are recommended as shown in Figure 21. In addition, an external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recover performance. For more information on cascode operation, see www.unitedsic.com.

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