30V 3.0A Synchronous CV/CC Step-Down Converter

General Description

AP2960 is a wide input voltage, high efficiency Synchronous CC/CV step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. AP2960 provides up to 3.0A output current at 350kHz switching frequency.

AP2960 eliminates the expensive, high accuracy current sense resistor, making it ideal for battery charging applications and adaptors with accurate current limit. The AP2960 achieves higher efficiency than traditional constant current switching regulators by eliminating its associated power loss on the additional current sensing resistor.

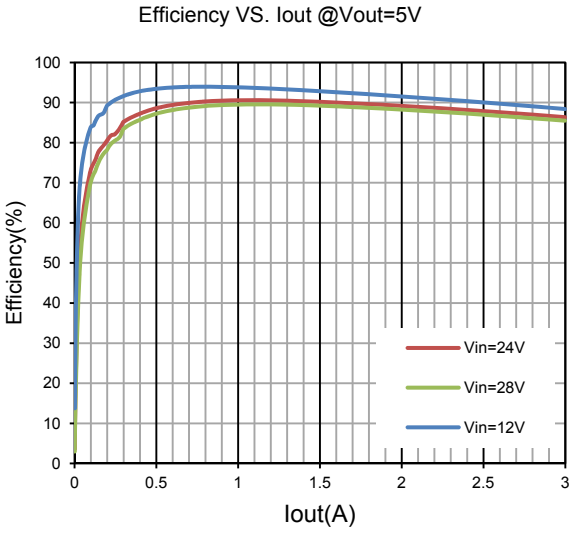
Protection features include cycle-by-cycle current limit, thermal shutdown, and short circuit recovery. AP2960 are available in a SOP8-EP package and require very few external devices for operation.

Applications

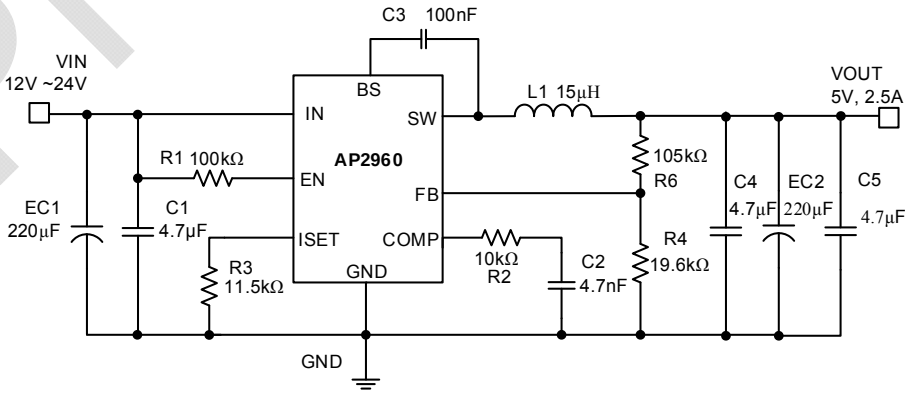
- Car Charger/ Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

Features

- 30V Input Voltage Surge
- 28V Steady State Operation
- Up to 3.0A Output Current
- 350kHz Switching Frequency
- Up to 93% Efficiency
- Stable with Low-ESR Ceramic Capacitors to Allow Low-Profile Designs
- Constant Current Control Without Additional Current Sensing Resistor Improves Efficiency and Lowers Cost.
- Resistor Programmable Current Limit from 1.5A to 3.0A
- Up to 0.5V Excellent Cable Voltage Drop Compensation
- ±7.5% CC Accuracy
- 2% Feedback Voltage Accuracy
- Advanced Feature Set
  Integrated Soft Start
  Thermal Shutdown
  Cycle-by-Cycle Current Limit
- SOP8-EP Package



Typical Application Circuit

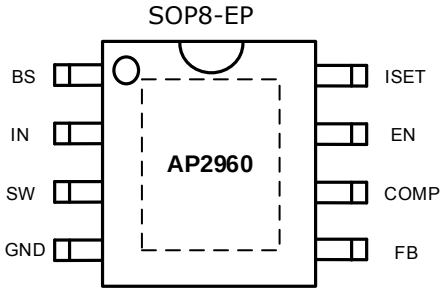


Ordering Information

Order codes	Mark	Package
AP2960SPER	AP2960 YYWWP[1]	SOP8-EP

1.YYWW=date code,P= Package factory

Package



Pin Description

Pin No.	Pin Name	Pin Function
1	BS	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 100nF capacitor from BS pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a minimum 4.7μF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	EN	Enable Input. EN is pulled up to 5V with a 2M resistance, and contains a precise 1.6V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter shutdown mode.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
9	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

Functional Block Diagram

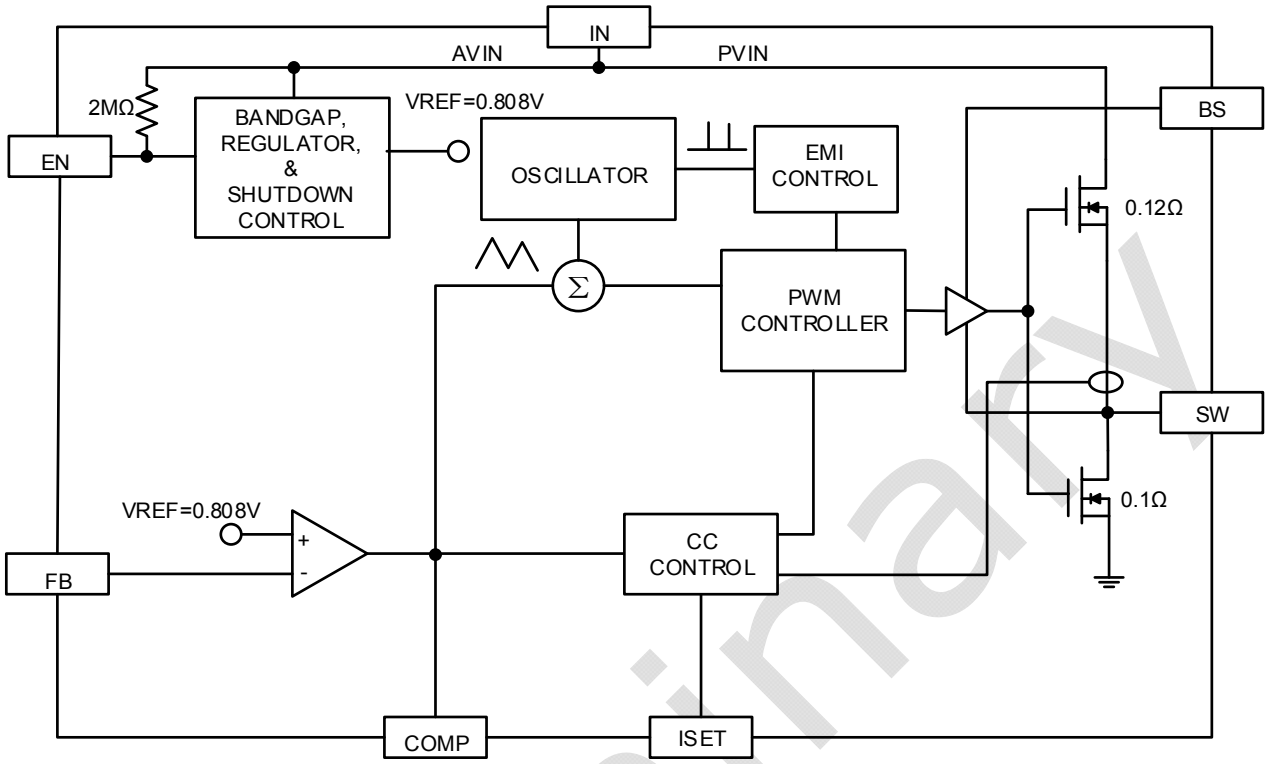


Figure 1 Functional Block Diagram

Absolute Maximum Ratings(Note 1)

Input Supply Voltage..... -0.3V~30V
SW Voltage.....-0.3V~30V
Boost Voltage.....-0.3 ~ (VSW+5.5V)
EN Pin.....-0.3V ~ 6V
FB COMP ISET Pin.....-0.3V ~ 5.5V
Junction Temperature.....Internal limit
Storage Temperature.....-55°C ~ 150°C
Lead Temperature (Soldering 10 sec.) .....260℃
ESD Rating per ESDA/JEDEC JS-001-2014
Human Body Mode.....±4 kV

Operating Ratings

Input Supply Voltage.....6V ~ 28V
Operating Temperatur.....–40℃ to +85℃
Max Junction Temperature.....-40°C ~ 125°C

Package Thermal Resistance

θ_{JA} ..... 50°C/W
θ_{JC} ..... 15°C/W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Electrical Characteristics

(V_{IN} = 12V, T_A = +25℃, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Supply Voltage						
Input Voltage			6		28	V
Input UVLO						
UVLO Threshold	VIN_{UVLO}	V_{IN} Rising	4.5	5	5.5	V
Hysteresis	VIN_{HYS}	V_{IN} Falling		0.3		V
Input Supply Current						
Standby Supply Current (no load)	I_Q	V_{FB} = 0.8V		3		mA
Standby Supply Current	I_{VIN}	V_{FB} = 1V		2.5		mA
Shutdown Supply Current				10		μA
ENABLE						
Enable threshold (High)	V_{EN_HIGH}		1.47	1.6	1.73	V
Enable threshold (Low)	V_{EN_LOW}			1.3		V
Enable internal pull up	I_{EN}			6		μA
Cable Compensation						
ISET voltage	V_{ISET}			1		V
ISET to IOUT DC Current Gain	$ISET_{GAIN}$	R_{ISET} = 11.5kΩ		30000		A/A
Error Amplifier						
Output sink current	I_{SINK}	V_{FB}=0.7V		100		μA
Output source current	I_{SOURCE}	V_{FB}=0.9V		100		μA
Open loop gain	GVO			4000		
Input voltage	VI			0.808		V
Output Voltage						
Feedback voltage	V_{FB}		792	808	824	mV
Feedback current	I_{FB}			1	50	nA
Frequency						
Operation frequency	Fsw_0.8V	V_{FB} = 0.8V		350		kHz
Hiccup Waiting Time	Fsw_0V	V_{FB} = 0V		120		ms
Maximum duty cycle	D max	F_{sw} = 350kHz		93		%
Minimum duty cycle	D min	F_{sw} = 350kHz		7		%

Electrical Characteristics (Continued)

(V_{IN} = 12V, T_A = +25℃, unless otherwise noted.)

MOSFET						
High Side MOSFET On Resistance (1)	$R_{DS(ON\_H)}$			0.12		Ω
Low Side MOSFET On Resistance (1)	$R_{DS(ON\_L)}$			0.1		Ω
High-Side MOSFET Leakage Current	$R_{DS(HIGH\_LEAK)}$	V_{SW} = 0V		1		μA
Low-Side MOSFET Leakage Current	$R_{DS(LOW\_LEAK)}$	V_{SW} = VIN		1		μA
Current Limit						
High Side MOSFET current Limit	I_{LIM_HS}	R_{ISET}=5.1kΩ		3.8		A
ISET voltage	V_{ISET}	IOUT / ISET, R_{ISET} = 11.5kΩ	0.98	1	1.02	V
Soft start						
Soft start time (1)	T_{SS}			2		ms
Thermal Shutdown						
Thermal Shutdown threshold(1)	T_{SDN}			165		°C
Thermal Shutdown Hysteresis	T_{SDN_HYS}			25		°C

Notes:

(1) Guaranteed by design.

Functional Description

CV/CC Loop Regulation

As seen in Functional Block Diagram, the AP2960 is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to VIN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off. At this point, the SW side of the inductor swings to ground through the internal Low Side Power Switch, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using BS as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will be transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 350kHz.

However, if FB voltage is lower than 0.25V, AP2960 will go into short circuit of auto-restart mode with very low power.

Enable Pin

The AP2960 has an enable input EN for turning the IC on or off. The EN pin contains a precision 1.6V comparator with 300mV hysteresis and a 2M pull-up resistance. The comparator can be used with a resistor divider from VIN to program a startup voltage higher than the normal UVLO value. It can be used with a resistor divider from VOUT to disable charging of a deeply discharged battery, or it can be used with a resistor divider containing a thermistor to provide a temperature-dependent shutoff protection for over temperature battery. The thermistor should be thermally coupled to the battery pack for this usage.

If left floating, the EN pin will be pulled up to roughly 5V by the internal 2M pull-up resistance. It can be driven from standard logic signals greater than 1.6V, or driven with open-drain logic to provide digital on/off control.

Thermal Shutdown

The AP2960 disables switching when its junction temperature exceeds 160°C and resumes when the temperature has dropped by 25°C.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 2:

Output Voltage Setting

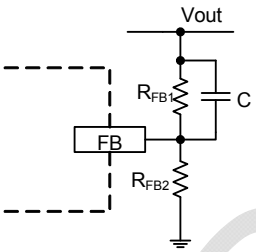


Figure 2 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use R_{FB2} ≈20kΩ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.808V} - 1\right)$$

CC Current Setting

AP2960 constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is approximating linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 30000 (30mA/1μA). To determine the proper resistor for a desired current, please refer to Figure 5 below.

Figure 3:
Curve for Programming Output CC Current

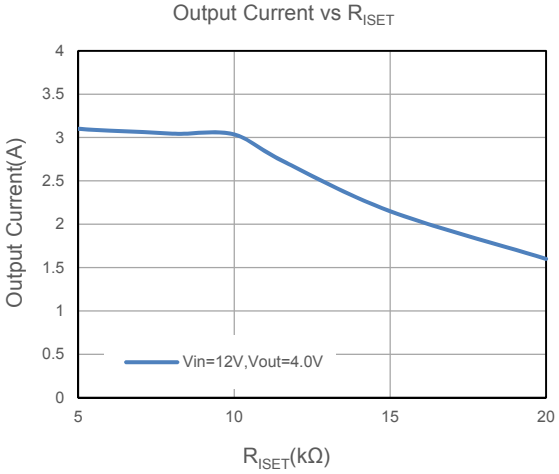
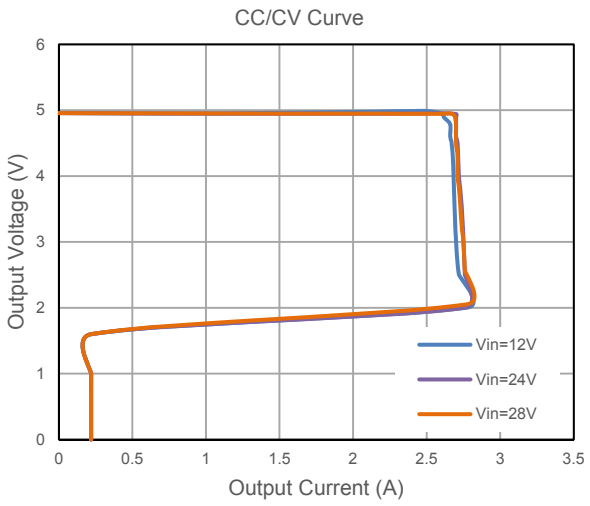


Figure 4:
CC/CV Curve（R3=11.5k, R4=19.6k, R6=105k）



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:
Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOADMAX} K_{RIPPLE}}$$

where VIN is the input voltage, VOUT is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.
With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}}$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK}$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

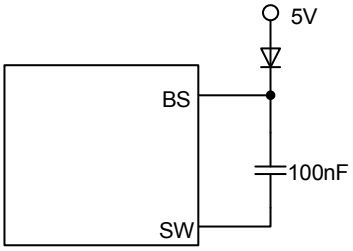
$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK}$$

L_{LIM} is the internal current limit, which is typically 3.8A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.

Figure 5: External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.
The input capacitance needs to be higher than 4.7μF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 4.7μF ceramic capacitor is placed right next to the IC.

Output Capacitor

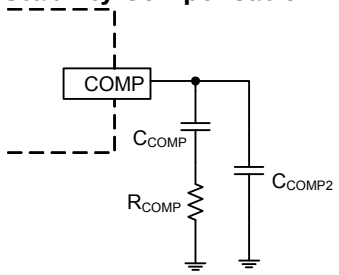
The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{8 \times f_{SW}^{2} LC_{OUT}}$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.
For ceramic output capacitor, typically choose a capacitance of about 4.7μF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

STABILITY COMPENSATION

Figure 6:
Stability Compensation



CCOMP2 is needed only for high ESR output capacitor The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 6. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808V}{I_{OUT}} A_{VEA} G_{COMP}$$

The dominant pole P1 is due to CCOMP:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}}$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}}$$

The first zero Z1 is due to RCOMP and CCOMP:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}}$$

And finally, the third pole is due to RCOMP and CCOMP2 (if CCOMP2 is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via RCOMP:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.808V}$$

$$= 5.12 \times 10^{7} V_{OUT} C_{OUT} \ (\Omega)$$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If RCOMP is less than 15kΩ, the equation for CCOMP is:

$$C_{COMP} = \frac{2.83 \times 10^{5}}{R_{COMP}} \ (F)$$

If RCOMP is limited to 15kΩ, then the actual cross over frequency is 6.58 / (VOUTCOUT). Therefore:

$$C_{COMP} = 6.45 \times 10^{-6} V_{OUT} C_{OUT} \ (F)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor CCOMP2 is required. The condition for using CCOMP2 is:

$$R_{ESRCOUT} \geq \left(Min \frac{1.77 \times 10^{-6}}{C_{OUT}}, 0.006 \times V_{OUT} \right) (\Omega)$$

And the proper value for CCOMP2 is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}}$$

Though CCOMP2 is unnecessary when the output capacitor has sufficiently low ESR, a small value CCOMP2 such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1:
Typical Compensation for Different Output Voltages and Output Capacitors

VOUT	COUT	RCOMP	CCOMP	CCOMP2①
3.3V	47uF Ceramic CAP	10KΩ	4.7nF	None
5.0V	47uF Ceramic CAP	10KΩ	4.7nF	None
3.3V	220uF/10V/30mΩ	10KΩ	4.7nF	None
5.0V	220uF/10V/30mΩ	10KΩ	4.7nF	None

CC Loop Stability

The constant-current control loop is internally compensated over the 1500mA-3000mA output range. No additional external compensation is required to stabilize the CC current.

Output Cable Voltage-Drop Compensation

To compensate for resistive voltage drop across the charger's output cable, the AP2960 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 7 to choose the proper feedback resistance values for cable compensation. RFB1 is the high side resistor of voltage divider.

In the case of high RFB1 used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 8, adding a capacitor in paralleled with RFB1 or increasing the compensation capacitance at COMP pin helps the system stability.

Figure 7:
Cable Voltage-Drop Compensation at Various Resistor Divider Values

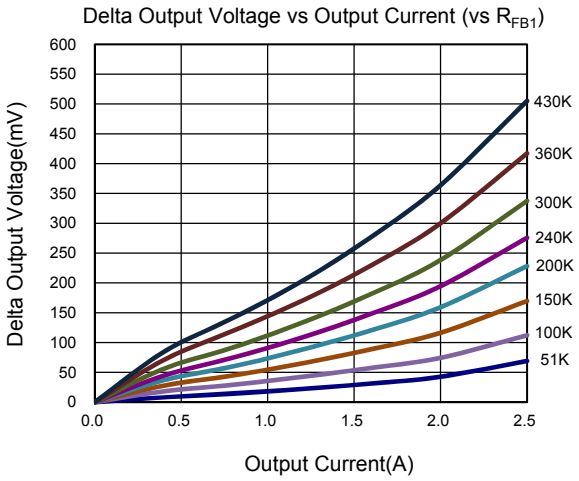
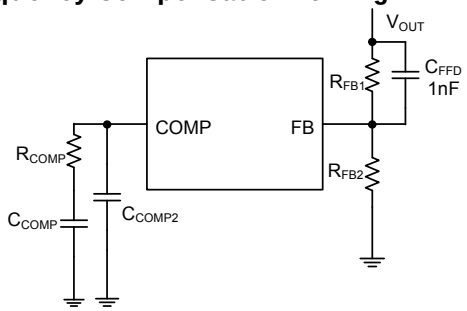


Figure 8:
Frequency Compensation for High RFB1

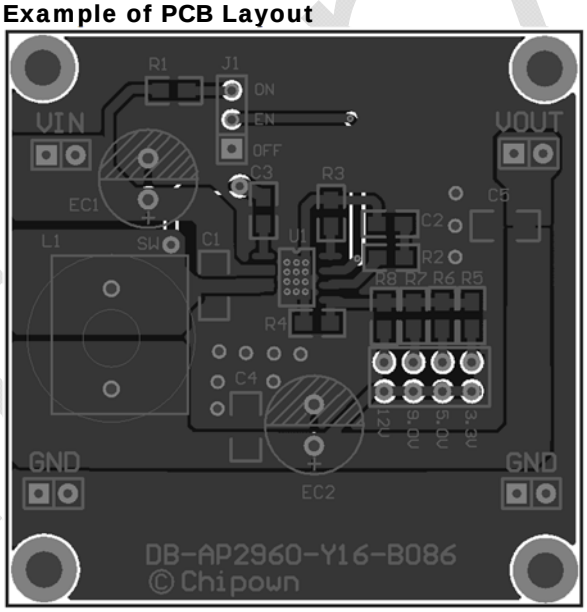


PC Board Layout Guidance

Figure 9 showed the example of components placement and PCB layout. When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

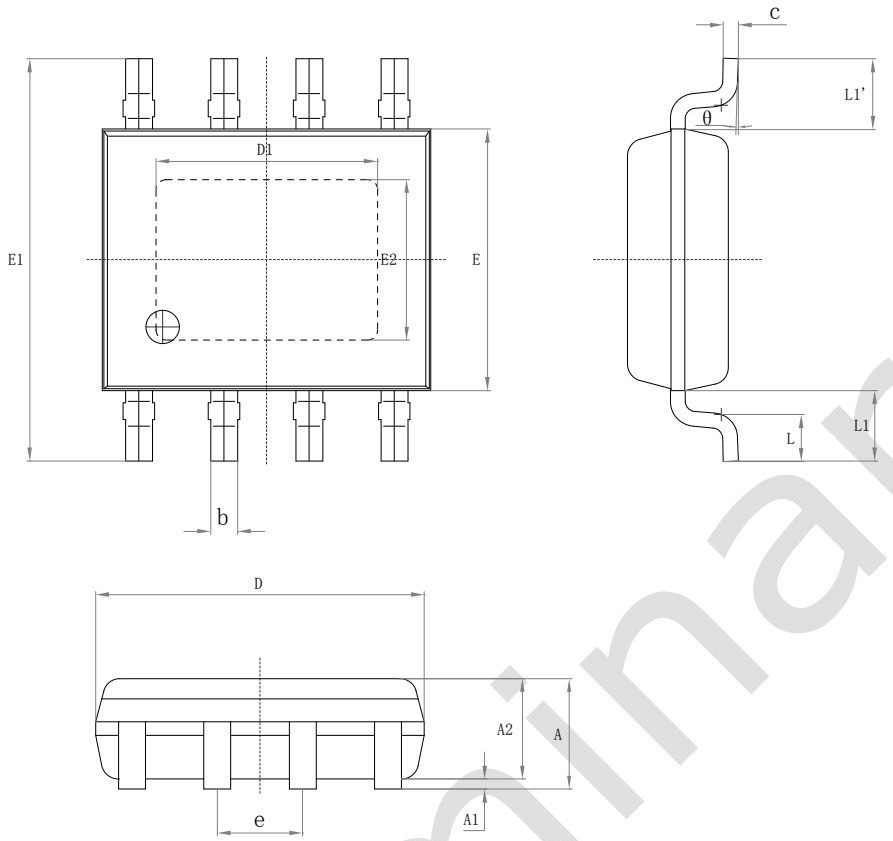
1) Arrange the power components to reduce the AC loop size, consisting of input ceramic capacitor C1, VIN pin, SW pin .
2) Place input decoupling ceramic capacitor C1 as close to VIN pin as possible. C1 is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting BS-C3-SW loop.

Figure 9:
Example of PCB Layout



Package Information

SOP8-EP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.700	0.055	0.067
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
L1	1.04REF		0.041REF	
L1-L1'	----	0.12	----	0.005
θ	0°	8°	0°	8°

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