GENERAL DESCRIPTION

HG9942 is a high performance offline PSR controller for low power AC/DC charger and adapter applications. It operates in primary-side sensing and regulation. Consequently, opto-coupler and TL431 could be eliminated. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below.

In CC control, the current and output power setting can be adjusted externally by the sense resistor Rs at CS pin. In CV control, PFM operations are utilized to achieve high performance and high efficiency. In addition, good load regulation is achieved by the built-in cable drop compensation. The chip consumes very low operation current (typical 400uA), it can achieve low standby power and high efficiency.

HG9942 offers comprehensive protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD over voltage protection, feedback loop open protection, short circuit protection, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

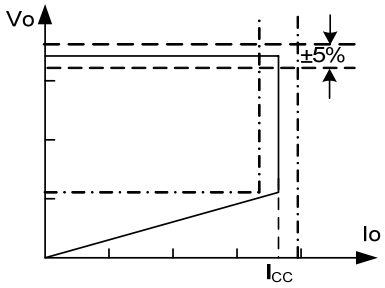


Figure.1. Typical CC/CV Curve

FEATURES

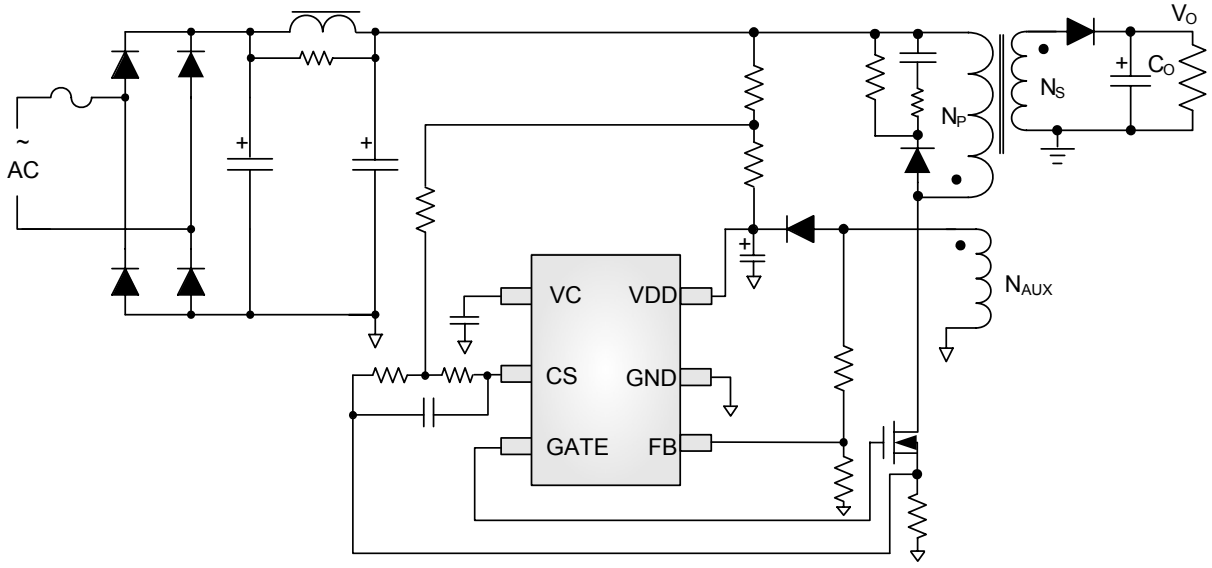
- ±5% Constant Voltage Regulation at Universal AC input
- High precision Constant Current Regulation at Universal AC input
- Primary-side Sensing and Regulation Without TL431 and Opto-coupler
- Programmable CV and CC Regulation
- Built-in Primary winding inductance compensation
- Programmable Cable Drop Compensation
- Ultra Low Start-up Current (Typ. 1uA)
- VDD Over Voltage Protection
- Built-in Feedback Loop Open Protection
- Built-in Short Circuit Protection
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)

APPLICATIONS

Low Power AC/DC offline SMPS for

- Mini-charger/Adapter
- Cell Phone Charger
- Digital Cameras Charger
- Linear Regulator/RCC Replacement

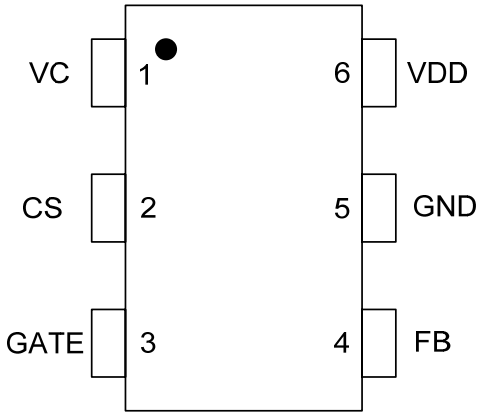
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for SOT23-6.



Package Dissipation Rating

Package	RθJA (℃/W)
SOT23-6	200

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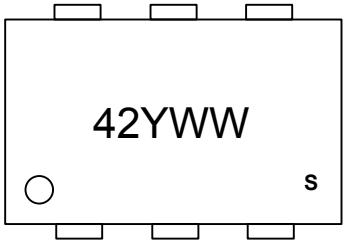
Absolute Maximum Ratings

Parameter	Value
VDD Voltage	-0.3 to 30V
VC Voltage	-0.3 to 7V
GATE Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Marking Information

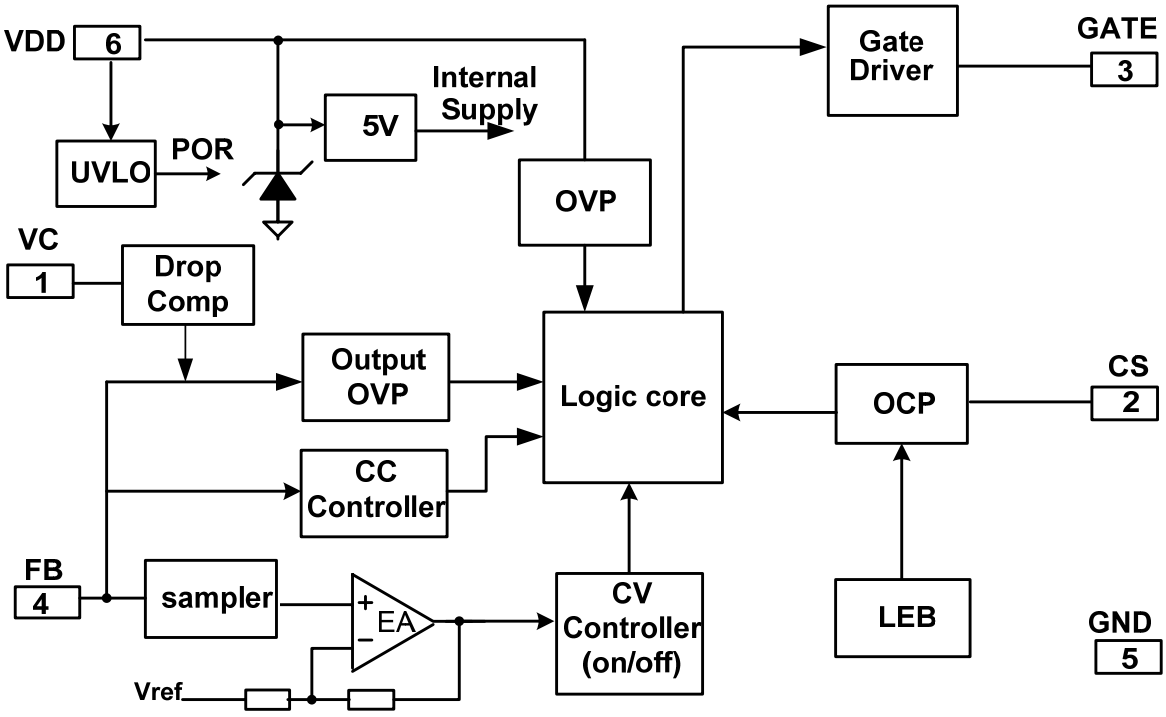


Y: Year Code
WW: Week Code(01-52)
S: Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	VC	I	Low pass filter capacitor for cable compensation
2	CS	I	Current sense input.
3	GATE	O	Gate drive output for power MOSFET.
4	FB	I	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
5	GND	P	Ground
6	VDD	P	Power Supply

BLOCK DIAGRAM

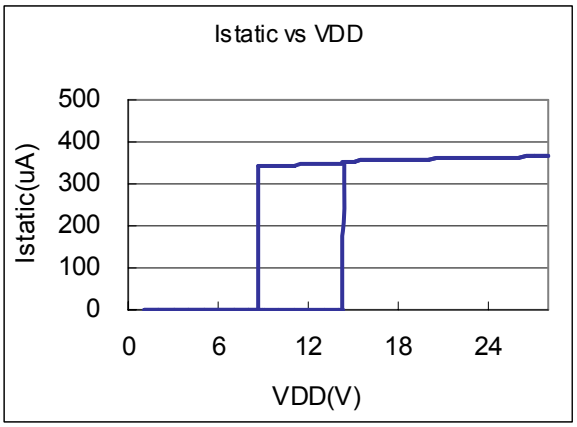


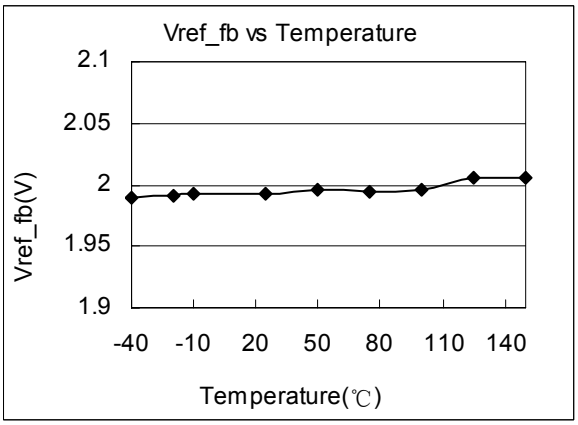
ELECTRICAL CHARACTERISTICS

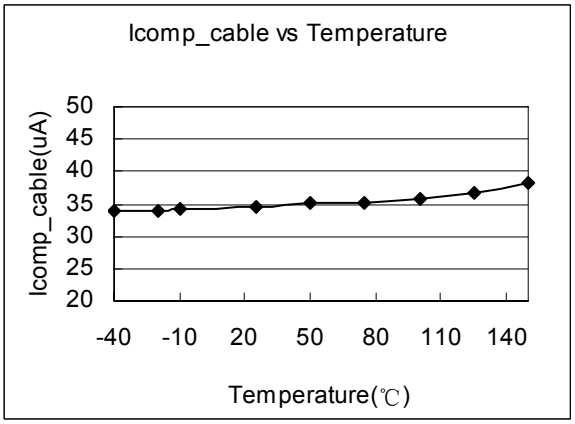
(TA = 25℃, VDD=15V, if not otherwise noted)

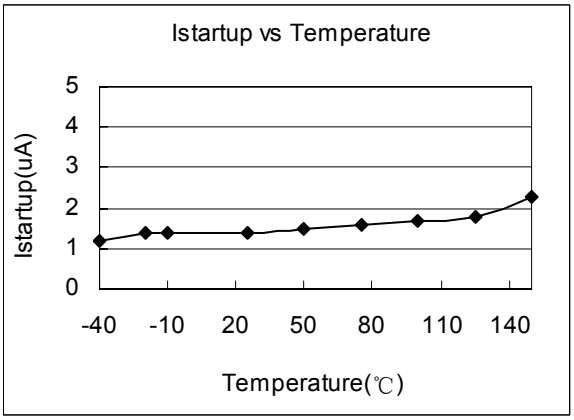
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
$I_{start-up}$	Start up current	VDD=13.8V		1	3	uA
I_{static}	Static current	VDD=15V		400	500	uA
UVLO(OFF)	VDD under voltage lockout exit		13.8	14.8	15.8	V
UVLO(ON)	VDD under voltage lockout enter		8.0	9.0	10.0	V
VDD_OVP	VDD over voltage protection		25	27	29	V
Max. Operating Voltage					25	V
Current Sense Input Section						
TLEB	LEB time			350		nS
Vth_ocp	Over current threshold		485	500	515	mV
Td_oc	OCP propagation delay	From ocp comparator to gate drive		100		nS
Ics_max	Maximum source current to CS pin		33.5	37	40.5	uA
FB Input Section						
Vref_fb	Reference voltage for feedback threshold		1.98	2.00	2.02	V
Tpause_min	Minimum pause			1.0		uS
Tpause_max	Maximum pause		360	400	440	uS
Icomp_cable	Maximum cable compensation current		22	25	28	uA
GATE Drive Section						
Tr	Output rising time	CL=0.47nF		300		nS
Tf	Output falling time	CL=0.47nF		25		nS
V_clamp	Output clamp voltage level			10		V

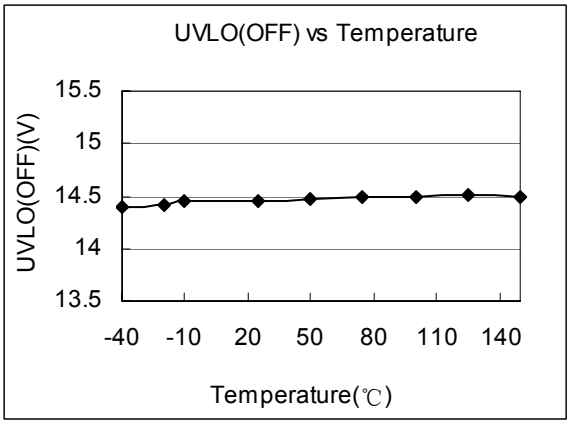
CHARACTERIZATION PLOTS

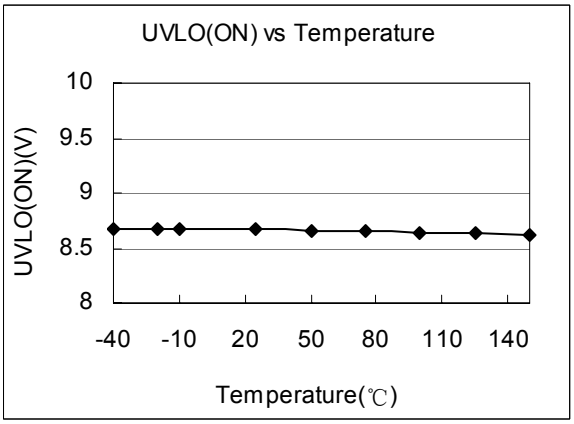












OPERATION DESCRIPTION

HG9942 is a cost effective PSR controller optimized for off-line low power AC/DC applications including battery chargers. It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger application requirements.

- **Startup Current and Start up Control**

Startup current of HG9942 is designed to be very low so that VDD could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

- **Operating Current**

The Operating current of HG9942 is as low as 400uA. Good efficiency and very low standby power is achieved with the low operating current.

- **CC/CV Operation**

HG9942 is designed to produce good CC/CV control characteristic as shown in the Figure. 1. In charger applications, a discharged battery charging starts in the CC portion of the curve until it is nearly full charged and smoothly switches to operate in CV portion of the curve. The CC portion provides output current limiting. In CV operation, the output voltage is regulated through the primary side control. In CC operation mode, HG9942 will regulate the output current constant regardless of the output voltage.

- **Principle of Operation**

To support HG9942 proprietary CC/CV control, system needs to be designed in DCM mode for flyback system (Refer to Typical Application Diagram on page1).

In the DCM flyback converter, the output voltage can be sensed via the auxiliary winding. During power MOSFET turn-on time, the load current is supplied from the output filter capacitor, Co. The current in the primary winding ramps up. When power MOSFET turns off, the energy stored in the primary winding is transfered to the secondary side such that the current in the secondary winding is

$$I_S = \frac{N_P}{N_S} \cdot I_P \qquad (1)$$

The auxiliary voltage reflects the output voltage as shown in Figure.2 and it is given by

$$V_{AUX} = \frac{N_{AUX}}{N_S} \cdot (V_O + \Delta V) \qquad (2)$$

Where ΔV indicates the drop voltage of the output Diode.

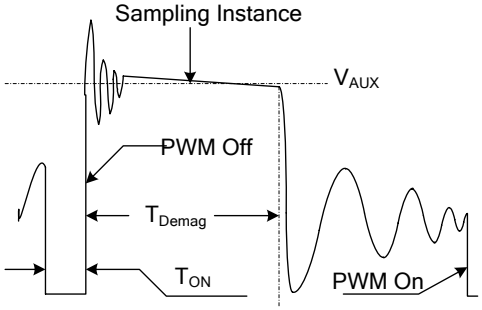


Figure.2. Auxiliary voltage waveform

Via a resistor divider connected between the auxiliary winding and FB (pin 4), the auxiliary voltage is sampled at the middle of the de-magnetization and it is hold until the next sampling. The sampled voltage is compared with Vref (2.0V) and the error is amplified. The error amplifier output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

When the sampled voltage is below Vref and the error amplifier output reaches its minimum, the switching frequency is controlled by the sampled voltage to regulate the output current, thus the constant output current can be achieved.

- **Adjustable CC point and Output Power**

In HG9942, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in typical application diagram. The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Figure.3.

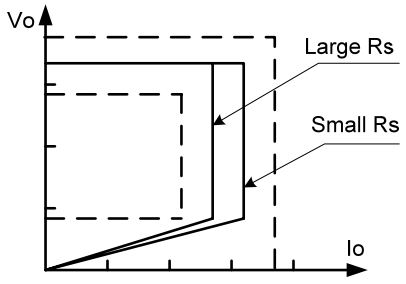


Figure.3. Adjustable output power by changing Rs

- **Operation switching frequency**

The switching frequency of HG9942 is adaptively controlled according to the load conditions and the operation modes.

For flyback operating in DCM, The maximum output power is given by

$$Po_{MAX} = \frac{1}{2} L_P F_{SW} I_p^2 \quad (3)$$

Where Lp indicate the inductance of primary winding and Ip is the peak current of primary winding.
Refer to the equation 3, the change of the primary winding inductance results in the change of the maximum output power and the constant output current in CC mode. To compensate the change from variations of primary winding inductance, the switching frequency is locked by an internal loop such that the switching frequency is

$$F_{SW} = \frac{1}{2T_{Demag}} \quad (4)$$

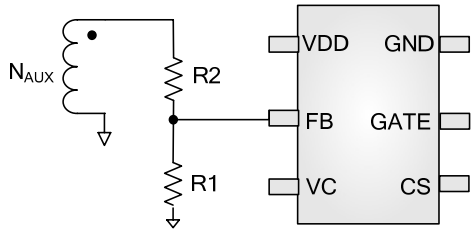
Since T_{Demag} is inversely proportional to the inductance, as a result, the product *Lp* and *fsw* is constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to $\pm$7% variation of the primary winding inductance can be compensated.

● Programmable Cable drop Compensation
In HG9942, cable drop compensation is implemented to achieve good load regulation. An offset voltage is generated at FB pin by an internal current flowing into the resister divider. The current is proportional to the switching off time, as a result, it is inversely proportional to the output load current, thus the drop due to the cable loss can be compensated. As the load current decreases from full-load to no-load, the offset voltage at FB will increase. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.
The percentage of maximum compensation is

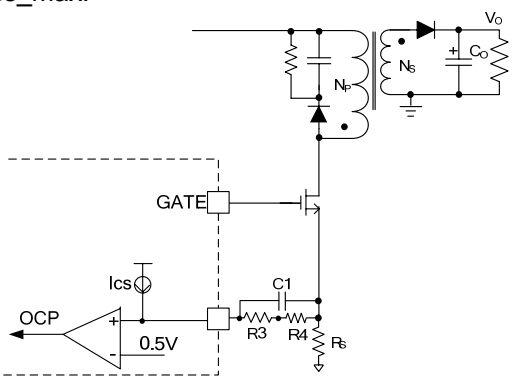
$$\frac{\Delta V}{Vout} = \frac{Icomp\_cable \times (R1 // R2) \times 10^{-6}}{2} \times 100\%$$

ΔV is load compensation voltage and Vout is output voltage;
For example:R1=6Kohm,R2=24Kohm,the percentage of maximum compensation is

$$\frac{\Delta V}{Vout} = \frac{25 \times (6000 // 24000) \times 10^{-6}}{2} \times 100\% = 6\%$$



● CS modulation to improve dynamic response
At light or no load, an internal current Ics is flowing into CS pin; the current Ics is modulated with the output loading, the maximum current Ics is limited to Ics_max.



At no load, the actual CS threshold is

$$Vcsth\_no\_load = 0.5 - (Ics\_\max) \times (R3 + R4) \quad (V)$$

Above Vcsth_no_load is not considered AC line compensation.

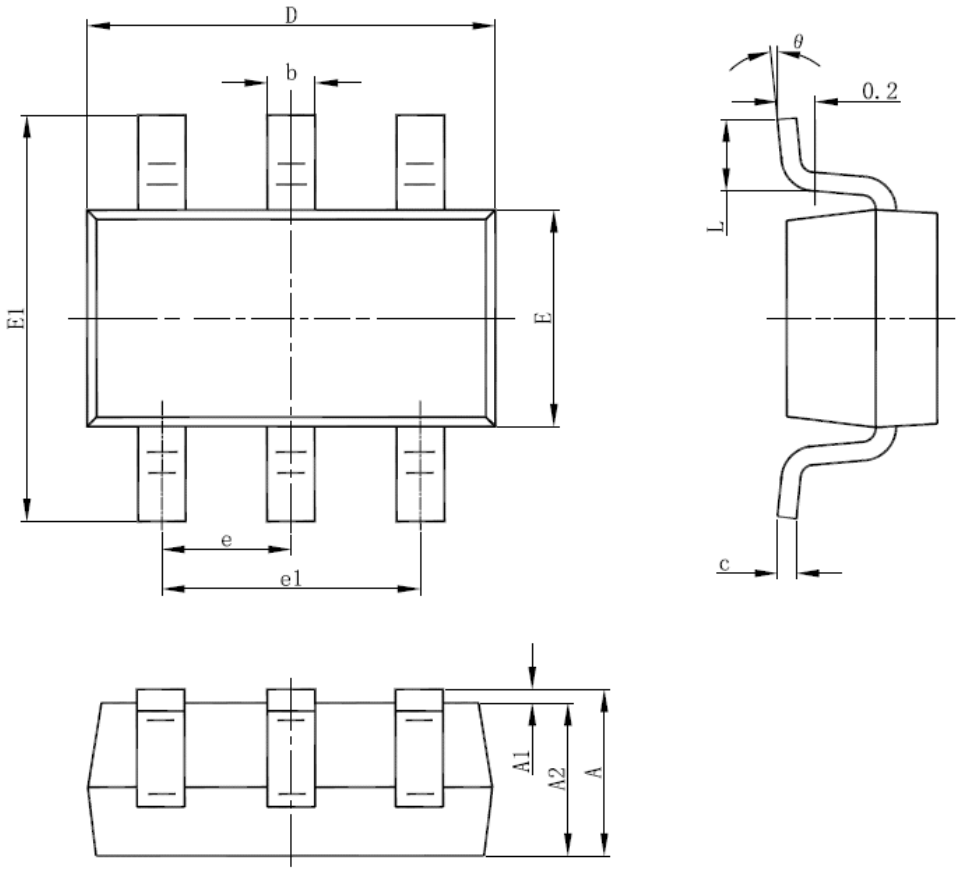
● Current Sensing and Leading Edge Blanking
Cycle-by-Cycle current limiting is offered in HG9942.The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state so that the external RC filtering on sense input is no longer needed.

● Gate Drive
The GATE pin is connected to the gate of an external power switch. An internal 10V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the GATE pin is internally pull low to maintain the off state.

● Protection Control
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), VDD over voltage protection, feedback loop open protection, short circuit protection and Under Voltage Lockout on VDD (UVLO).
VDD is supplied by transformer auxiliary winding output. The output of HG9942 is shut down when VDD drops below UVLO (ON) and the power converter enters power on start-up sequence thereafter.

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°