Design Example Report

Title	*18 W USB-PD Power Supply Using Weltrend WT6630P and InnoSwitch™-CP INN2215K*
Specification	90 VAC – 264 VAC Input; 5 V, 3 A; 9 V, 2 A Outputs
Application	Mobile Phone Charger
Author	Applications Engineering Department
Document Number	DER-567
Date	April 19, 2017
Revision	1.1

Summary and Features

- InnoSwitch-CP industry first AC/DC IC with isolated, safety rated integrated feedback
- USB-PD compliance via single secondary side IC (Weltrend WT6630P)
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Built in synchronous rectification for high efficiency
- Meets DOE6 and CoC V5 2016 at the end of cable (cable impedance ≤100 mΩ)
- <30 mW no-load input power
- >84.9% efficiency for 9 V, 2 A for all line conditions
- >87 % efficiency for 9 V, 2 A and 230 VAC input
- >8% CoC Tier 2 efficiency margin for 10% load
- Integrated thermal protection
- Primary sensed overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 5 V, 3 A or 9 V, 2 A output USB Type-C and USB-PD charger using the InnoSwitch-CP and Weltrend WT6630P USB Type-C USB-PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch-CP controller providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data

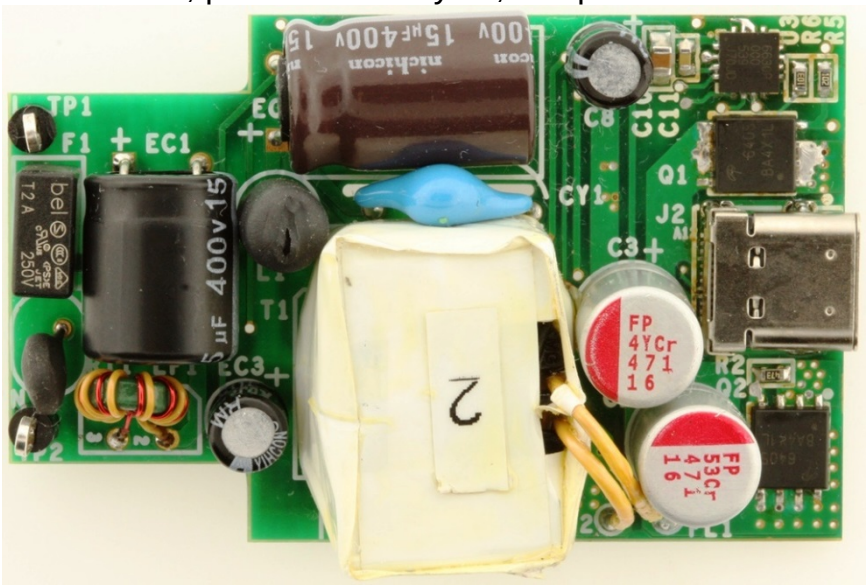

Figure 1 – Populated Circuit Board Photograph, Top.

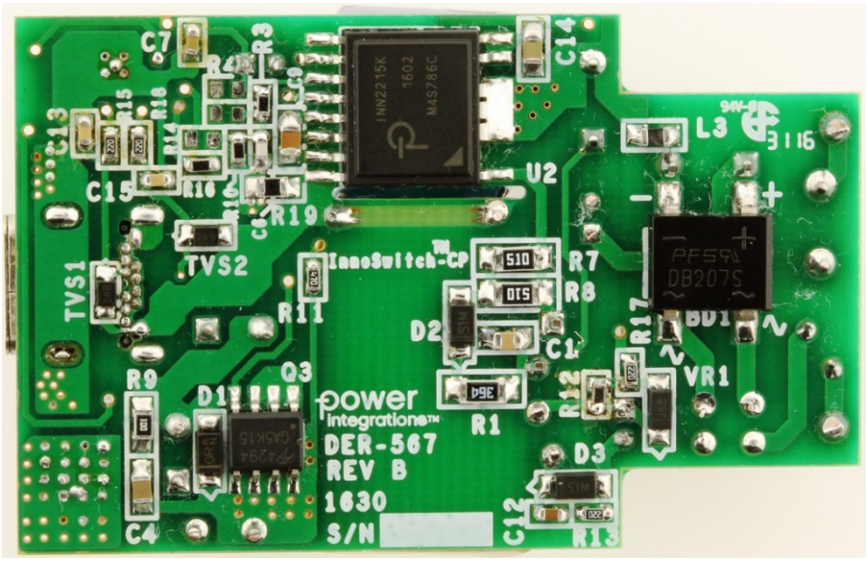

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)			25	28	mW	Measured at 230 VAC.
5 V Output						
Output Voltage	V_{OUT}		5		V	±3%
Output Ripple Voltage	V_{RIPPLE}			150	mV	End of Cable. Cable Needs to Have a Resistance of 100 mΩ.
Output Current	I_{OUT}	3			A	20 MHz Bandwidth.
Efficiency (Full Load)	η	80%				115 VAC, 230 VAC.
Efficiency (Average)	η	83%				Average Measured at End of 100 mΩ Cable for 115 and 230 VAC.
Efficiency (10% Load)	η	87%				
9 V Output						
Output Voltage	V_{OUT}		9		V	±5%
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of Cable. Cable Needs to Have a Resistance of 100 mΩ.
Output Current	I_{OUT}	2			A	At End of Cable. Cable Needs to Have a Resistance of 100 mΩ.
Efficiency (Full Load)		86%				115 VAC, 230 VAC.
Efficiency (Average)		87%				Average Measured at End of 100 mΩ Cable for 115 and 230 VAC.
Efficiency (10% Load)	η	84%				
Continuous Output Power	P_{OUT}			18	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

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3 Schematic

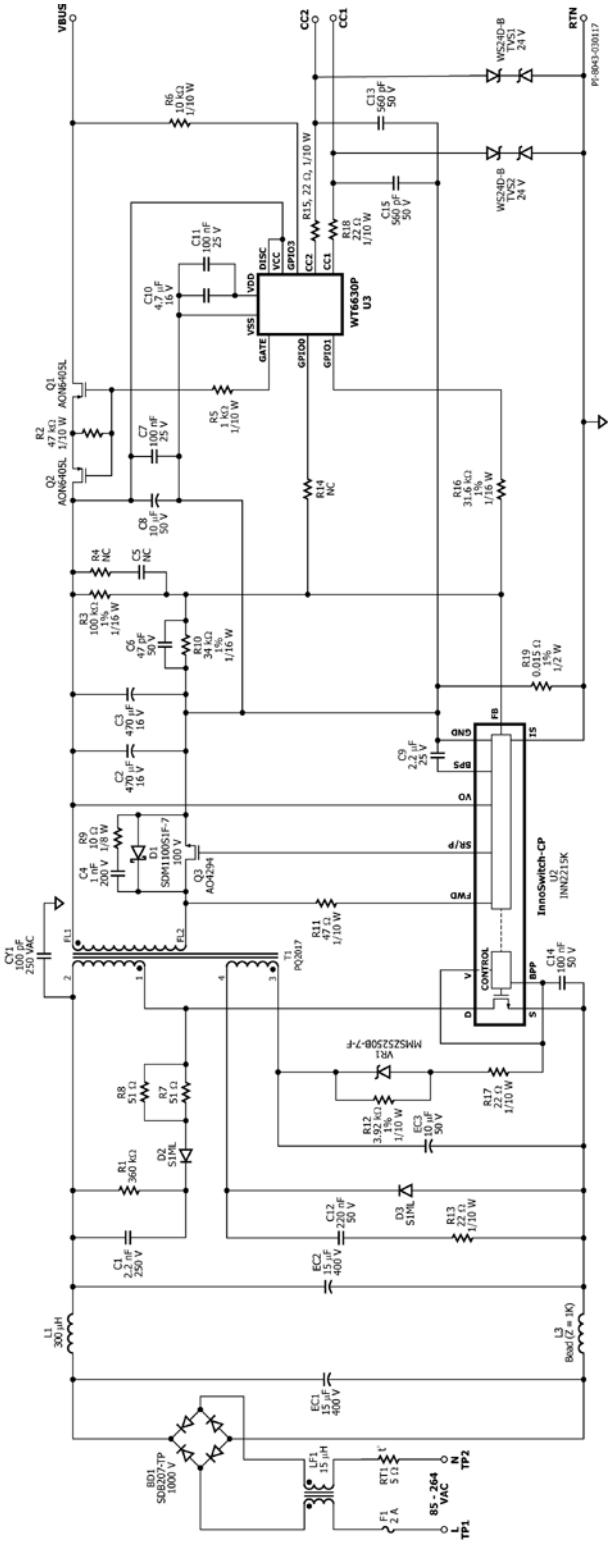

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Common mode choke LF1 provides attenuation for EMI. Bridge rectifier BD1 rectifies the AC line voltage and provides a full wave rectified DC. The inductor L1, L3 and capacitors EC1, EC2 form a pi-filter. This filter provides differential and common mode noise filtering. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection from component failure.

4.2 **InnoSwitch-CP IC Primary**

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the InnoSwitch-CP IC (U2).

A low cost RCD clamp formed by diode D2, resistors R1, R7 and R8, and capacitor C1 limits the peak Drain voltage of U2 at the instant of turn off of the MOSFET inside U2. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS (BPP) pin capacitor (C14) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D3 and filtered using capacitor EC3. Resistor R12 and R17 limit the current being supplied to the BPP pin of the InnoSwitch-CP IC (U2). The Zener VR1 along with resistor R17 provides latching OVP for output over voltage condition. The RC network comprising of resistor R13 and capacitor C12 offer damping to the high frequency ringing in the voltage across diode D3 which reduces radiated EMI.

Output regulation is achieved using on/off control, the number of enabled switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled, and at light load or no-load most cycles are disabled or skipped. Once a cycle is enabled, the MOSFET will remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arranged such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch-CP IC U2. If the current flowing into the BPP pin increases above the I_{SD}

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threshold which has a nominal value of 7.6 mA, the InnoSwitch-CP controller will latch off and prevent any further increase in output voltage.

4.3 InnoSwitch-CP IC Secondary

The secondary side of the InnoSwitch-CP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q3 and filtered by capacitors C2 and C3. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R9 and C4.

The gate of Q3 is turned on by secondary side controller inside IC U2, based on the winding voltage sensed via resistor R11 and fed into the FORWARD (FWD) pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 24 mV. Secondary side control of the primary side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9 connected to the SECONDARY BYPASS (BPS) pin of InnoSwitch-CP IC U2 provides decoupling for the internal circuitry.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C9 via resistor R11 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R19 between the ISENSE (IS) and SECONDARY GROUND (GND) pins with a threshold of approximately 50 mV to reduce losses. Once the internal current sense threshold is exceeded the device adjusts the number of switch pulses to maintain a fixed output current.

Below the CC threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve a voltage of 1.265 V on the FEEDBACK (FB) pin. Capacitor C6 provides noise filtering of the signal at the FB pin.

4.4 USB Type-C and PD Interface

In this design, Weltrend WT6630P (U3) is the USB Type-C and PD controller. Output of the InnoSwitch-CP based flyback power converter stage powers the Weltrend device through its VCC pin.

Resistor R6 senses the output of flyback power stage secondary side to provide voltage feedback to the PD controller. Output voltage is changed to 9 V when sink requests for the same. To change the output to 9 V, pin 5 of IC U3 goes low and adds resistor R16 in parallel to the bottom resistor of the feedback divider network.

USB-PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

P-MOSFETS Q1 and Q2 make the USB Type-C receptacle a cold socket when no device is attached to the charger as per the USB Type-C specification.

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5 PCB Layout

PCB copper thickness is 2.0 oz.

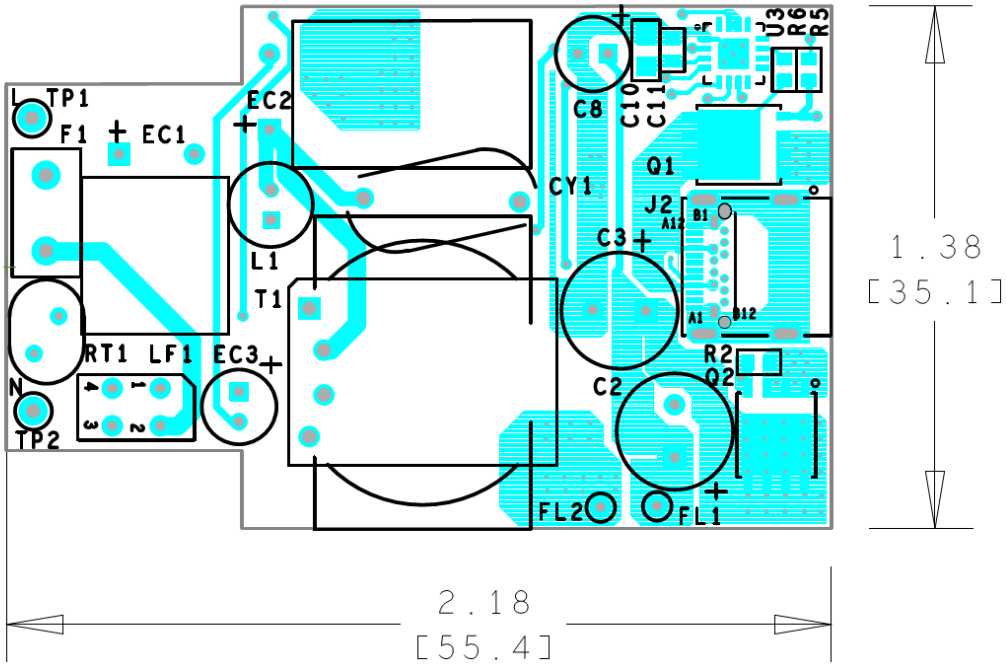

Figure 4 – Printed Circuit Layout, Top.

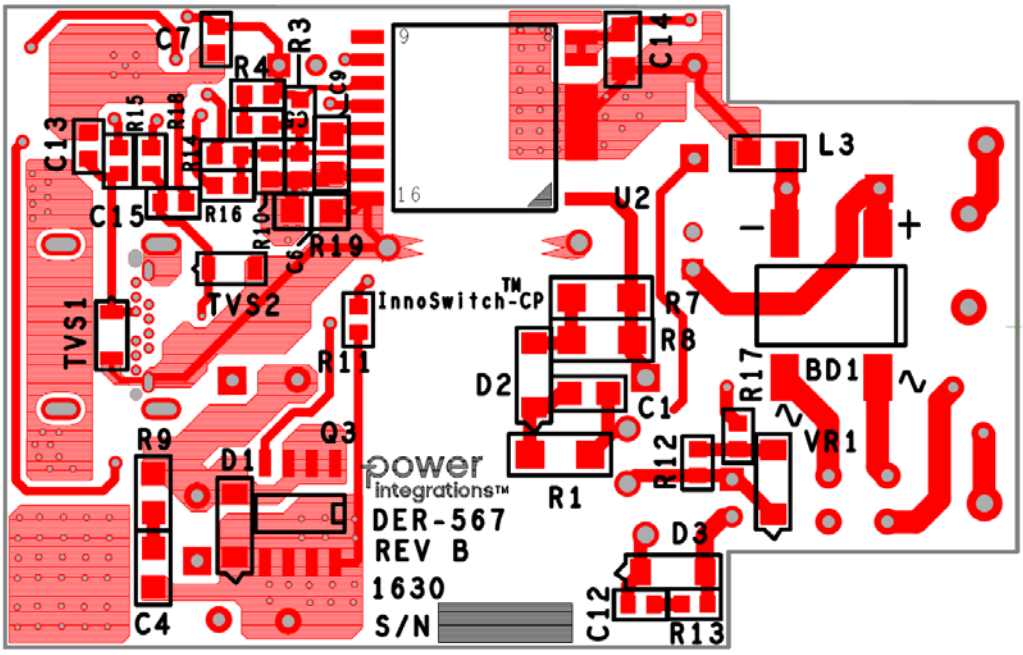

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BD1	DIODE, BRIDGE, GPP, 2A, 1000V, SDB-1	SDB207-TP	Micro Commercial
2	1	C1	2.2 nF, 250 V, Ceramic, X7R, 0805	C2012X7R2E222K085AA	TDK
3	1	C2	470 µF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
4	1	C3	470 µF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
5	1	C4	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
6	1	C5	No Connect. 47 pF, 50 V, Ceramic, C0G, NP0, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	C0603C470F5GACTU	Kemet
7	1	C6	47 pF, 50 V, Ceramic, C0G, NP0, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	C0603C470F5GACTU	Kemet
8	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
9	1	C8	10 µF, 50 V, Electrolytic, Gen. Purpose, (4 x 7)		
10	1	C9	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	1	C10	4.7 µF, 16 V, Ceramic, X7R, 0805	GRM21BR71C475KA73L	Murata
12	1	C11	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
13	1	C12	220 nF 50 V, Ceramic, X7R, 0603	CGA3E3X7R1H224K	TDK
14	1	C13	560 pF, 50 V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B561KB8NNNC	Samsung
15	1	C14	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
16	1	C15	560 pF, 50 V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B561KB8NNNC	Samsung
17	1	CY1	100 pF, 250 VAC, Film, X1Y1	DE1B3KX101KB4BN01F	TDK
18	1	D1	Diode, SCHOTTKY, 100 V, 1A, SOD123F	SDM1100S1F-7	Diodes, Inc.
19	1	D2	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
20	1	D3	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
21	1	EC1	15 µF, 400 V, Electrolytic, (10 x 12)	ERK2GM150G12OT	AISHI
22	1	EC2	15 µF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
23	1	EC3	10 µF, 50 V, Electrolytic, Gen. Purpose, (4 x 7)		
24	1	F1	2 A, 250V, Slow, Long Time Lag,RST	RST 2	Belfuse
25	1	FL1	Flying Lead , Hole size 30mils	N/A	N/A
26	1	FL2	Flying Lead , Hole size 30mils	N/A	N/A
27	1	J2	USB 3.1 CF STD CL1. 75- H3.45mm type 1.20mm	A32-0XS1-X12	Chinese
28	1	L1	300 µH, I-Core, 5 x 7, Custom wound	30-00444-00	Power Integrations
29	1	L3	Ferrite Bead, 1 kΩ Impedance, 0805 (2012 Metric), Surface Mount, 300 mA, 1 Lines, 400 mΩ Max DCR, -55°C ~ 125°C	BK2125HS102-T	Taiyo Yuden
30	1	LF1	15 µH	32-00340-00	Power Integrations
31	1	Q1	MOSFET, P-CH, 30 V, 15 A, 8DFN	AON6405L	Alpha & Omega Semiconductor
32	1	Q2	MOSFET, P-CH, 30 V, 15 A, 8DFN	AON6405L	Alpha & Omega Semiconductor
33	1	Q3	MOSFET, N-CH, 100 V, 11.5 A, 8SOIC,	AO4294	Alpha & Omega Semiconductor
34	1	R1	RES, 360 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ364V	Panasonic
35	1	R2	RES, 47 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
36	1	R3	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
37	1	R4	No Connect. RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
38	1	R5	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
39	1	R6	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
40	1	R7	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
41	1	R8	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
42	1	R9	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
43	1	R10	RES, 34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
44	1	R11	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic

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45	1	R12	RES, 3.92 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3921V	Panasonic
46	1	R13	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
47	1	R14	No Connect. RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
48	1	R15	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
49	1	R16	RES, 31.6 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3162V	Panasonic
50	1	R17	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
51	1	R18	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
52	1	R19	RES, 0.015 Ω, 0.5 W, 1%, 0805	ERJ-6BWFR015V	Panasonic
53	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
54	1	T1	Custom Transformer, PQ2017,Horizontal, 6 pins	PQ2017B	Shenzen MI GE
55	1	TP1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
56	1	TP2	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
57	1	TVS1	Diode, TVS, 500 W, 24 V, <1 nS, 5%, SOD-323	WS24D-B	CYG WAYON
58	1	TVS2	Diode, TVS, 500 W, 24 V, <1 nS, 5%, SOD-323	WS24D-B	CYG WAYON
59	1	U2	InnoSwitch-CP,INN2215K,Off-Line_CV/CC_Flyback_Switcher,ReSOP-16B	INN2215K	Power Integrations
60	1	U3	IC, USB PD Controller, 16-QFN	WT6630P	Weltrend
61	1	VR1	Diode ZENER 20 V 500 MW SOD123	MMSZ5250B-7-F	Diodes, Inc.

7 Transformer Specification

7.1 *Electrical Diagram*

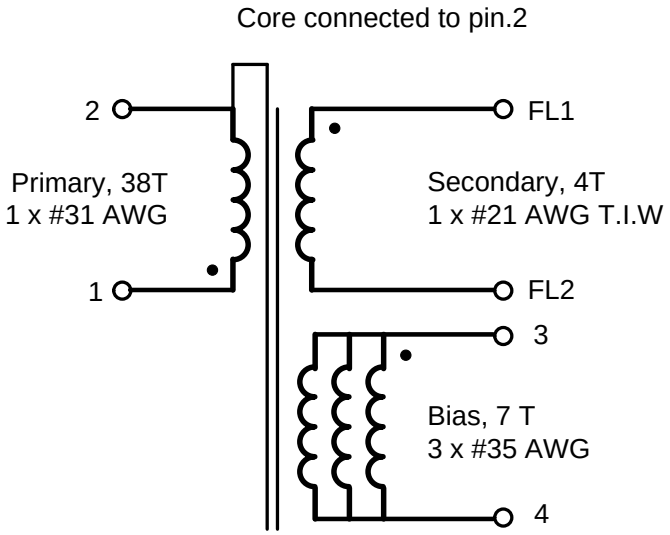

Figure 6 –Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-2 to leads FL1-FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 0.4 V_{RMS}.	583 µH, ±7%
Resonant Frequency	Pins 1-2, all other open.	1,100 kHz (Min.)
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured 100 kHz, 0.4 V_{RMS}.	16 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: PQ2017, TP4; or Equivalent. Gapped ALG: 415nH/T².
[2]	Bobbin: PQ2017, Vertical, 6 pins (4/2), PI#: 25-01092-00; or Equivalent.
[3]	Magnet Wire: #31 AWG, Double Coated.
[4]	Magnet Wire: #35 AWG, Double Coated.
[5]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[6]	Bus Wire: #26 AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 4.0 mm Wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 15.0mm wide.
[9]	Varnish: Dolph BC-359; or Equivalent.

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7.4 *Transformer Build Diagram*

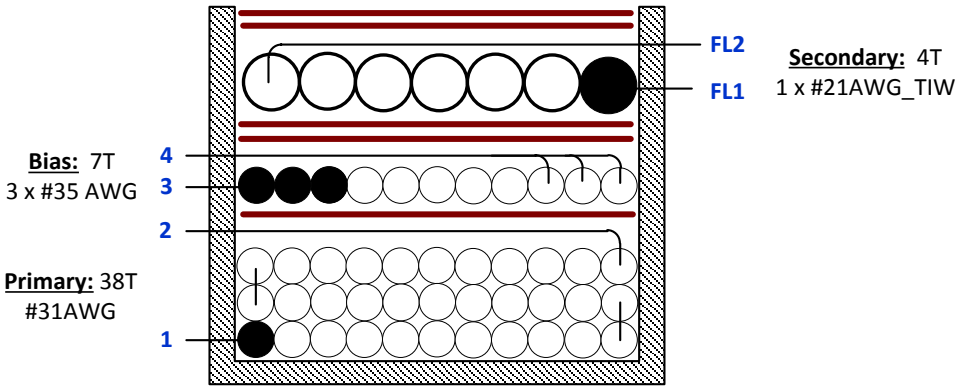
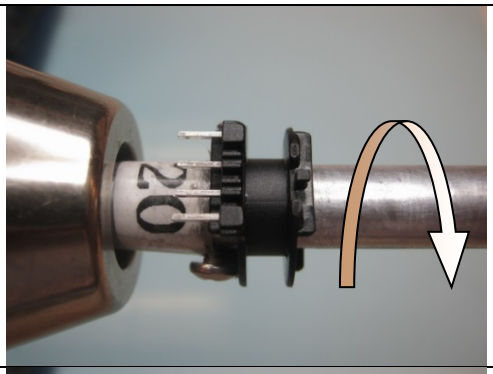
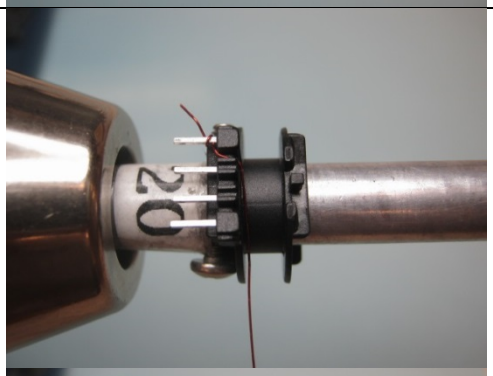
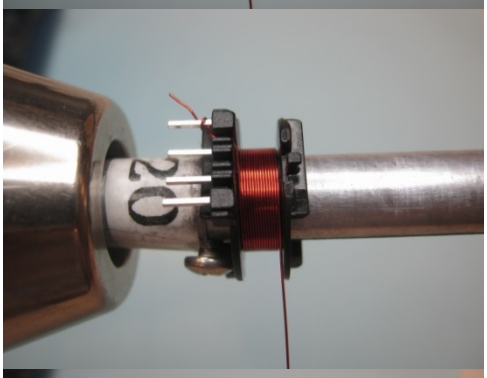
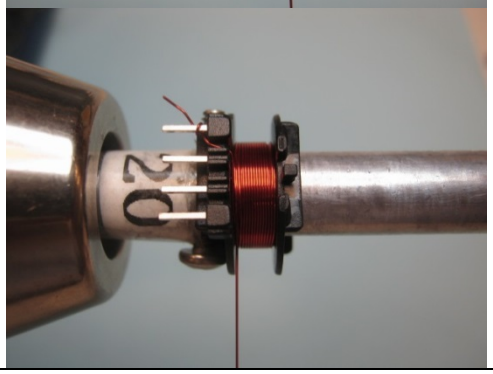


Figure 7 – Transformer Build Diagram.

7.5 *Transformer Construction*

Winding Preparation	Position the bobbin item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 Primary	Start at pin 1, wind 38 turns of wire item [3] in 3 layers, with tight tension, and finish at pin 2. (note: spread wire evenly across the bobbin for 3rd layer).
Insulation	1 layer of tape item [7].
WD2 Bias	Start at pin 3, use 3 wires item [4], wind 7 turns in 1 layer, and finish at pin 4.
Insulation	2 layers of tape item [7].
WD3 Secondary	Start from the right (top of bobbin) with wire item [5], leave ~ 1” floating as FL1, wind 4 turns from right to left. At the last turn bring the wire back to the right (top of bobbin) and also leave ~ 1” floating as FL2.
Insulation	2 layers of tape item [7] to secure the windings and for insulation.
Finish	Gap cores to get 583 µH. Solder 1” of bus wire item [6] with pin 2 and lean along with 2 cores (see illustration below). Wrap cores and this bus wire with tape. Wrap around front to back of transformer with 2 layers of tape item [8], and also wrap around top to bottom with 2 layers of tape item [8] (see illustration below) Varnish with item [9].

7.6 *Transformer Winding Illustrations*

Winding Preparation		Position the bobbin item [2] on the mandrel with pin side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 Primary	  	Start at pin 1, wind 38 turns of wire item [3] in 3 layers, with tight tension, and finish at pin 2. (Note: spread wire evenly across the bobbin for 3rd layer).

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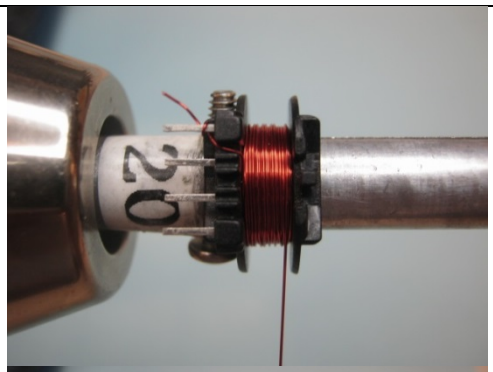
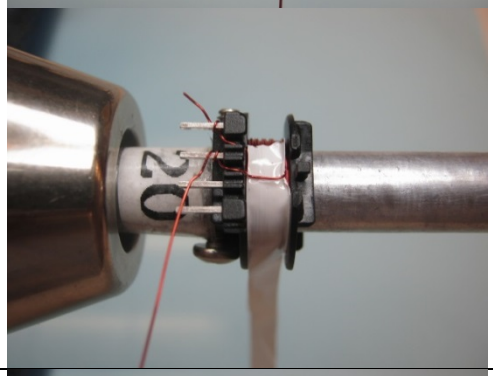
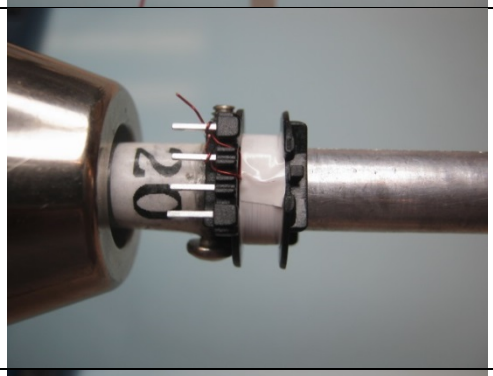
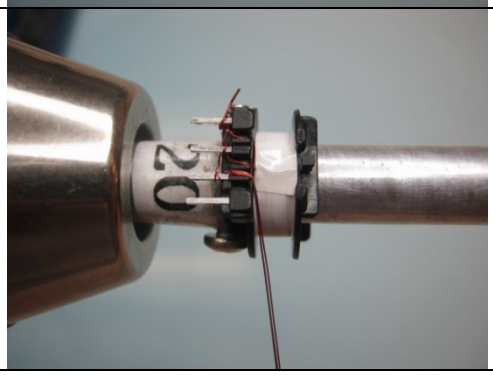
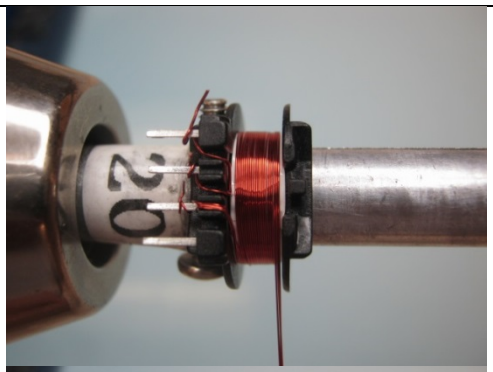
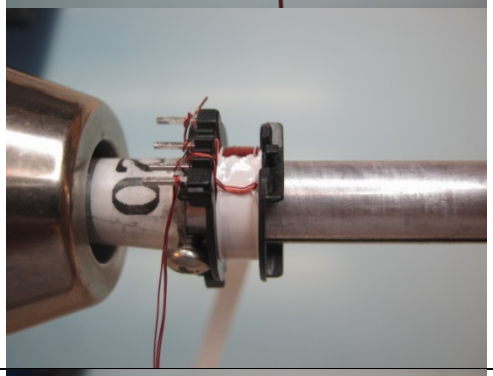
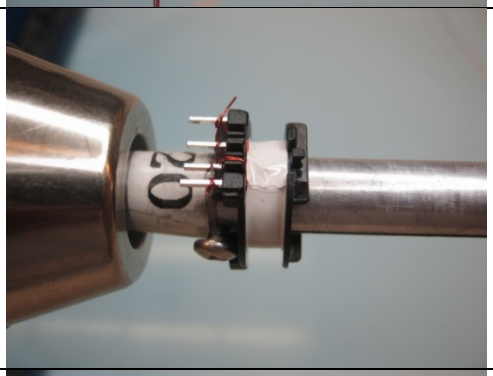
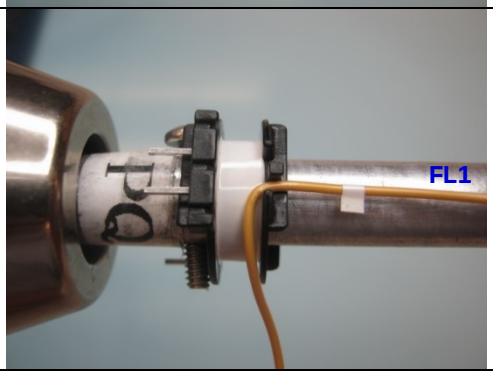
	 	
Insulation		1 layer of tape item [7].
WD2 Bias		Start at pin 3, use 3 wires item [4], wind 7 turns in 1 layer, and finish at pin 4.

	 	
Insulation		2 layer of tape item [7].
WD3 Secondary		Start from the right (top of bobbin) with wire item [5], leave ~ 1” floating as FL1, wind 4 turns from right to left. At the last turn bring the wire back to the right (top of bobbin) and also leave ~ 1” floating as FL2.

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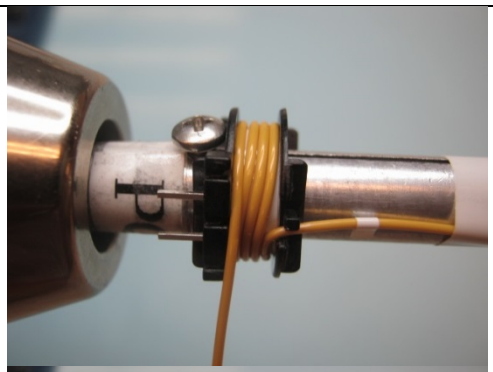
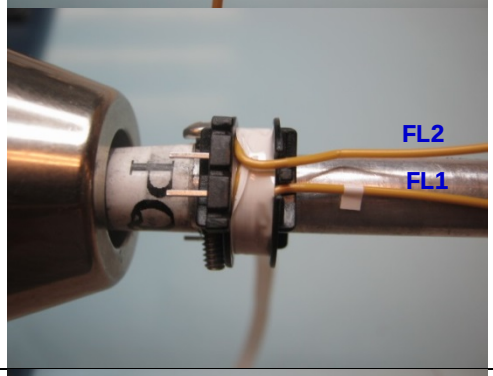
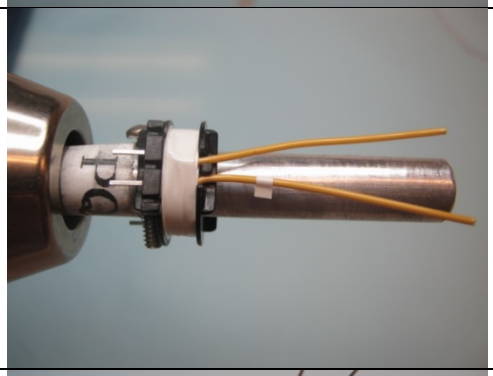
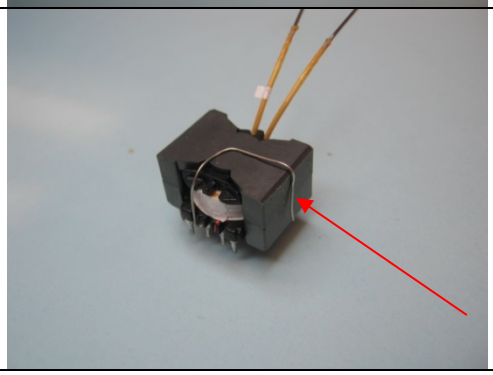
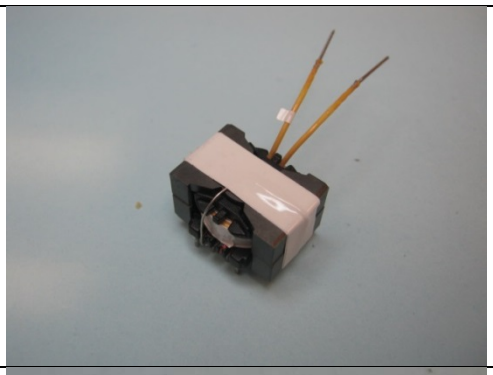
	 	
Insulation		2 layers of tape item [7] to secure the windings and for insulation.
Finish		Gap cores to get 583 μH. Solder ~1" of bus wire item [6] with pin 2 and lean along with 2 cores (see illustration beside). Wrap cores and this bus wire with tape.

		
	 	Wrap around front to back of transformer with 2 layers of tape item [8], and also wrap around top to bottom with 2 layers of tape item [8] (see illustration below) Varnish with item [9].

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8 Common Mode Choke Specifications

8.1 *15 µH Common Mode Choke (LF1)*

8.1.1 Electrical Diagram

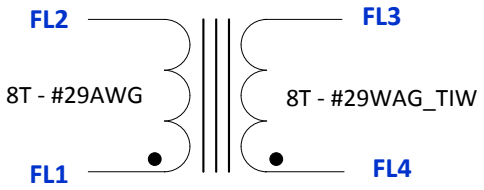


Figure 8 – Common Mode Choke Electrical Diagram.

8.1.2 Electrical Specifications

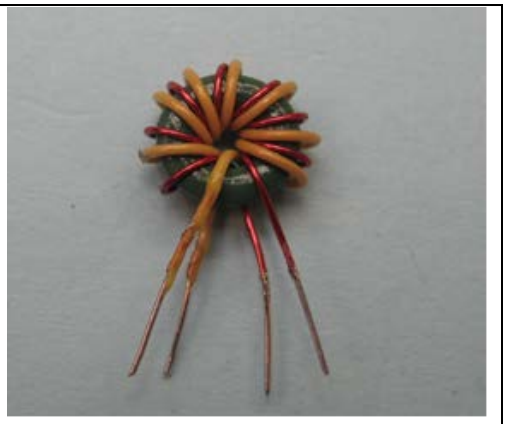
Inductance	Pins FL1-FL2 measured at 100 kHz, 0.4 RMS.	15 µH ± 10%
Primary Leakage Inductance	Pins FL1-FL2, with FL3-FL4 shorted.	0.5 µH

8.1.3 Material List

Item	Description
[1]	Toroid: 32-00339-00.
[2]	Magnet Wire: #29 AWG, Solderable Double Coated.
[3]	Magnet Wire: #29 AWG, Triple Insulated Wire.

8.1.4 Common Mode Choke Illustrations

Bare Toroid



Final Common Mode Choke

8.2 300 µH Differential Mode Choke (L1)

8.2.1 Electrical Diagram

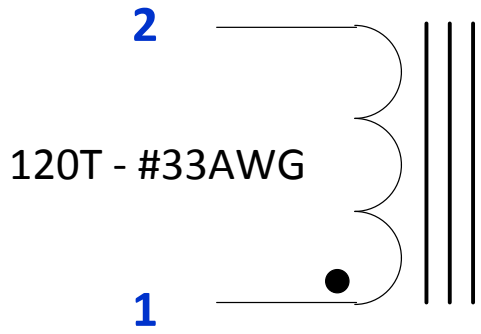


Figure 9 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Core effective Inductance		AL = 22 nH/ T²
Inductance	Pins 1- 2, measured at 100 kHz.	310 µH ±10%
Resonant Frequency	Pins 1- 2.	3,500 kHz (Min.)

8.2.3 Materials List

Item	Description
[1]	Ferrite, PI#: 30-00443-00.
[2]	Magnet Wire: #33 AWG, Solderable Double Coated.
[3]	Shrink Tube: Mouser Electronics, P/N: 602-22316-4BK.

8.2.4 Winding Instructions

- Place item [1] on the chuck of the winding machine, use wire item [2] start at 1 lead as pin 1, wind 120 turns in approximately 8 layers (~15 turns/layer), and finish at other lead as pin 2.
- Use shrink tube item [3] cover choke body for insulation and use heat gun to shrink the tube.

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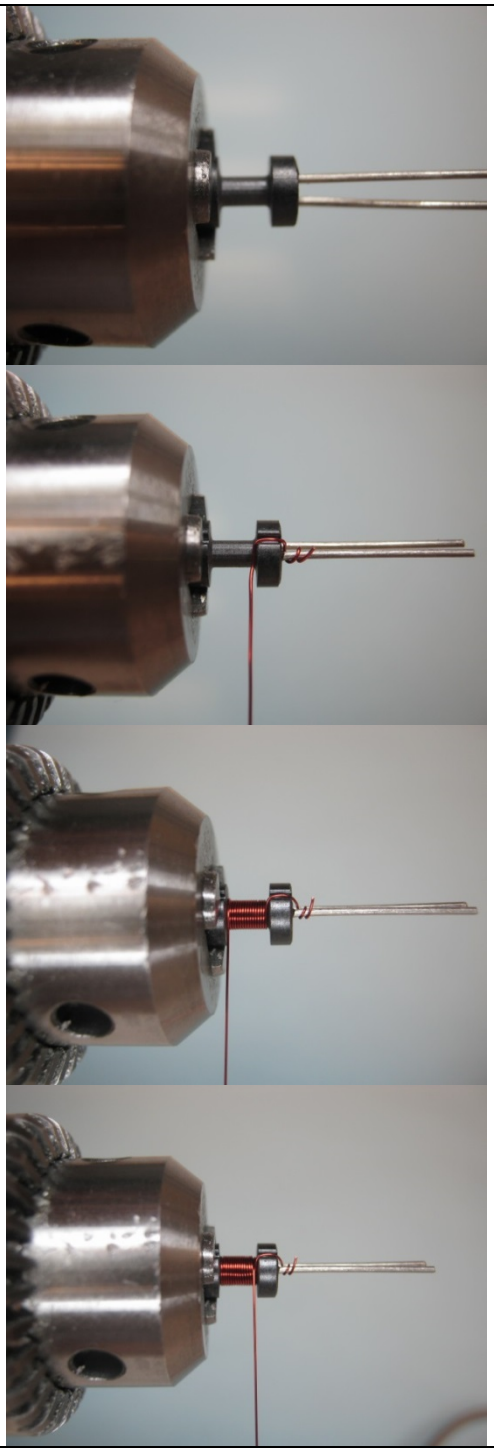
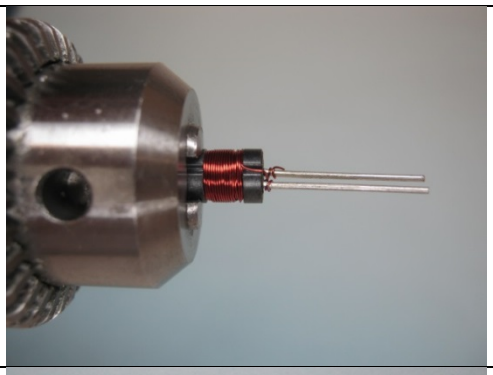
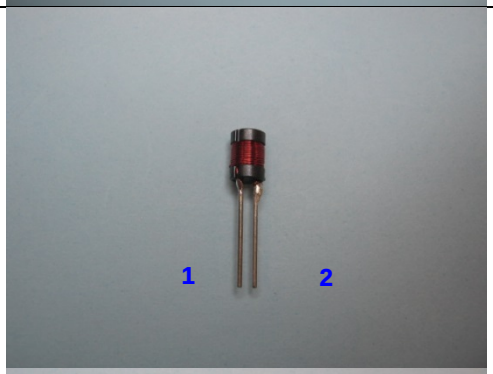
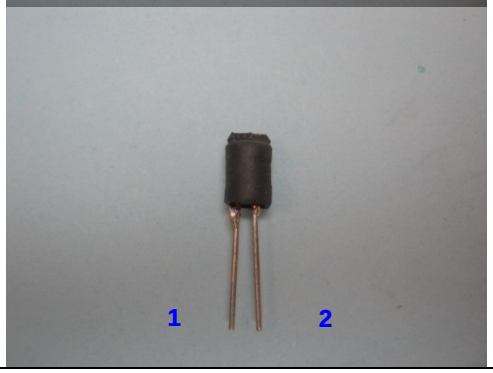
8.2.5 Differential Mode Choke Winding Illustrations

Place toroid item [1] on the chuck of the winding machine, use wire item [2] start at 1 lead as pin 1, wind 120 turns in approximately 8 layers (~15 turns/layer), and finish at other lead as pin 2.	

	
Use shrink tube item [3] cover choke body for insulation and use heat gun to shrink the tube.	 

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch-CP_063016; Rev.1.3; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	InnoSwitch-CP Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC Input Voltage. Universal=85VAC to 155VAC. High-Line=185VAC to 215VAC
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC line frequency
VO_1	9.00		9.36	V	Desired output voltage at the end of cable for configuration 1
IO_1	2.00		2.00	A	Output current for configuration 1
Power_1			18.72	W	Continuous output power, including cable drop compensation for configuration 1
n_1	0.85		0.85		Efficiency Estimate at output terminals for configuration 1. Use 0.8 if no better data available
Z_1	0.50		0.50		Ratio of secondary side losses to the total losses in the power supply for configuration 1. Use 0.5 if no better data available
VO_2	5.00		5.30	V	Desired output voltage at the end of cable for configuration 2
IO_2	3.00		3.00	A	Power Supply Output Current (corresponding to peak power) for configuration 2
Power_2			15.90	W	Continuous Output Power, including cable drop compensation for configuration 2
n_2	0.85		0.85		Efficiency Estimate at output terminals for configuration 2. Use 0.8 if no better data available
Z_2	0.50		0.50		Ratio of secondary side losses to the total losses in the power supply for configuration 2. Use 0.5 if no better data available
VO_3			0.00	V	Configuration 3 is turned off
IO_3			0.00	A	Configuration 3 is turned off
Power_3			0.00	W	Configuration 3 is turned off
n_3	0.80		0.80		Configuration 3 is turned off
Z_3	0.50		0.50		Configuration 3 is turned off
VO_4			0.00	V	Configuration 4 is turned off
IO_4			0.00	A	Configuration 4 is turned off
Power_4			0.00	W	Configuration 4 is turned off
n_4	0.80		0.80		Configuration 4 is turned off
Z_4	0.50		0.50		Configuration 4 is turned off
tC			3.00	mS	Bridge Rectifier Conduction Time Estimate
CIN	30.00	**Warning**	30.00	uF	The capacitance entered is less than that required to deliver power and maintain the minimum input voltage. Increase the capacitance.
Enclosure	Adapter		Adapter		Select between Adapter and Open Frame
Cable compensation type	Potential Divider		Potential Divider		The output voltage is varied by varying the lower feedback resistor (CHY100)
ENTER InnoSwitch-CP VARIABLES					
InnoSwitch-CP	INN2215		INN2215		User defined InnoSwitch
Cable drop compensation	6%		6%		Cable Drop Compensation.
Complete Part Number			INN2215 K		Final part number including package
Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit, "STD" for standard current limit or "INC" for increased current limit
ILIMITMIN			0.893	A	Minimum Current Limit
ILIMITTYP			0.950	A	Typical Current Limit
ILIMITMAX			1.007	A	Maximum Current Limit

fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			78.52	A^2kHz	Worst case I2f for power delivery
VOR	81		81	V	Reflected output voltage assigned to configuration 1
VDS			2.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.419		Minimum Value of KP given all configurations and i2f conditions
KP_TRANSIENT			0.274		Minimum Value of KP_TRANSIENT given all configurations and i2f conditions
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Minimum bias winding voltage. Bias voltage will be higher for higher output voltages. Verify performance on the bench.
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			8.00		Minimum bias winding number of turns to ensure the minimum bias winding voltage.
PIVB			128.59	V	Minimum PIV rating of the bias diode given all configurations and i2f conditions.
ENTER TRANSFORMER CORE VARIABLES					
Core Type	Custom		Custom		Enter Transformer Core
Core	PQ20-11		PQ20-11		Enter core part number, if necessary
Bobbin			0		Enter bobbin part number, if necessary
AE	0.59		0.59	cm^2	Core Effective Cross Sectional Area
LE	3.10		3.10	cm	Core Effective Path Length
AL	2000		2000	nH/T^2	Ungapped Core Effective Inductance
BW	4.20		4.20	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
LAYERS_PRIMARY	3		3		Number of Primary Layers
NS			4		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN		**Warning**	73	V	Verify if the design duty cycle has not been exceeded or increase the input capacitance
VMAX			375	V	Maximum DC Input Voltage
PRIMARY CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.535		Maximum value of DMAX given all configurations and i2f conditions
IP_AVG			0.288	A	Maximum value of the average primary current given all configurations and i2f conditions
IP_PEAK			1.014	A	Maximum value of the peak primary current given all configurations and i2f conditions
IP_RMS			0.535	A	Maximum value of the primary RMS current given all configurations and i2f conditions
IP_RIPPLE			0.749	A	Maximum value of the primary ripple current given all configurations and i2f conditions
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			583	uHenry	Typical Primary Inductance. +/- 7% to ensure a minimum primary inductance of 542 uH
LP_TOLERANCE			7.0	%	Primary inductance tolerance
NP			36		Primary Winding Number of Turns
ALG			450	nH/T^2	Gapped Core Effective Inductance
BM			2962	Gauss	Maximum operating flux density given all configurations and i2f conditions
BAC			951	Gauss	Maximum AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) given all configurations and i2f conditions
ur			832		Relative Permeability of Ungapped Core
LG			0.13	mm	Gap Length (Lg > 0.1 mm)
BWE			12.6	mm	Effective Bobbin Width

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OD			0.35	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.29	mm	Bare conductor diameter
AWGP			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CMP			128	Cmils	Bare conductor effective area in circular mils
CMAP			239	Cmils/ Amp	Primary wire circular mils per amp
CDP			8.3	A/mm ^2	Primary wire current density
SECONDARY CURRENT WAVEFORM SHAPE PARAMETERS					
IS_PEAK			9.063	A	Maximum value of the peak secondary current, given all configurations and i2f conditions
IS_RMS			5.633	A	Maximum value of the secondary RMS current, given all configurations and i2f conditions
IS_RIPPLE			4.768	A	Maximum value of the output capacitor RMS ripple current, given all configurations and i2f conditions
TRANSFORMER SECONDARY DESIGN PARAMETERS					
CMS			1127	Cmils	Secondary Bare Conductor minimum circular mils
CMAS			200	Cmils/ Amp	Worst-case secondary wire circular mils per amp given all configurations and i2f conditions
CDS			8.6	A/mm ^2	Worst-case secondary wire current density given all configurations and i2f conditions
AWGS			19	AWG	Worst-case secondary wire gauge (Rounded up to next larger standard AWG value) given all configurations and i2f conditions
DIAS			0.91	mm	Minimum Bare Conductor Diameter
ODS			1.05	mm	Maximum Outside Diameter for Triple Insulated Wire
SECONDARY SR FET DESIGN PARAMETERS					
SRFET	Auto		DMT8012 LFG		Recommended SR FET for the design
RDSON			22.0	mOhm s	RDSon at 25C
PIV_rated			80	V	Rated voltage of selected SR FET
VD			0.073	V	Output Synchronous Rectification FET Forward Voltage Drop
PD			244.5	mW	Output Synchronous Rectification FET Power Dissipation
VOLTAGE STRESS PARAMETERS					
VDRAIN			557	V	Maximum Drain Voltage Estimate
PIVS			51	V	Output Rectifier Maximum Peak Inverse Voltage, neglecting the parasitic spike
DESIGN CONFIGURATION PARAMETERS					
Configuration	1		1		Select the configuration number
VO			9.00	V	Output voltage at the end of the cable for the selected configuration
IO			2.00	A	Output current for the selected configuration
PO			18.72	W	Output power at the end of the cable for the selected configuration
n			0.85		Efficiency for the selected configuration
Z			0.50		Loss allocation factor for the selected configuration
DMAX			0.535		DMAX for the selected configuration
VOR			81.0	V	VOR for the desired configuration
KP			0.708		KP for the selected configuration
KP_transient			0.494		KP_transient for the selected configuration
IPP			1.01	A	Primary switch peak current given all i2f conditions
IPRMS			0.53	A	Primary switch RMS current given all i2f conditions
IPRIPPLE			0.75	A	Primary switch current ripple given all i2f

					conditions
ISP			9.06	A	Secondary switch peak current given all i2f conditions
ISRMS			4.49	A	Secondary switch RMS current given all i2f conditions
ISRIPPLE			4.02	A	Secondary switch current ripple given all i2f conditions

Note: The spreadsheet shows two warnings since a smaller input capacitor has been used and the resulting DC bus voltage ripple is higher. This is however acceptable since the same has not resulted in any other warnings or the design reaching duty cycle limit of the InnoSwitch-CP IC.

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10 Performance Data

Note: Efficiency data was obtained by connecting a 100 mΩ resistor at the USB connector on the board right next to the drain of Q1. This resistor was used to simulate cable impedance.

10.1 *Full Load Efficiency vs. Line (End of a 100 mΩ Resistor)*

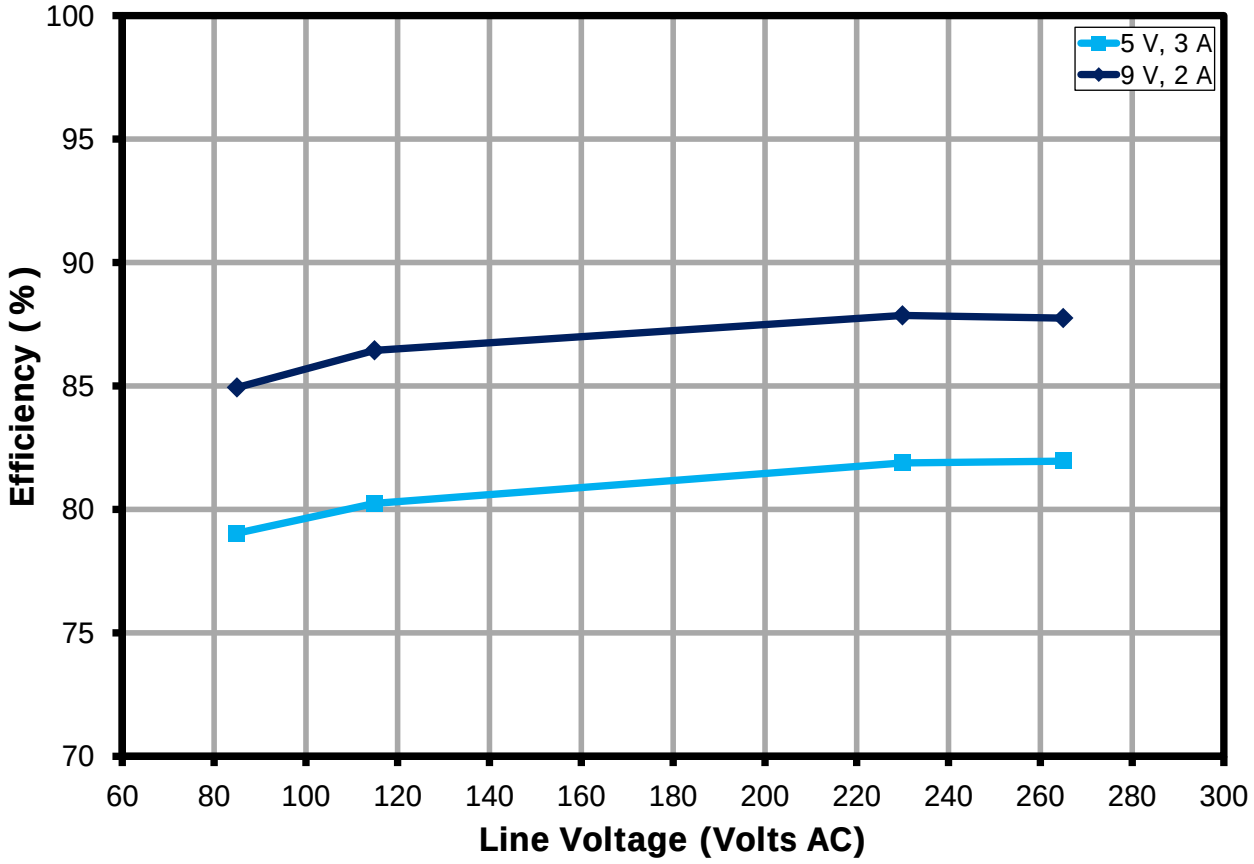

Figure 10 – Efficiency vs. Line Voltage, Room Temperature.

10.2 Efficiency vs. Load (End of a 100 mΩ Resistor)

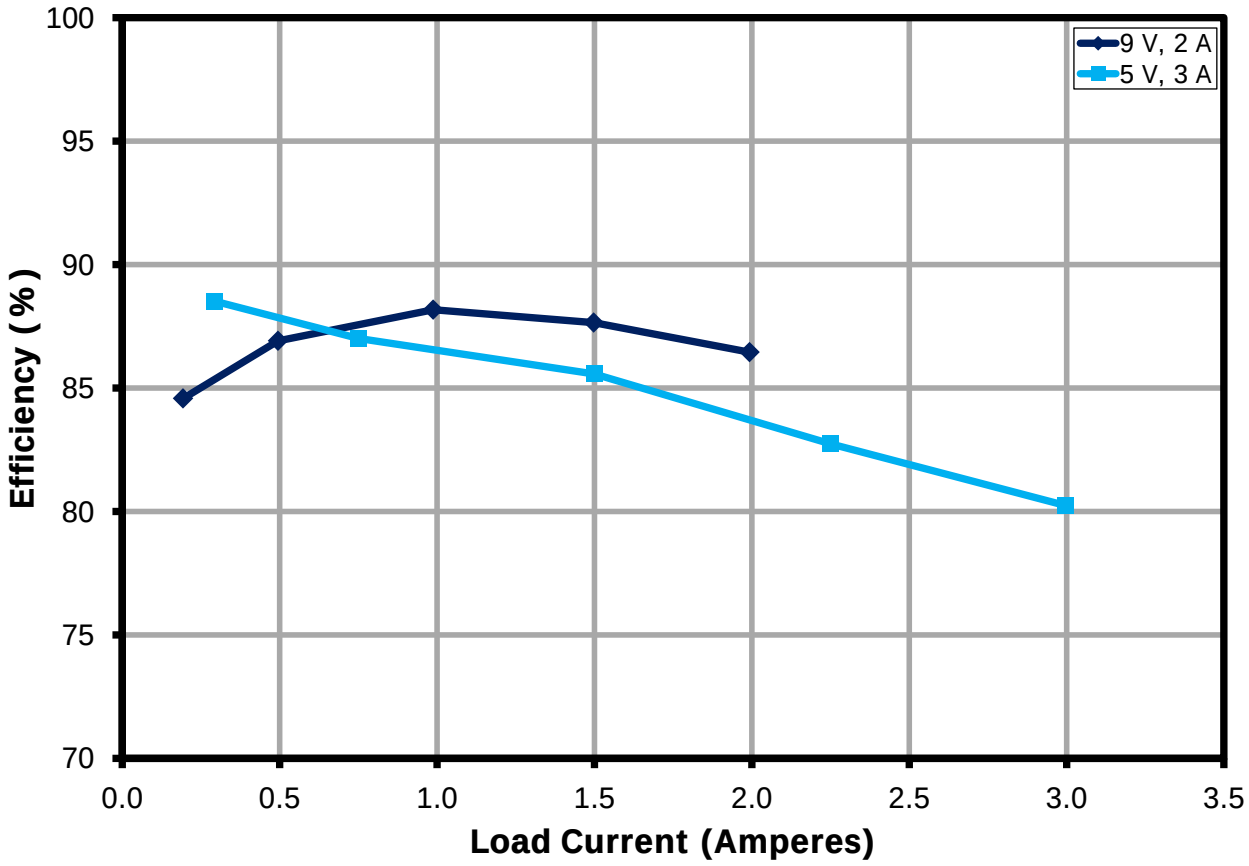

Figure 11 – Efficiency vs. Load, Room Ambient. 115 VAC.

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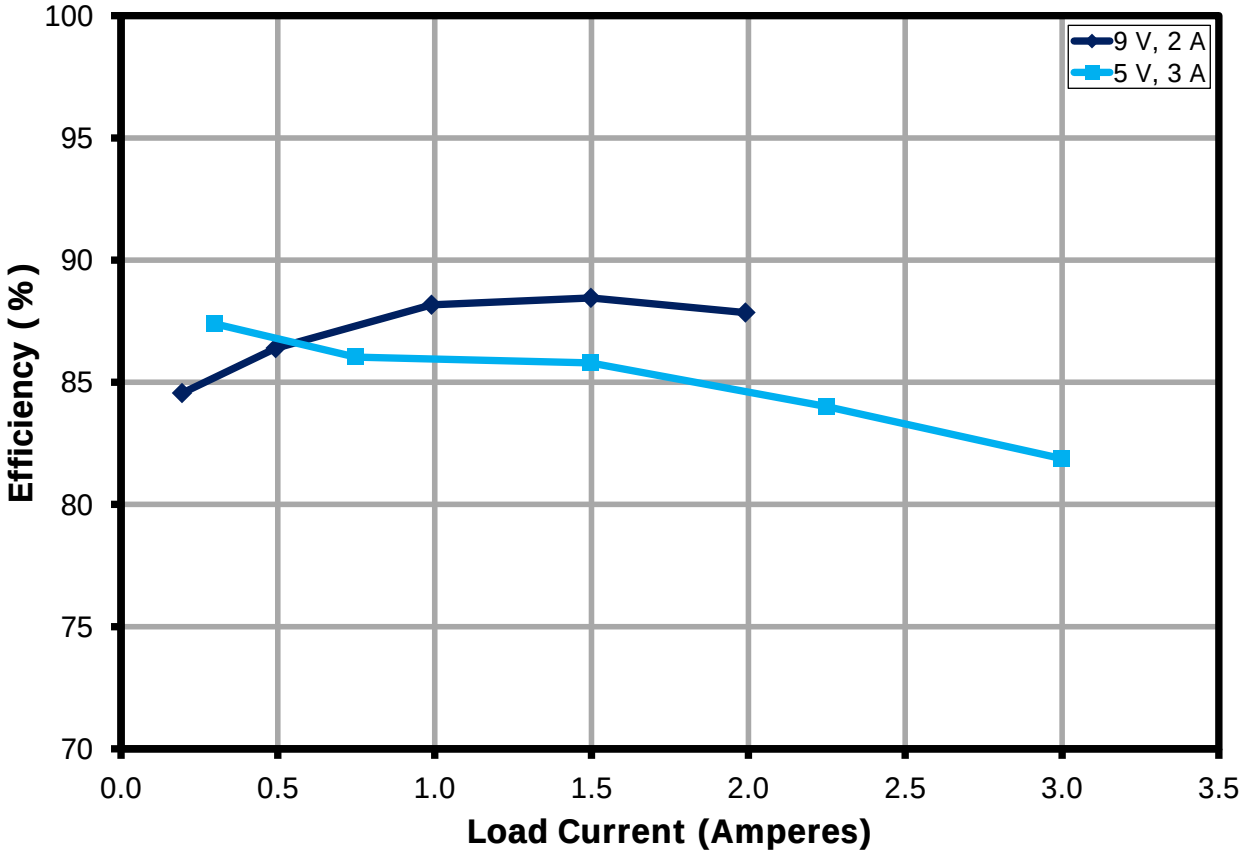

Figure 12 – Efficiency vs. Load, Room Ambient. 230 VAC.

10.3 *Average Efficiency (End of a 100 mΩ Resistor)*

LINE	9 V, 2 A		5 V, 3 A	
	Load Current (Amperes)	Efficiency (%)	Load Current (Amperes)	Efficiency (%)
Line: 115 VAC, 60 Hz Load: 9 V, 5 V	1.993	86.44	2.996	80.24
	1.498	87.65	2.250	82.73
	0.988	88.17	1.500	85.57
	0.495	86.91	0.750	87.01
	0.193	84.57	0.294	88.51
Line: 230 VAC, 50 Hz Load: 9 V, 5 V	1.991	87.85	2.998	81.88
	1.498	88.45	2.248	84.01
	0.990	88.17	1.496	85.80
	0.493	86.40	0.748	86.03
	0.195	84.55	0.298	87.39

LOAD	9 V, 2 A		5 V, 3 A	
LINE	115 VAC	230 VAC	115 VAC	230 VAC
New IESA2007	78.60%	78.60%	81.40%	81.40%
CoC v5 Tier 2 (Average)	86.00%	86.00%	81.80%	81.80%
Power Supply Average Data	87.29%	87.72%	83.89%	84.43%
CoC v5 Tier 2 (10%)	76.00%	76.00%	72.50%	72.50%
Power Supply Data	84.57%	84.55%	88.51%	87.39%

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10.4 No-Load Input Power at 5 V_{OUT}

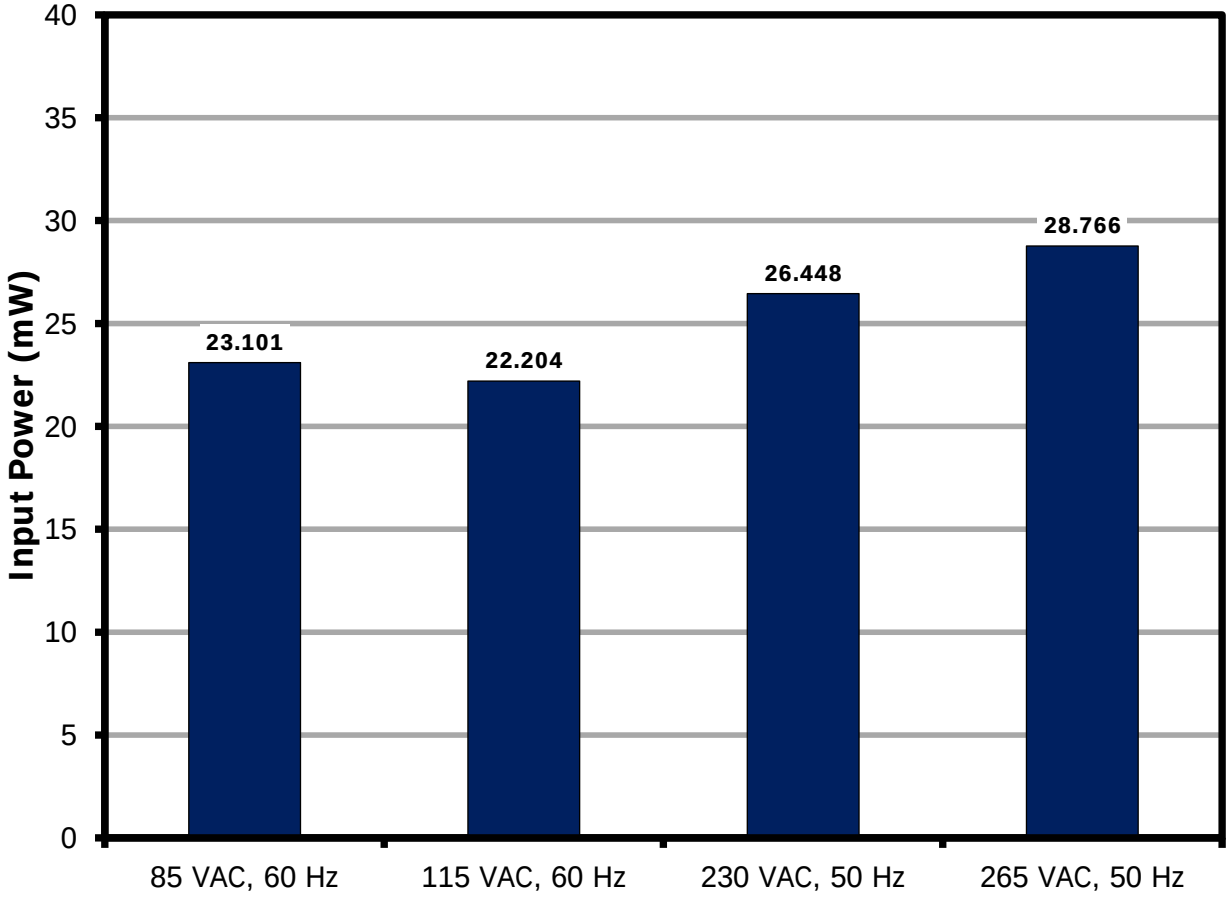

Figure 13 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.5 *Line and Load Regulation*

10.5.1 Line Regulation (End of a 100 mΩ Resistor Used to Simulate Cable)

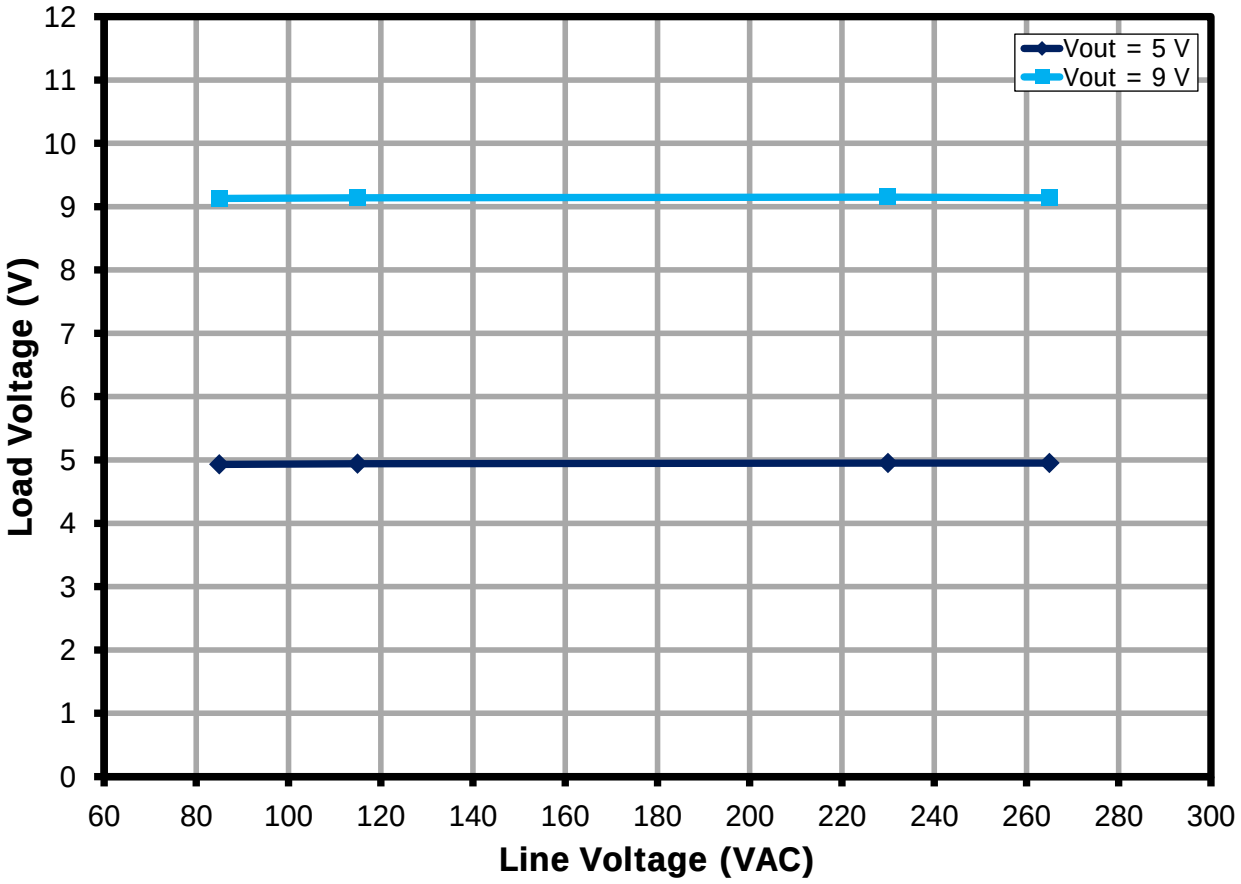

Figure 14 – Output Voltage vs. Input Line Voltage, Room Temperature.

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10.5.2 Load Regulation (End of a 100 mΩ Resistor Used to Simulate Cable)

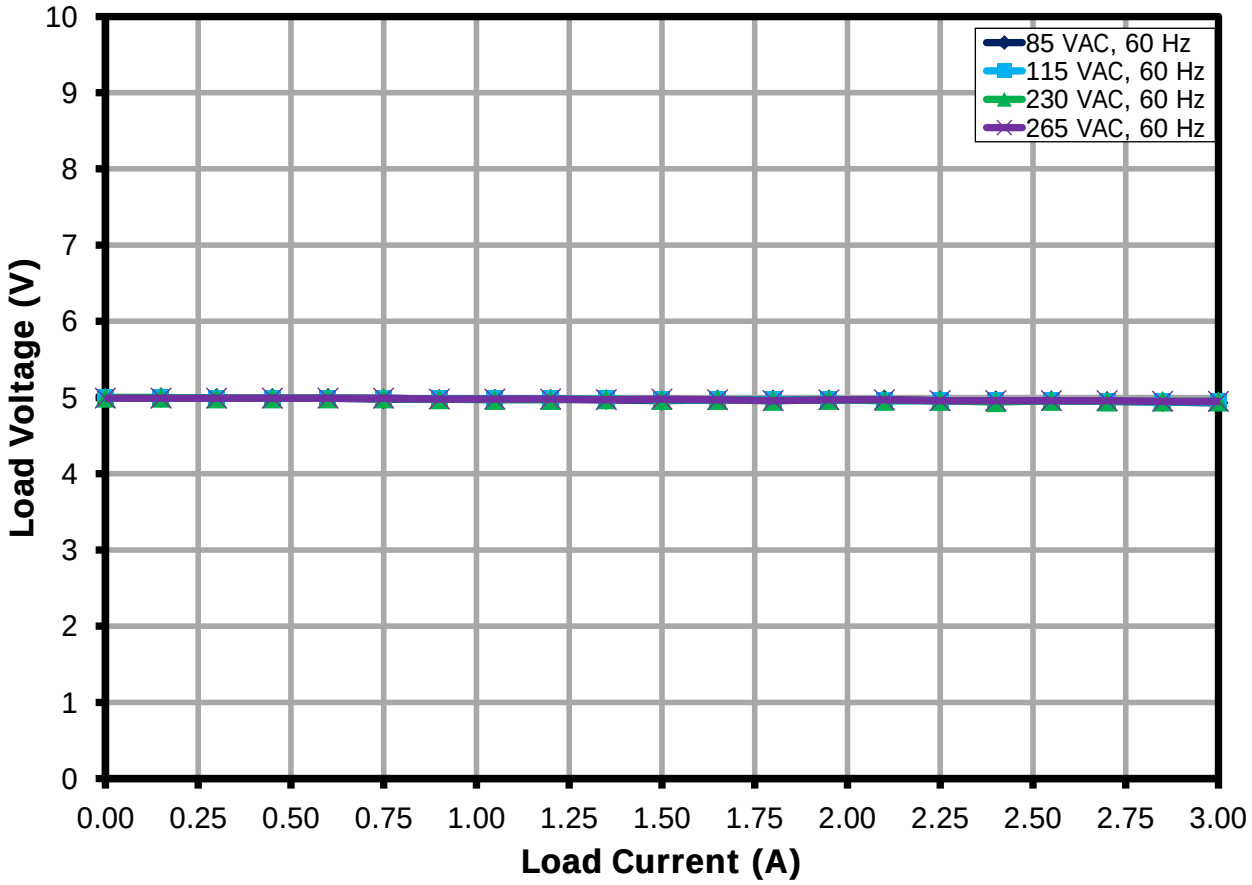

Figure 15 – Output Voltage vs. Output Load, Room Temperature. V_{OUT} = 5 V.

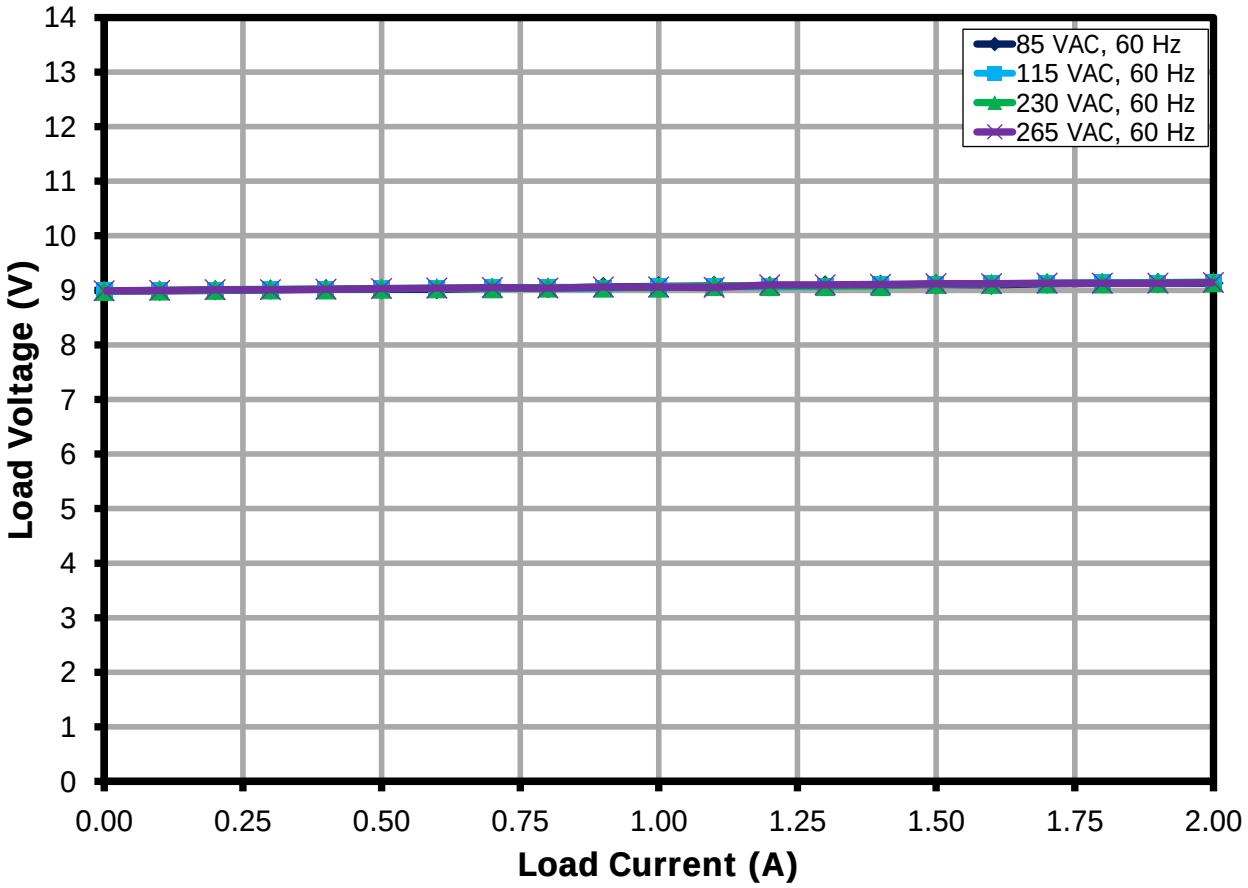

Figure 16 – Output Voltage vs. Output Load, Room Temperature. V_{OUT} = 9 V.

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10.6 CV/CC vs. Line (End of a 100 mΩ Resistor Used to Simulate Cable)

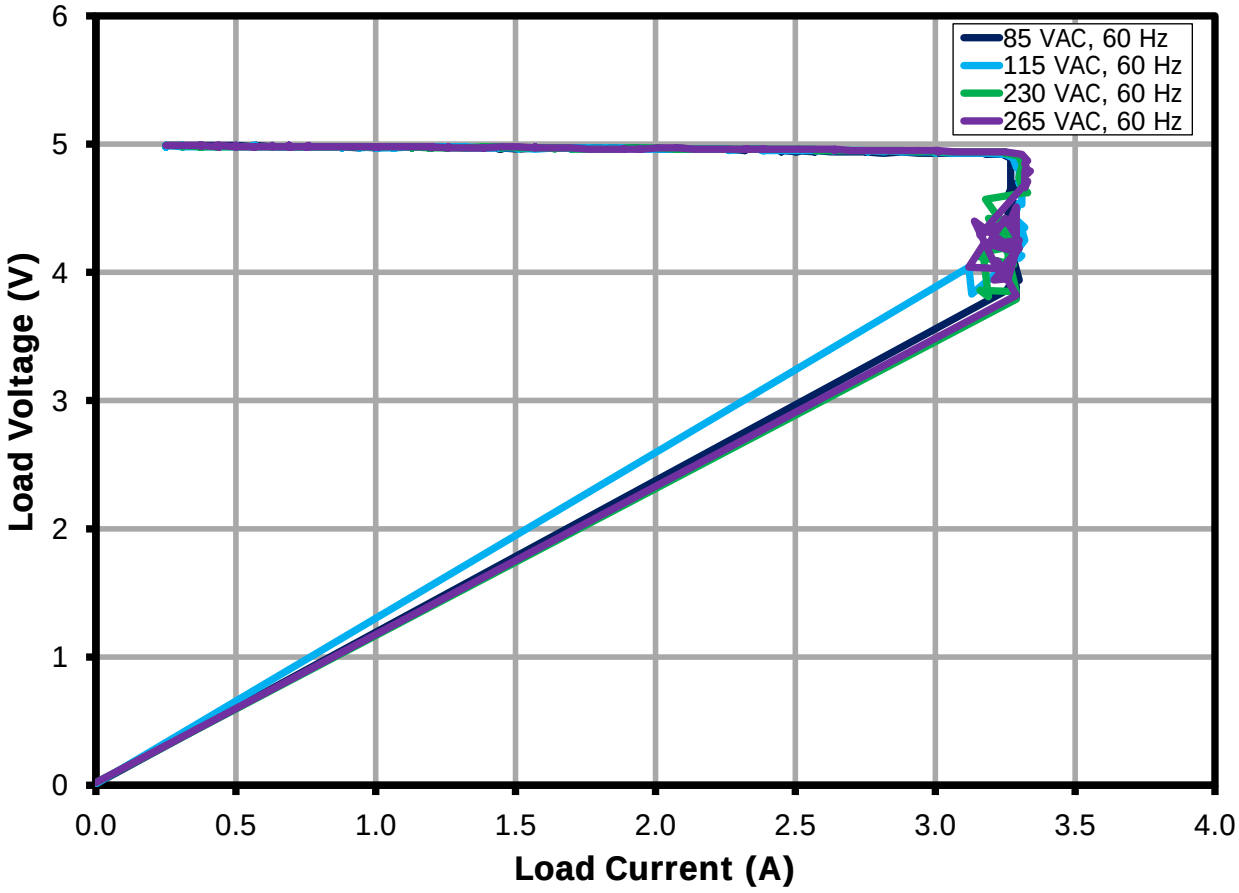

Figure 17 – Output Voltage vs. Output Current, Room Temperature. 5 V Output.

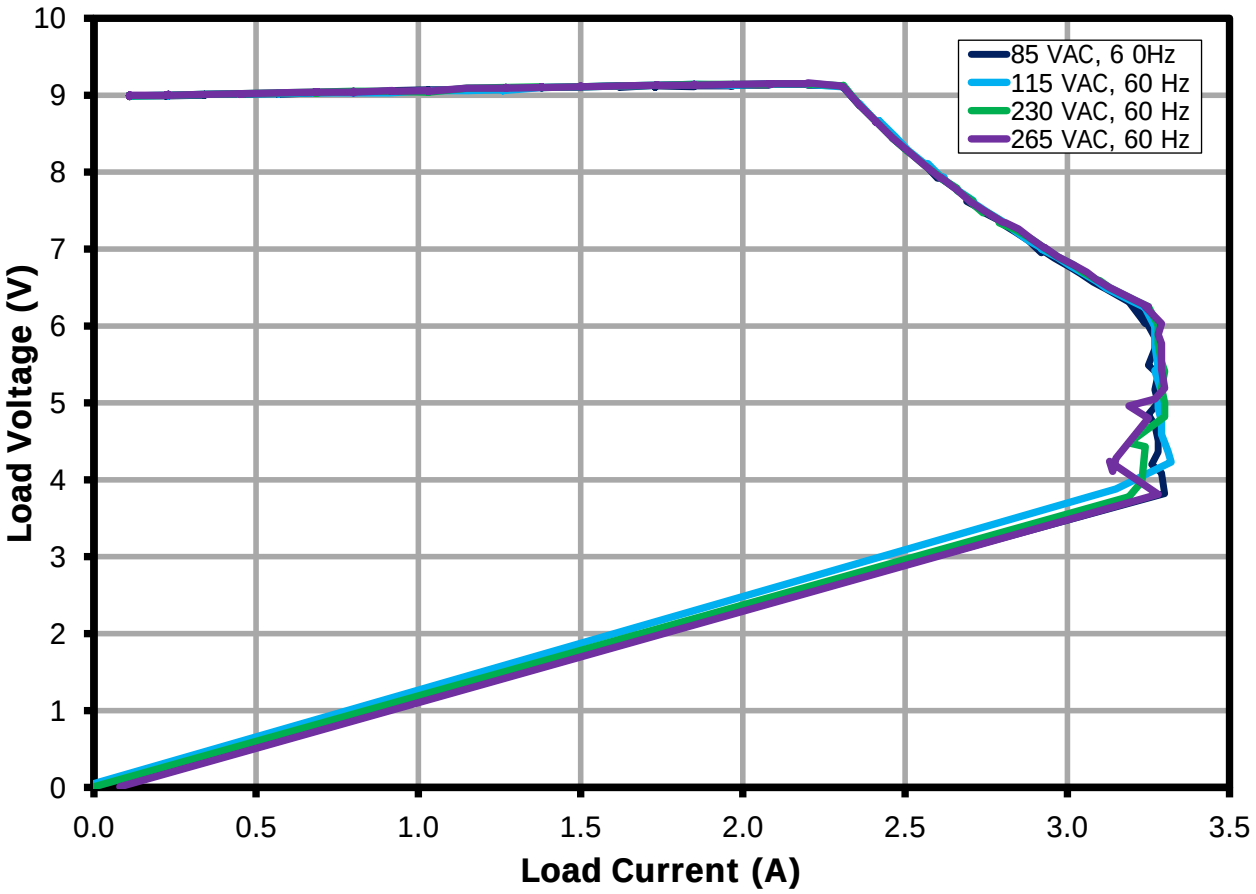

Figure 18 – Output Voltage vs. Output Current, Room Temperature. 9 V Output.

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11 Thermal Performance in Open Case at 9 V / 2 A Output

11.1 85 VAC Input

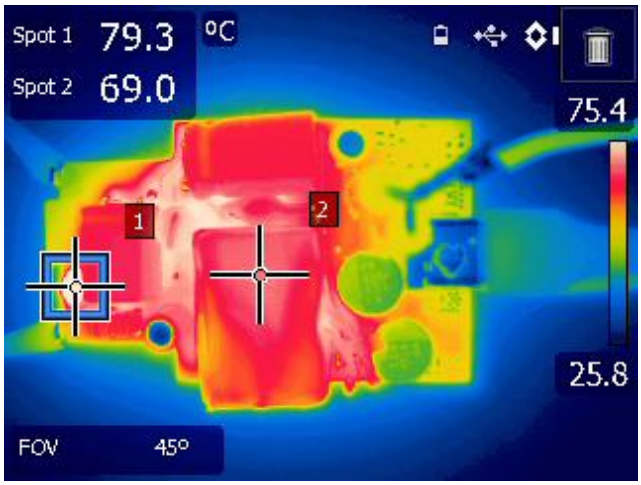

Figure 19 – Ambient = 25.8 ºC.
Thermistor, RT1 = 79.3 ºC.
Transformer, T1 = 69.0 ºC.

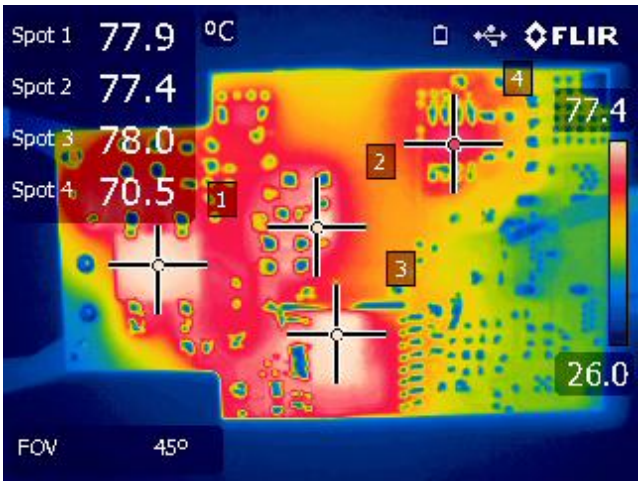

Figure 20 – Ambient = 26.0 ºC.
Bridge Rectifier, BD1 = 77.9 ºC.
Clamp Diode, D2 = 77.4 ºC.
InnoSwitch-CP, U2 = 78.0 ºC.
SR FET, Q3 = 70.5 ºC.

11.2 115 VAC Input

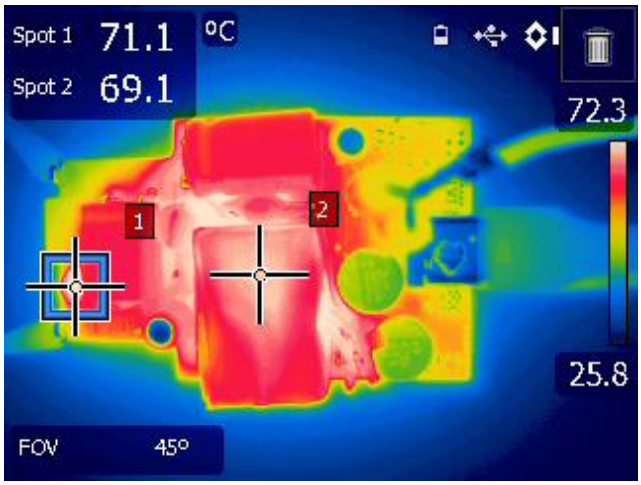

Figure 21 – Ambient = 25.8 ºC.
Thermistor, RT1 = 71.1 ºC.
Transformer, T1 = 69.1 ºC.

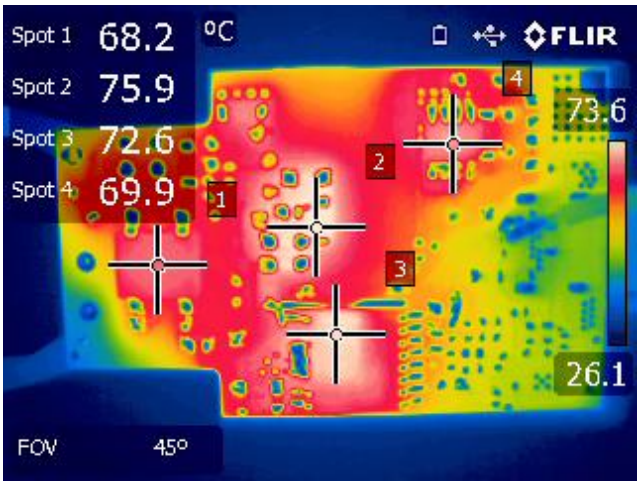

Figure 22 – Ambient = 26.1 ºC.
Bridge Rectifier, BD1 = 68.2 ºC.
Clamp Diode, D2 = 75.9 ºC.
InnoSwitch-CP, U2 = 72.6 ºC.
SR FET, Q3 = 69.9 ºC.

11.3 230 VAC Input

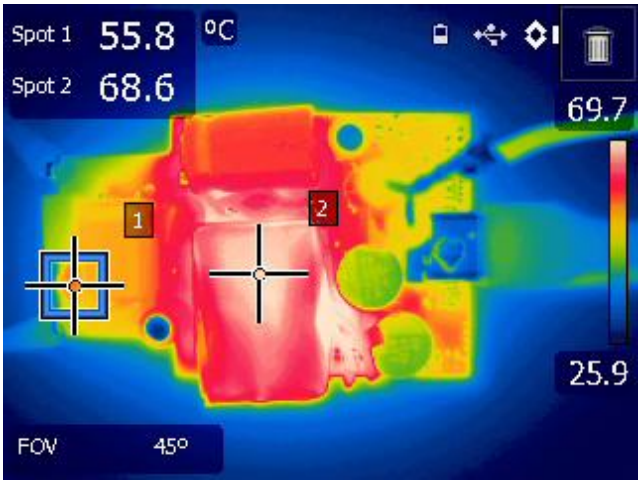

Figure 23 – Ambient = 25.9 ºC.
Thermistor, RT1 = 55.8 ºC.
Transformer, T1 = 68.6 ºC.

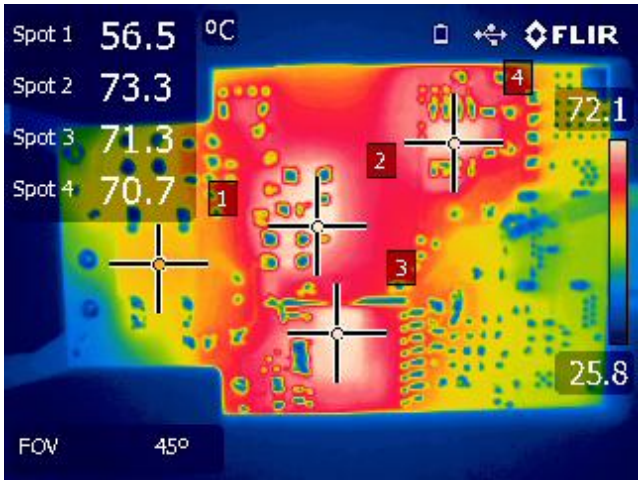

Figure 24 – Ambient = 25.8 ºC.
Bridge Rectifier, BD1 = 56.5 ºC.
Clamp Diode, D2 = 73.3 ºC.
InnoSwitch-CP, U2 = 71.3 ºC.
SR FET, Q3 = 70.7 ºC.

11.4 265 VAC Input

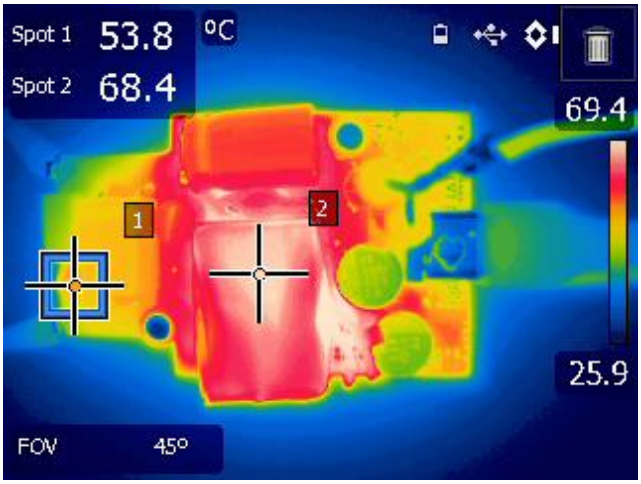

Figure 25 – Ambient = 25.9 ºC.
Thermistor, RT1 = 53.8 ºC.
Transformer, T1 = 68.7 ºC.

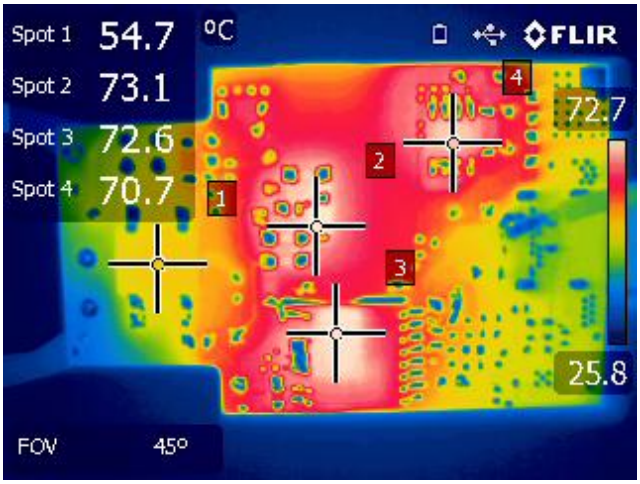

Figure 26 – Ambient = 25.8 ºC.
Bridge Rectifier, BD1 = 54.7 ºC.
Clamp Diode, D2 = 73.1 ºC.
InnoSwitch-CP, U2 = 72.6 ºC.
SR FET, Q3 = 70.7 ºC.

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12 Waveforms

12.1 Load Transient Response (End of a 100 mΩ Resistor)

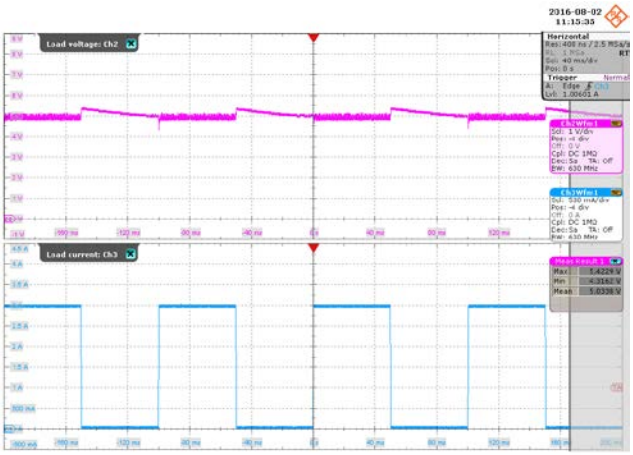

Figure 27 – Transient Response.
85 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN} 4.3162 V, V_{MAX}: 5.4229 V.
Upper: V_{OUT}, 1 V / div., 40 ms / div.
Lower: I_{LOAD}, 500 mA / div.

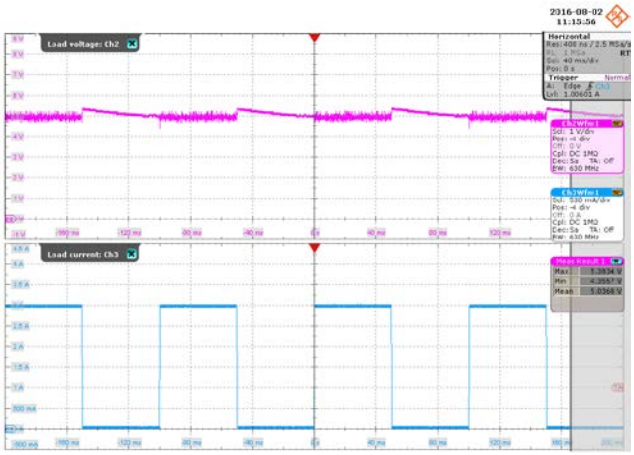

Figure 28 – Transient Response.
265 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN} 4.3557 V, V_{MAX}: 5.3834 V.
Upper: V_{OUT}, 1 V / div., 40 ms / div.
Lower: I_{LOAD}, 500 mA / div.

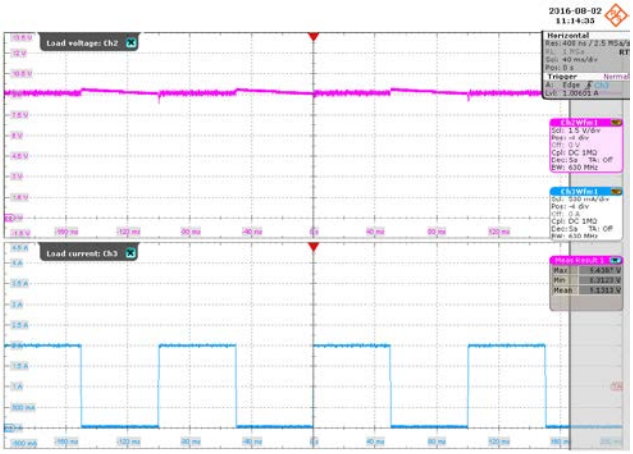

Figure 29 – Transient Response.
85 VAC, 9 V, 0 – 2 A Load Step.
V_{MIN}: 8.3123 V, V_{MAX}: 9.4387 V.
Upper: V_{OUT}, 1.5 V / div., 40 ms / div.
Lower: I_{LOAD}, 500 mA / div.

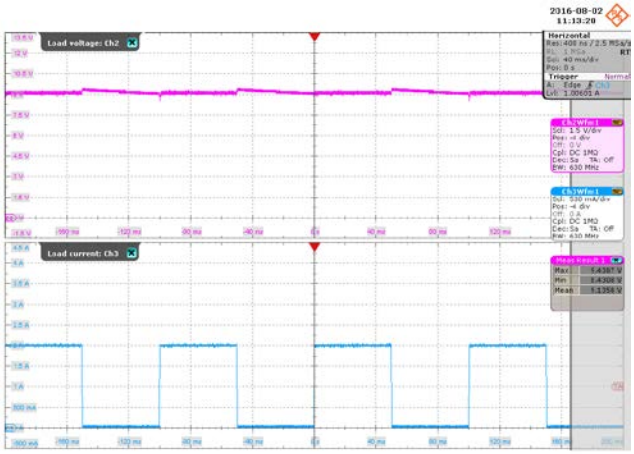

Figure 30 – Transient Response.
265 VAC, 9 V, 0 – 2 A Load Step.
V_{MIN}: 8.4308 V, V_{MAX}: 9.4387 V.
Upper: V_{OUT}, 1.5 V / div., 40 ms / div.
Lower: I_{LOAD}, 500 mA / div.

12.2 **Switching Waveforms**

12.2.1 Drain Voltage and Current

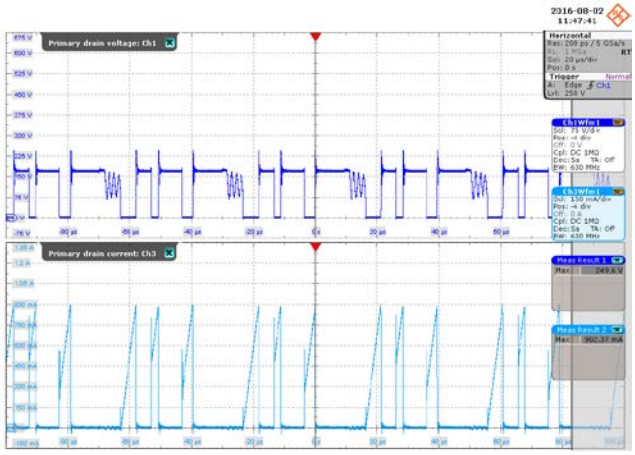

Figure 31 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3 A Load, (249.6 V_{MAX}).
Upper: V_{DRAIN}, 75 V /div., 20 µs / div.
Lower: I_{DRAIN}, 150 mA / div.

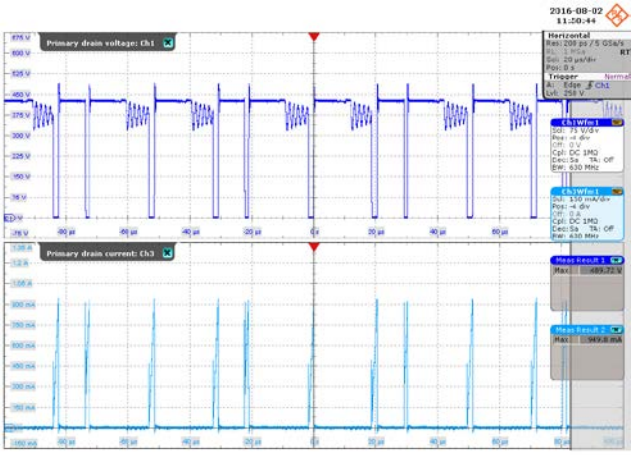

Figure 32 – Drain Voltage and Current Waveforms.
265 VAC, 5 V, 3 A Load, (489.7 V_{MAX}).
Upper: V_{DRAIN}, 75 V /div., 20 µs / div.
Lower: I_{DRAIN}, 150 mA / div.

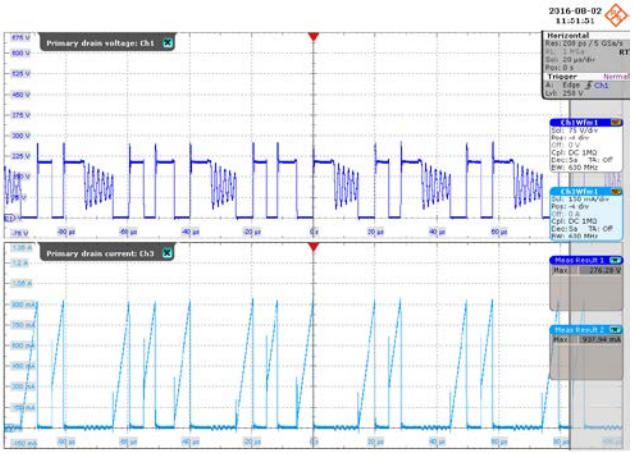

Figure 33 – Drain Voltage and Current Waveforms.
85 VAC, 9.0 V, 2 A Load, (276.3 V_{MAX}).
Upper: V_{DRAIN}, 75 V / div., 20 µs / div.
Lower: I_{DRAIN}, 150 mA / div.

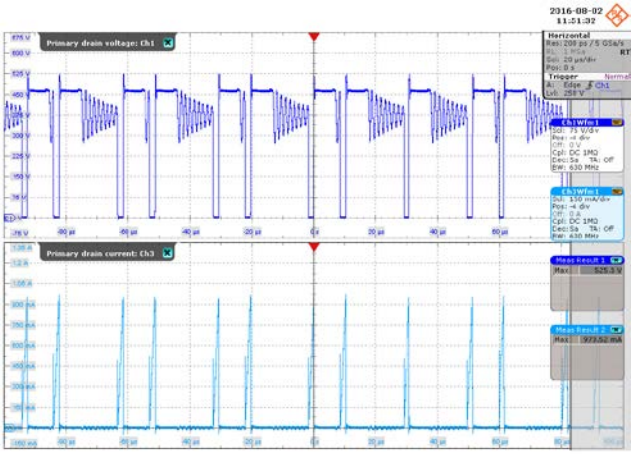

Figure 34 – Drain Voltage and Current Waveforms.
265 VAC, 9 V, 2 A Load, (525.3 V_{MAX}).
Upper: V_{DRAIN}, 75 V / div., 20 µs / div.
Lower: I_{DRAIN}, 150 mA / div.

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12.2.2 Drain Voltage and Current Start-up

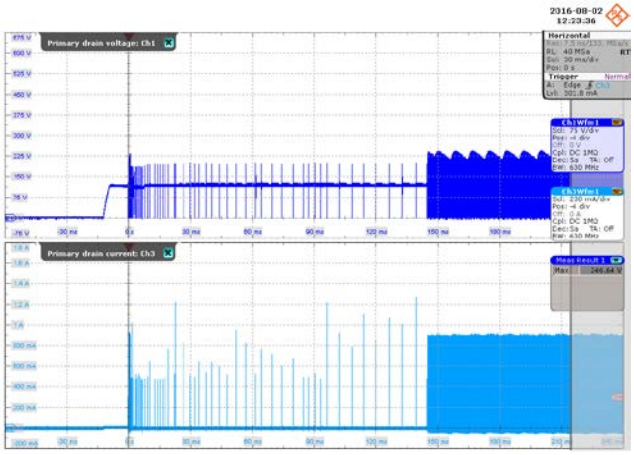

Figure 35 – Drain Voltage and Current Waveforms.
85 VAC, 5 V, 3 A Load, (246.6 V_{MAX})
Upper: V_{DRAIN}, 75 V / div., 30 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

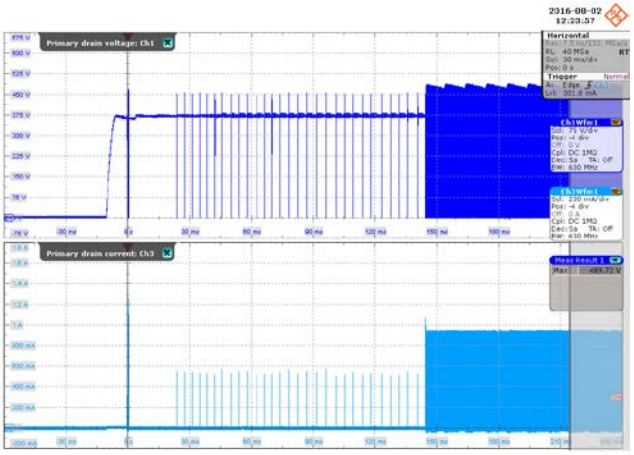

Figure 36 – Drain Voltage and Current Waveforms.
265 VAC, 5 V, 3 A Load, (499 V_{MAX})
Upper: V_{DRAIN}, 75 V / div., 30 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

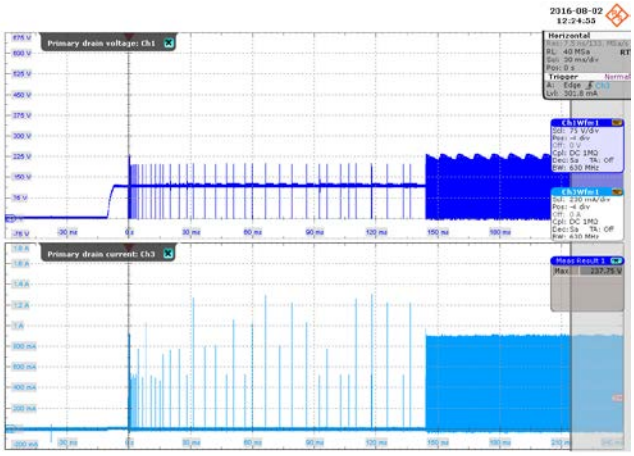

Figure 37 – Drain Voltage and Current Waveforms.
85 VAC, 9 V, 2 A Load, (237.8 V_{MAX})
Upper: V_{DRAIN}, 75 V / div, 30 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

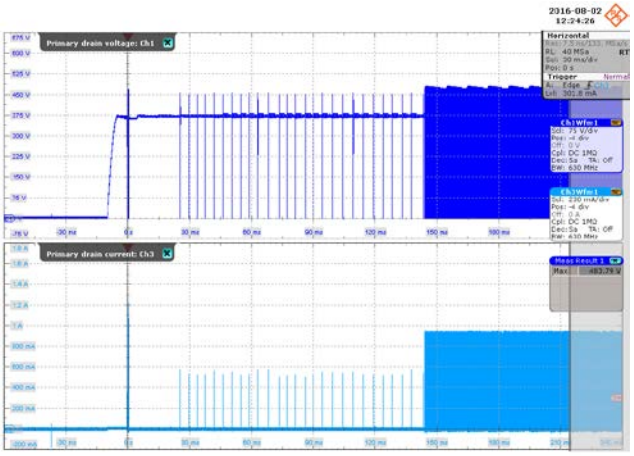

Figure 38 – Drain Voltage and Current Waveforms.
265 VAC, 9 V, 2 A Load, (483.8 V_{MAX})
Upper: V_{DRAIN}, 75 V / div., 30 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

12.2.3 SR FET Voltage

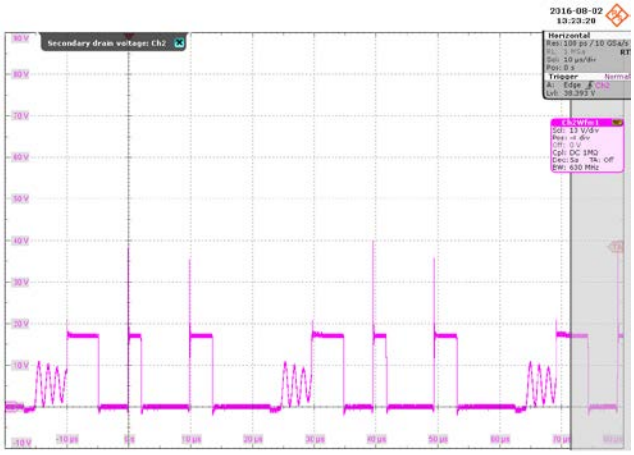

Figure 39 – SR FET Voltage Waveforms.
85 VAC, 5 V, 3 A Load, (40 V_{MAX}).
V_{DRAIN}, 10 V / div., 10 µs / div.

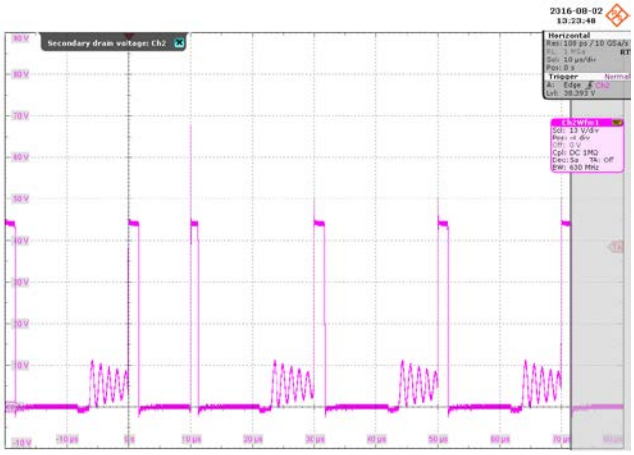

Figure 40 – SR FET Voltage Waveforms.
265 VAC, 5 V, 3 A Load, (67 V_{MAX}).
V_{DRAIN}, 10 V / div., 10 µs / div.

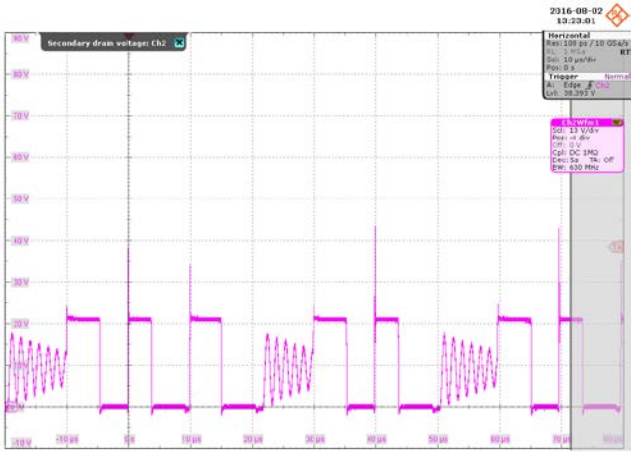

Figure 41 – SR FET Voltage Waveforms.
85 VAC, 9 V, 2 A Load, (44 V_{MAX}).
V_{DRAIN}, 10 V / div., 10 µs / div.

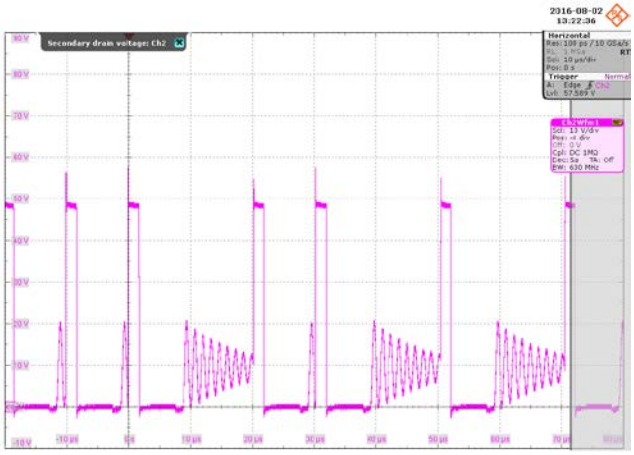

Figure 42 – SR FET Voltage Waveforms.
265 VAC, 9 V, 2 A Load, (57 V_{MAX}).
V_{DRAIN}, 10 V / div., 10 µs / div.

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12.2.4 Output Voltage and Current Start-up (End of Cable)

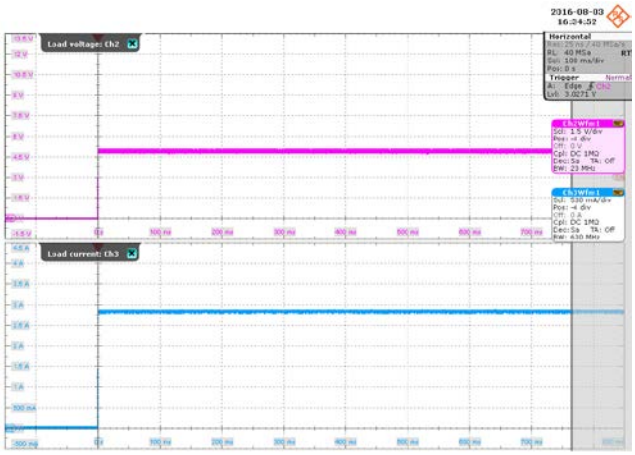

Figure 43 – Output Voltage and Current Waveforms.
85 VAC Input, 1.667 Ω Resistive Load.
Upper: V_{OUT}: 1.5 V / div., 100 ms / div.
Lower: I_{OUT}, 500 mA / div., 100 ms / div.

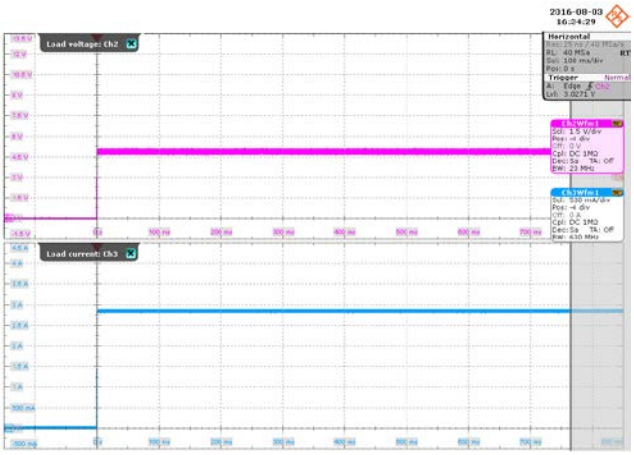

Figure 44 – Output Voltage and Current Waveforms.
265 VAC Input, 1.667 Ω Resistive Load.
Upper: V_{OUT}: 1.5 V / div., 100 ms / div.
Lower: I_{OUT}, 500 mA / div., 100 ms / div.

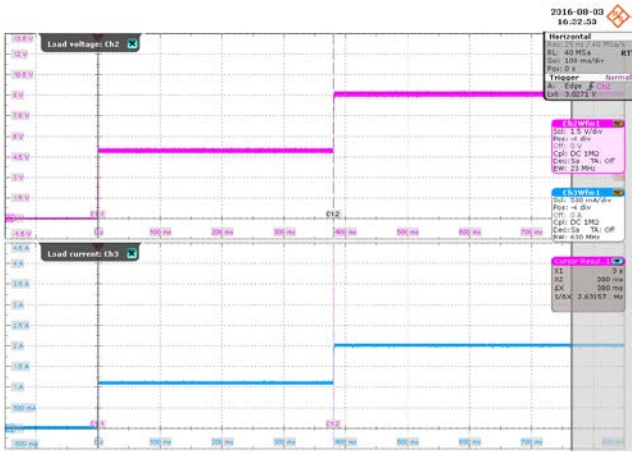

Figure 45 – Output Voltage and Current Waveforms.
85 VAC Input, 4.5 Ω Resistive Load.
Upper: V_{OUT}: 1.5 V / div., 100 ms / div.
Lower: I_{OUT}, 500 mA / div., 100 ms / div.

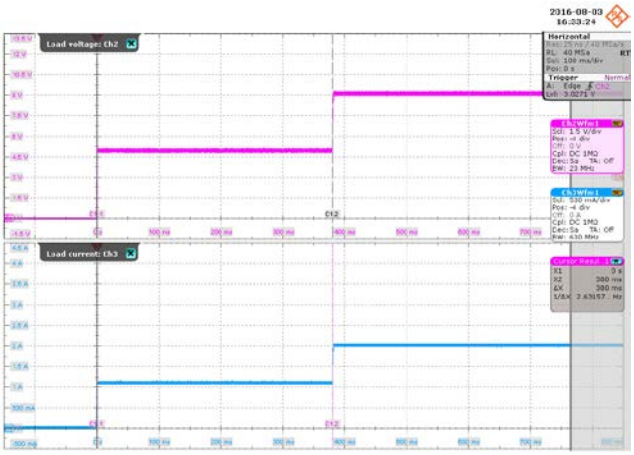

Figure 46 – Output Voltage and Current Waveforms.
265 VAC Input, 4.5 Ω Resistive Load.
Upper: V_{OUT}: 1.5 V / div., 100 ms / div.
Lower: I_{OUT}, 500 mA / div., 100 ms / div.

12.3 **Output Voltage Change (Measured at End of Cable)**

12.3.1 Output Voltage Change (USB-PD)

12.3.1.1 2.2 A Load

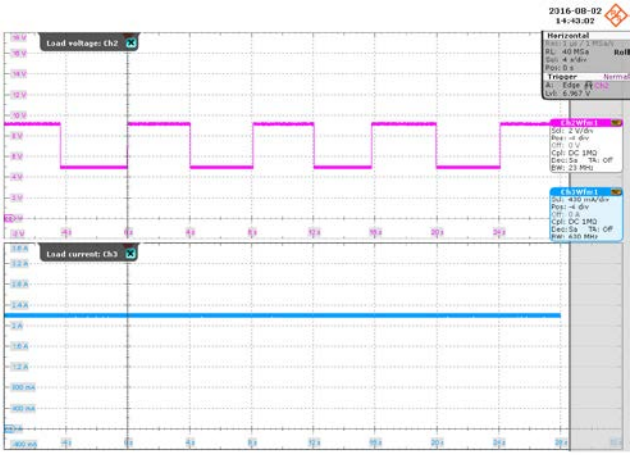

Figure 47 – Output Voltage and Current Waveforms.
85 VAC Input, 2.2 A Load.
Upper: V_{OUT}, 2 V / div., 4 s / div.
Lower: I_{OUT}, 400 mA / div.

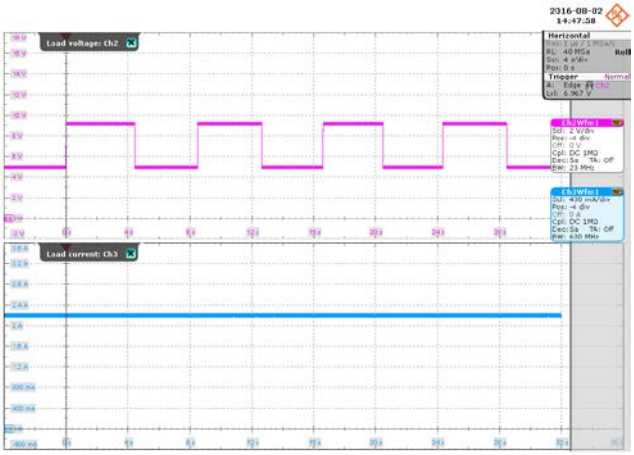

Figure 48 – Output Voltage and Current Waveforms.
265 VAC Input, 2.2 A Load.
Upper: V_{OUT}, 2 V / div., 4 s / div.
Lower: I_{OUT}, 400 mA / div.

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12.4 *Output Ripple Measurements*

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below. The ripple was measured at the end of a Google type-C cable. The load end of the type-C cable was connected to the Weltrend host emulator board.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

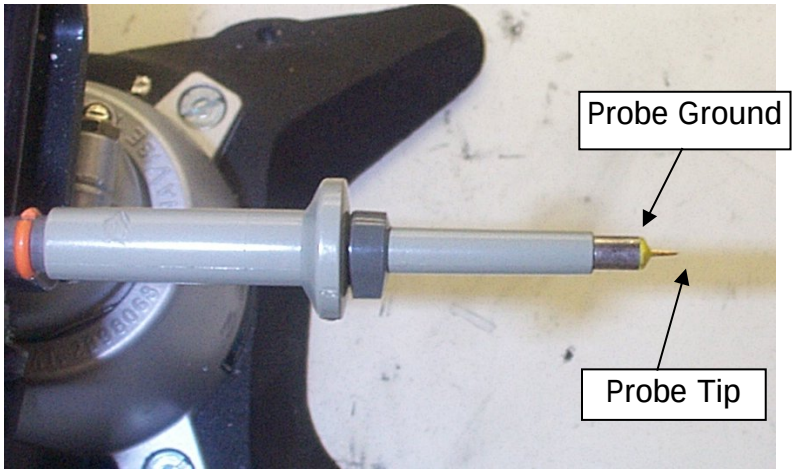


Figure 49 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

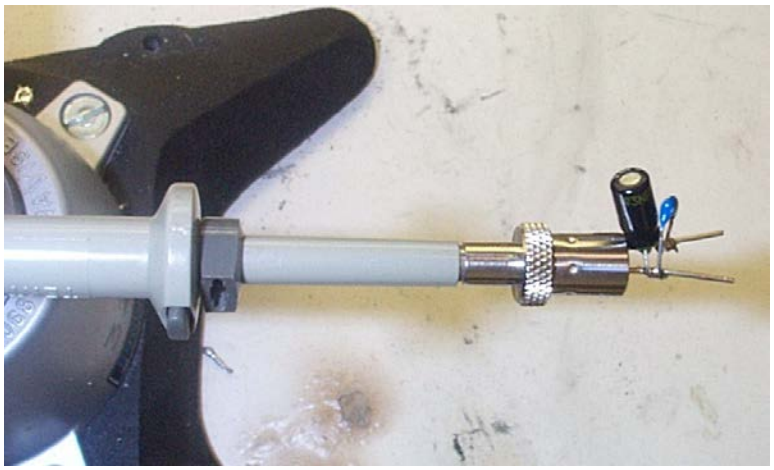
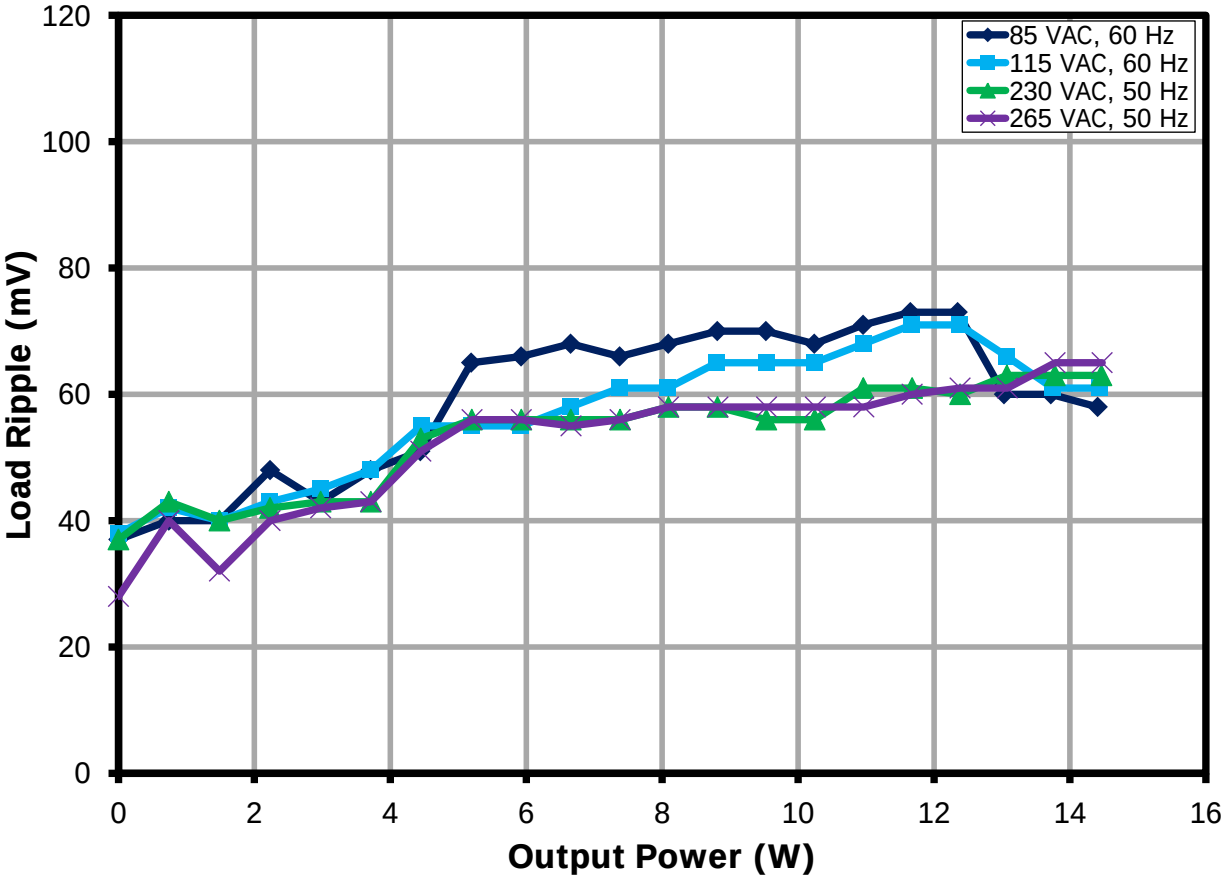


Figure 50 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.4.2 Ripple Amplitude vs. Line

12.4.2.1 5.0 V



Input	85 VAC	115 VAC	230 VAC	265 VAC
Max Ripple (mV)	73	71	63	65

Figure 51 – Ripple Amplitude vs. Output Power 5 V.

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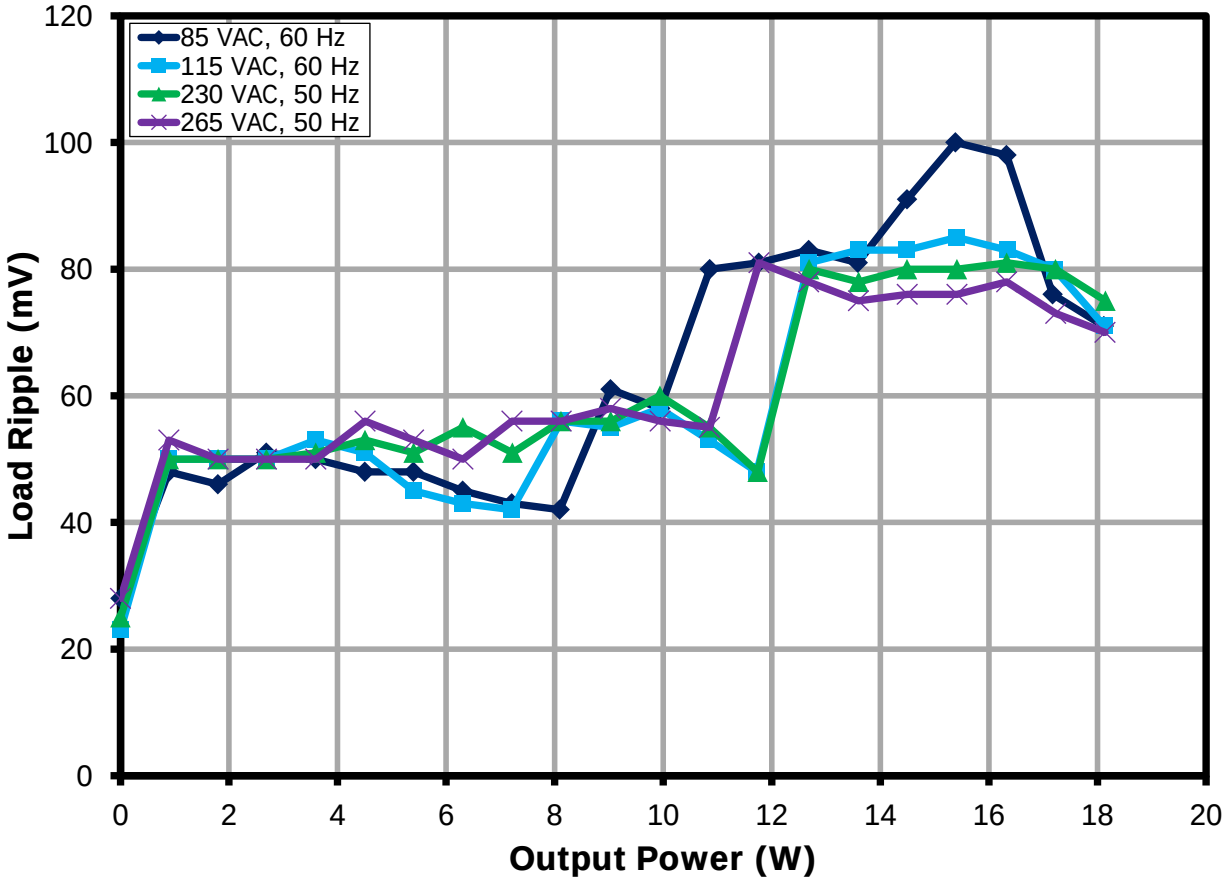
12.4.2.2 9.0 V



Input	85 VAC	115 VAC	230 VAC	265 VAC
Max Ripple (mV)	100	85	81	81

Figure 52 – Ripple Amplitude vs. Output Power 9 V.

12.4.2.3 5 V

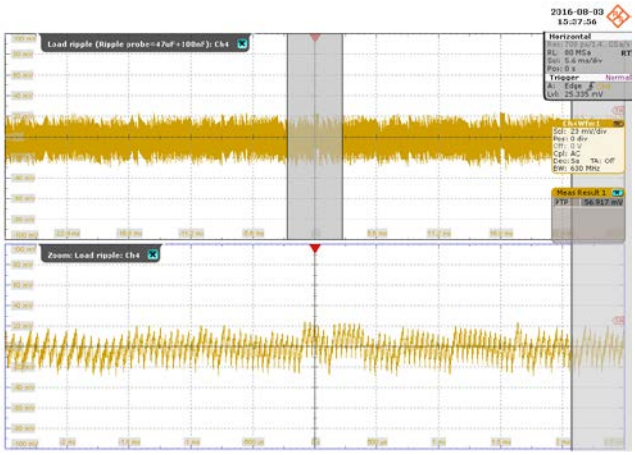


Figure 53 – Output Ripple at End of Cable.
85 VAC Input 5.0 V, 3 A Load.
V_{OUT}: 20 mV / div., 5.6 ms / div.

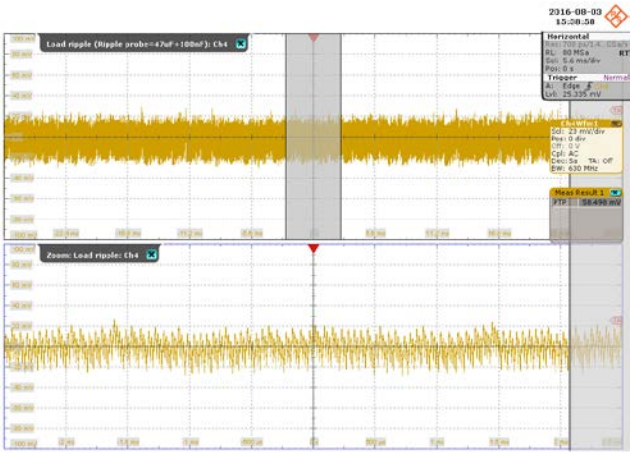


Figure 54 – Output Ripple at End of Cable.
265 VAC Input 5.0 V, 3 A Load.
V_{OUT}: 20 mV / div., 5.6 ms / div.

12.4.2.4 9 V

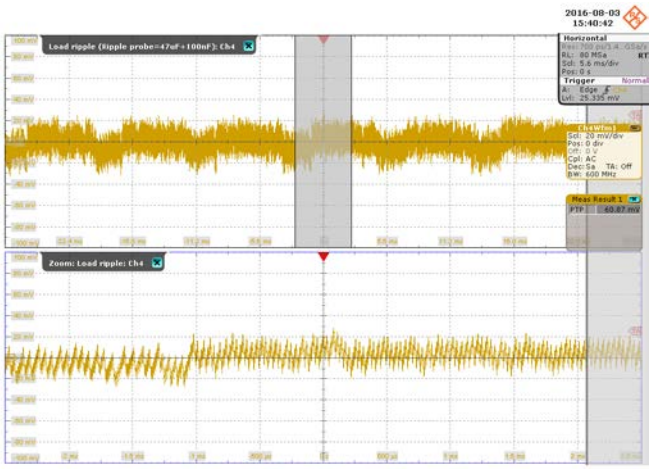


Figure 55 – Output Ripple at End of Cable.
85 VAC Input, 9.0 V, 2 A Load.
V_{OUT}: 20 mV / div., 5.6 ms / div.

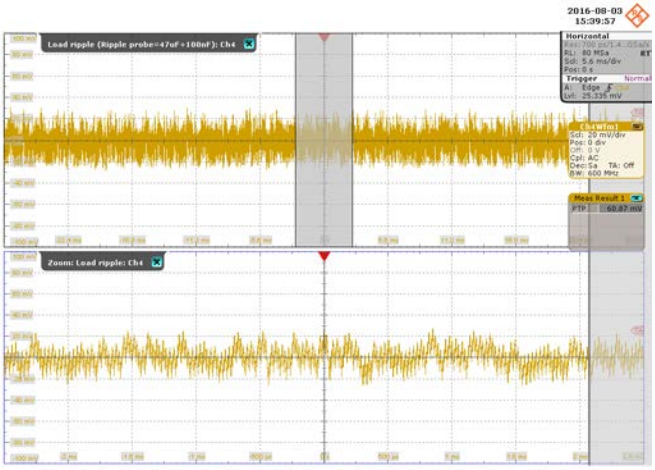


Figure 56 – Output Ripple at End of Cable.
265 VAC Input 9.0 V, 2 A Load.
V_{OUT}: 20 mV / div., 5.6 ms / div.

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13 Conducted EMI

13.1 *Floating Output (QPK / AV)*

13.1.1 5 V, 3 A

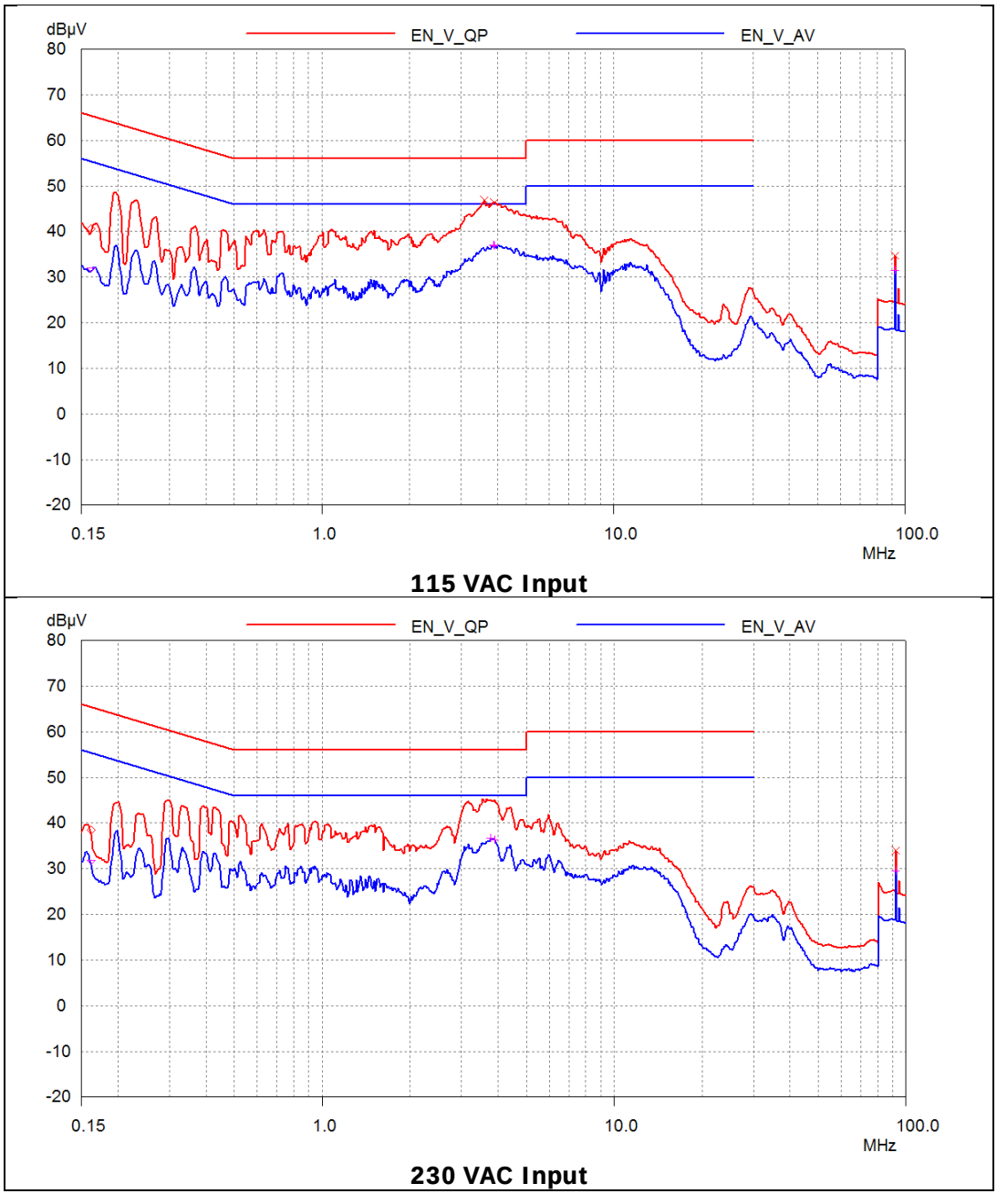

Figure 57 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].

13.1.2 9 V, 2 A

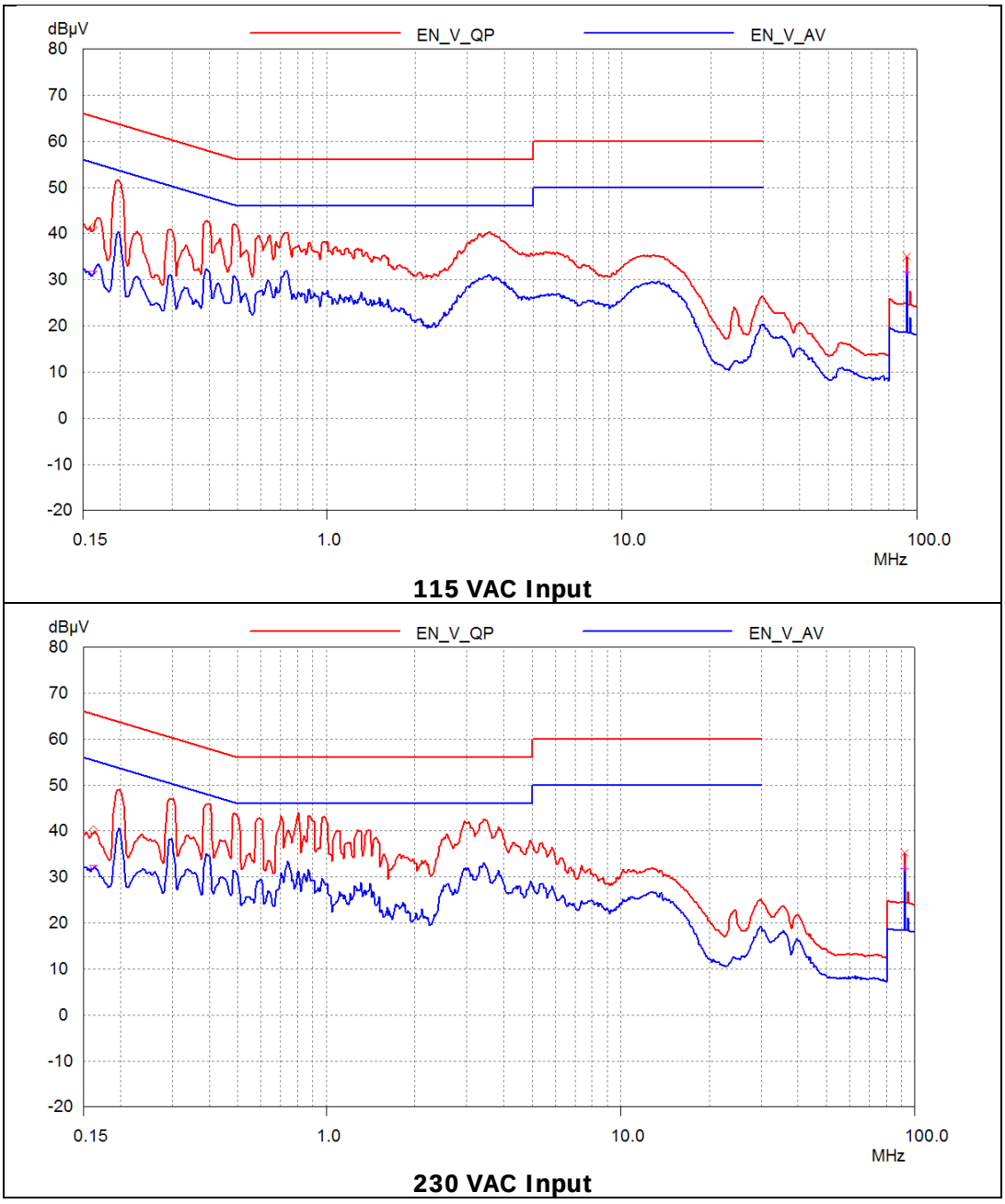

Figure 58 – Floating Ground EMI, 9 V / 2 A Load [Line Scan].

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13.2 *Artificial Hand Ground (QPK / AV)*

13.2.1 5 V, 3 A

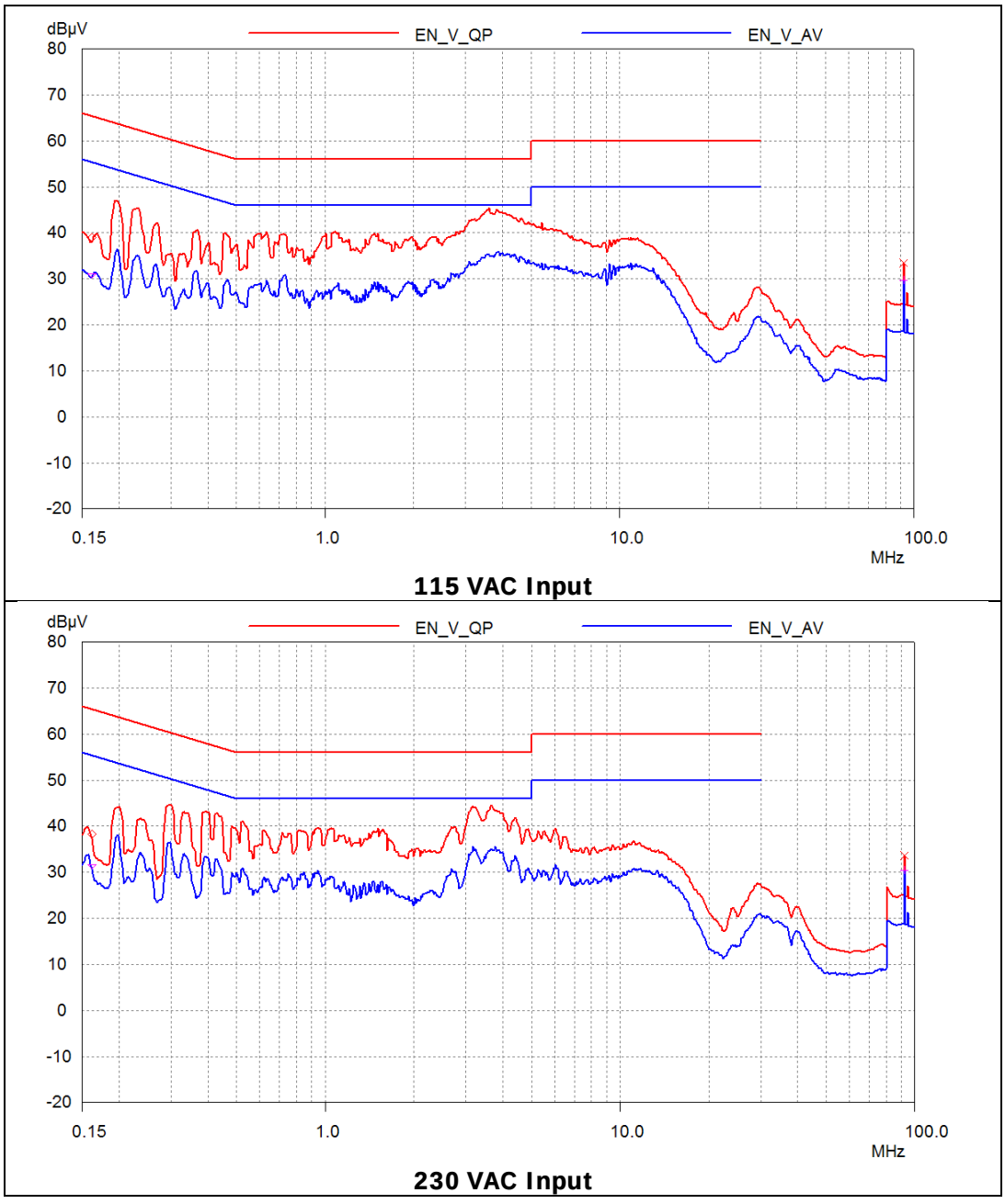

Figure 59 – Artificial Hand Ground EMI, 5 V / 3 A Load [Line Scan].

13.2.2 9 V, 2 A

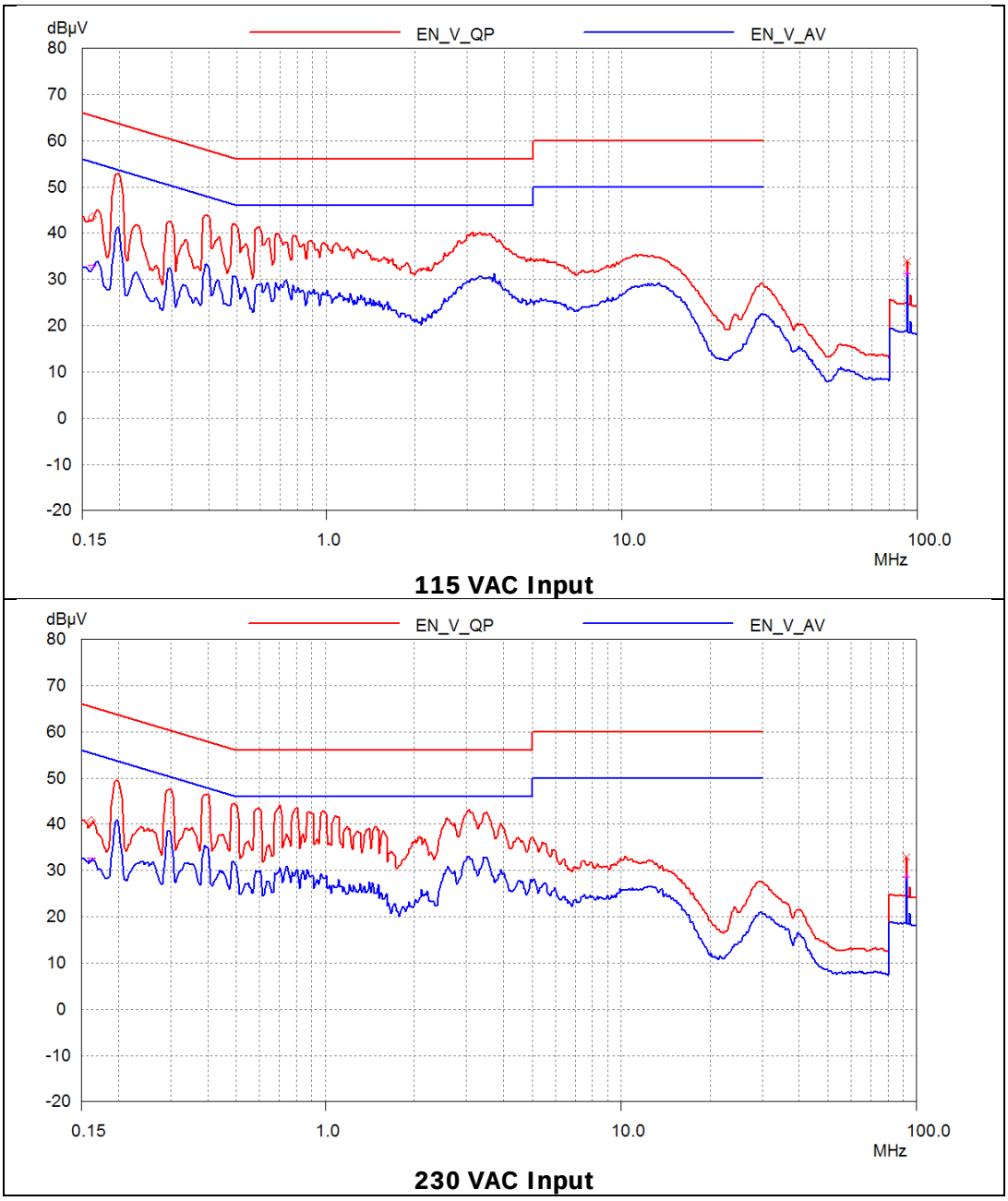

Figure 60 – Artificial Hand Ground EMI, 9 V / 2 A Load [Line Scan].

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13.3 *Earth Ground (QPK / AV)*

13.3.1 5 V, 3 A

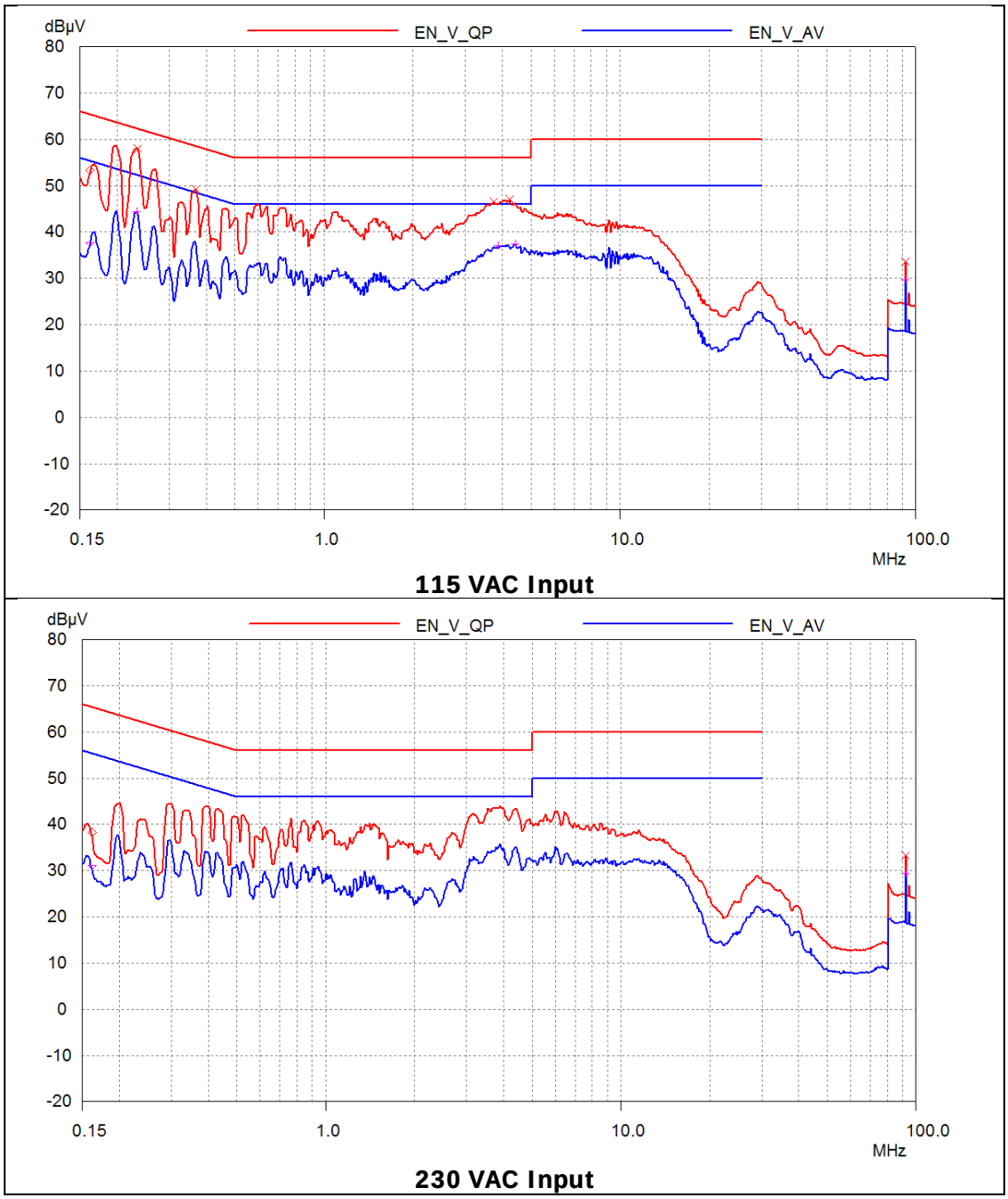

Figure 61 – Earth Ground EMI, 5 V / 3 A Load [Line Scan].

13.3.2 9 V, 2 A

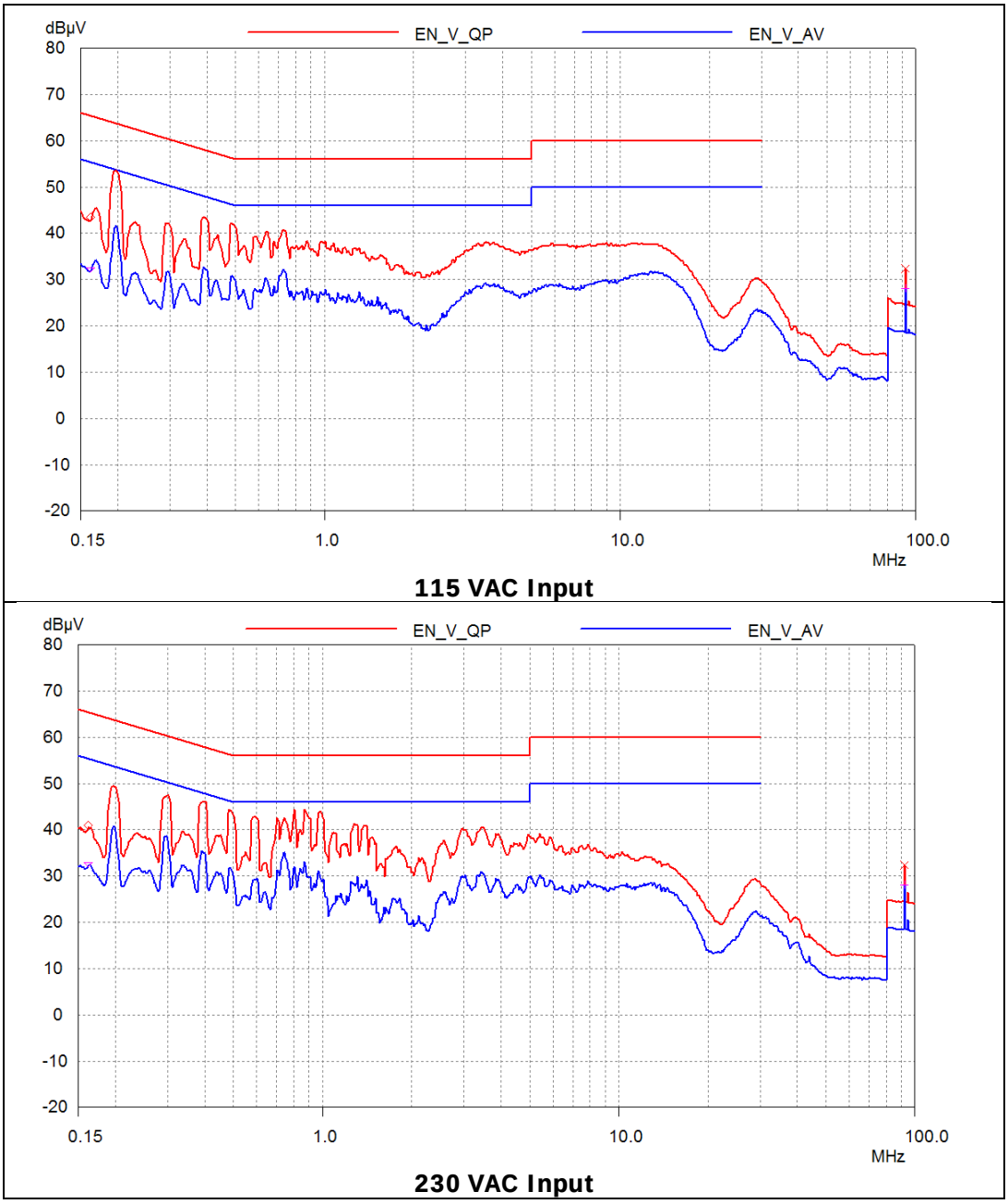

Figure 62 – Earth Ground EMI, 9 V / 2 A Load [Line Scan].

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14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
01-Mar-17	ID	1.0	Initial Release	Apps & Mktg
19-Apr-17	ID	1.1	Updated Magnetics Information	

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