VIA Labs, Inc.

VLI-VP300 + SDT30A120CT-AP3108

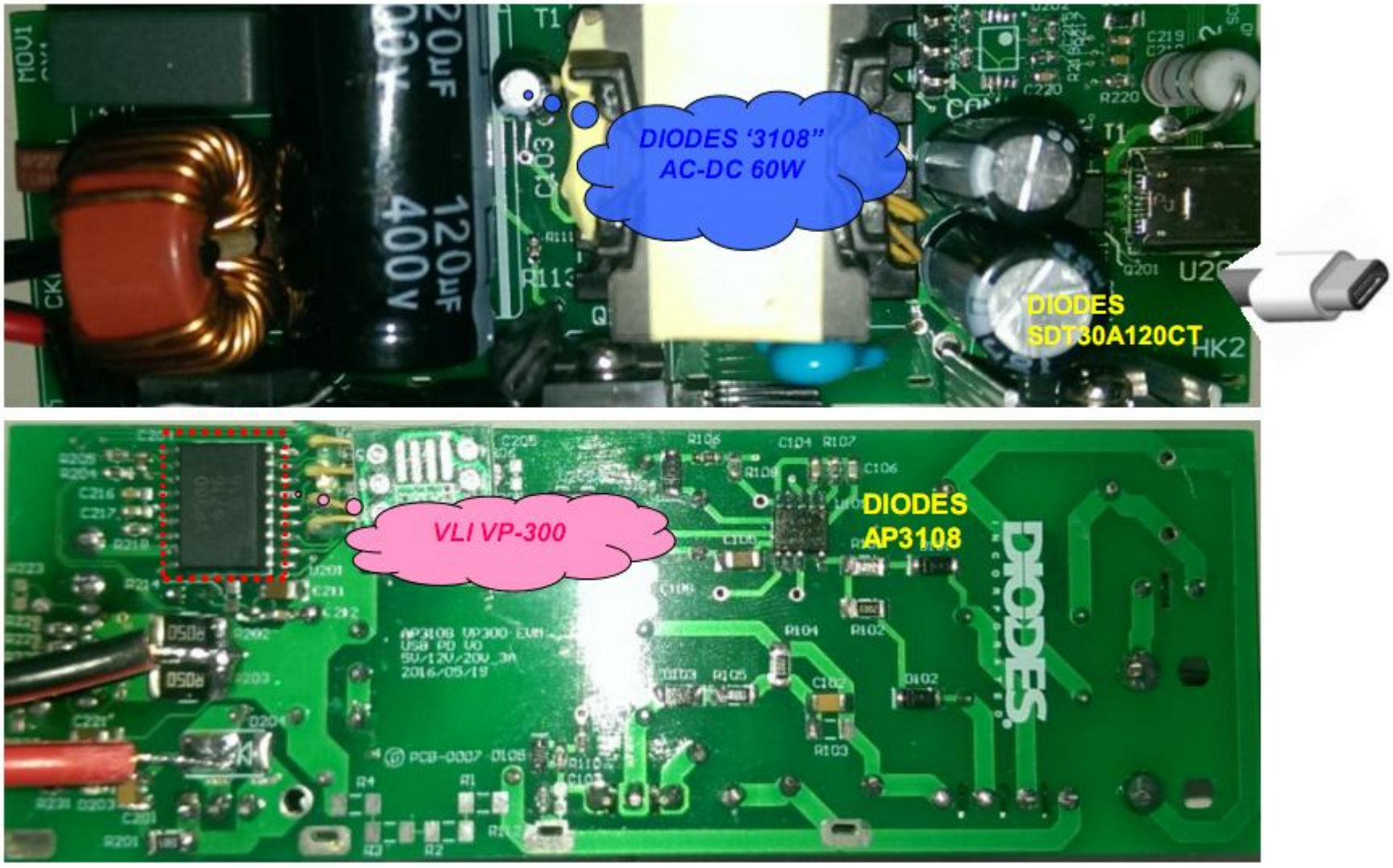
USB PD Compliance test report

Document date: 2016, 06, 30

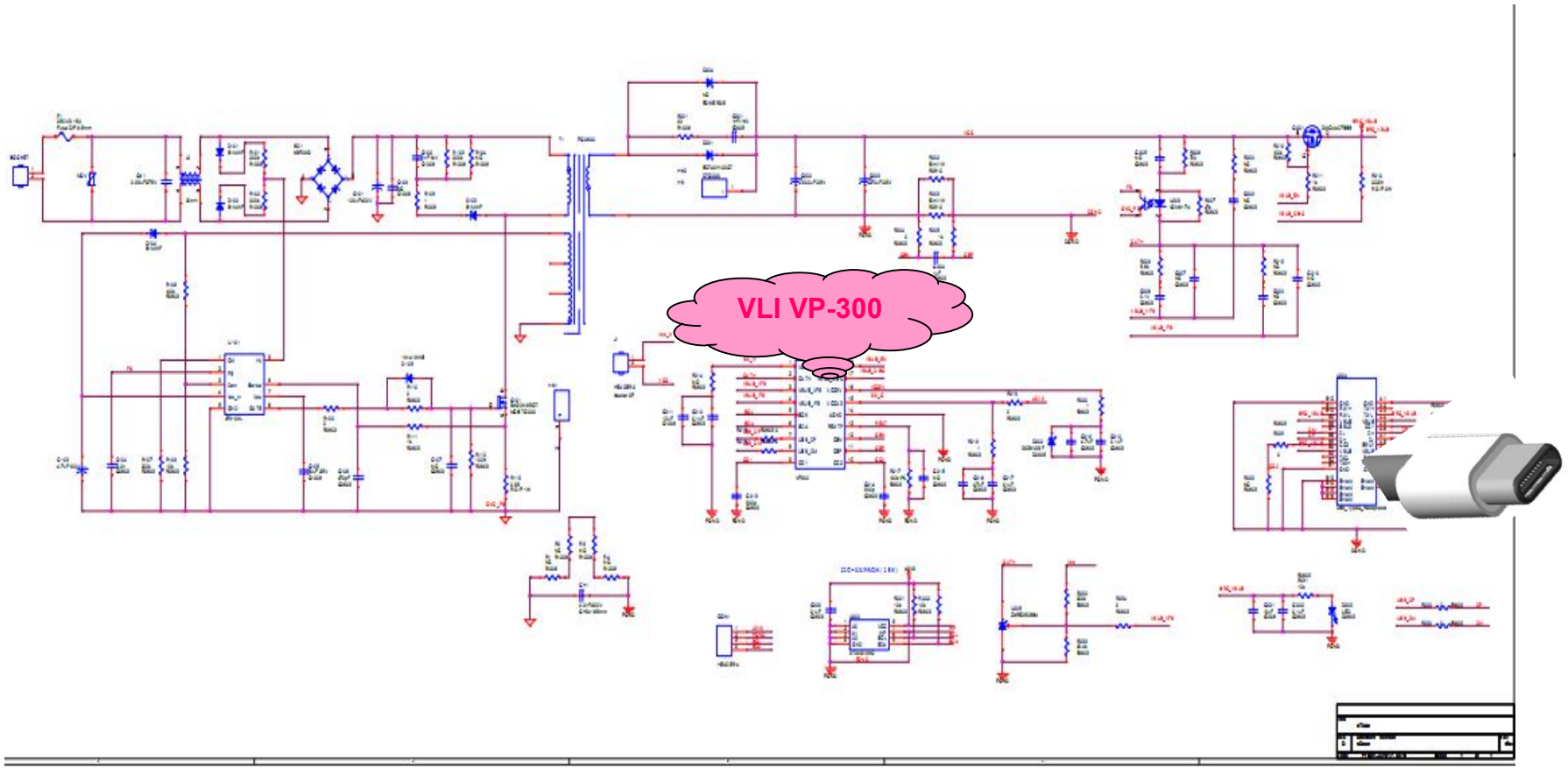
Document author: Benny Wang

Type-C PD System Platform

- **Svstem Platform (Board Size L:110mm : W:38mm)**



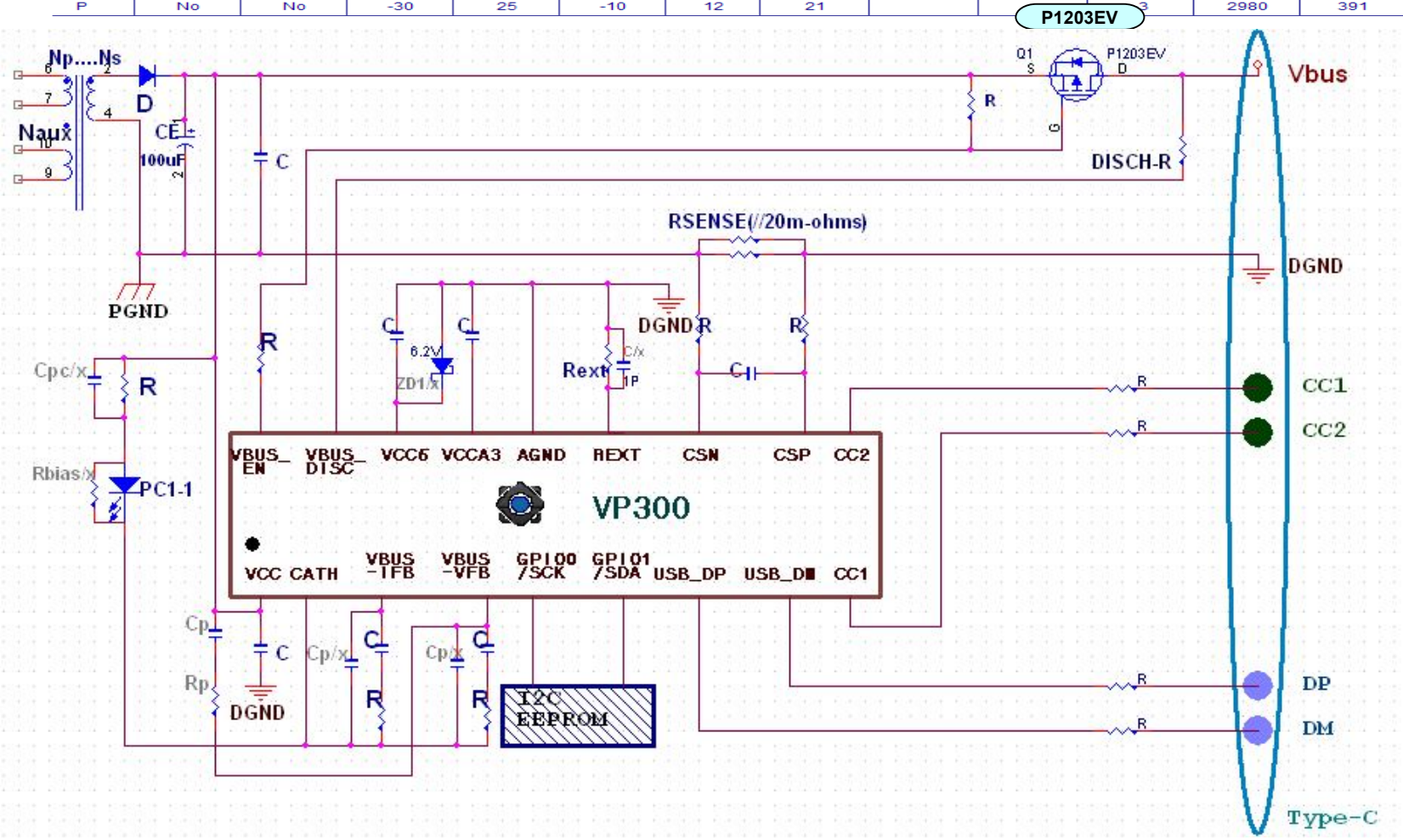
USB PD for Wall Adapter (Type C)



VLI VP300 Application

- **Example of Application**

Type	ESD Diode	Schottky Diode	V_{DS} (V)	V_{GS} (±V)	I_D (A)	$R_{DS(ON)}$ mΩ max at 10V	at 4.5V	at 2.5V	at 1.8V	V_{GS} (th) max	Typical Ciss (pF)	Typical Crss (pF)	Typical Qg (nC)
P	No	No	-30	25	-10	12	21			3	2980	391	64



VP300 for Wall Adapter (Type C)

Introduction

The VP300 is a USB Power Delivery controller which is compliant with USB Type-C Cable Connector Specification Release 1.2 and USB Power Delivery Specification Revision 2_0 V1.0.

The VP300 could automatic detect the attachment and detachment of Type-C port to negotiate capabilities and to support up to 100W (20V * 5A) of power over Type-C connector and Cable.

VP-300 for USB PD (Type C) Controller

Features

- **Automatic detection the attachment and detachment of Type-C port.**
- **Provide the selection of VBUS PD (5V/5A~20V/5A) profile capabilities.**
- **Support baseband BMC Hardware Coding/De-coding for USB PD Type-C specification.**
- **Provide VCONN application with maximum 70 m-W (Application to E-Marked Cable).**
- **Support Battery Charge 1.2 and Quick Charge 3.0 specification.**
- **High Integration for VLI-VP300**
  LDO-5V, TL431, Current –Sensing Amplifier, Quick-Discharge pre-driver, 10bits-ADC, VBUS-EN pre-driver, VBUS cable compensation
- **High Safety for VLI-VP300**
  - **VBUS Over Voltage sensing**. (**OVP:** first level and second level protection)
  - **VBUS Over Current sensing**. (**OCP:** first level and second level protection)
  - **VBUS Under Voltage sensing**. (**UVP:** first level and second level protection)
  - **VBUS Short-Circuit sensing**. (**SCP:** second level protection)
  - **VP300 Chip Over Temperature sensing**. (**OTP:** first level protection)
- **Provide the system Error Handle Algorithm.**

VP-300 for Wall Adapter USB PD (Type C) Controller

- **System safety features and power mode features**

Safety Features		Programmable	Power Mode
First Level (Warning Level) Protection			
Firmware ADC for VBUS over voltage protection	VBUS O.V.P	V-Threshold1 and Delay-Time1(S)	Normal Mode
Hardware comparator for VBUS over voltage protection	VBUS O.V.P	V-Threshold2 and Delay-Time2(mS)	Normal Mode
Firmware ADC for VBUS under voltage protection	VBUS U.V.P	V-Threshold3 and Delay-Time3(S)	Normal Mode
Hardware comparator for VBUS under voltage protection	VBUS U.V.P	V-Threshold4 and Delay-Time4(mS)	Normal Mode
Firmware ADC for VBUS over current protection	VBUS O.C.P	I-Threshold5 and Delay-Time5(S)	Normal Mode
Hardware comparator for VBUS over current protection	VBUS O.C.P	I-Threshold6 and Delay-Time6(mS)	Normal Mode
Hardware comparator for VCONN over current protection	VCONN O.C.P	I-Threshold7and Delay-Time7(mS)	Normal Mode
Hardware comparator for VBUS short circuit protection	VBUS S.C.P	I-Threshold8 and Delay-Time8(uS)	Normal Mode
Internal thermal sensing protection	System O.T.P	I-Threshold9 and Delay-Time9(S)	Normal Mode
Watchdog timer protection	System I.S.R	NA	Normal Mode
Second Level (Critical Level) Protection			
Safety for VBUS over voltage protection	System Fault	Retry-Times	Shutdown Mode
Safety for VBUS over current protection	System Fault	Retry-Times	Shutdown Mode
Failed voltage and current measurement	System Fault	NA	Shutdown Mode
External P-MOSFET failure or loss of P-MOSFET control	System Fault	NA	Shutdown Mode
VBUS Compensation			
R-sense Resistances compensation	TBD	Resistances m-Ω	Normal Mode
Cable Resistances compensation	TBD	Resistances m-Ω	Normal Mode

Power Mode	Description
Normal Mode	The VP-300 performs PD-functions, measurements and protections. The Type-C PD wall adapter is fully functional in this mode.
Suspend Mode	The VP-300 performs as in normal mode but at a dramatically reduced clock rate(32KHz) to lower power consumption. All safety circuitry remains hardware functional in this mode.
Shutdown Mode	In this mode, the external P-MOSFET is disabled and VCC will be vsafe5V. (Support LED display)

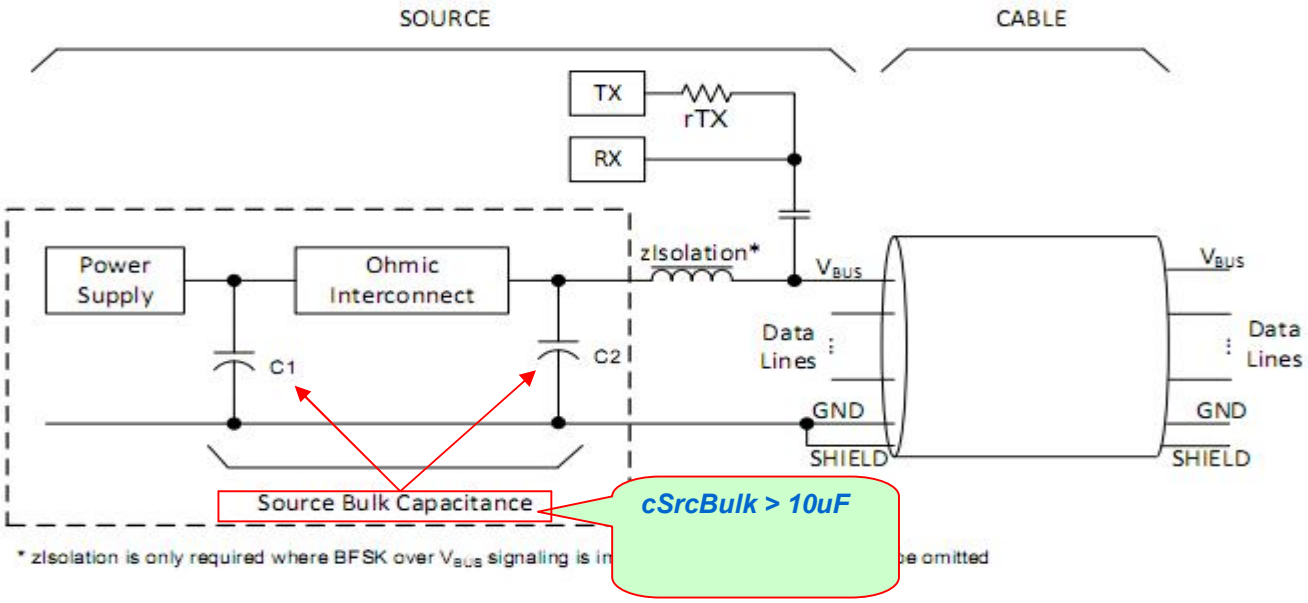
Power Supply (Source Requirements)

- **Source Bulk Capacitance**

  [Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
cSrcBulk	10			uF	Dedicated supply

Figure 7-1 Placement of Source Bulk Capacitance



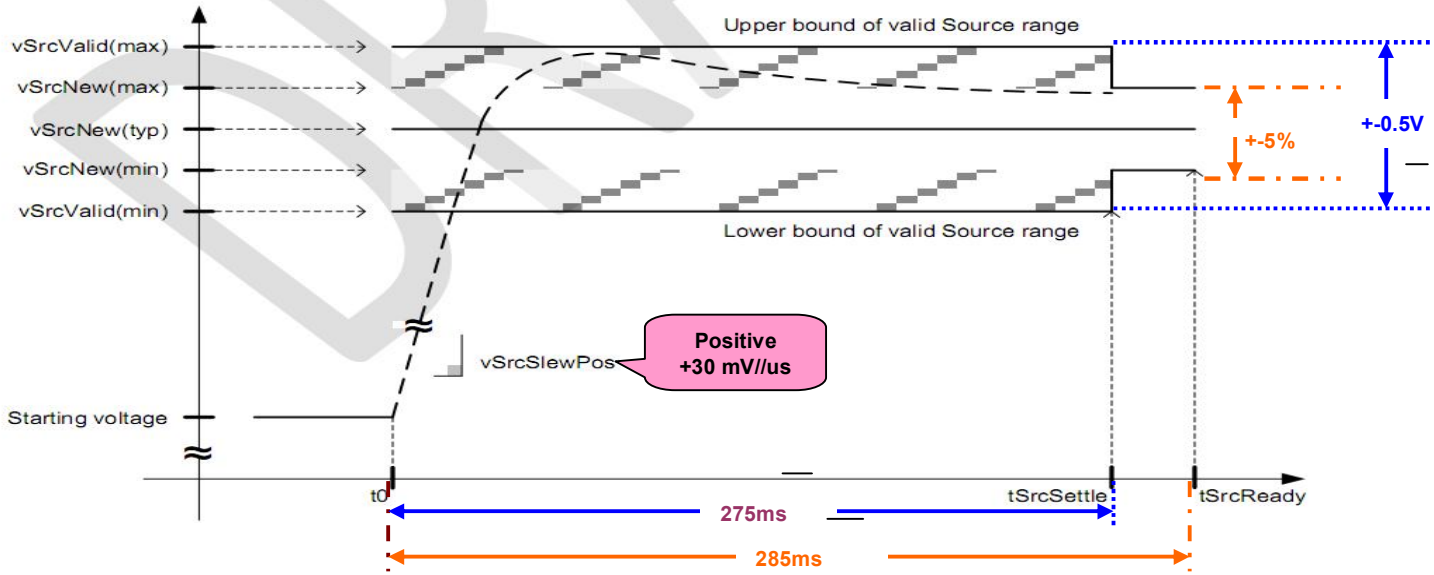
Power Supply (Source Requirements)

- **Positive Voltage Transitions**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
vSrcNew	-5		+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5		+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewPos	NA		30	mV/us	Positive slew rate < +30 mV/us
T0 → tSrcSettle	NA		275	ms	tSrcSettle < 275ms
T0 → tSrcReady	NA		285	ms	tSrcReady < 285ms

Figure 7-2 Transition Envelope for Positive Voltage Transitions



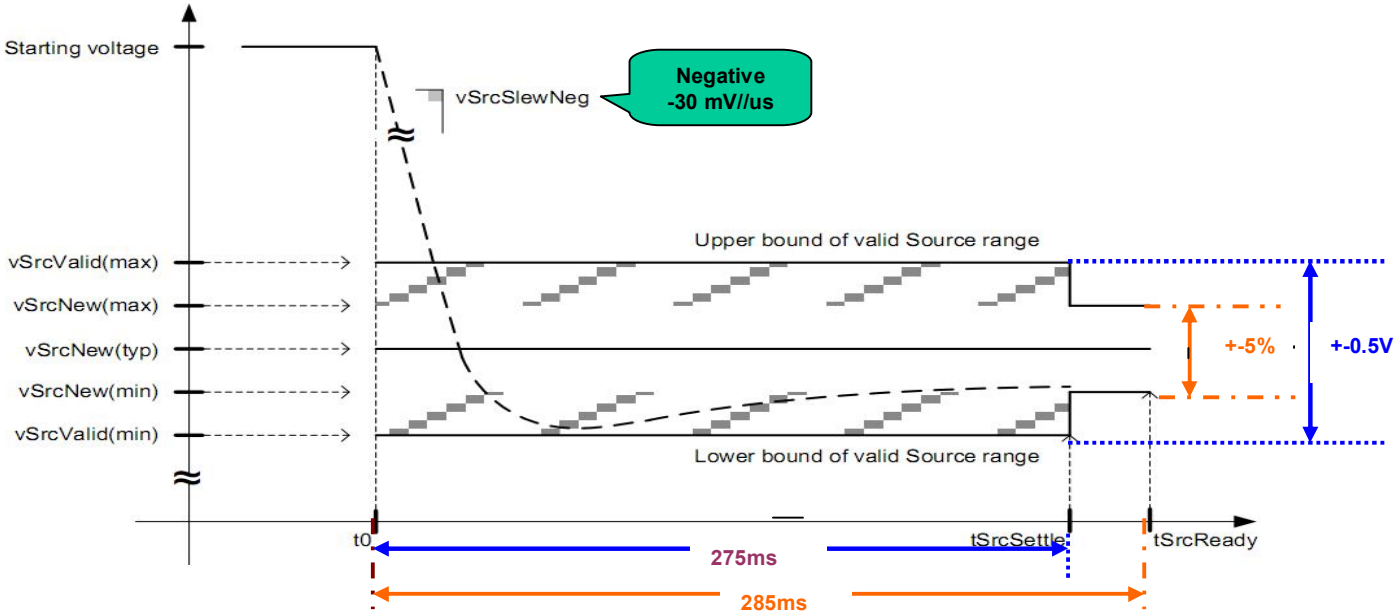
Power Supply (Source Requirements)

- **Negative Voltage Transitions**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
vSrcNew	-5		+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5		+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewNeg	NA		-30	mV/us	Negative slew rate < -30 mV/us
T0 → tSrcSettle	NA		275	ms	tSrcSettle < 275ms
T0 → tSrcReady	NA		285	ms	tSrcReady < 285ms

Figure 7-3 Transition Envelope for Negative Voltage Transitions



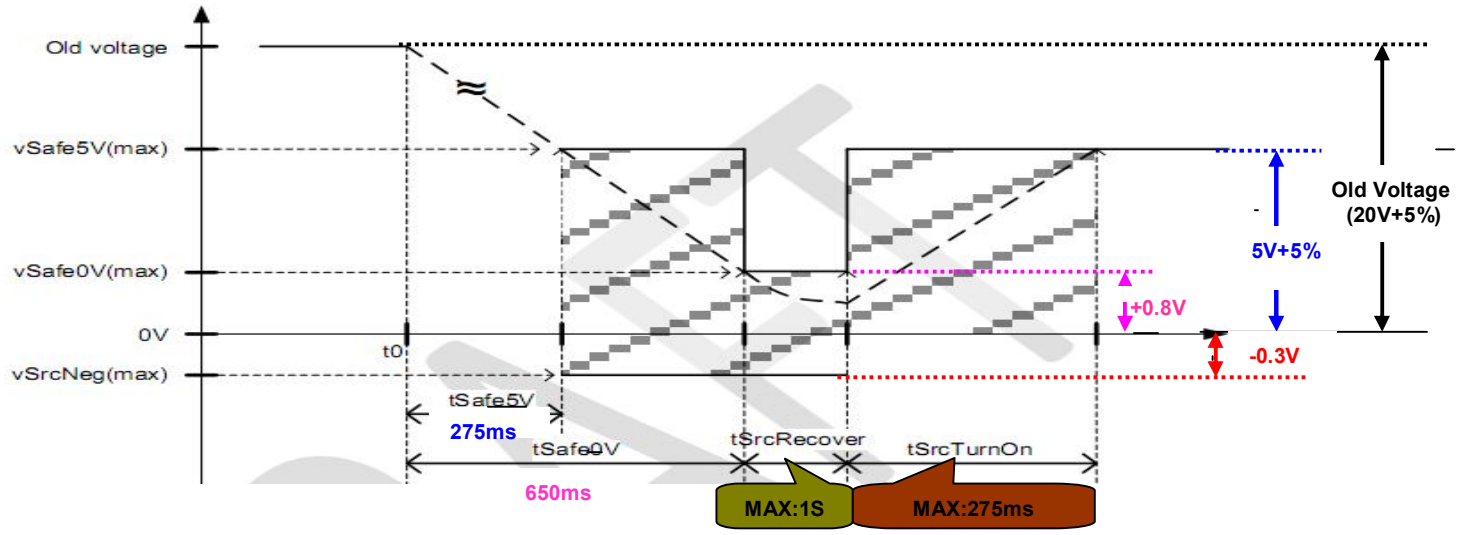
Power Supply (Source Requirements)

- **Response to Hard Reset**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
Old Voltage	-5		+5	%	vSrcOld Voltage MAX:20V+5%
vSafe5V	-5		+5	%	vSafe5V Voltage MAX:5V+5%
vSafe0V	0		+0.8	V	vSafe0V Voltage MAX:0V+0.8V
vSrcNeg	NA		-0.3	V	vSrcNeg Voltage MAX:0V+(-0.3V)
T0 → tSafe5V	NA		275	ms	tSafe5V < 275ms
T0 → tSafe0V	NA		650	ms	tSafe0V < 650ms
tSrcRecover	0.66		1	s	*660ms < tSrcRecover* < 1s (control by PD-Controller)
tSrcTurnOn	NA		275	ms	*tSrcTurnOn* < 275ms

Figure 7-4 Source Response to Hard Reset



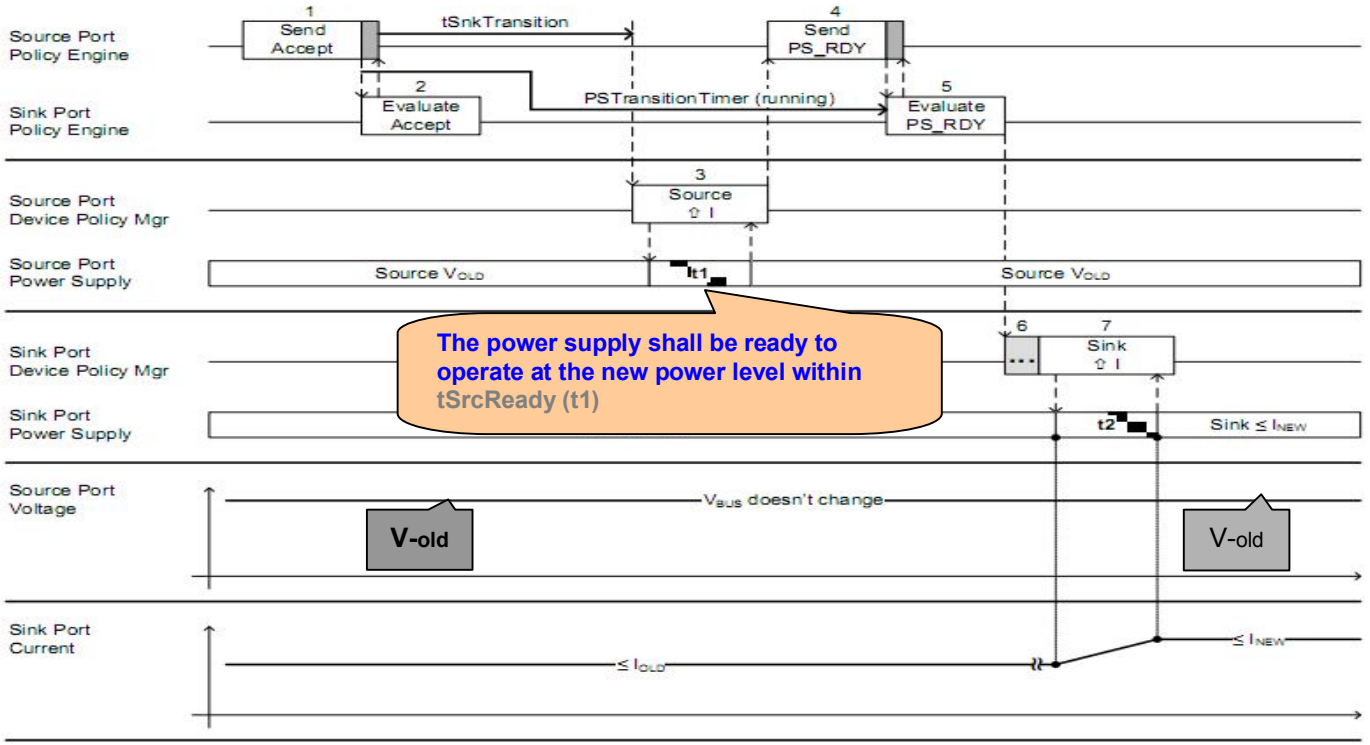
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Increasing the Current**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t1)	NA		285	ms	t1 < 285ms

Figure 7-10 Transition Diagram for Increasing the Current



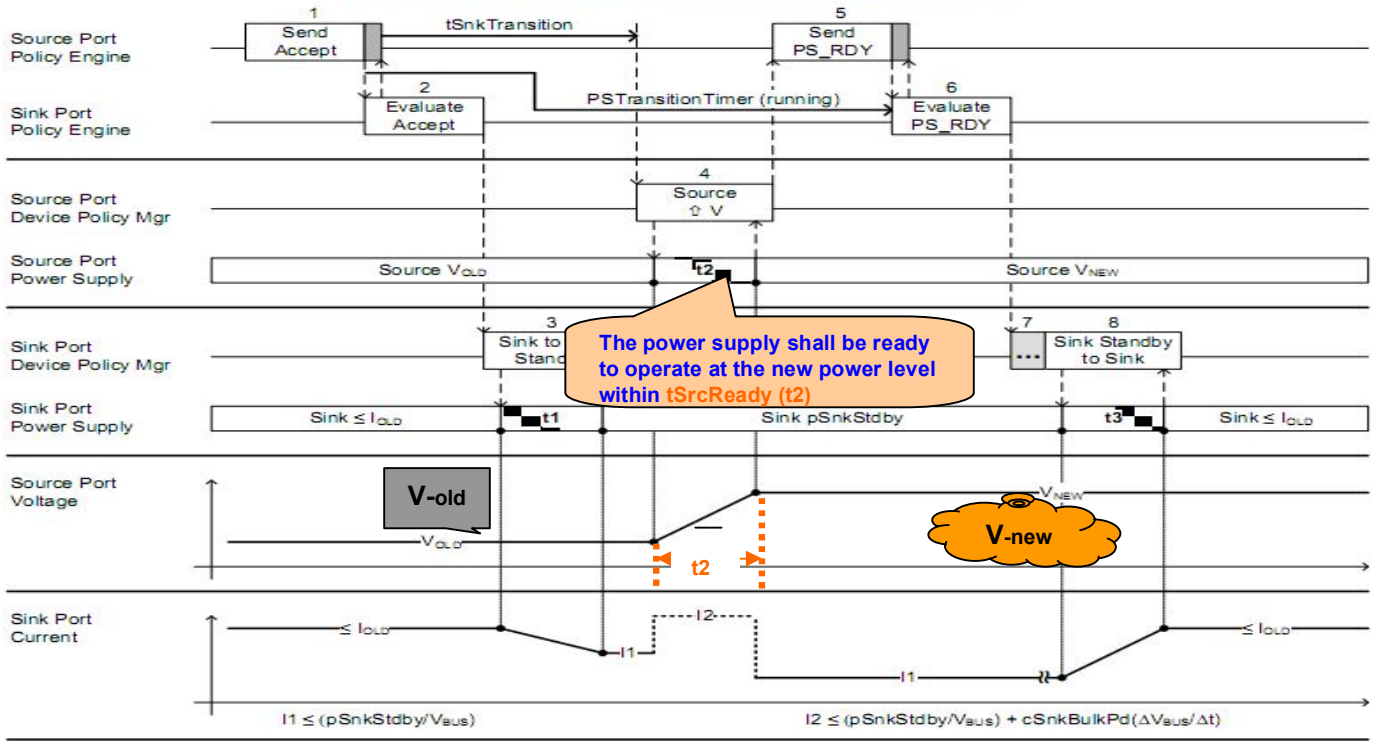
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Increasing the Voltage**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-11 Transition Diagram for Increasing the Voltage



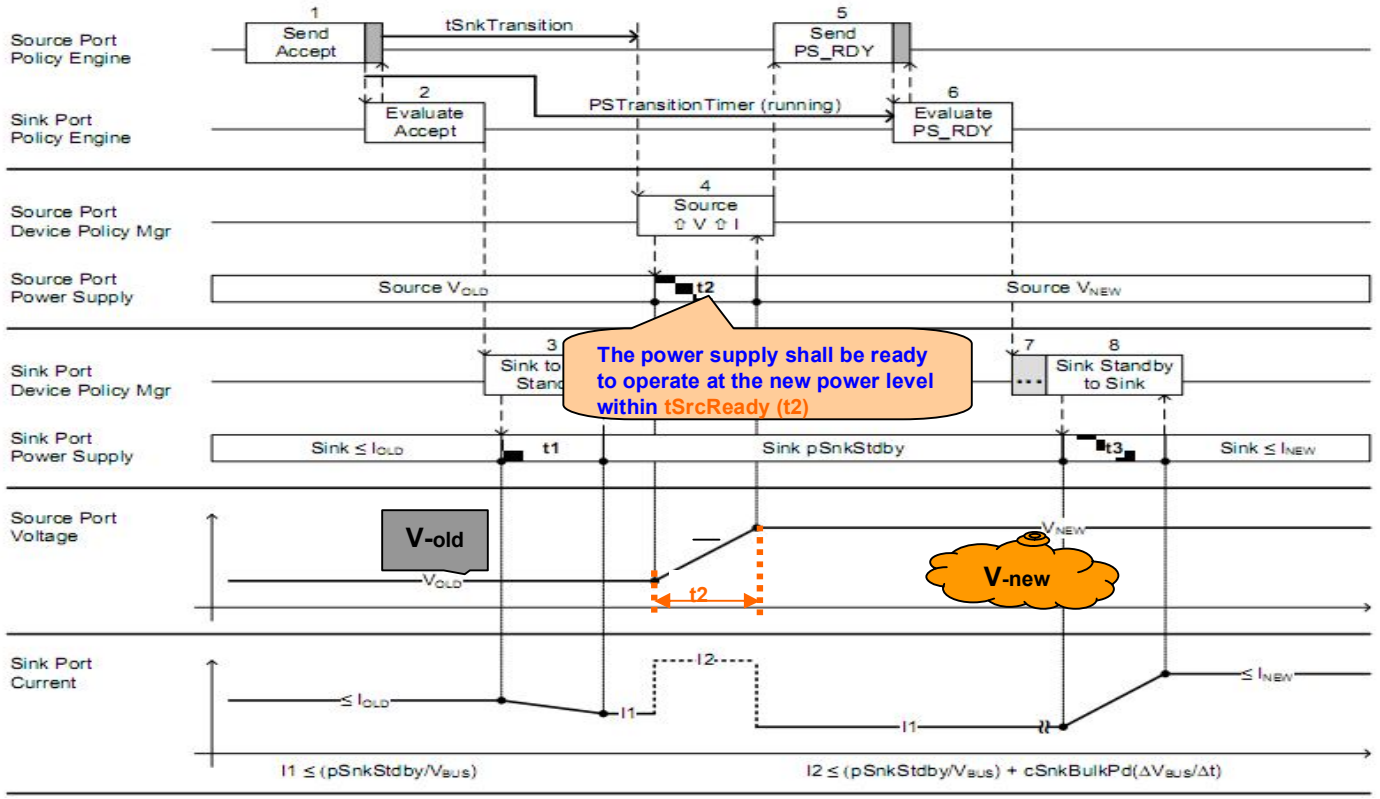
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Increasing the Voltage and Current**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-12 Transition Diagram for Increasing the Voltage and Current



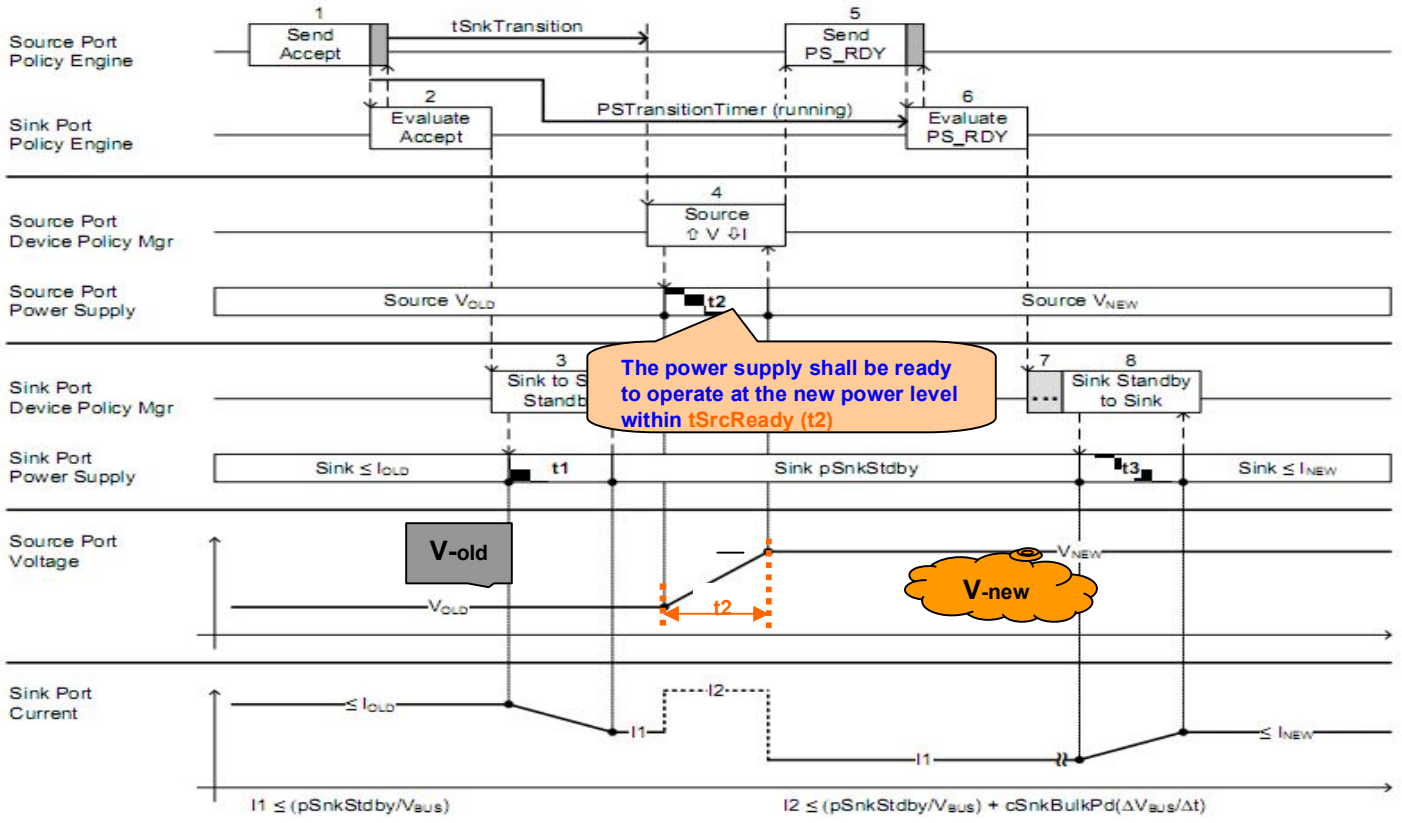
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Increasing the Voltage and Decreasing the Current**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-13 Transition Diagram for Increasing the Voltage and Decreasing the Current



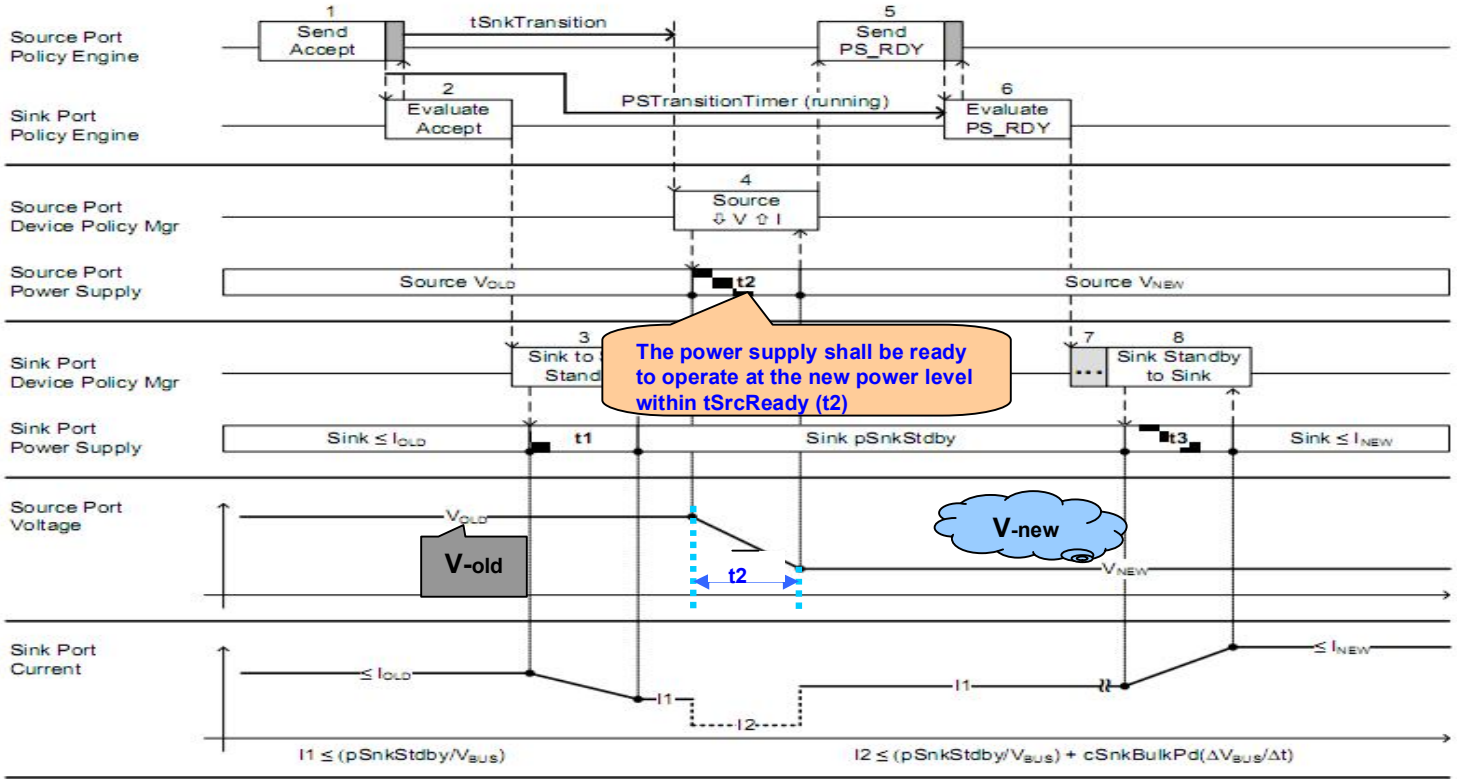
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Decreasing the Voltage and Increasing the Current**

  [Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-14 Transition Diagram for Decreasing the Voltage and Increasing the Current



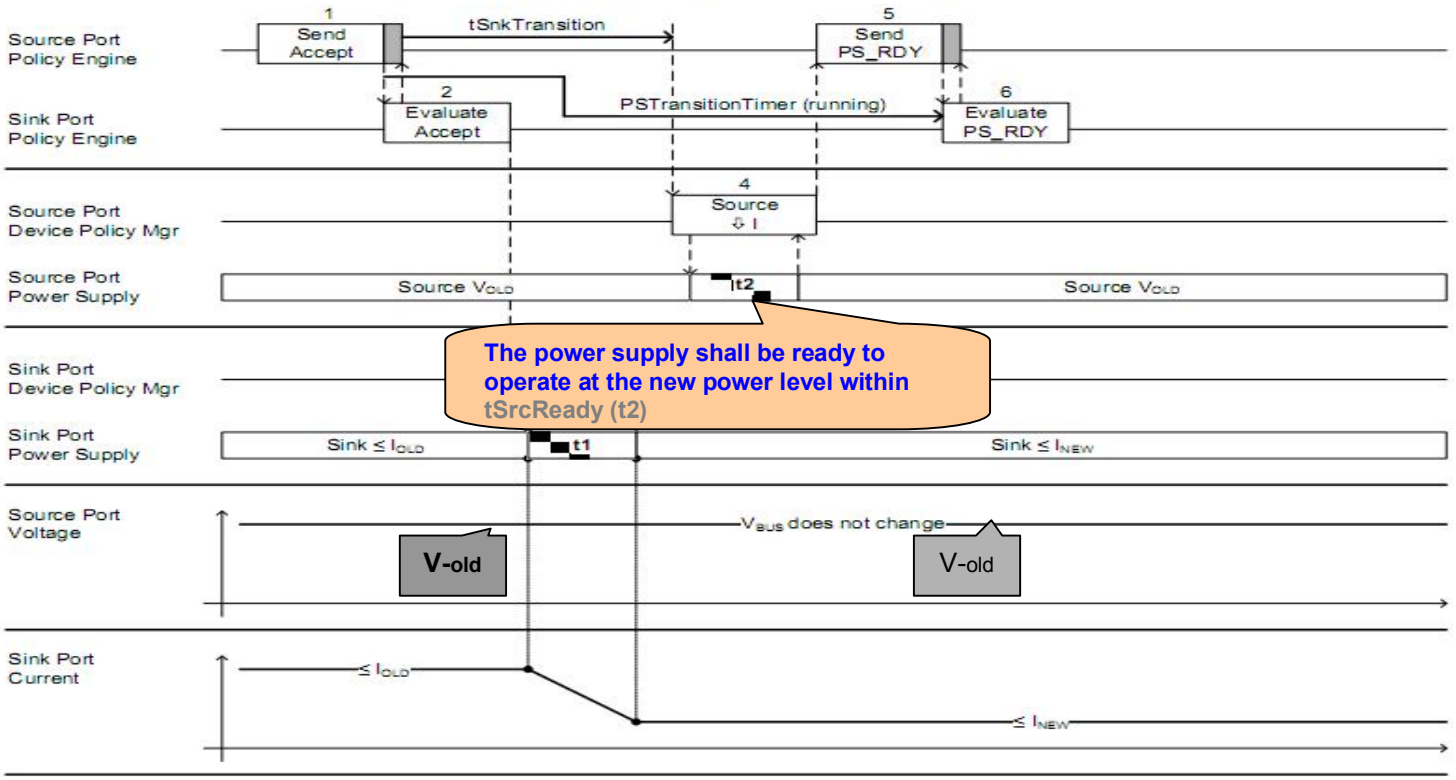
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Decreasing the Current**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-15 Transition Diagram for Decreasing the Current



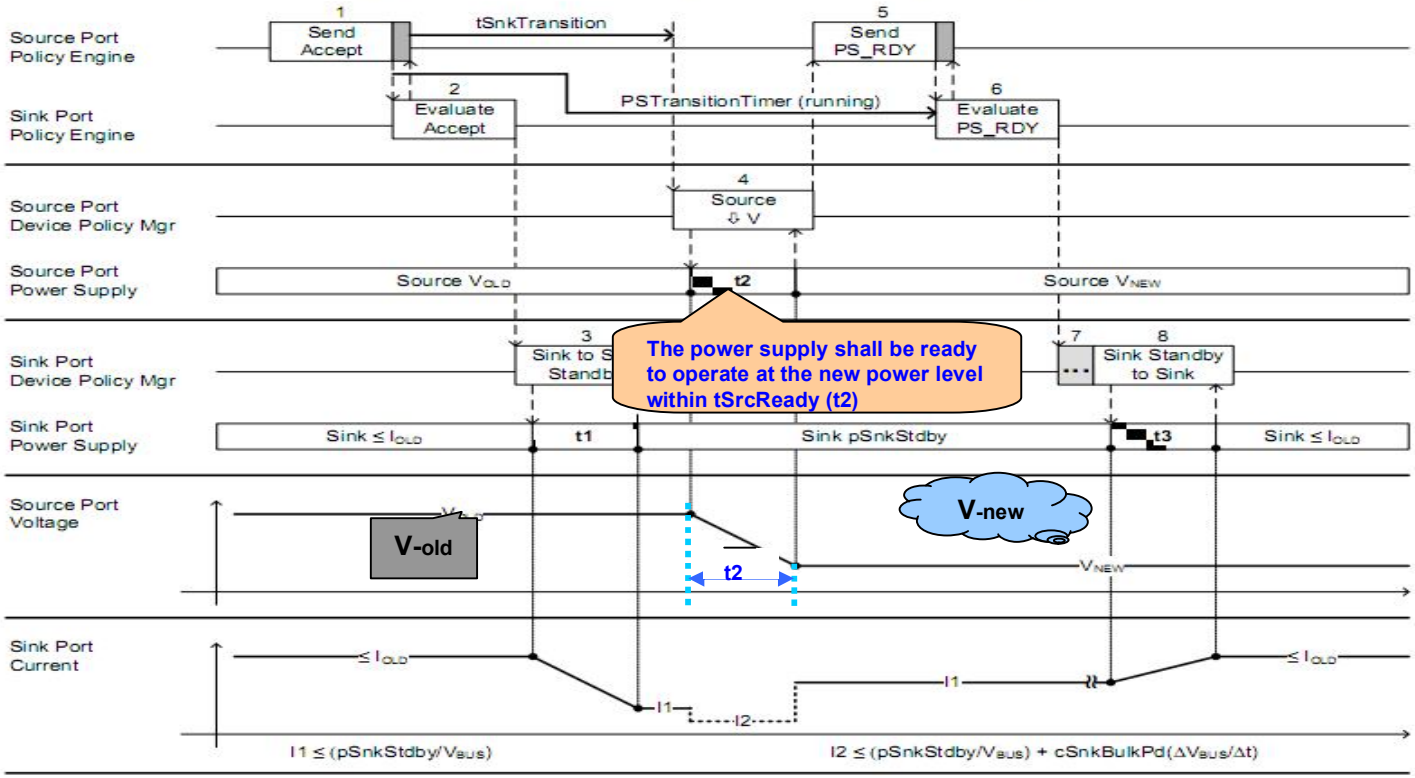
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Decreasing the Voltage**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-16 Transition Diagram for Decreasing the Voltage



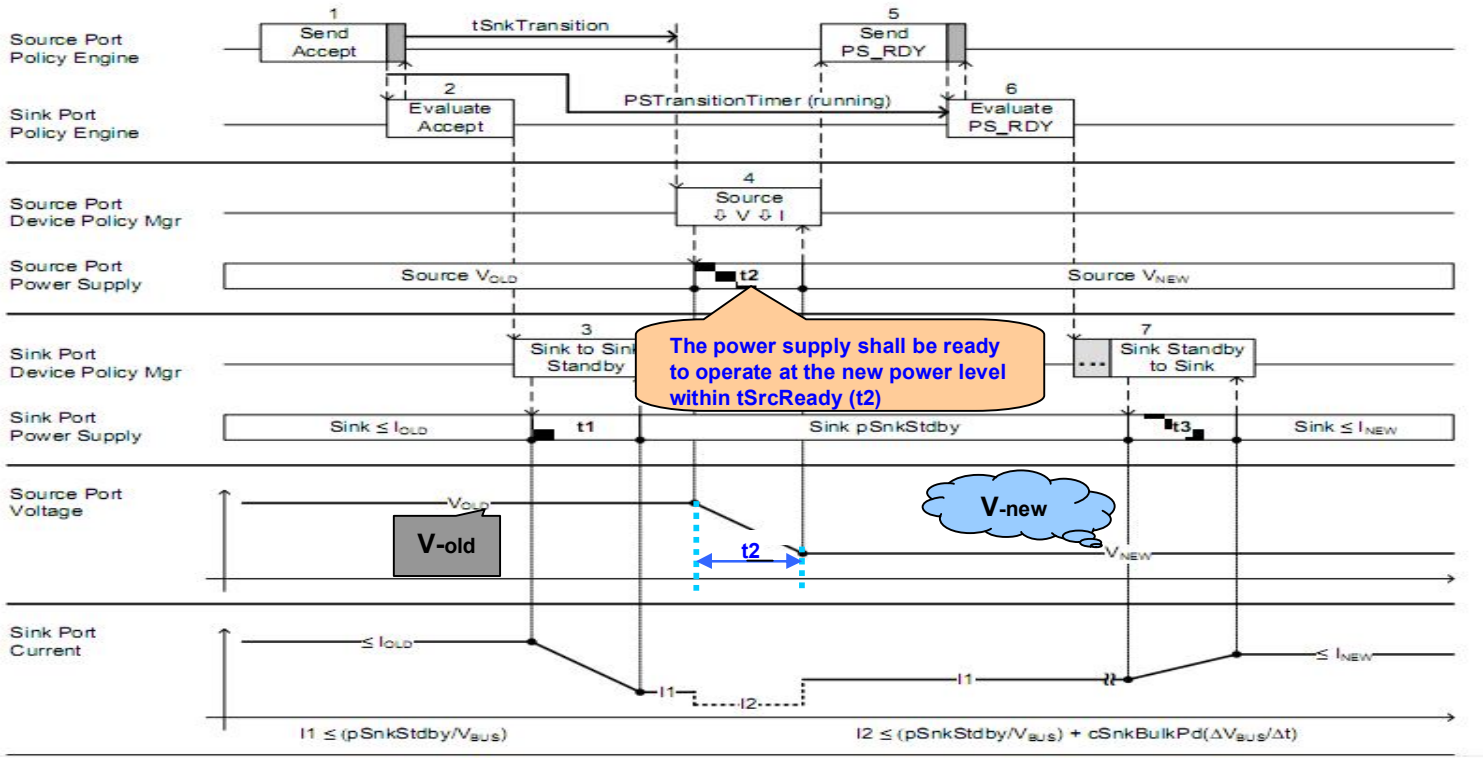
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Decreasing the Voltage and the Current**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-17 Transition Diagram for Decreasing the Voltage and the Current



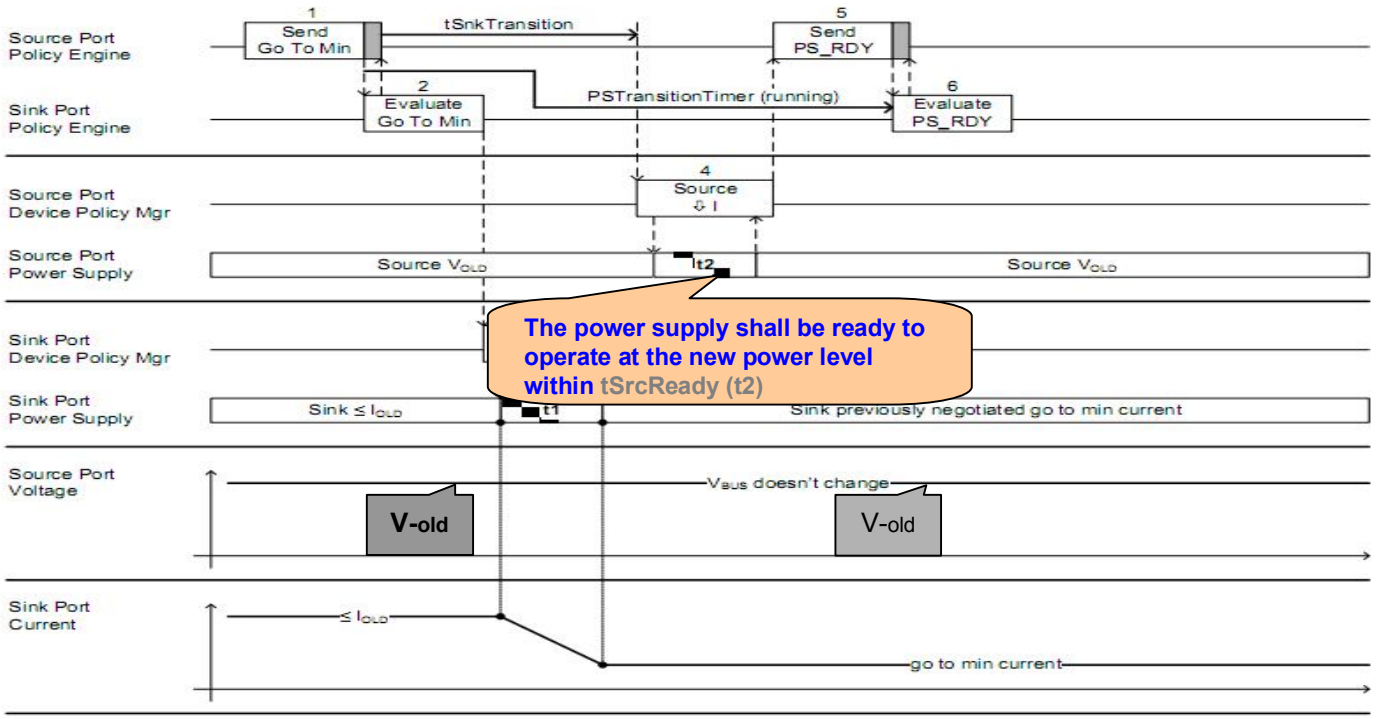
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **GotoMin Current Decrease**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
tSrcReady (t2)	NA		285	ms	t2 < 285ms

Figure 7-20 Transition Diagram for a GotoMin Current Decrease



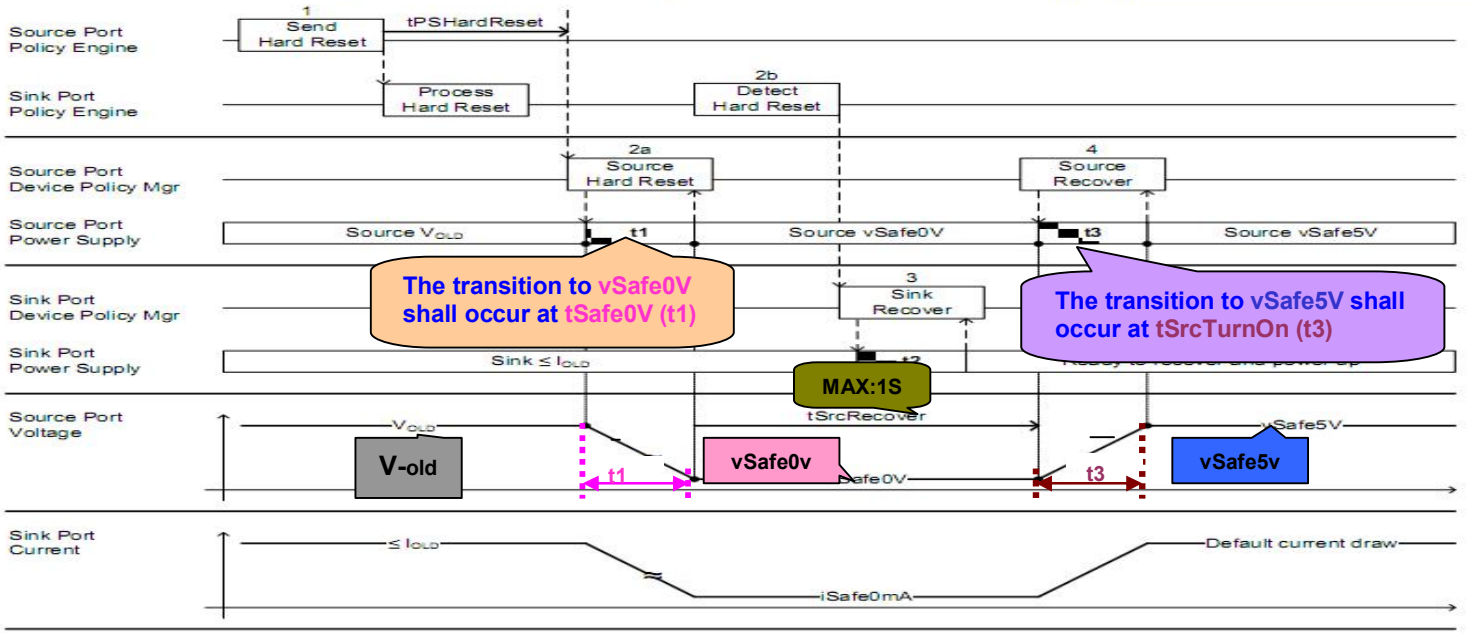
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Source Initiated Hard Reset**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
Old Voltage	-5		+5	%	vSrcOld Voltage MAX:20V+5%
vSafe5V	-5		+5	%	vSafe5V Voltage MAX:5V+5%
vSafe0V	0		+0.8	V	vSafe0V Voltage MAX:0V+0.8V
vSrcNeg	NA		-0.3	V	vSrcNeg Voltage MAX:0V+(-0.3V)
T0 → tSafe5V	NA		275	ms	tSafe5V < 275ms
T0 → tSafe0V(t1)	NA		650	ms	tSafe0V < 650ms
tSrcRecover	0.66		1	s	*660ms < tSrcRecover* < 1s (control by PD-Controller)
tSrcTurnOn(t3)	NA		275	ms	*tSrcTurnOn* < 275ms

Figure 7-21 Transition Diagram for a Source Initiated Hard Reset



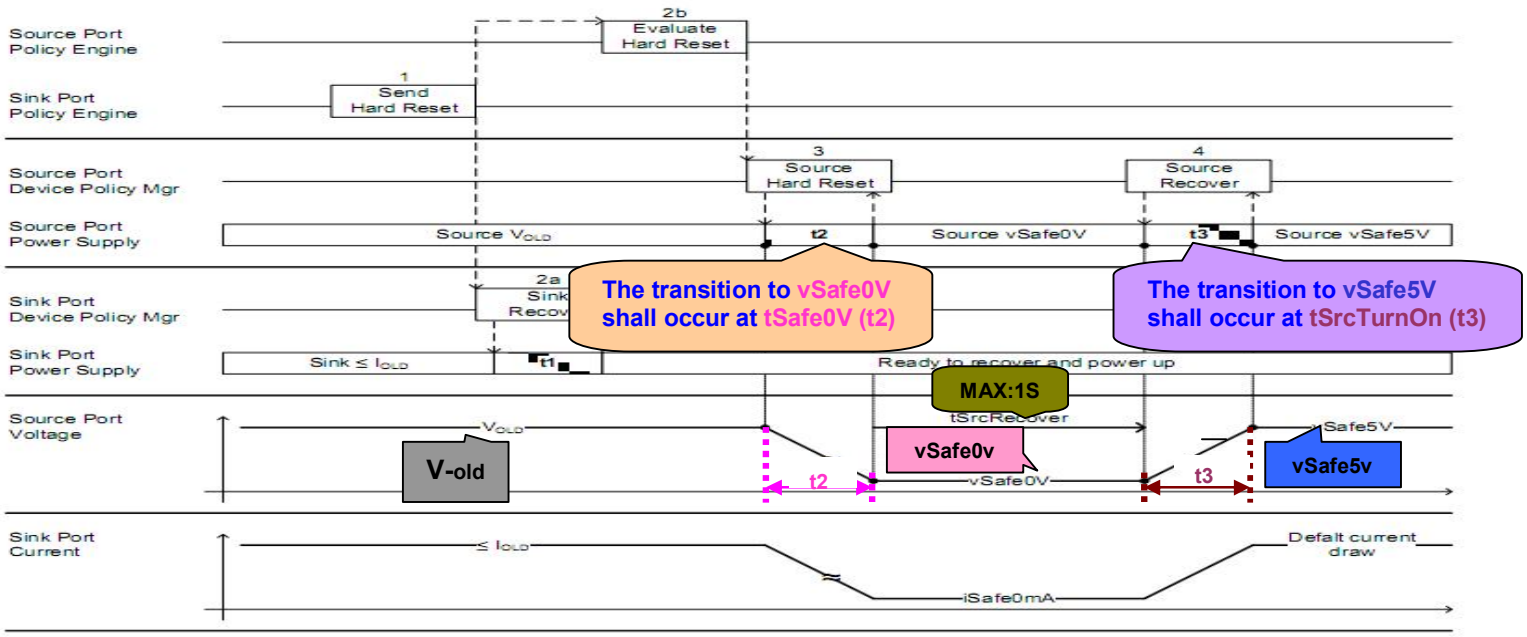
USB PD for Wall Adapter (Type C) System (Source Requirements)

- **Sink Initiated Hard Reset**

[Parameters]:

Parameter	MIN	TYP	MAX	UNIT	Description
Old Voltage	-5		+5	%	vSrcOld Voltage MAX:20V+5%
vSafe5V	-5		+5	%	vSafe5V Voltage MAX:5V+5%
vSafe0V	0		+0.8	V	vSafe0V Voltage MAX:0V+0.8V
vSrcNeg	NA		-0.3	V	vSrcNeg Voltage MAX:0V+(-0.3V)
T0 → tSafe5V	NA		275	ms	tSafe5V < 275ms
T0 → tSafe0V(t2)	NA		650	ms	tSafe0V < 650ms
tSrcRecover	0.66		1	s	*660ms < tSrcRecover* < 1s (control by PD-Controller)
tSrcTurnOn(t3)	NA		275	ms	*tSrcTurnOn* < 275ms

Figure 7-22 Transition Diagram for a Sink Initiated Hard Reset

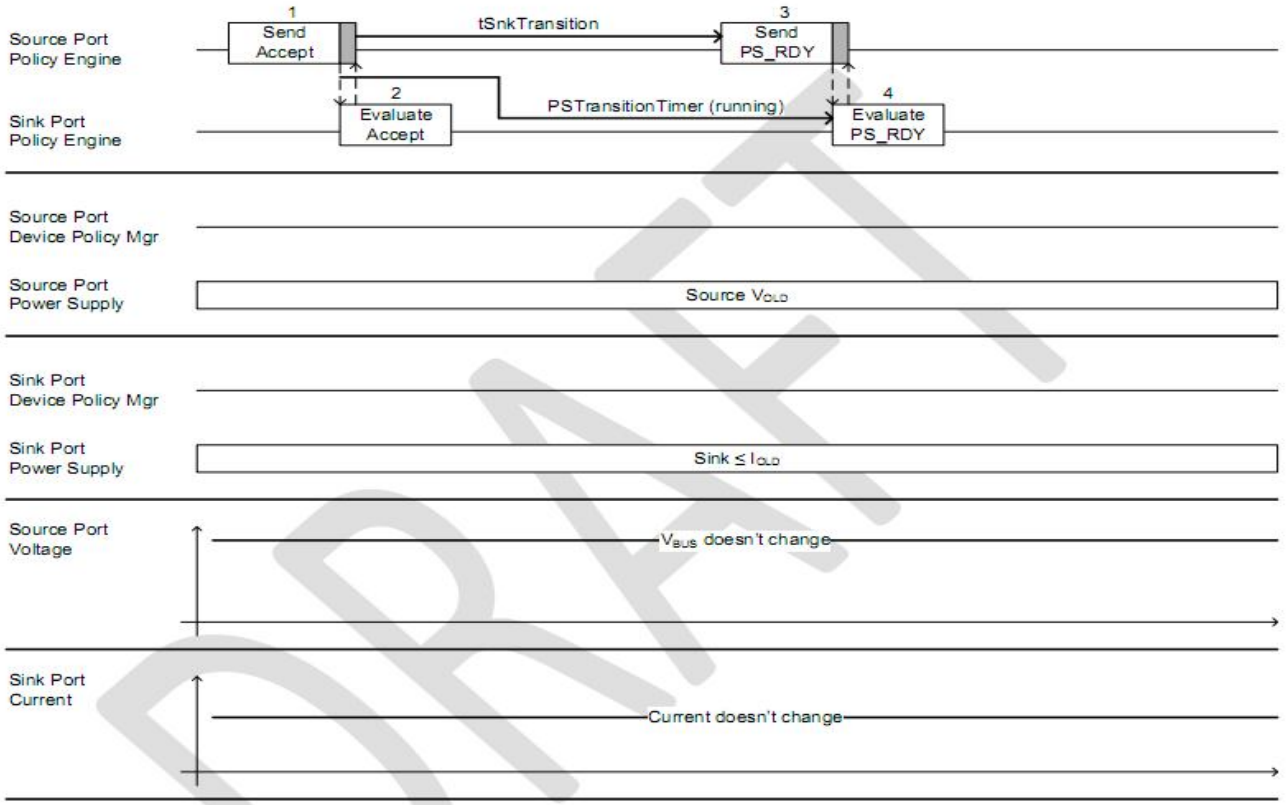


USB PD for Wall Adapter (Type C) System (Source Requirements)

- **No change in Current or Voltage**

  [Parameters]: No

Figure 7-28 Transition Diagram for no change in Current or Voltage

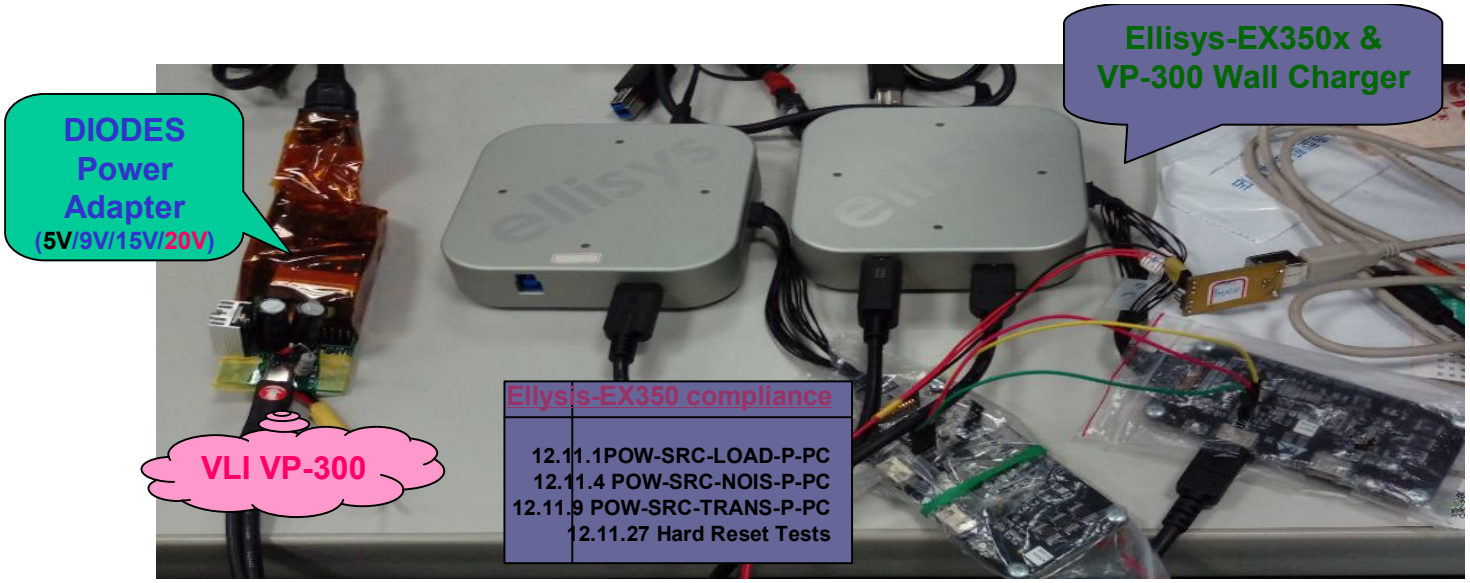


USB-PD Compliance (Test by using Ellisys-EX350x)

Source (UUT): VLI-VT3512+DIODES-Power_Adapter

Ellisys USB Compliance Report

Date and time	Thursday, 30 June 2016 09:44:28 GMT+8
Vendor	VLI
Product	VP300
Product version	0001
Test ID	0001
Generator used	Ellisys USB Explorer 350 (EX350-62201)
Analyzer used	Ellisys USB Explorer 350 (EX350-62200)
Software version	Report generated with version 3.1.6020
Overall result	**Passed**



USB-PD Compliance (Test by using Ellisys-EX350x)

- **Ellisys-EX350x**

Ellisys USB Compliance Report

Date and time	Thursday, 30 June 2016 09:44:28 GMT+8
Vendor	VLI
Product	VP300
Product version	0001
Test ID	0001
Generator used	Ellisys USB Explorer 350 (EX350-62201)
Analyzer used	Ellisys USB Explorer 350 (EX350-62200)
Software version	Report generated with version 3.1.6020
Overall result	**Passed**

Summary

		Test status	Last updated on
USB Type-C Tests	**Passed**		
» TD.PD.C.E1 DFP Attach/Detach Detection	**Passed**	Stable	2015-06-17
USB Type-C Functional Tests	**Passed**		
» TD.4.1.1 Initial Voltage	**Passed**	Stable	2016-06-17
» TD.4.2.1 Source Connect Sink	**Passed**	Stable	2015-09-02
» TD.4.2.2 Source Connect Sink Accessory	**Passed**	Stable	2015-08-10
» TD.4.2.3 Source Connect DRP	**Passed**	Stable	2015-08-10
» TD.4.2.6 Source Connect Audio Accessory	**Passed**	Stable	2015-08-10
» TD.4.2.8 Source Connect Powered Accessory	**Not Applicable**	Stable	2015-09-09
» TD.4.9.2 USB Type-C Current Advertisement	**Passed**	Stable	2016-06-17
» TD.4.9.3 Source Power Role Swap	**Not Applicable**	Stable	2016-06-17
» TD.4.9.4 Source Vconn Swap	**Not Applicable**	Stable	2016-06-17
» TD.4.11.1 Data Role Swap	**Not Applicable**	RC	2016-03-30
USB PD Physical Tests	**Passed**		
» TD.PD.PHY.E1 BIST Test Data	**Passed**	Stable	2015-08-18
» TD.PD.PHY.E2 BIST Receiver Mode	**Not Applicable**	Stable	2016-02-10
» TD.PD.PHY.E3 BIST Transmitter Mode	**Not Applicable**	Stable	2015-08-18
» TD.PD.PHY.E4 Transmitter Bit Rate Drift	**Passed**	Stable	2016-04-13
» TD.PD.PHY.E5 Transmitter Collision Avoidance	**Passed**	Stable	2016-01-20
» TD.PD.PHY.E6 Receiver Swing Tolerance	**Passed**	Stable	2015-08-18
» TD.PD.PHY.E7 Receiver Bit Rate Tolerance	**Passed**	Stable	2015-08-18

USB-PD Compliance (Test by using Ellisys-EX350x)

» TD.PD.PHY.E8 Receiver Bit Rate Deviation Tolerance	Passed	Stable	2015-08-18
» TD.PD.PHY.E9 Valid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E10 Invalid SOP Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E11 Valid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E12 Invalid SOP' Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E13 Valid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E14 Invalid SOP" Framing	Passed	Stable	2015-11-27
» TD.PD.PHY.E15 Valid SOP'/" Debug Framings	Passed	Stable	2015-11-27
» TD.PD.PHY.E16 Valid Hard Reset Framing	Passed	Stable	2015-08-21
» TD.PD.PHY.E17 Invalid Hard Reset Framing	Passed	Stable	2015-08-21
» TD.PD.PHY.E18 Valid Cable Reset Framing	Passed	Stable	2015-08-21
» TD.PD.PHY.E19 Invalid Cable Reset Framing	Passed	Stable	2015-08-21
» TD.PD.PHY.E20 EOP Framing	Passed	Stable	2015-08-18
» TD.PD.PHY.E21 Preamble	Passed	Stable	2015-08-18
USB PD Link Tests	Passed		
» TD.PD.LL.E2 Retransmission	Passed	Stable	2015-11-27
» TD.PD.LL.E3 Soft Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E4 Hard Reset Usage	Passed	Stable	2015-08-18
» TD.PD.LL.E5 Soft Reset	Passed	Stable	2015-08-18
USB PD Source Tests	Passed		
» TD.PD.SRC.E1 Source Capabilities sent timely	Passed	Stable	2016-01-19
» TD.PD.SRC.E2 Source Capabilities Fields Checks	Passed	Stable	2016-06-17
» TD.PD.SRC.E6 PSHardResetTimer Timeout	Passed	Stable	2016-03-10
» TD.PD.SRC.E7 Accept sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E8 Accept Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E9 PS_RDY sent timely	Passed	Stable	2015-08-27
» TD.PD.SRC.E10 PS_RDY Fields Checks	Passed	Stable	2015-08-27
» TD.PD.SRC.E11 Accept Requests can be met	Passed	Stable	2015-08-27
» TD.PD.SRC.E12 Reject Requests can't be met	Passed	Stable	2015-08-27
» TD.PD.SRC.E13 Reject Request - Invalid Object Position	Passed	Stable	2015-08-27
» TD.PD.SRC.E14 Atomic Message Sequence	Passed	Stable	2015-09-23
» TD.PD.SRC.E15 Give_Source_Cap	Passed	Stable	2015-09-23
» TD.PD.SRC.E16 PDO Transition	Passed	RC	2015-11-06
USB PD Sink Tests	Passed		
USB PD Provider / Consumer Tests	Passed		
» TD.PD.PC.E1 tSrcTransition Check	Not Applicable	Stable	2016-03-24
» TD.PD.PC.E2 PS_RDY Sent Timely	Not Applicable	Stable	2016-03-24
» TD.PD.PC.E3 PSSourceOnTimer Deadline	Not Applicable	Stable	2016-03-24
» TD.PD.PC.E4 PSSourceOnTimer Timeout	Not Applicable	Stable	2016-03-24
» TD.PD.PC.E5 tSwapSinkReady Check	Not Applicable	Stable	2016-03-24
» TD.PD.PC.E6 Externally Powered Bit Usage	Passed	Stable	2016-04-28
» TD.PD.PC.E7 PDO Transition After PR_Swap	Not Applicable	Stable	2016-06-24
USB PD Consumer / Provider Tests	Passed		
USB PD VDM Tests for UFPs and Cables	Passed		
DisplayPort Alt-Mode Tests for UFPs and Cables	Passed		

USB-PD Compliance (Test by using Ellisys-EX350x)

DisplayPort Alt-Mode Tests for DFPs	Not Applicable		
» TD.PD.DPD.E1 Cable Determination	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E2 DP SVID in Arbitrary Location	Not Applicable	Stable	2015-09-17
» TD.PD.DPD.E3 Status Update Presence	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E4 Enter Mode Rejected	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E5 Enter Mode Not Responded	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E6 DisplayPort Not Connected	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E7 Status Update Port Resolution	Not Applicable	Stable	2015-09-16
» TD.PD.DPD.E8 Not Compatible Connection	Not Applicable	Stable	2015-10-28
» TD.PD.DPD.E9 Field Checks - DisplayPort Configure	Not Applicable	Alpha	2016-03-10
USB PD Consistency Tests	**Passed**		
» TD.PD.VNDI.E4 SOP* Handling	**Passed**	Stable	2015-08-18
» TD.PD.VNDI.E5 Source Capabilities	**Passed**	Stable	2016-06-24
» TD.PD.VNDI.E7 Accepts PR_Swap as Source	Not Applicable	Stable	2016-03-14
» TD.PD.VNDI.E9 Requests PR_Swap as Source	Not Applicable	Stable	2016-02-10

USB-PD Compliance (Test by using MQP-Packet-Master)

Source (UUT): VLI-VT3512+DIODES-Power_Adapter

Packet-Master USB-PDT Report on VLI VT3512

GraphicUSB V4.91 -- Scripts PDT Rev:0.9.2.1

Test run on Wednesday, June 29, 2016 22:05:22

TID: Unknown

Vendor Name: VLI

Product Name: VT3512

Version Info: Discovered

The following tests have been selected:
BMC-POW-SRC-LOAD-P-PC
BMC-POW-SRC-TRANS-P-PC

USB-PD Compliance (Test by using MQP-Packet-Master)

Error Summary

No Post-Run Errors found.
0 Runtime Errors

Test Summary

BMC-PHY-TX-EYE

BMC-PHY-TX-EYE Primary - PASS
BMC-PHY-TX-EYE Secondary - PASS

BMC-PHY-RX-INT-REJ

BMC-PHY-RX-INT-REJ - PASS
BMC-PHY-RX-INT-REJ Secondary - PASS

BMC-PHY-RX-BUSIDL

BMC-PHY-RX-BUSIDL - PASS
BMC-PHY-RX-BUSIDL Secondary - PASS

BMC-PHY-TERM

BMC-PHY-TERM - PASS
BMC-PHY-TERM Secondary - PASS

Packet-Master USB-PDT Report on VLI VT3512

GraphicUSB V4.91 -- Scripts PDT Rev:0.9.2.1

Test run on Wednesday, June 29, 2016 22:00:27

TID: Unknown

Vendor Name: VLI

Product Name: VT3512

Version Info: Discovered

The following tests have been selected:
BMC-PHY-TX-EYE
BMC-PHY-RX-INT-REJ
BMC-PHY-RX-BUSIDL
BMC-PHY-TERM
BMC-PHY-MSG

USB-PD Compliance (Test by using MQP-Packet-Master)

Error Summary

No Post-Run Errors found.
0 Runtime Errors

Test Summary

BMC-PHY-TX-EYE

BMC-PHY-TX-EYE Primary - PASS
BMC-PHY-TX-EYE Secondary - PASS

BMC-PHY-RX-INT-REJ

BMC-PHY-RX-INT-REJ - PASS
BMC-PHY-RX-INT-REJ Secondary - PASS

BMC-PHY-RX-BUSIDL

BMC-PHY-RX-BUSIDL - PASS
BMC-PHY-RX-BUSIDL Secondary - PASS

BMC-PHY-TERM

BMC-PHY-TERM - PASS
BMC-PHY-TERM Secondary - PASS

BMC-PHY-MSG

BMC-PHY-MSG - PASS
BMC-PHY-MSG Secondary - PASS

USB-IF Summary

BMC PHY Tx: PASS
BMC PHY Rx: PASS
BMC PHY Misc: PASS
Protocol Specific:
Power Specific:
Secondary: PASS

End of Report

USB-PD Compliance (Test by using MQP-Packet-Master)

Packet-Master USB-PDT Report on VLI VT3512

GraphicUSB V4.91 -- Scripts PDT Rev:0.9.2.1

Test run on Wednesday, June 29, 2016 22:03:38

TID: Unknown

Vendor Name: VLI

Product Name: VT3512

Version Info: Discovered

The following tests have been selected:
BMC-PROT-SEQ-GETCAPS
BMC-PROT-SEQ-CHKCAB-P-PC
BMC-PROT-SEQ-NOMRK-P-PC
BMC-PROT-SEQ-PRSWAP
BMC-PROT-SEQ-DRSWAP
BMC-PROT-SEQ-VCSWAP
BMC-PROT-BIST-NOT-5V-SRC
BMC-PROT-REV-NUM

Error Summary

No Post-Run Errors found.
0 Runtime Errors

Test Summary

BMC-PROT-SEQ-GETCAPS

BMC-PROT-SEQ-GETCAPS - PASS
BMC-PROT-SEQ-GETCAPS Secondary - PASS

BMC-PROT-SEQ-CHKCAB-P-PC

BMC-PROT-SEQ-CHKCAB-P-PC - PASS
BMC-PROT-SEQ-CHKCAB-P-PC Secondary - PASS

BMC-PROT-SEQ-NOMRK-P-PC

BMC-PROT-SEQ-NOMRK-P-PC - PASS
BMC-PROT-SEQ-NOMRK-P-PC Secondary - PASS

BMC-PROT-SEQ-PRSWAP

BMC-PROT-SEQ-PRSWAP - PASS
BMC-PROT-SEQ-PRSWAP Secondary - PASS

BMC-PROT-SEQ-DRSWAP

BMC-PROT-SEQ-DRSWAP - PASS
BMC-PROT-SEQ-DRSWAP Secondary - PASS

BMC-PROT-SEQ-VCSWAP

BMC-PROT-SEQ-VCSWAP - PASS
BMC-PROT-SEQ-VCSWAP Secondary - PASS

BMC-PROT-REV-NUM

BMC-PROT-REV-NUM - PASS
BMC-PROT-REV-NUM Secondary - PASS

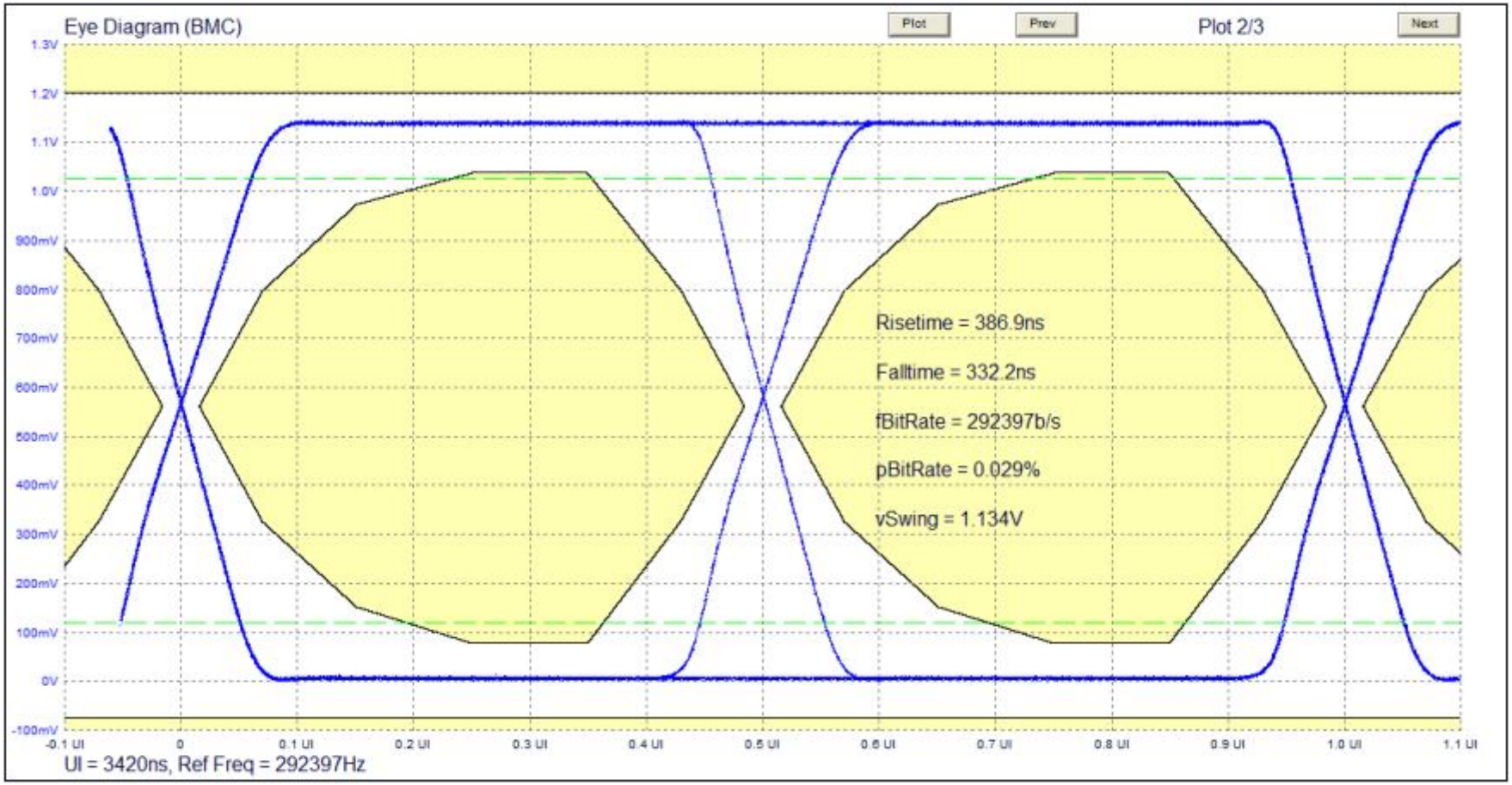
USB-IF Summary

BMC PHY Tx:
BMC PHY Rx:
BMC PHY Misc:
Protocol Specific: PASS
Power Specific:
Secondary: PASS

End of Report

USB-PD Compliance (Test by using MQP-Packet-Master)

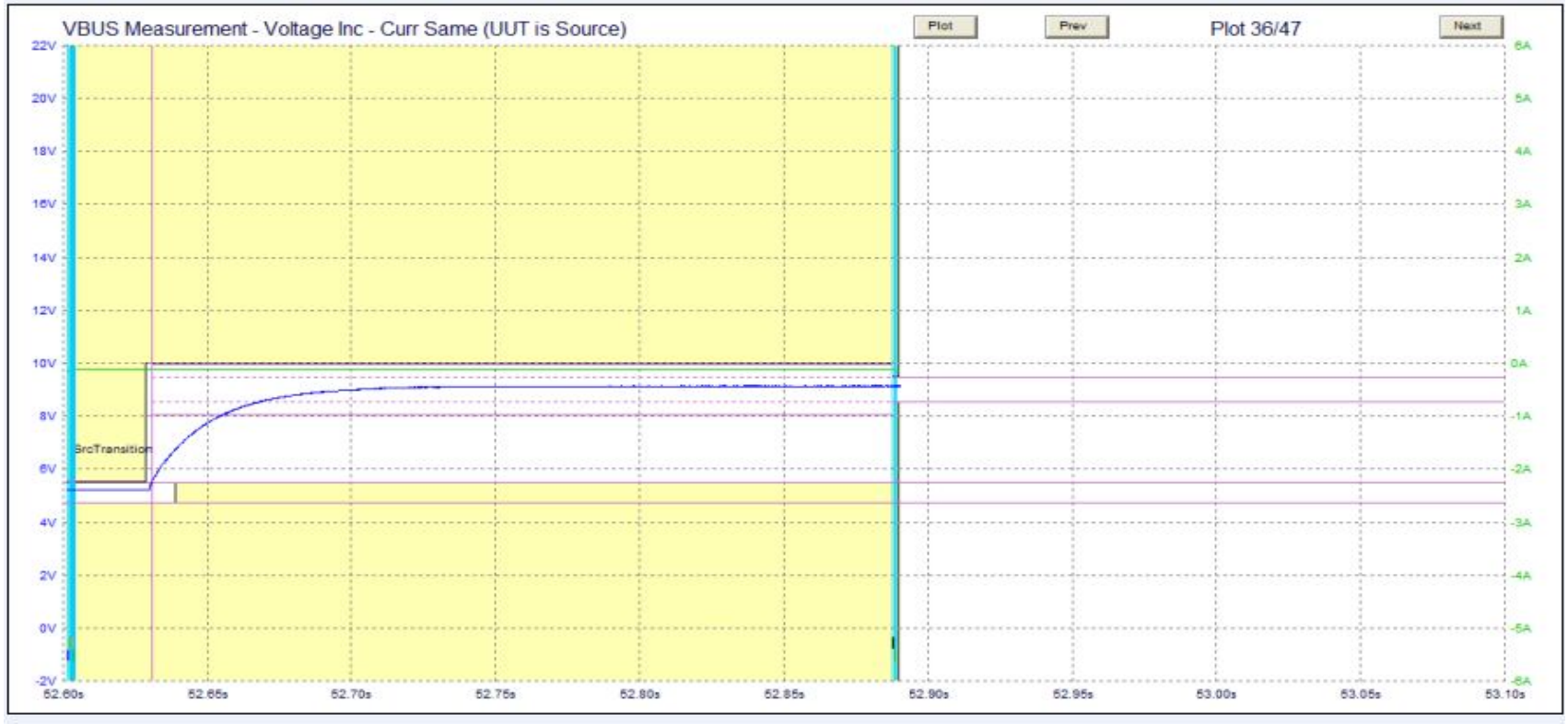
- **Eye Diagram (BMC)**



USB-PD Compliance (PDO Transition Test)

- [Positive] POW-SRC-TRANS-P: +5V → +9V

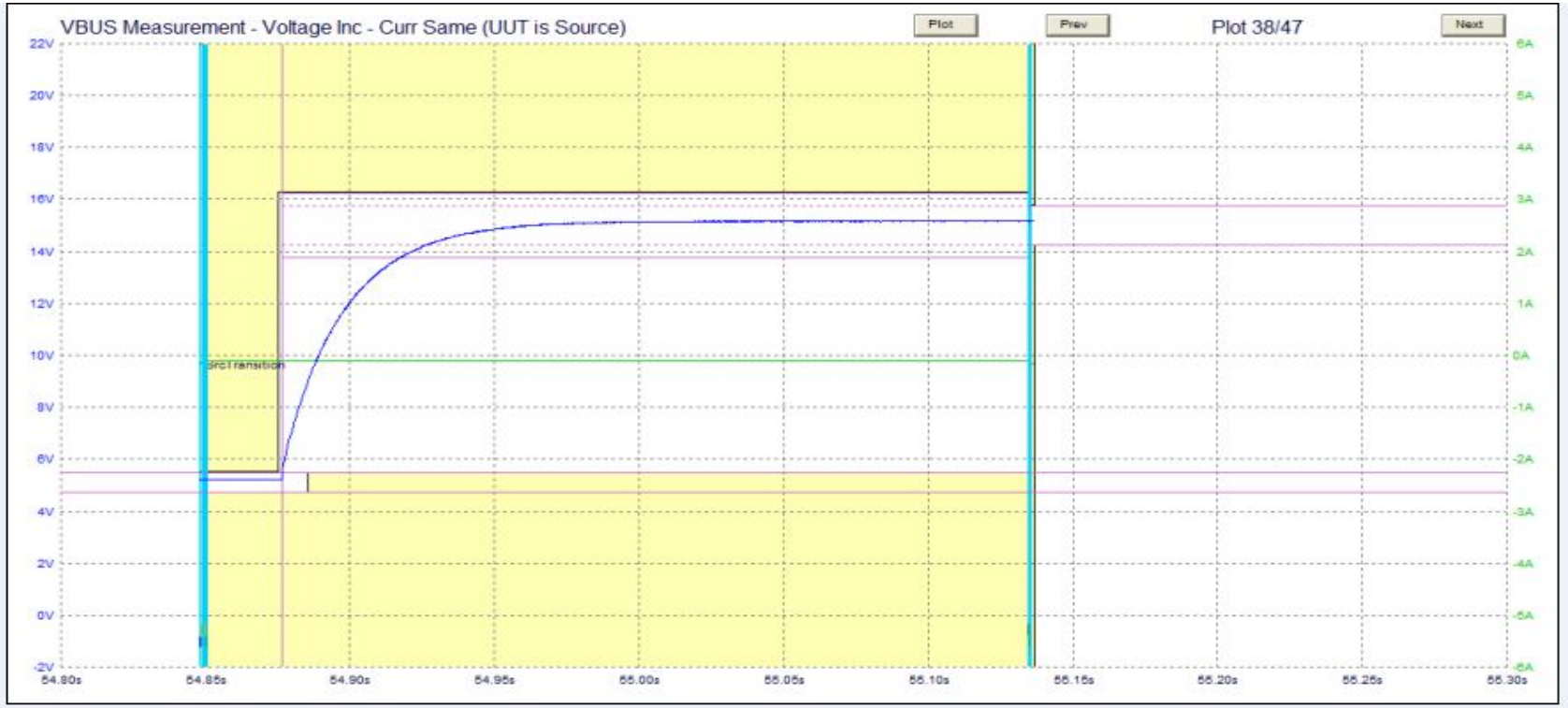
Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+0.8*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewPos	NA	*+0.4*	30	mV/us	7000mV/17.48ms < +30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



USB-PD Compliance (PDO Transition Test)

- [Positive] POW-SRC-TRANS-P: +5V → +15V

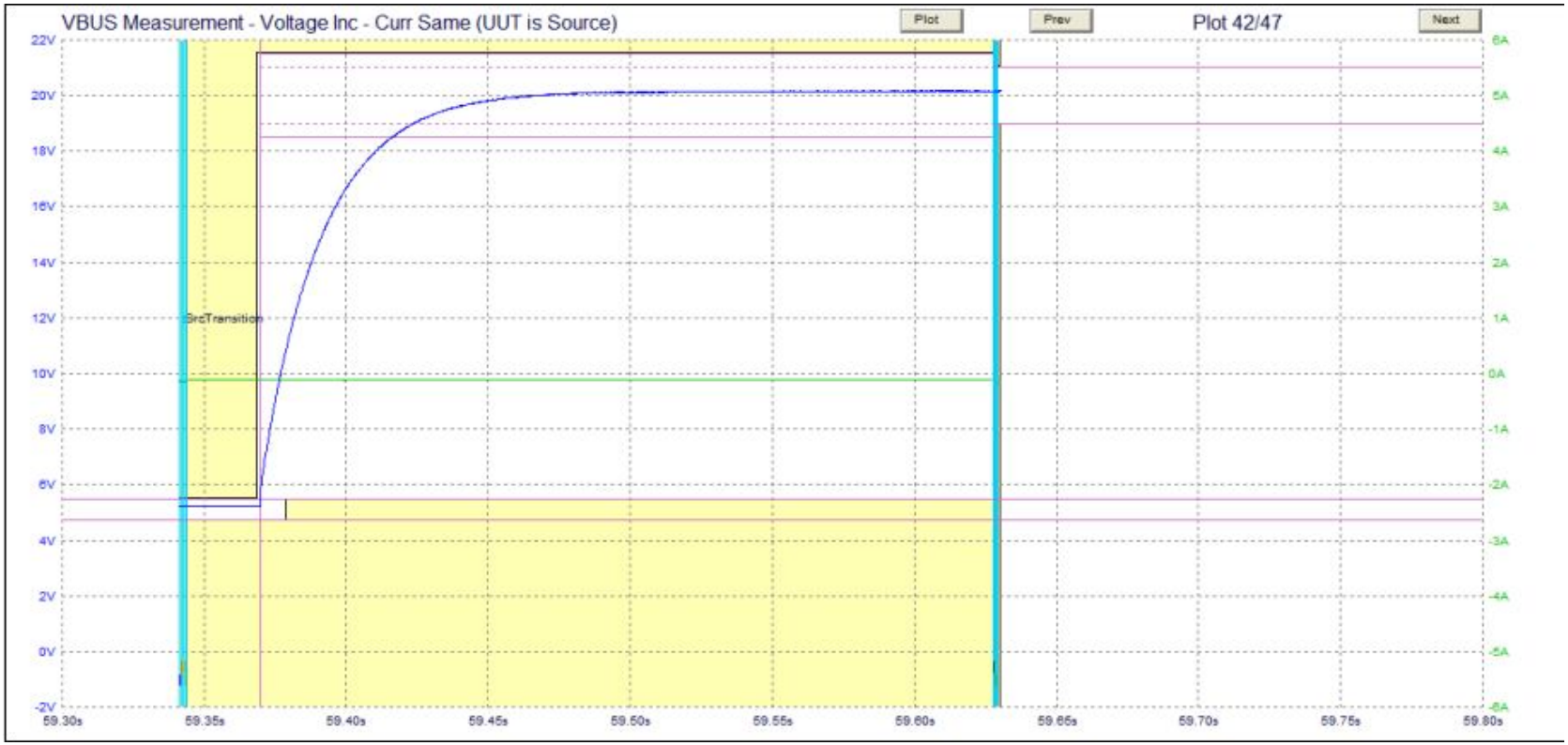
Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+0.5*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewPos	NA	*+0.75*	30	mV/us	15000mV/20.48ms < +30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



USB-PD Compliance (PDO Transition Test)

- [Positive] POW-SRC-TRANS-P: +5V → +20V

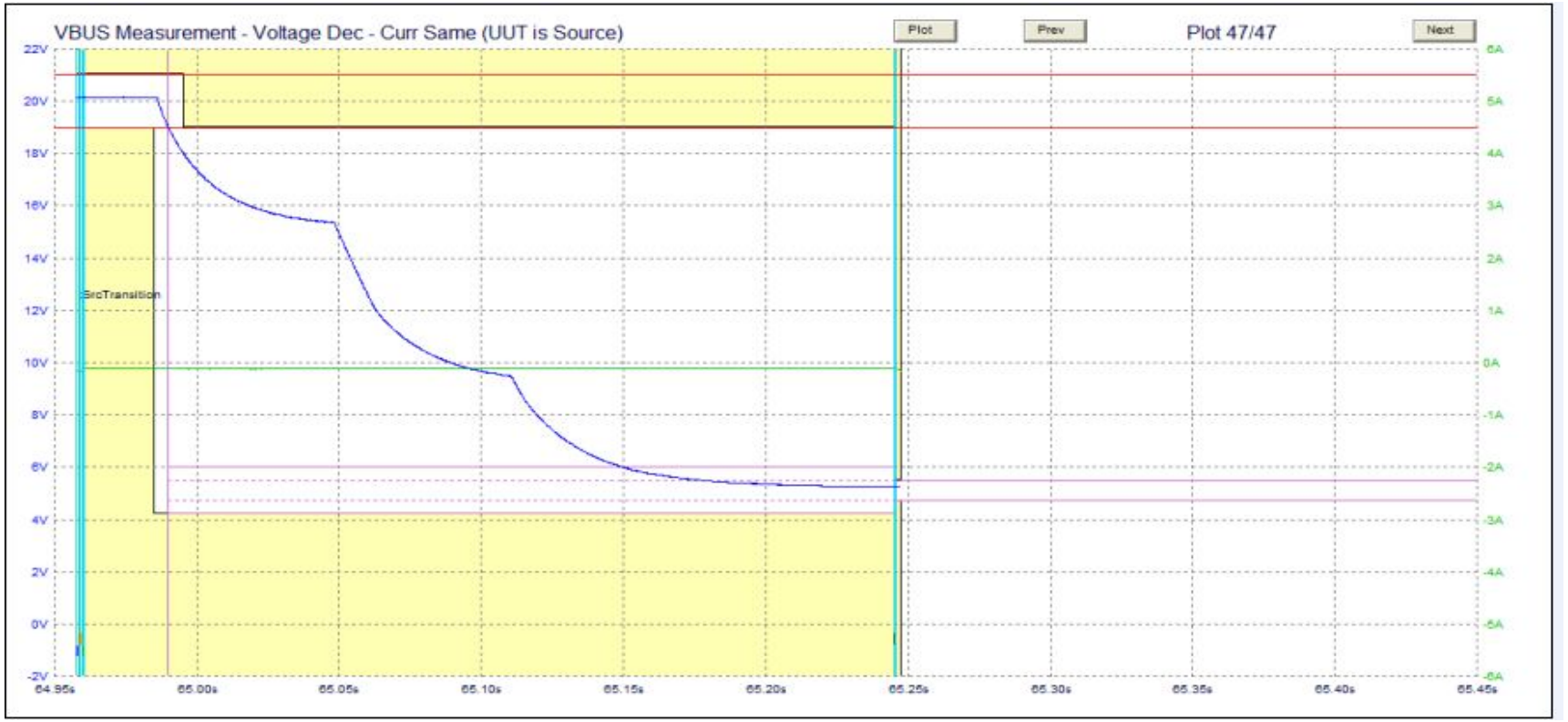
Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+0.5*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewPos	NA	*+0.75*	30	mV/us	15000mV/20.48ms < +30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



USB-PD Compliance (PDO Transition Test)

- [Negative] POW-SRC-TRANS-P: +20V → +5V

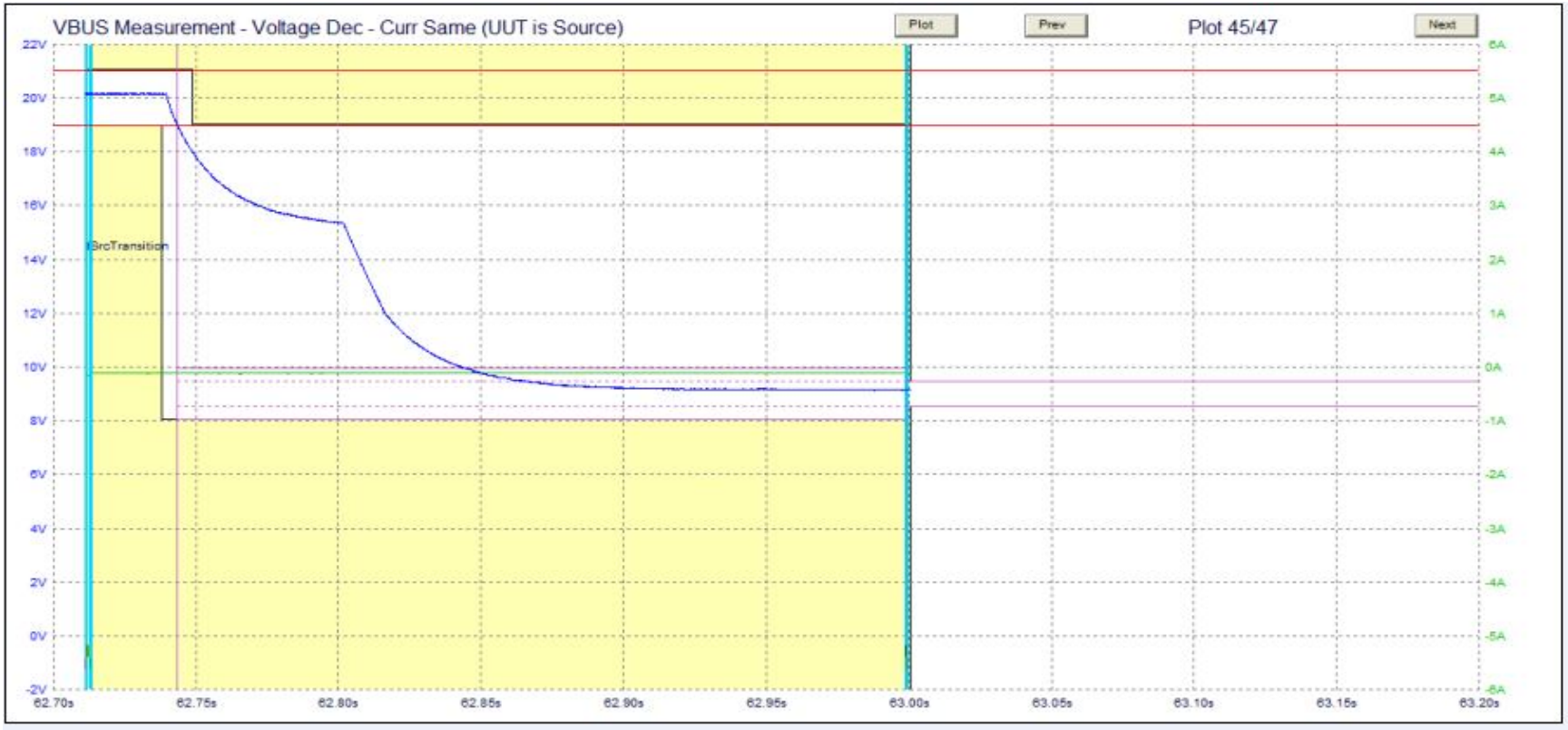
Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+2.0*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewNeg	NA	*-0.2*	-30	mV/us	-7000mV/36.48ms > -30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



USB-PD Compliance (PDO Transition Test)

- [Negative] POW-SRC-TRANS-P: +20V → +9V

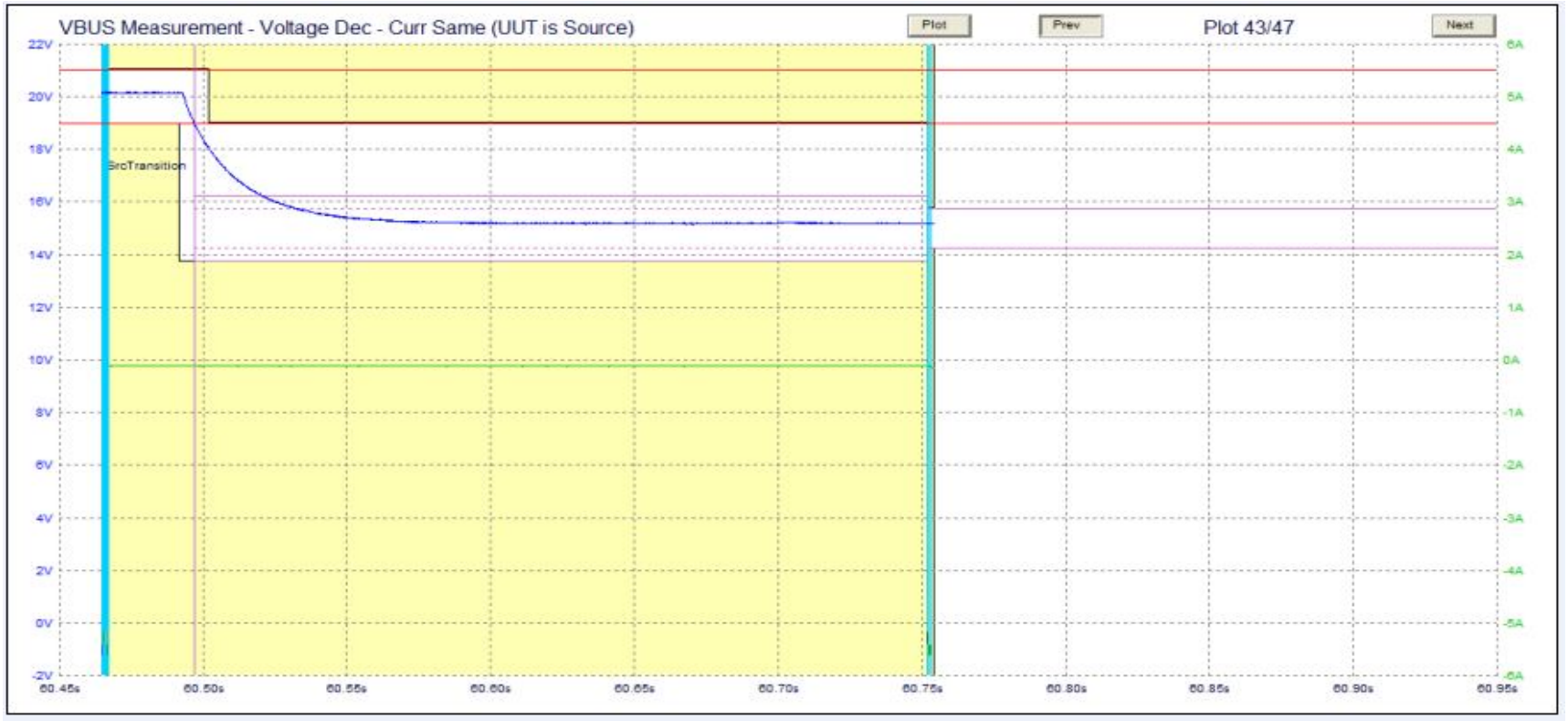
Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+2.0*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewNeg	NA	*-0.2*	-30	mV/us	-7000mV/36.48ms > -30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



USB-PD Compliance (PDO Transition Test)

- [Negative] POW-SRC-TRANS-P: +20V → +15V

Parameter	min	Measure	MAX	UNIT	Description
vSrcNew	-5	*+2.0*	+5	%	vSrcNew Tolerance limitation
vSrcValid	-0.5	*+0.1*	+0.5	V	vSrcNew upper/lower bound limitation
cSrcSlewNeg	NA	*-0.2*	-30	mV/us	-7000mV/36.48ms > -30 mV/us
T0 → tSrcSettle	NA	*20ms*	NA	ms	tSnkTransition
T0 → tSrcReady	NA	*60ms*	285	ms	tSrcReady(60ms) < 285ms



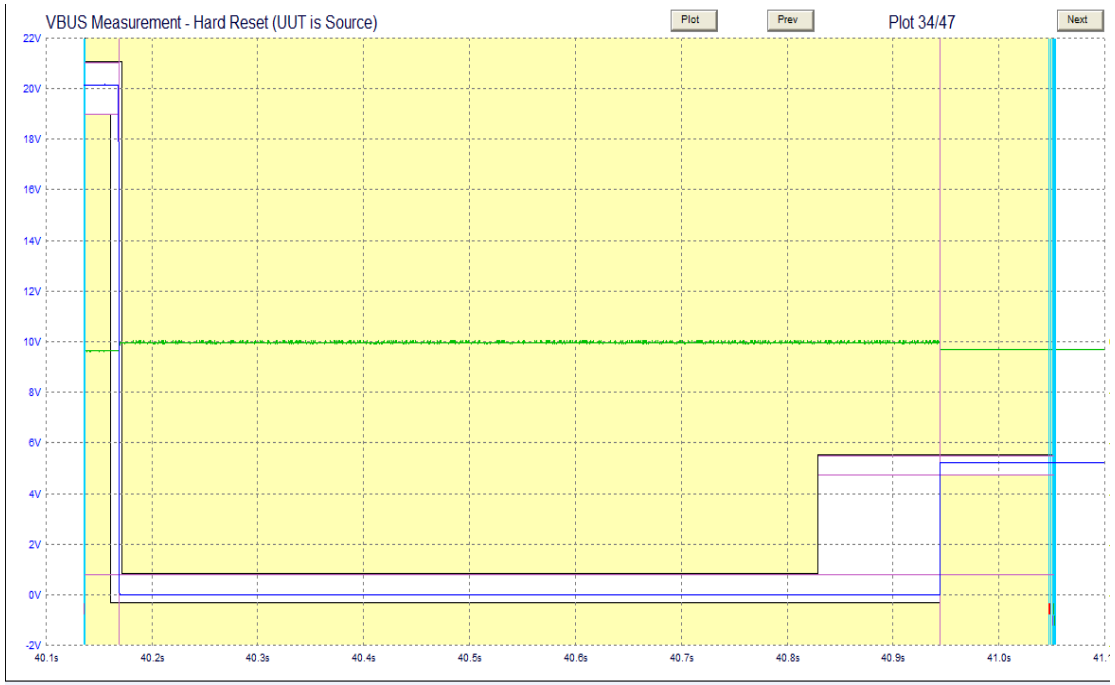
USB-PD Compliance (Hard Reset Tests)

Source (UUT): VLI-VT3512+DIODES-Power_Adapter

Parameter	MIN	Measure	MAX	UNIT	Description
Old Voltage	-5	*+0.5*	+5	%	vSrcOld Voltage MAX:20V+5%
vSafe5V	-5	*+2.0*	+5	%	vSafe5V Voltage MAX:5V+5%
vSafe0V	0	*0*	+0.8	V	vSafe0V Voltage MAX:0V+0.8V
vSrcNeg	NA	*0*	-0.3	V	vSrcNeg Voltage MAX:0V+(-0.3V)
T0 → tSafe5V	NA	*50ms*	275	ms	tSafe5V < 275ms
T0 → tSafe0V(t1)	NA	*120ms*	650	ms	tSafe0V < 650ms
tSrcRecover	0.66	*682ms*	1	s	*660ms < tSrcRecover* < 1s (control by PD-Controller)
tSrcTurnOn(t3)	NA	*90ms*	275	ms	*tSrcTurnOn* < 275ms

A source performs a hard reset (HR) for one of the following reason:

1.No-Response-Timer timeout & HR-Counter < n-HR-Counter
2.Hard Reset request from Device Policy Manager
3.Sender-Response-Timer Timeout
4.Transmission Error indication from protocol Layer
5.Ping massage not sent after retries (No Good-CRC received) HR
6.OCP/OVP/OTP protection event



USB-PD Compliance (Test by using Granite River Labs)

- ***USB PD Protocol Decode Report***

USB-PD Compliance and Protocol Decode Report

DUT Information

Manufacturer	:	VT3512
Model	:	<DUT MODEL NUMBER>
Serial No.	:	<DUT SERIAL NUMBER>

VLI VP-300

Test Information

Test Lab	:	<TEST LAB>
Test Engineer	:	<TEST ENGINEER>
Remarks	:	BMC PHY(Tx & Rx)
Date	:	7_7_2016 10_59_18 AM

Environment Information

Parameter	Value
Signal Source	LIVE
Signal Source Channel Number	CH1

USB-PD Compliance (Test by using GRL)

- ***USB PD Protocol Decode Software***

Compliance Test Result

Sl No	Test Sec	Test ID	Test Name	Test Result
1	13.7.1	TDA.2.1.1.1	BMC-PHY-TX-EYE	PASS
			BMC-PHY-TX-EYE-1 >> Valid Protocol response for BIST Request	PASS
			BMC-PHY-TX-EYE-2 >> Valid BIST response pattern	PASS
			BMC-PHY-TX-EYE-3 >> Eye diagram plot	PASS
			BMC-PHY-TX-EYE-4 >> BIST pattern duration 51.3085359 mS (Limit <= 60ms)	PASS
			BMC_PHY_TX_EYE_5 >> Rise time: Average value = 386.981650 nS Minimum value = 382.258760 nS Maximum value = 392.693698 nS Minimum Limit = 300 ns Fall time: Average value = 336.524306 nS Minimum value = 332.334757 nS Maximum value = 341.248440 nS Minimum Limit = 300 ns	PASS
2	13.7.2	TDA.2.1.1.2	BMC-PHY-TX-BIT	PASS
			BMC-PHY-TX-BIT-1 >> Valid Protocol response for BIST Request	PASS
			BMC-PHY-TX-BIT-2 >> Valid BIST response pattern	PASS

USB-PD Compliance (Test by using GRL)

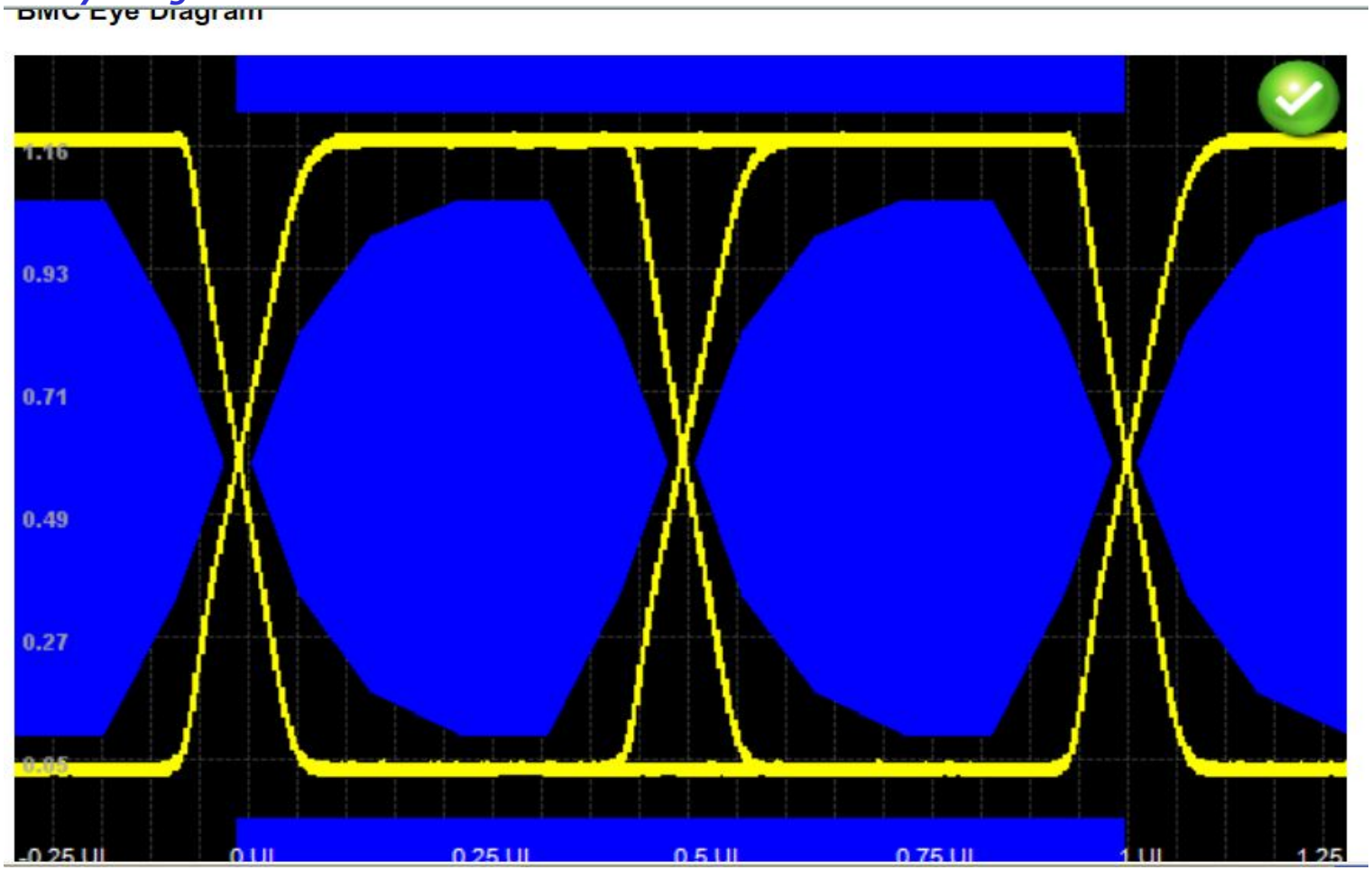
- ***USB PD Protocol Decode Software***

GRL-USB-PD Compliance and Protocol Decode Software

Sl No	Test Sec	Test ID	Test Name	Test Result
			BMC-PHY-TX-BIT-3 >> Bit Rate Test: Average value = 292.898 Kbps Minimum value = 292.898 Kbps Maximum value = 292.898 Kbps Minimum Limit: 270 Kbps Maximum Limit: 330 Kbps	PASS
			BMC-PHY-TX-BIT-4 >> pBitRate Test: Average value = 0.033 % Minimum value = 0.033 % Maximum value = 0.033 % Maximum Limit = 0.25 %	PASS
			BMC-PHY-TX-BIT-4 >> BIST pattern duration 51.3085359 mS (Limit <= 60ms)	PASS
3	13.8.2	TDA.2.1.2.2	BMC-PHY-RX-INT-REJ	PASS
			BMC-PHY-RX-INT-REJ4_TstrSink	PASS
			BMC-PHY-RX-INT-REJ5_TstrSinkNoiseGrp1 >> Total Message Count: BIST Test Data = 13362; GoodCRC = 13362 Signal Capture Message Count: BIST Test Data = 380; GoodCRC = 380)	PASS
			BMC-PHY-RX-INT-REJ6_TstrSinkNoiseGrp3 >> Total Message Count: BIST Test Data = 13362; GoodCRC = 13362 Signal Capture Message Count: BIST Test Data = 380; GoodCRC = 380)	PASS
4	13.8.1	TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	PASS
			BMC-PHY-RX-BUSIDL1_TstrSink	PASS
			BMC-PHY-RX-BUSIDL3_TstrSink	PASS
			BMC-PHY-RX-BUSIDL2_TstrSink	PASS

USB-PD Compliance (Test by using GRL)

- ***BMC Eye Diagram***



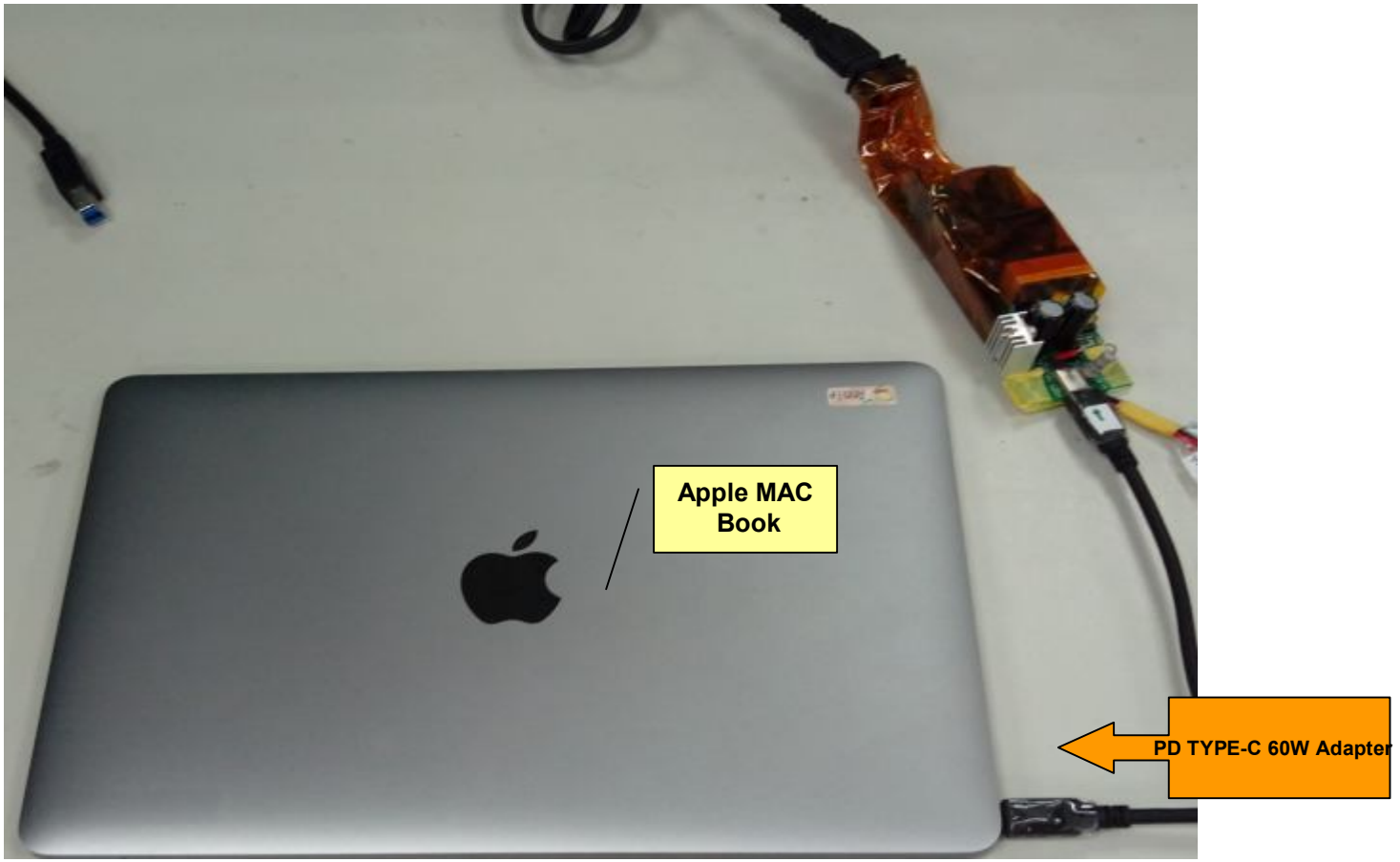
Type-C PD Device test list (Summary)

Test Procedure (DFP-Source)	Apple : MAC-Book VLI : E-marker	Apple MAC-Book	Google: Chrome-Book VLI : E-marker	Google Chrome-Book
1.Detect Rd / Ra at CC1 or CC2	●	●	●	●
2.VCONN Enable	●	●	●	●
3. t-VCONN < -30ms	●	●	●	●
4. DFP send SOPP Discover Identity Packet and received SOPP Good-CRC Packet	●	●	●	●
5. UFP send SOPP Discover Identity ACK Packet and received SOPP Good-CRC Packet	●	NA	●	NA
6. Vsafe5V Enable	●	●	●	●
7. Error Handle process	●	●	●	●
8. DFP PE-SRC-Send-Capabilities and UFP Send Good-CRC Message (fixed 5V, 9V, 15V, 20V @3A)	●	●	●	●
9. DFP Request Message received	●	●	●	●
10. DFP PE-SRC-Negotiate-Capability and can be met	●	●	●	●
11. DFP PE-SRC-Transition-Supply and UFP Send Accept Message	● (Object4/1.4A)	● (Object4/1.4A)	● (Object4/3A)	● (Object4/3A)
12. DFP PE-SRC-Ready and send PS_RDY Message to UFP	●	●	●	●
Other Function test				
Dead-Battery Test	●	●	●	●
Source Power OCP/ OVP test	NA	NA	NA	NA
Hard-Reset test	●	●	●	●

● : Workable ×: Can't Work

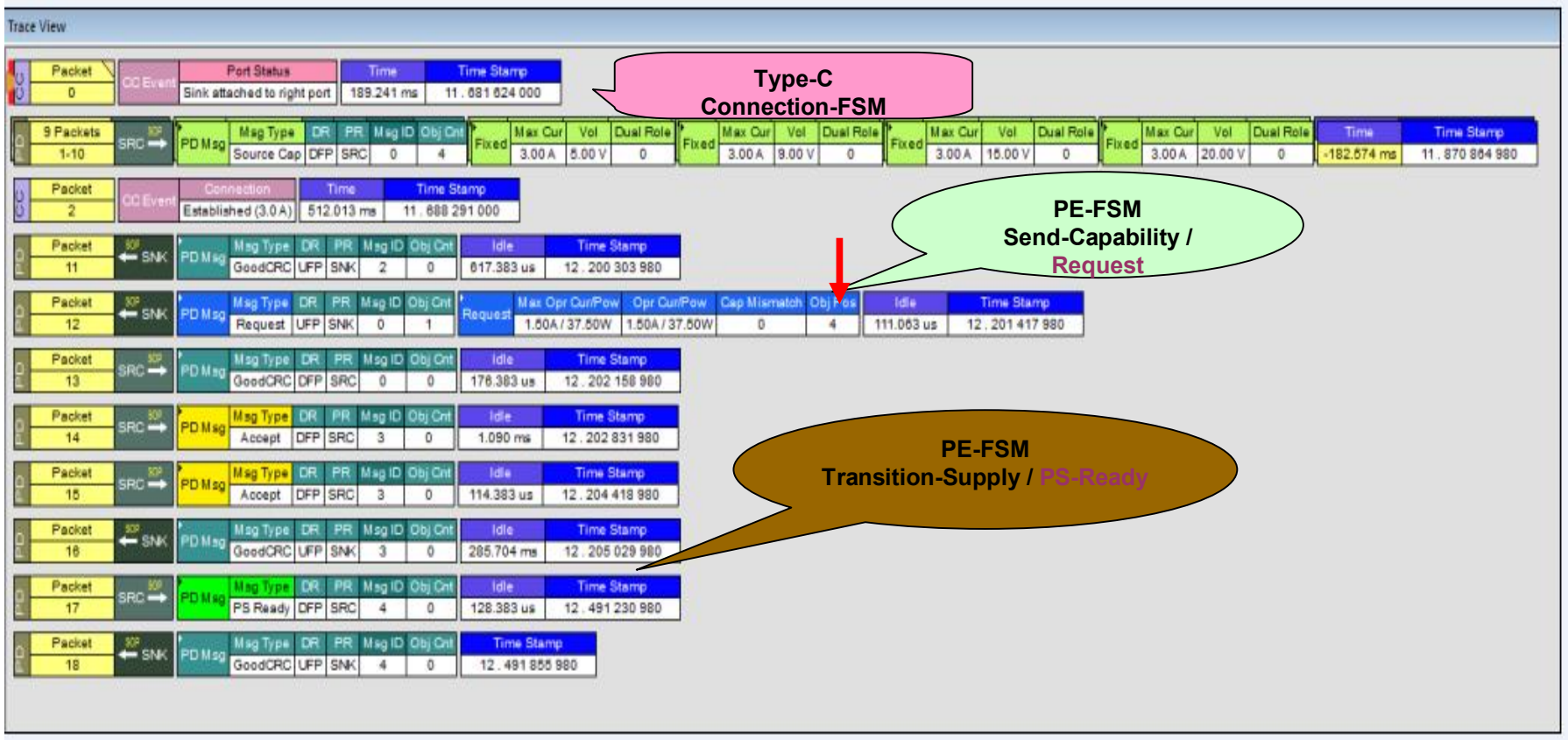
Apple MAC Book (TYPE-C)

- **VBUS: 20V @ 1.4A (Apple MAC Object-4 charging mode)**



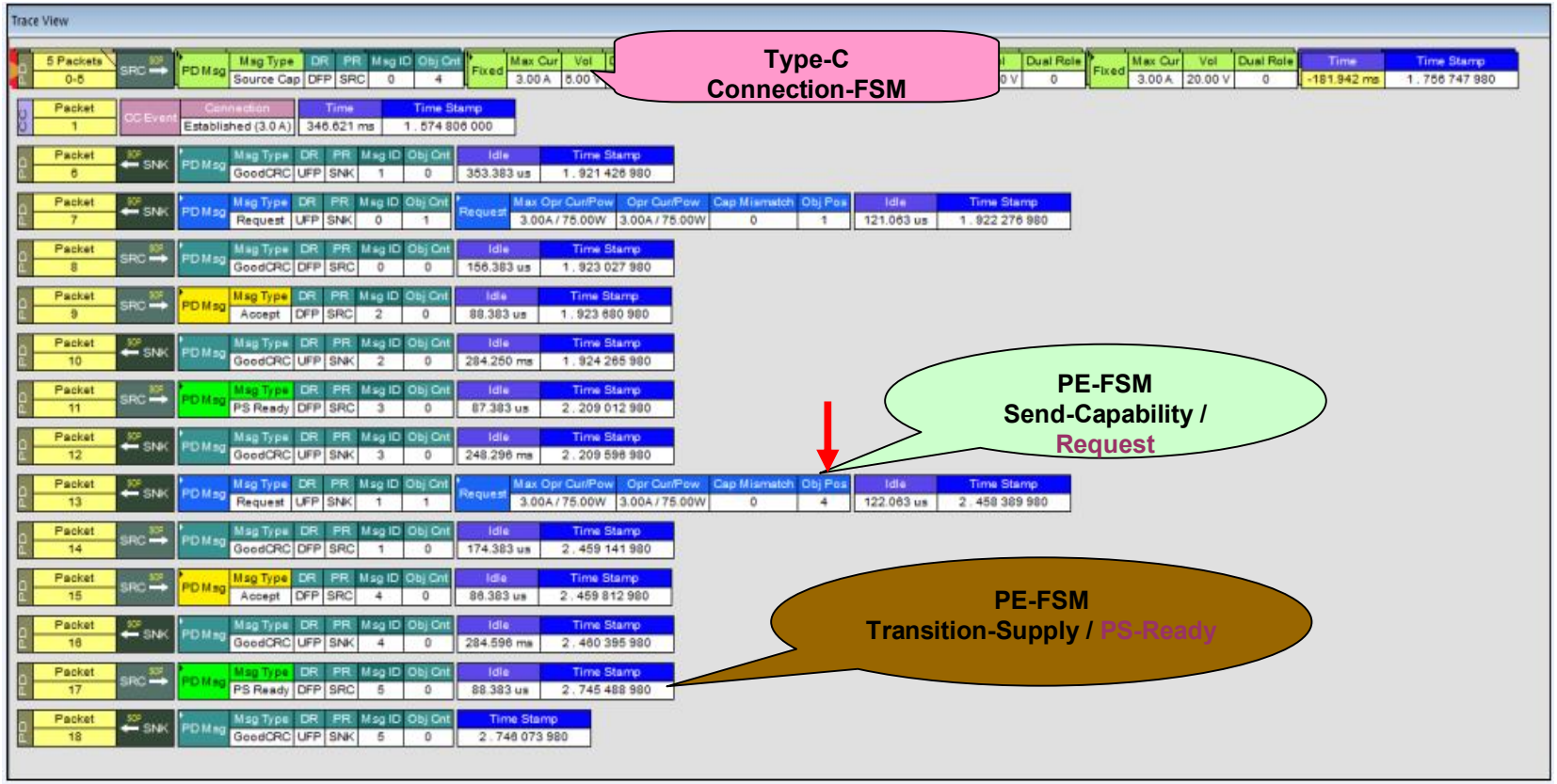
Apple MAC Book (TYPE-C)

- **MAC-Book Protocol (Charging VBUS:20V@1.5A)**



Google Chrome Book (TYPE-C)

- **Chrome-Book Protocol (Charging VBUS:20V@3A)**



AC-DC Adapter (60W) Performance Validation

- **System Performance Test Specification**

TEST ITEM	SPEC.	OUTPUT	RESULT
Input Characteristics			
HI-POT	TUV SPEC		
INRUSH CURRENT	30A MAX		
Input Power / Input Current	TBD		
Line Regulation / Cross Regulation	Output Voltage+-5%	Output VBUS: 20V/15V/9V/5V	
Efficiency (MAX Load)	TBD		
Efficiency (Stand-By)	TBD		
Start-up Time	TBD		
Brown-in and Brown-Out	TBD		
Output Characteristics			
Load Regulation / Cross Regulation	Output Voltage+-5%	Output VBUS: 20V/15V/9V/5V	
Output Ripple & Noise	50mV & 200mV	Output VBUS: 20V/15V/9V/5V	
Output Voltage Rising / Falling Time	30mV / us	Output VBUS: 20V/15V/9V/5V	
Hold Up Time	TBD	Output VBUS: 20V/15V/9V/5V	
Load Transient and Cycling test	TBD	Output VBUS: 20V/15V/9V/5V	
Safety Protections			
Feedback Loop Fault protection	TBD		
Constant Current	TBD		
O.V.P / S.C.P /O.P.P	TBD		
Reliability			
Storage and Vibration Environment Test	TBD		
MTBF	TBD		

Type-C USB Device test list (Summary)

Charging Mode / Device Type	Type-C Charging AC Mode (5V@3A/5V@1.5A)	DCP Charging AC Mode (5V@ >500mA)	Apple Charging AC-2.4A Mode (5V@2.4A)	Quick Charging Qc3.0 Mode (5V/9V/15V/20V)	Samsung Charging AC Mode (5V@ > 500mA)
HUAWEI (Mobil Phone)					
mi(小米) Mobil Phone					
Sony Ericsson XPERIA-Z3					
Apple-Phone 3G Mobil Phone					
HTC-Butterfly Mobil Phone					
Samsung-GALAXY Mobil Phone					
Samsung-PAD (Micro-B Header)					

VLI-VP300 Type-C PD wall charger functional flowchart (Source)