SYNCHRONOUS BOOST CONTROLLER

3V~36V Input 5V~36V Output， Extended NMOS

GENERAL DESCRIPTION

XR4981 is a high efficiency synchronous boost controller that converts from 3V ~36V input range and up to 36V output voltage with an outside N-channel MOSFET for the synchronous switch.

The XR4981 includes adjustable current limit, adjustable soft-start, adjustable compensation net and thermal shutdown preventing damage in the event of an output overload.

For different application we can select suitable compensation net、current limit、soft start and select suitable MOSFET to obtain a high efficiency。

FEATURES

- 3V~36V input voltage range
- Adjustable output voltage from 5V to 36V
- 1.21V VFB reference voltage
- Adjustable current limit
- Adjustable soft-start
- Adjustable compensation net
- Input under voltage lockout
- 400Khz fixed Switching Frequency
- Thermal Shutdown
- QFN3x3-16 Package
- Rohs Compliant and Halogen Free

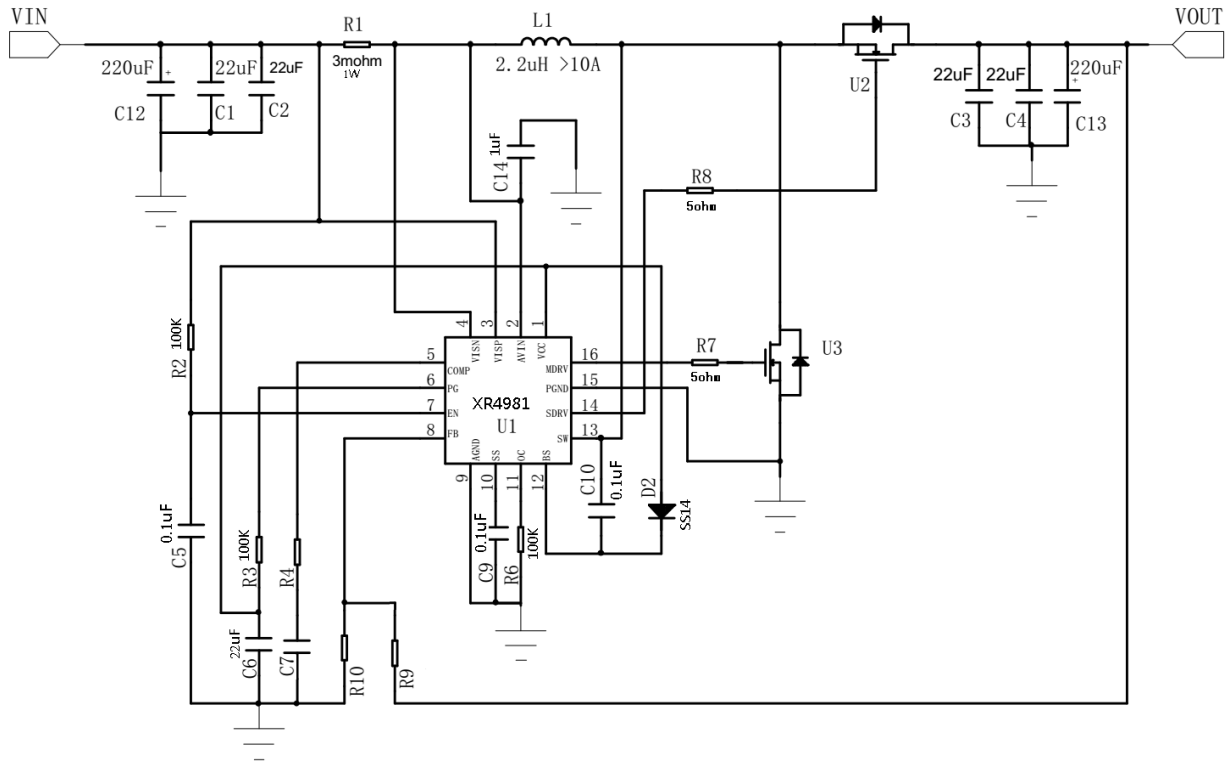


Figure 1. Typical Application Circuit1

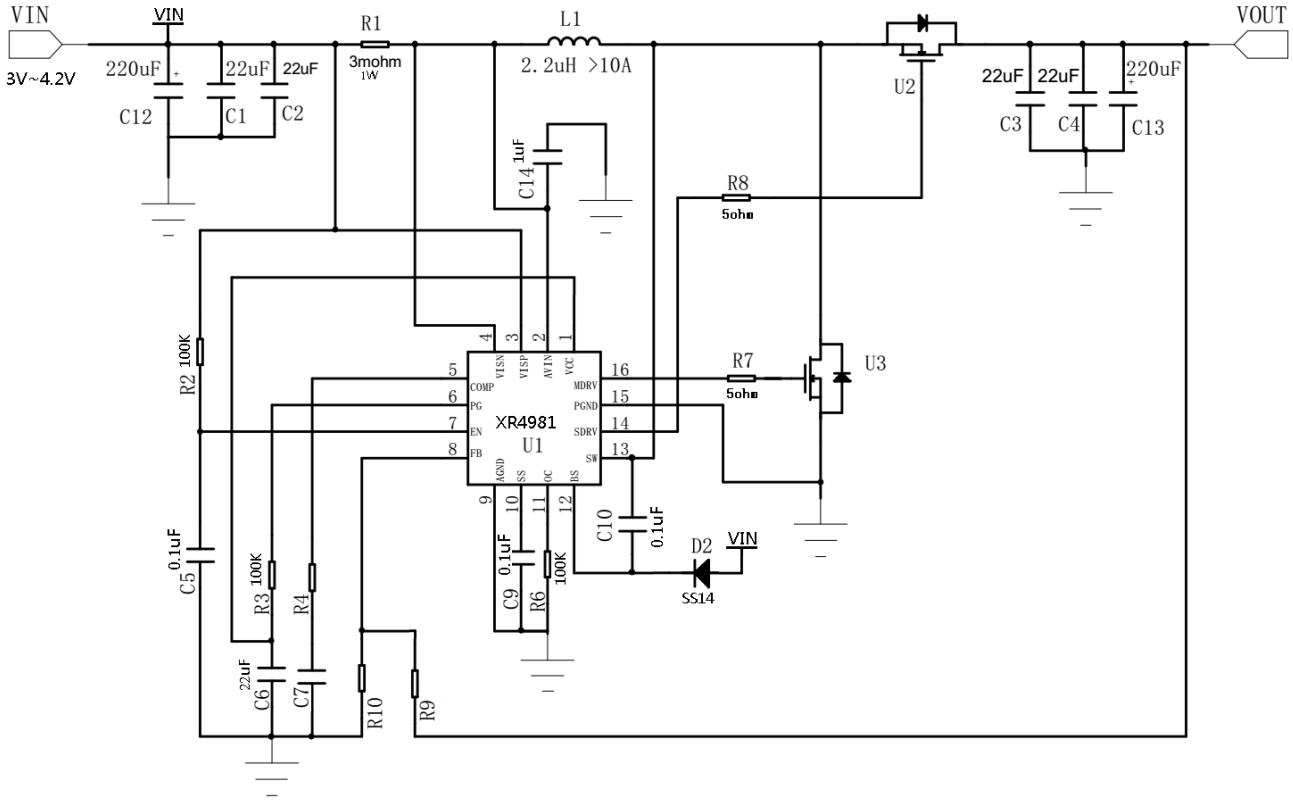


Figure 2. Typical Application Circuit2(Special for Single Li-Battery Input)

APPLICATIONS

- Power Bank
- QC 2.0 Device
- Type C USB Device
- Power Amplify Device
- Portable Class D Device
- 5V/9V/12V BUS Power Supply

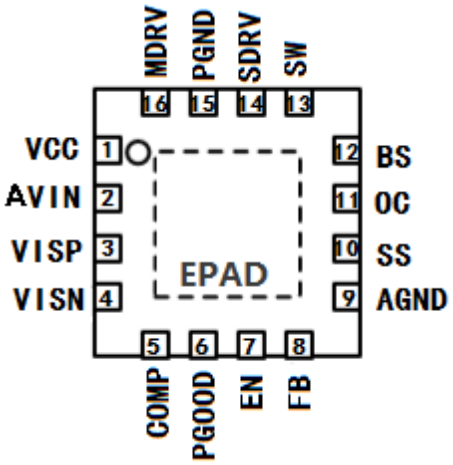
Typical application for input and output:

Input Voltage(V)	Output Voltage(V) /Output Current(A)					schematic
3.3~4.35	5V/5A	9V/3A	12V/2A	14.8V/2A	20V/1.5A	Circuit2
5		9V/4A	12V/3A	14.8V/2A	20V/1.5A	Circuit1
6~8.4		9V/5A	12V/3A	14.8V/2.5A	20V/2A	Circuit1
12~16.8			19V/4A	24V4A	20V/5.5A	Circuit1

ORDERING INFORMATION

PART NUMBER	TEMP RANGE	SWICHING FREQUENCY	OUTPUT VOLTAGE (V)	PACKAGE	PINS
XR4981	-40°C to 85°C	400KHZ	ADJ	QFN3x3	16

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VCC	Controller inside power logic Power Supply，inside LDO output pin，Must be closely decoupled to GND with a 22uF MLCC capacitor.
2	AVIN	Controller Power Supply，inside LDO input pin., Connect this pin with input voltage. Must be closely decoupled to GND with a 1uF MLCC capacitor.
3	VISP	Input current sense pin1-Positive side
4	VISN	Input current sense pin1-Negative side
5	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
6	PGOOD	Power good indicator. Open drain output, pull low when the output < 90% or >110% of regulation voltage, high impendence otherwise.
7	EN	Enable Input. Pull high to turn on the IC. Do not let this pin float.
8	FB	Feedback pin. Connect to the center of resistor voltage divider to program the output voltage: VOUT=1.2V×(R1/R2+1), please place this network close to FB pin
9	AGND	Analog ground
10	SS	Soft-start setting pin, Select 10nF~100nF Css to set different soft-start time
11	OC	Input current setting pin. Connect a resistor Roc from this pin to AGND to program output current limitation threshold. For Example,10A~12A current limit by 100K

12	BS	Boot-Strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with 0.1uFceramic cap .Please select Low VF schottky Diode.
13	SW	Switching Pin. Connect an inductor from power input to LX pin. Please select low Rdson & Big Enough Id & Isat inductor.
14	SDRV	High Side Power NMOS gate driver pin, Connect this pin to the gate of the high side synchronous rectifier N-channel MOSFET.
15	PGND	Power Ground
16	MDRV	LOW Side Power NMOS gate driver pin, Connect this pin to the gate of the low side N-channel MOSFET
EPAD	EPAD	GND and Thermal Pad, Please connect with mass metal plane for good heat dissipation

ABSOLUTE MAXIMUM RATINGS

(Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

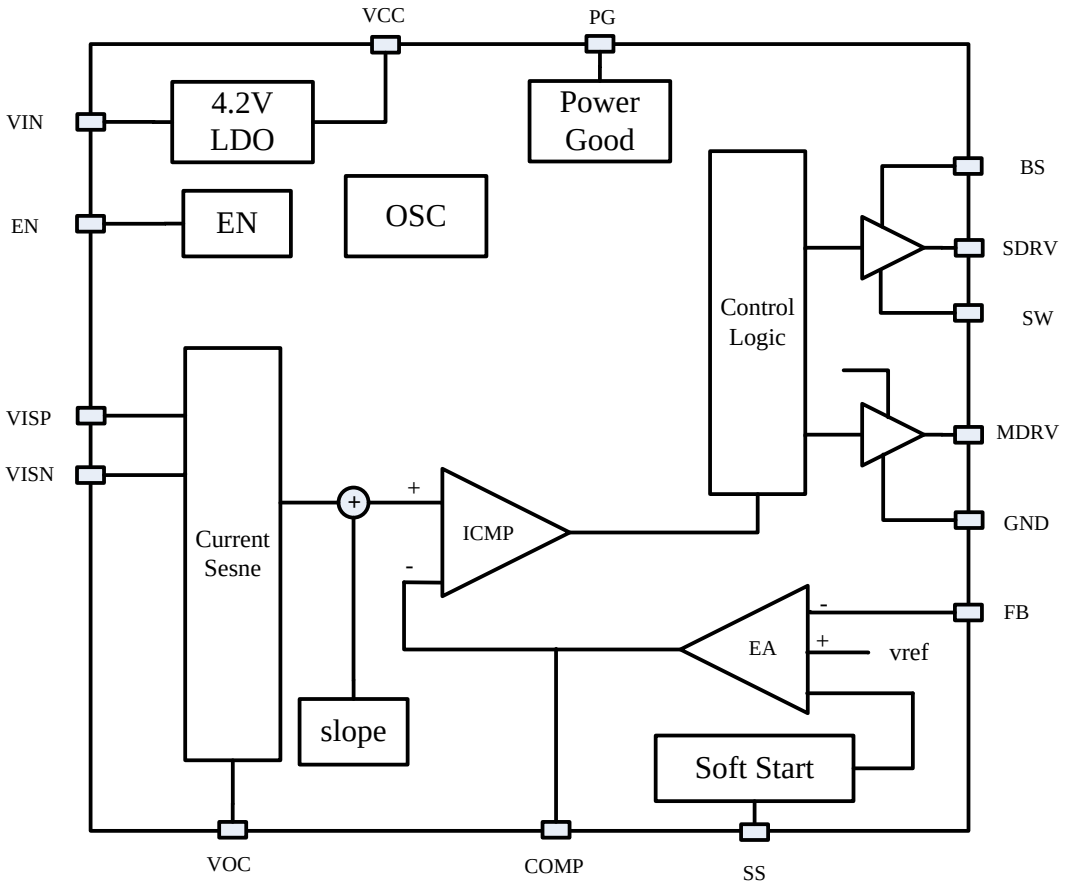
PARAMETER	VALUE	UNIT
AVIN、VISP、VISN、BS、SW、EN	40V	V
SDRV	SW+6	V
Other Pins	6V	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		3		36	V
Inside LDO output	VCC	Vin>=5V		4.2		V
Boost output voltage range	Vout		5		40	V
UVLO Threshold	V_{UVLO}	$V_{HYSTERESIS}$ =100mV		2.7		V
Operating Supply Current	I_{SUPPLY}	V_{FB} =1.5V , EN=Vin=3.6V, I_{Load} =0		70		μA
Shutdown Supply Current		V_{EN} =0V, V_{IN} =3.6V			10	
Regulated Feedback Voltage	V_{FB}		1.18	1.21	1.24	V
Peak inductor Current limit (N-MOSFET current limit)	Ilim	Roc=100K & Rs=3mohm		12.5		A
Oscillator Frequency	F_{OSC}		0.32	0.4	0.48	MHz
Enable Threshold		V_{IN} = 2.3V to 5.5V	0.3	1	1.5	V
Enable Leakage Current			-0.1		0.1	μA
Soft Start Time	Tss	Css=100nF Io=2A		300		ms

Functional Block Diagram



CONTROLLER CIRCUIT

The XR4981 is a constant-frequency ,PWM control , current mode boost controller. In normal operation, the external Main MOSFET is turned on each cycle when the oscillator gives an on-state. and then turned off when the main comparator -ICMP give an off state. The peak inductor current is controlled by the “COMP” pin, which is the output of the error amplifier EA. The EA compares the signal VFB pin which is the feedback of VOUT , with the internal bandgap reference voltage 1.21V.. Peak inductor current is sensed by a resistor which is connected series with inductor. The inductor current is determined by the output of EA. A slope compensation is added because of the PWM control method. When the load current increases, it causes decrease in VFB, which in turn causes the output of EA increases until the average inductor current matches the new load current.

OUTPUT VOLTAGE PROGRAMMING

The output voltage is set by a resistive divider according to the following equation:

$$R_9 = R_{10} \times \left(\frac{V_{OUT}}{1.21} - 1 \right)$$

Typically we suggest R10=10K or 12K and then determine R9 from the above equation。

For Example R10=12K,R9=107K Vout=12V

SOFT START SETTING

The soft-start time is programmed using a soft-start capacitor Css(C9) from the SS pin to AGND. When the converter is enabled, an internal 0.25μA current source charges the soft-start capacitor. When Css=0.1uF, Tss will be about 300ms, It is suggested to choose Css=0.1uF or 10nF. Do not use too small Css that will effect on load capacity.

CURRENT LIMIT SETTING

Input current limit can be set by Rs(R1) & Roc(R6) according to the following equation:

$$I_{oc} = \frac{16 * 10^{-6} * R_{oc} - 0.7}{24 * R_s}$$

For example, If Rs=3mΩ,Roc=100K，then Ioc=12.5A

For different input & output status, the current limit exist a little different.

The XR4981 monitors the inductor current and limits the current peak at current-limit level. For big current application we select small resistor such as 3mΩ~5mΩ to improve efficiency, for small current & high input voltage application we select a little big resistor such as 10mΩ~20mΩ to increase precision of current limit setting.

INDUCTOR SELECTION

In normal operation, the inductor maintains continuous current to the output. The inductor current has a ripple that is dependent on the inductance value. The high inductance reduces the ripple current & output ripple voltage..

Selected inductor by actual application:

Manufacturer	*Part Number*	*Inductance (uH)*	*DRC max (mOhms)*	*Dimensions L*W*H(mm3)*	*Id*	*Isat*
WURTH	74439358022	2.2	3.7	8.8*8.3*7.8	13A	30A
	74437368022	2.2	6.5	11*10*3.8	10A	28A
	7443330220	2.2	4.6	10.9*10*9.3	16.5A	22A
	74437349022	2.2	11.2	7.3*6.6*4.8	7.5A	14A
	744311220	2.2	11.4	6.9*7.0*3.8	9A	13A
TDK	SPM6530T	2.2	17	7.1*6.5*3	8.4A	
	VLP6045	2.2	20	6*6*4.5	6.4A	

Table 1. Recommend Surface Mount Inductors

Notes：Please select inductor according to Iin. The IL need to be 1.5~2*Iin.

For getting higher efficiency, need to use low DRC inductors.

INPUT CAPACITOR SELECTION

Two 22µF MLCC +220uF E-cap capacitors are recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. Based on the application requirements additional bulk capacitance are needed to meet input voltage ripple, transient and EMI requirements. Please select low ESR capacitor to reduce input ripple. Please ensure One 1uF MLCC capacitor is needed close to AVIN Pin. All input capacitor voltage rating should comfortably exceed the maximum input voltage, normally twice than max input voltage.

OUTPUT CAPACITOR SELECTION

Two 22µF MLCC +220uF E-cap capacitors are recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. Based on the application requirements additional bulk capacitance are needed to meet output voltage ripple, transient and EMI requirements. Please select low ESR capacitor to reduce input ripple. The ripple can be given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where Cout is the output filter capacitor. The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (e.g., OS-CON and POSCAP).

All output capacitor voltage rating should comfortably exceed the maximum output voltage, normally twice than max output voltage.

MOSFET SELECTION

Two external power MOSFETs must be selected for the MT5086: one N-channel MOSFET for the low side (main)switch, and one N-channel MOSFET for the high side (synchronous) switch. The maximum gate drive voltage levels are set by the VCC voltage which is typically 4.2V. Consequently, use low logic-level threshold MOSFETs in most applications.

The power loss in the MOSFETs are switching and conduction losses. Both losses are the highest at the minimum input voltage when the output current is the maximum. Low Rdson & small Crss/Ciss/Coss of MOSFET is very important to reduce these two losses for high efficiency. The voltage rating of MOSFET-Vds should comfortably exceed the maximum output voltage, normally twice than max output voltage.

For good heat dissipation please select MOSFET with thermal pad such as Power Pack、ESOP、TO-252.

For Example: For 12Vin 20Vout 5A Application

MOSFET‘s specification request:

Vds>=40V Id>=15A Rdson(Vgs=4.5V) <10mΩ Low Ciss/Coss/Crss

Power Pack SO-8 or ESOP8 package(TO-252 also OK) Si7848 is one of your choice.

POWER GOOD

The PGOOD pin is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.21V reference voltage. When the FB pin voltage is within the ±10% regulation threshold range, the internal MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to VCC pin, normally use 100K resistor.

BOOTSTRAP CAPACITOR SELECTION

Place a 0.1μF~1μF X5R or X7R ceramic capacitor between the BST and SW pins for proper operation. This capacitor provides the instantaneous charge and gate drive voltage needed to turn on the high-side MOSFET. Please place this capacitor close BS pin & SW.

VCC LDO REGULATOR

XR4981 integrate an internal P-channel low dropout linear regulator (LDO) that supplies power to the VCC pin from the VIN supply pin. VCC powers the gate drivers and much of the XR4981's internal circuitry. The LDO output VCC is regulated to 4.2V. It can supply at least 50mA and must be bypassed to ground with a 22μF X5R or better grade ceramic capacitor, The capacitor should have a 10 V voltage rating. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. Please place this capacitor close to VCC pin & GND。

A VCC under-voltage detection circuit prevents the internal PWM control circuitry and gate drivers from operation when VCC voltage is below 2.7V (typical).

CONTROL LOOP COMPENSATION

XR4981 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

$$A_{VDC}=\frac{A_{VEA}*V_{IN}*R_{load}*V_{fb}*G_{cs}}{0.5*V_{out}},\ w_{p1}=\frac{1}{0.5R_{load}C_{out}},\ w_{p2}=\frac{G_{EA}}{A_{VEA}C_z},\ w_z=\frac{1}{R_z*C_z},\ w_{zRHP}=\frac{Rload*(\frac{V_{IN}}{V_{OUT}})^2}{L}$$

Suitable loop compensation is very important for steady output & startup. if want to get better transient response, you should increase band width. On the promise of stability you can increase Rz or reduce Cz to get better performance.

$$Bandwith=\frac{V_{fb}G_{cs}*V_{IN}*G_{EA}*R_z}{2*V_{OUT}*C_z}.$$

Table 2. Recommended Compensation Network Values

VIN	VOUT	L(uH)	Cz	Rz(K)
3	12	2.2	20nF	20K
3	20	2.2	20nF	40K
5	12	2.2	20nF	20K
5	20	2.2	20nF	40K
12	24	10	20nF	50K

Also, you can select Rz=0,Cz=50nF to make steady for every input & output status, for example 3.3V~12V input 9V~24V output, but it will be decrease the performance of circuit.

STARTUP AND SHUTDOWN

If both VIN and EN are higher than their appropriate thresholds, the chip starts. Firstly, the reference block starts to generate stable reference voltage and currents, and then the internal regulator is enabled. The regulator

provides stable supply for the remaining circuitries.

If Vin<UVLO threshold voltage or EN< Enable threshold voltage, the chip shuts down.

PCB LAYOUT GUIDE

1) Cavin and Cvcc should be placed as close as possible to the IC pins & GND

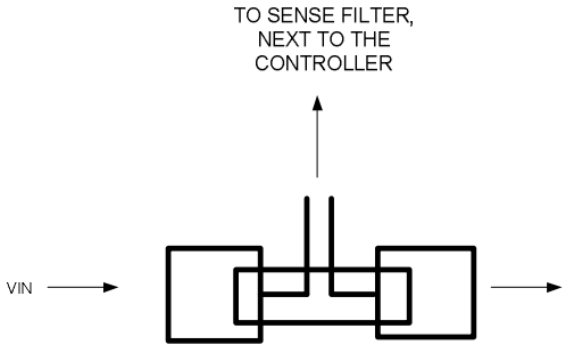
2) The feedback divider should be placed as close as possible to the control ground pin of the IC. The components R9 and R10, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem

3) Please ensure sensitive logic pins' circuit close to these pins, such as COMP、SS、OC

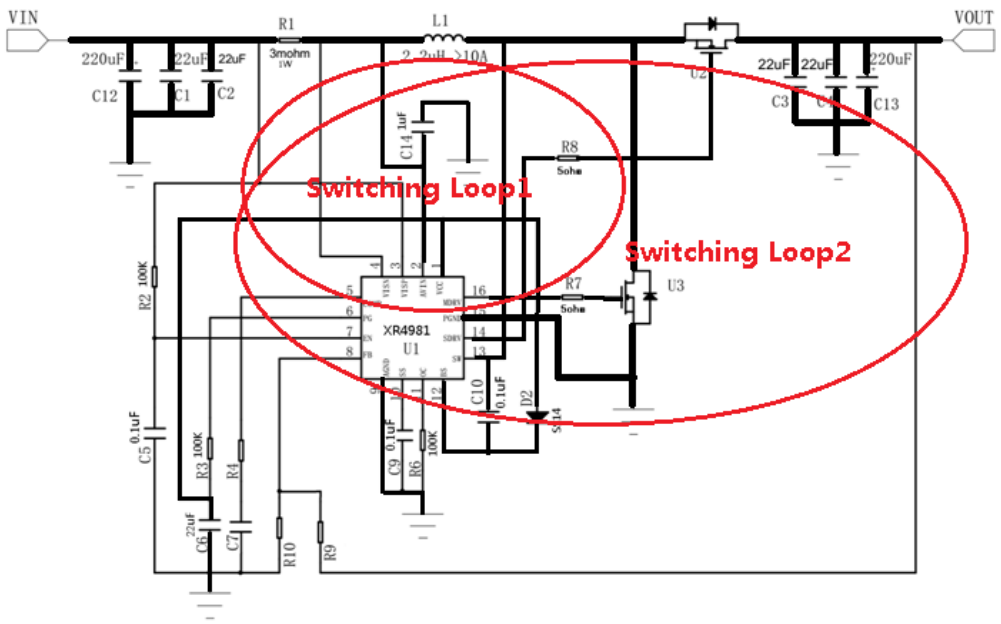
4) The big current path must be broad & short line in PCB just as below 。It is desirable to maximize the PCB copper area connecting to GND/EPAD pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable。

5) Please make sure MDRV & SDRV similar pcb layout and broad lines.

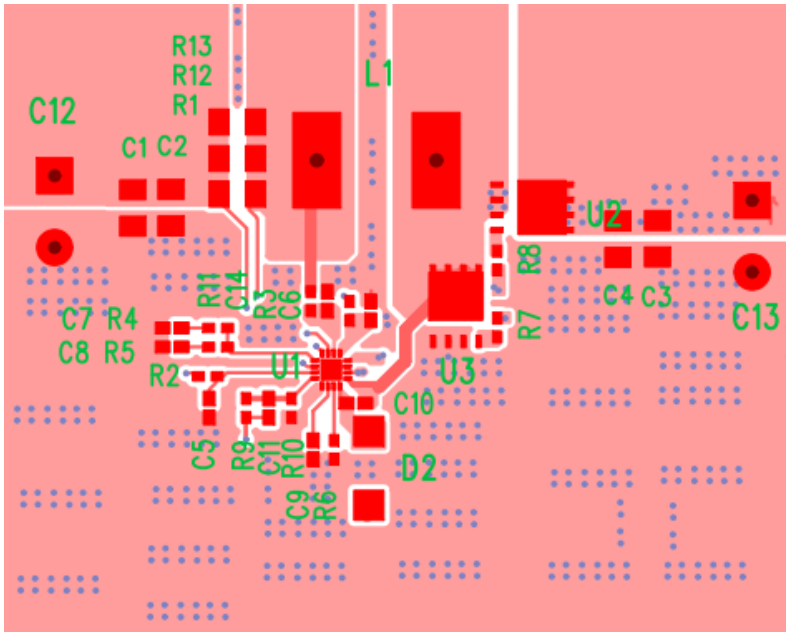
6) Please draw parallel lines for avoid Common-mode interference just as below:



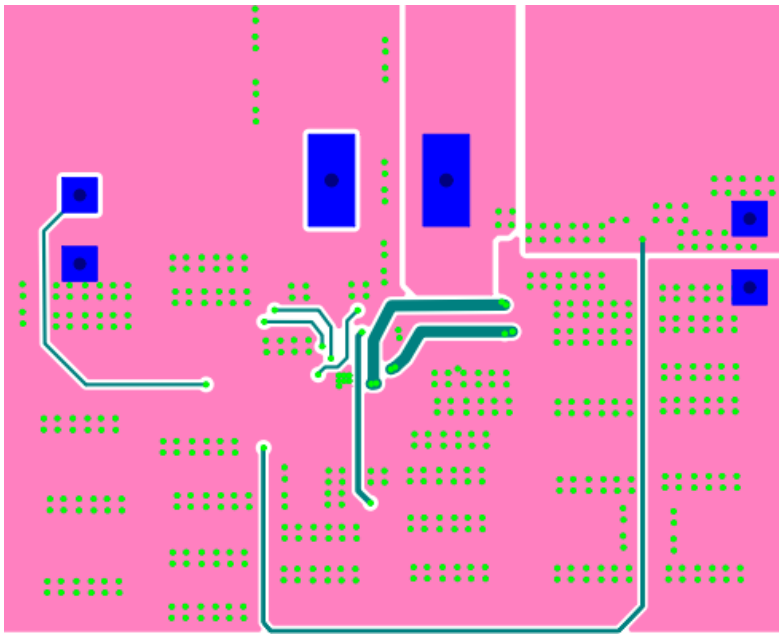
7) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.Just like Switching loop1 and Switching loop2, should minimize their area to avoid EMI problem.



SWITCHING LOOP & BIG CURRENT CIRCUIT



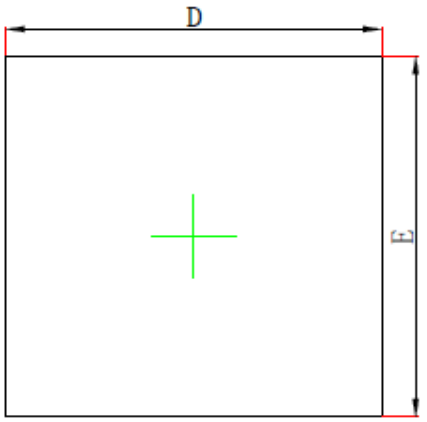
TOP LAYER



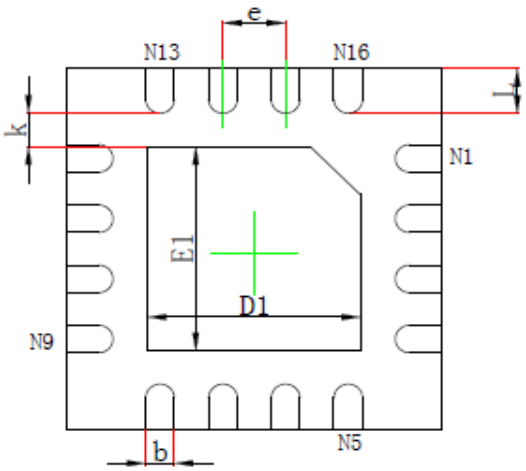
BOTTOM LAYER

PACKAGE OUTLINE（DFN3X3-16)

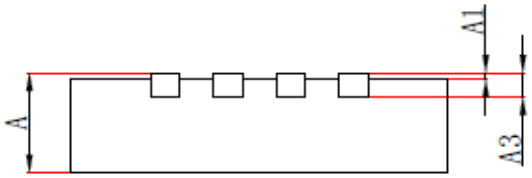
QFNWB3×3-16L(P0.50T0.75/0.85)PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.280	0.007	0.011
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019