LED driver IC

MV1011SC

Application Note
Version 1.0

新電元
SHINDENGEN

Smart-Resoic®

MV1011SC

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Caution	⚠	Improper handling may result in minor injury or property damage.

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	⚠	In the event of a problem, an excessive voltage may arise at an output terminal, or the voltage may drop. Anticipate these fluctuations and any consequential malfunctions or destruction and provide adequate protection for equipment, such as overvoltage or overcurrent protection.
	⚠	Check the polarity of the input and output terminals. Make sure they are properly connected before turning on power. <<Failure to do so may lead to failure of the protective element or generate smoke or fire.>>
	⚠	Use only the specified input voltage. Deploy a protective element on the input line. <<Problems may result in smoke or fire.>>
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Contents

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1. Overview

1.1 Features

The MV1011SC is an LED driver IC that can be operated through bus voltage direct. Omitting the auxiliary winding enables a single power supply configuration, and quasi-resonant operation in critical conduction mode raises efficiency and lowers noise.

In general critical conduction mode, the switching frequency increases when the dimming ratio decreases. This increases switching losses and imposes limitations on the lowest dimming ratios, disadvantageously. When the dimming ratio decreases, the MV1011SC automatically switches from critical conduction mode to discontinuous conduction mode. This prevents the switching frequency increasing, reduces switching losses, and achieves smooth and deep dimming free of flickering. The MV1011SC can stop gate output by holding the V_{REF} at or below the oscillation-off REF pin threshold voltage (Vth_REF_sp).

The MV1011SC has the following features:

■ Allows quasi-resonant operation without auxiliary winding.

■ Quasi-resonant operation in critical conduction mode helps achieve low input change, raises efficiency, and lowers noise.

■ Off-time modulation enables deep dimming (1% or less).

■ Allows PWM dimming input and linear dimming input.

■ Gate output stop at V_{REF}=< Vth_REF_sp.

■ Compatible with Glow wall switch

■ Allows LED open-circuit protection using auxiliary winding.

■ Features UVLO, and LED short-circuit protection.

■ Can be operated through bus voltage direct.

1.2 Block diagram

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1.3 Pin assignment

Index Mark

TOP VIEW

| Svout | 1 | | 8 | Vin |

Marking Area

Svin	2		7	REF
CS	3		6	Vcc
GND	4		5	Gate
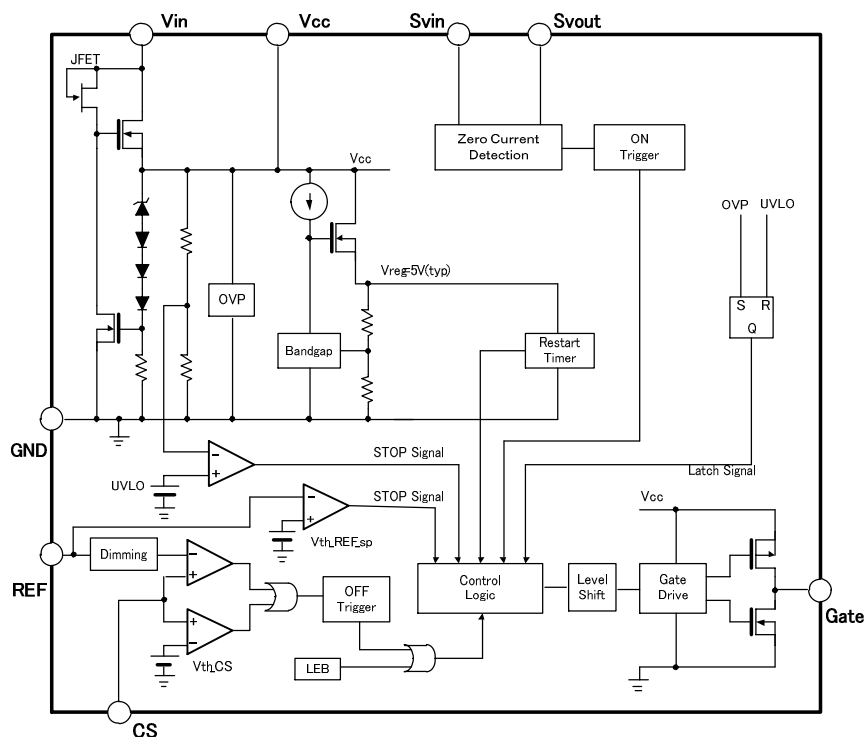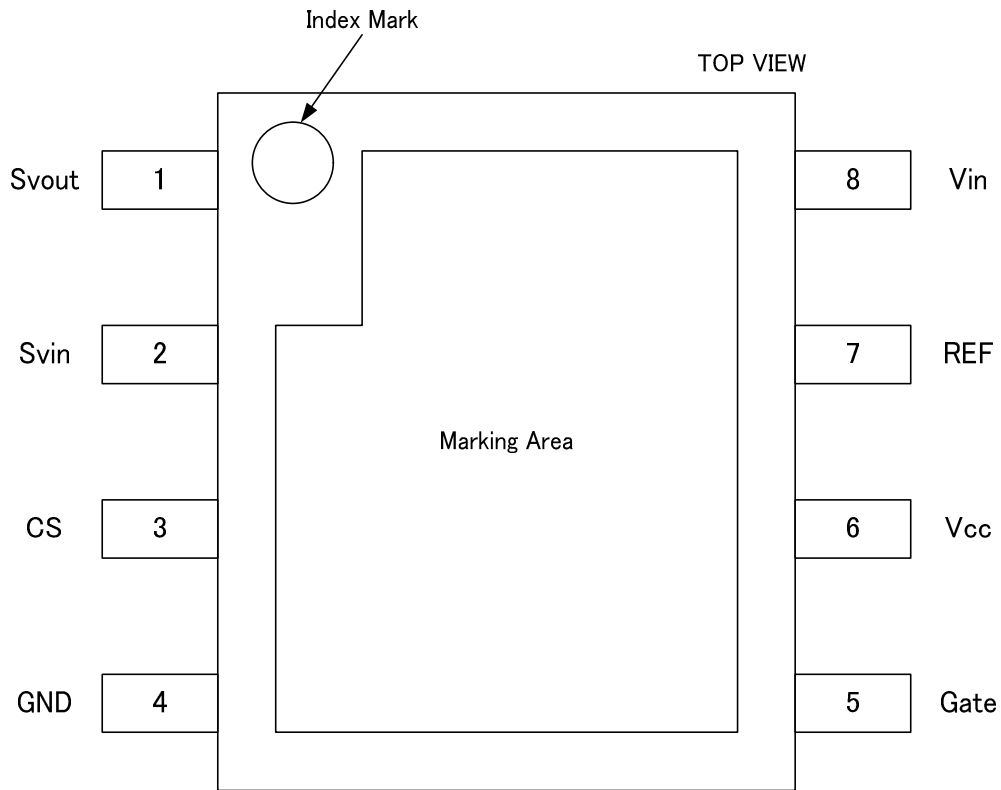
Package : SOP8J

1.4 Pin functions

Pin No.	Symbol	Name
1	Svout	Zero current detection pin
2	Svin	Zero current reference pin
3	CS	Current sense pin
4	GND	Ground pin
5	Gate	The output pin for main a MOSFET drive
6	Vcc	IC power supply pin
7	REF	Dimming pin
8	Vin	AC input pin

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2. Explanation of basic operations

The MV1011SC is a critical conduction mode (CRM) step-down chopper control IC. Figure 1 shows the circuit configuration. Figure 2 shows the waveforms of currents flowing to the MOSFET and the diode, represented by Id and I_F, respectively. In a general CRM step-down chopper circuit, the MOSFET is turned on after the I_F becomes zero, leaving little recovery current for the diode and lower losses and noises than a PWM circuit. Meanwhile, disadvantageously, the oscillation frequency changes dramatically as the output current (LED current) changes, resulting in poorer dimming characteristics and efficiency.

The MV1011SC detects Id, converted to a voltage, with the current detection pin (CS pin). When it reaches the CS reference voltage, the MV1011SC turns the MOSFET off (peak current detection). The IC performs CRM control in this way: When the diode current I_F becomes zero, the Svout voltage falls below the Svin voltage, so the IC detects this state (zero current detection) and turns the MOSFET on. The voltages on both ends of the choke (① and ② in Figure 2) are divided with resistors and input to the Svin pin and the Svout pin to achieve CRM operations without auxiliary winding. Additionally, the off-time modulation prevents the frequency increasing during dimming and achieves constant high efficiency and dimming characteristics during deep dimming. (See Section 5 [Dimming characteristics] on page 20.)
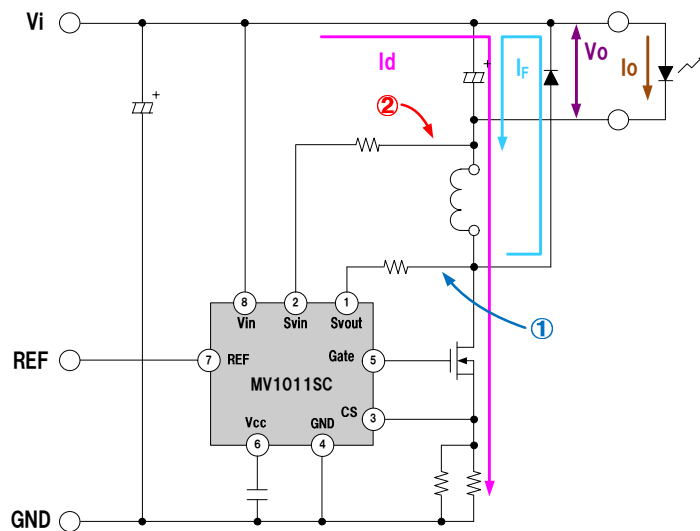
Figure 1 CRM step-down chopper circuit
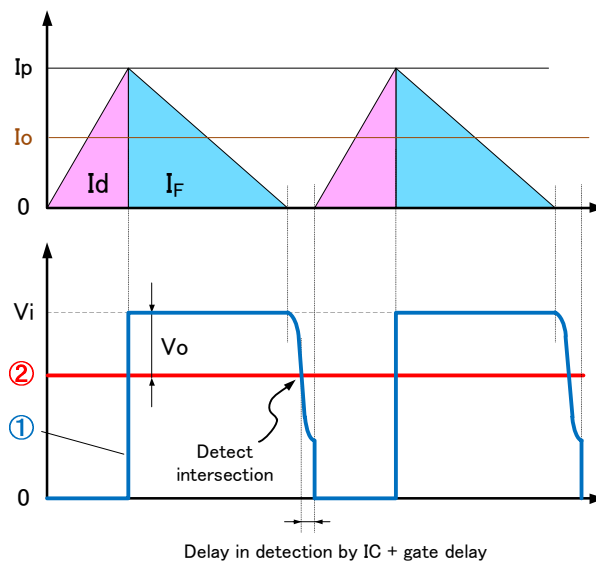
Figure 2 MOSFET and diode current waveforms of the CRM step-down chopper and voltage waveforms on both ends of the choke

2.1 Starting sequence

The MV1011SC can provide an internal power supply from the high-voltage start circuit in the Vin pin. The IC starts up when a voltage equal to or exceeding the starting voltage (Vcc_start). To ensure stable operations, the signal should be sent to the REF pin when the Vcc voltage is equal to or greater than the Vcc_start.

Figure 3 shows an example of a starting operation in the Vcc->REF sequence, using the circuit configuration shown in Figure 1.

In a normal start operation, oscillations start when the Vcc voltage reaches Vcc_start and the V_{REF} voltage reaches the oscillation-off REF pin threshold voltage (Vth_REF_sp). As the output voltage rises, the Svin voltage crosses the Svout voltage, enabling zero current detection. (Figure 3(a) Starting operation OK)

When it is difficult to charge the output capacitor—for instance, when the resistance of the gate resistor R4 is large or when the resistance of a dummy resistor connected in parallel with LED is small—the output voltage may not rise after oscillation has started and zero current detection may be disabled. When zero current detection cannot be performed, the IC is forcibly switched over to the restart operation, in which the minimum on-time and maximum off-time are used, instead of the normal peak current detection operation. When zero current detection is left disabled, the restart operation continues and LED will not light. (Figure 3(b) Starting operation NG)

Be sure to measure the Svin and Svout voltages at the start of the actual apparatus to confirm that zero current detection is enabled.
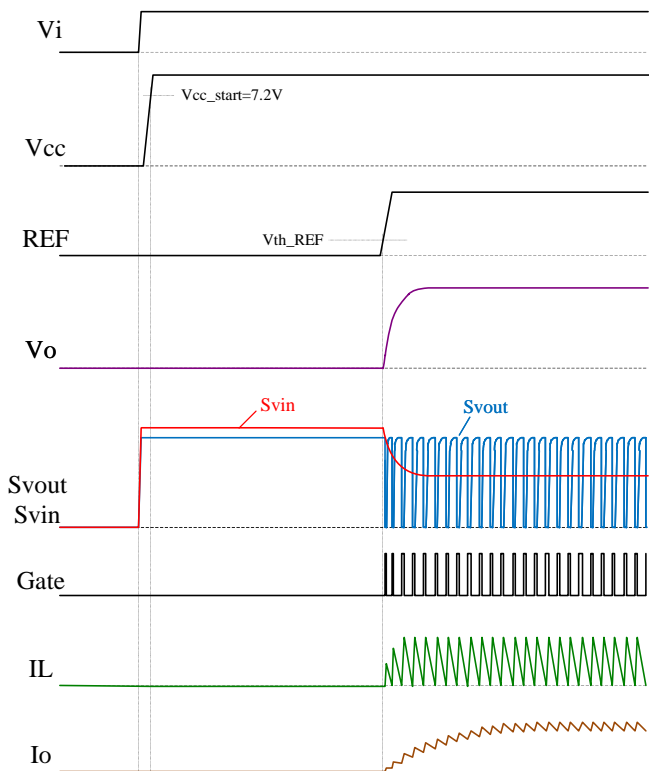
Figure 3(a) Starting operation OK
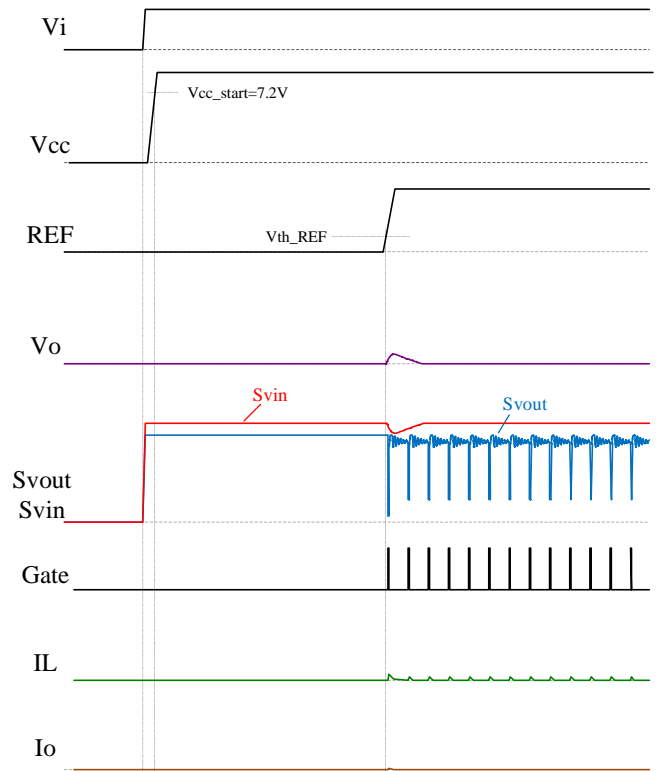
Figure 3(b) Starting operation NG

3. Component selection procedure and calculation method

The calculation is an estimate. In an actual circuit, errors may occur for various reasons, including the characteristics of individual parts and IC detection delays. Be sure to check with the actual apparatus and to make any adjustments needed.

When using an oscilloscope to verify waveforms, note that the waveform and characteristics change depending on probe capacitance. In particular, pay close attention when measuring the Svin, Svout, and CS pins, and D-S of the MOSFET.

Unless otherwise specified, the figures used in this document are typical values.

3.1 Basic circuit configuration

Figure 4 shows the basic circuit configuration. Figure 5 shows the basic operation waveforms. Since MV1011SC can provide an internal power supply from the high-voltage start circuit in the Vin pin, a high pressure (less than DC250V) after full-wave rectification can be input directly (bus voltage direct supply).

As shown in Figure 4, detecting the voltages on both ends of the choke eliminates the need for an auxiliary winding and enables a simple, low-cost circuit configuration.
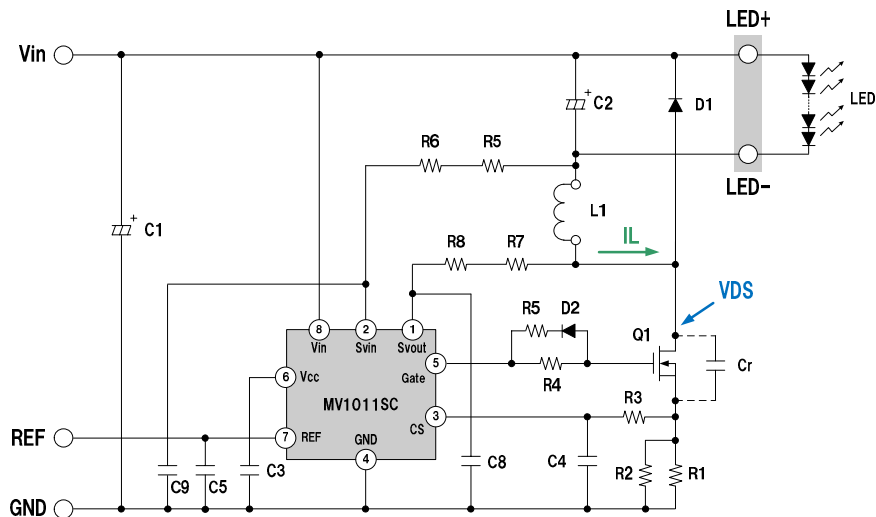
Figure 4 Basic circuit configuration

Figure 5 Basic operation waveforms

$$ton = \frac{L}{(Vi - Vo)} \times Ip$$

$$toff1 = \frac{L}{(Vo + V_F)} \times Ip$$

(∗) The chart emphasizes the toff2 period.

3.2 Component selection

The chart below shows a design procedure, from determination of the specification to adjustment. The design procedure provided in this section is an example of electrical design.

During the design process, be sure to comply with safety standards established by official bodies and with your company rules.

```
                    ┌──────────────────┐
                    │    Detarmine     │
                    │  specification   │
                    └──────────────────┘
                             │
            ┌────────────────────────────────────────┐
            │             Basic design               │
            │                                         │
            │  See [3.2 Component seletion] on pp.9-14 │
            │  See [3.3 Winding voltage supply] on pp.15-17 │
            └────────────────────────────────────────┘
                             │
                    ┌──────────────────┐
                    │   Build a power   │
                    │      supply       │
                    └──────────────────┘
```
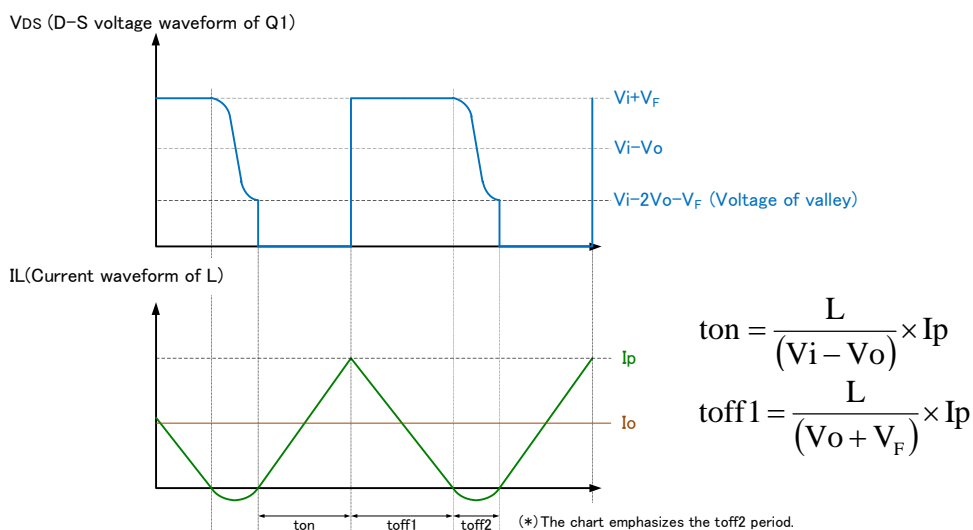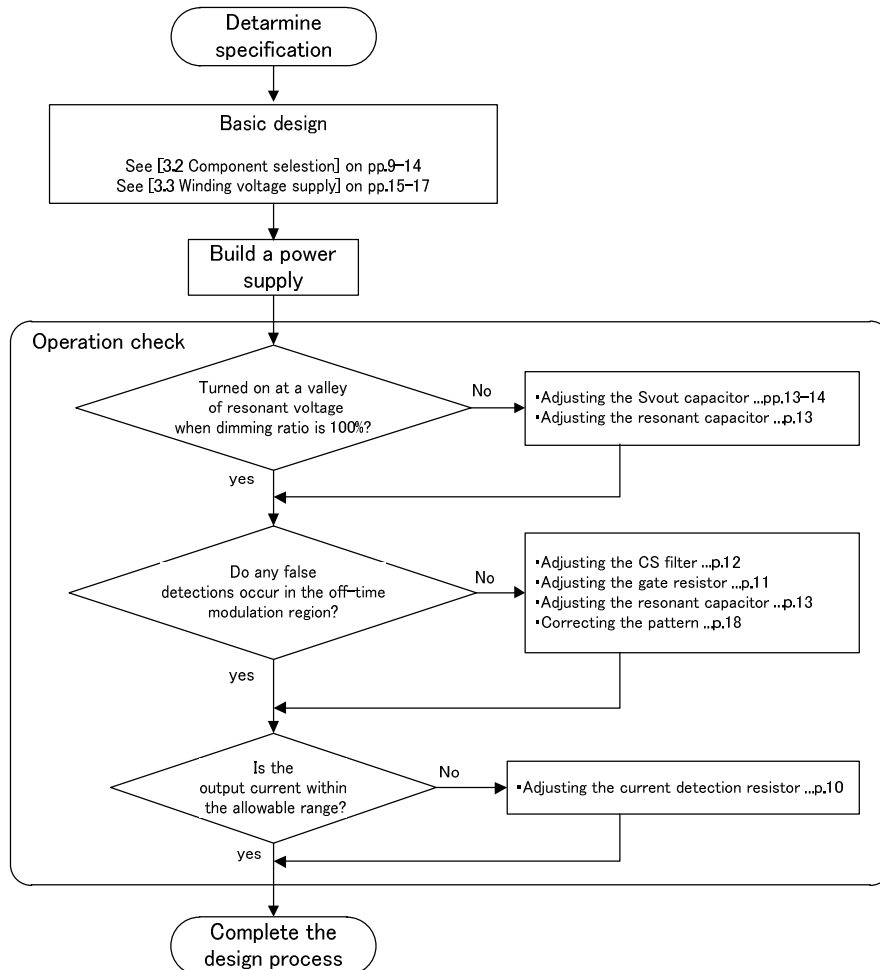
Operation check

Turned on at a valley of resonant voltage when dimming ratio is 100%?   → No →
- Adjusting the Svout capacitor ...pp.13-14
- Adjusting the resonant capacitor ...p.13

yes

Do any false detections occur in the off-time modulation region?   → No →
- Adjusting the CS filter ...p.12
- Adjusting the gate resistor ...p.11
- Adjusting the resonant capacitor ...p.13
- Correcting the pattern ...p.18

yes

Is the output current within the allowable range?   → No →
- Adjusting the current detection resistor ...p.10

yes

Complete the design process

* Repeat the operations check if a component constant changes after design has been completed.

3.2.1   MOSFET (Q1)

The MOSFET receives the voltages shown in Figure 5. The maximum applied voltage nearly equals the maximum input voltage. In actual use, voltage spikes may occur—for instance, due to parasitic inductance of the wiring pattern. Check with the actual apparatus and select a component with sufficient withstand voltage.

For a lighting apparatus that consumes a large amount of power, MOSFETs with low on-resistance offer advantages. When power consumption is small, MOSFETs with small capacitance, such as Ciss and Coss, help achieve highly efficient and advantageous dimming characteristics.

IC power consumption is the product of the input voltage and current consumption. Current consumption is the sum of the logic current and the gate drive current. Select MOSFETs that have the lowest possible gate capacitance. (See Table 1 Recommended MOSFETs.)

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Table 1 Recommended MOSFETs (as of January 2015)

Product name	Withstand voltage (V)	Id (A)	Ron (typ)	Ron (max)	Qg (nC)	Ciss (pF)	Coss (pF)	Manufacturer	Package
P3B28HP2	280	3	1.7	2	3.6	120	25	Shindengen	FB
P6B28HP2		6	0.66	0.85	5.7	240	43	Shindengen	FB
P1R5B40HP2	400	1.5	4.2	5	3.9	120	20	Shindengen	FB
P4B40HP2		4	1.54	1.9	6.5	245	33	Shindengen	FB
P1B52HP2	525	1	6	7.2	4.3	125	20	Shindengen	FB
P5B52HP2		5	1.4	1.7	10.5	400	45	Shindengen	FB
P6B52HP2		6	1.1	1.35	15	520	58	Shindengen	FB
P0R5B60HP2	600	0.5	8.3	10	4.3	120	18	Shindengen	FB

3.2.2 Fly-wheel diode (D1)

Just as with MOSFETs, the fly-wheel diode must have withstand voltage greater than the input voltage. Additionally, select a fast recovery diode (FRD) suitable for high-speed switching with trr of around 100 nsec or less. (See Table 2 Recommended fly-wheel diodes.)

Table 2 Recommended fly-wheel diodes (as of January 2015)

Product name	Withstand voltage (V)	Io (A)	V_F (V)	Cj (pF)	trr (ns)	Manufacturer	Package
D1FL20U	200	1.1	0.98	-	35	Shindengen	1F
D2FL20U		1.5	0.98	-	35	Shindengen	2F
D1FL40U	400	1.5	1.2	11	25	Shindengen	1F
D2FL40		1.3	1.3	-	50	Shindengen	2F
D1FK60	600	0.8	1.3	11	75	Shindengen	1F
D2FK60		1.5	1.3	16	75	Shindengen	2F

3.2.3 Current detection resistor (R1 and R2)

The current detection threshold of the CS pin should be Vth_CS = 0.495 V, and R1/R2 = Rcs. In Figure 5, when toff2 is significantly less than ton or toff1, the peak current of Id, Ip, is double the output current Io. Thus, the Rcs is calculated using the output current when the dimming ratio is 100%, Io (max), as follows:

$$Rcs = \frac{Vth\_CS}{Ip} = \frac{0.495}{2 \times Io(max)}$$

In actual use, the current will vary slightly from the calculated value due to toff2 and detection delay. Adjust to the appropriate resistance with the actual apparatus.

3.2.4 Inductor (L1)

Inductance is calculated, ignoring toff2, as follows, where the input voltage is represented by Vi, the output voltage (LED voltage) by Vo, the switching frequency by f, the inductance by L, the forward voltage of the fly-wheel diode D1 by V_F:

$$L = \frac{(Vi - Vo) \times (Vo + V_F)}{2 \times f \times Io \times (Vi + V_F)}$$

The switching frequency changes with changes in input voltage and with dimming.

A general inductor has the DC bias characteristics shown in Figure 6(a). As current increases, inductance decreases. This results in the MOSFET current waveform indicated by a solid line in Figure 6(b). The output current Io is slightly smaller than the calculated value.

The inductor receives the peak current Ip about twice larger than the output current Io and thus pay attention to a decrease in inductance with Ip when selecting the inductor.
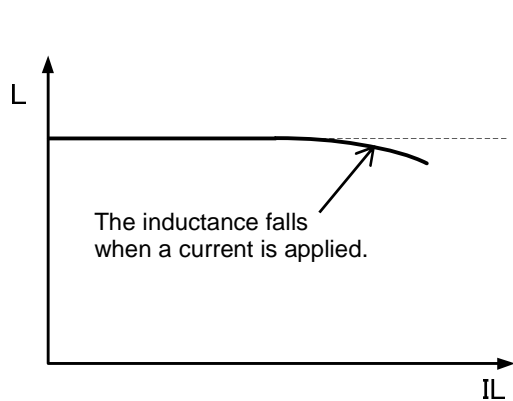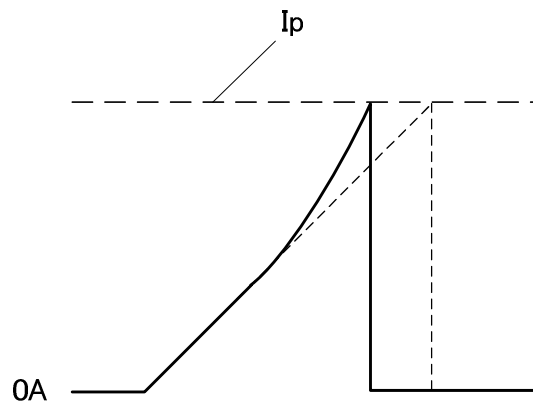

Figure 6(a) Inductor's DC bias characteristics   Figure 6(b) MOSFET current waveform at inductance drop

3.2.5 Gate drive circuit (R4, R9, and D2)

In the IC, the gate charging current (IG_source) is limited to about 40 mA and the discharge current (IG_sink) to about 425 mA. Thus, the circuit can be used with R4 = 0 Ω—i.e., with a direct connection. Using R4 enables adjustment for delays, noise reduction, and improved dimming characteristics. However, if the resistance of R4 is too large, zero current detection may not be performed once the restart operation starts. The restart operation may continue. To determine the resistance of R4, be sure to confirm that zero current detection can be performed even when oscillation starts with the REF voltage slowed up

When R4 is added to the circuit, the discharge current is limited. To achieve advantageous constant-current characteristics, the delay needs to be small; this means a discharge diode is required, D2. The discharge current can be adjusted with resistor R9.

The charge and discharge currents above are levels with Vcc = 9 V. They will vary depending on Vcc value.

3.2.6 Resistors for Svin and Svout pins(R5, R6, R7 and R8)

The Svin and Svout pins are used for comparator input to detect voltage inversions on both ends of L1 to determine switching timing on (zero current detection). To ensure advantageous comparator characteristics, the input voltage into the pins should not exceed 3.5 V. The voltages on both ends of L are very high; voltage dividing resistors (R5, R6, R7, and R8) are required, as shown in the circuit diagram (Figure 7).

Due to the configuration of the basic circuit, an LED leak current flows via the voltage dividing resistors (R5 to R8) and the IC internal resistor (25 kΩ). To reduce output current when the IC is not operating and the dimming ratio is at its minimum, use a winding voltage supply, as described in Section 3.3.

Figure 7 shows the voltage waveforms of the Svin and Svout pins and the internal circuit diagram.
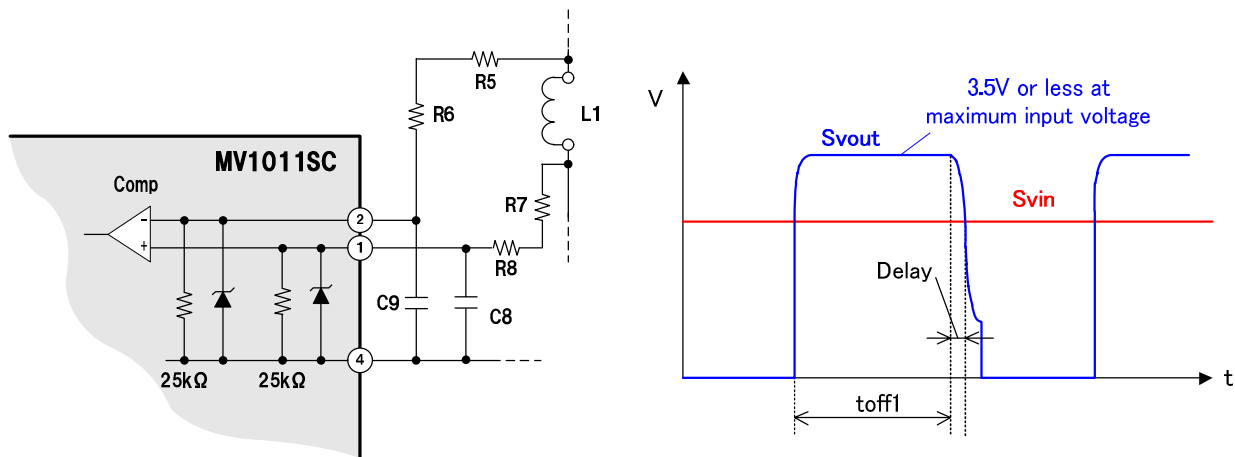

Figure 7 Zero current detecting operation waveforms and internal circuit diagram

Select R7 and R8 so that the Svout pin voltage is around 3 V when the input voltage is at maximum. Use the following formula:

$$R7 + R8 = \frac{25k \times (Vi\_max - V_F)}{3} - 25k$$

Select R5 and R6 with resistance about 5% lower than R7 and R8. (See Section 6.2 [LED short circuits] on page 29.)

Select highly accurate resistors as R5, R6, R7, and R8 (accuracy ±1% or better).

When the output voltage Vo does not exceed 10% of the maximum input voltage Vi, zero current detection may be disabled. In that case, use the winding voltage supply, as described in Section 3.3 on page 15.

3.2.7 CS pin filter (R3 and C4)

R3 and C4 are filters used to shield the CS pin from noise. Adjusting R3 to range between 0 Ω and several kΩ and C4 between 10 pF and 100 pF will reduce false detections of off-timing due to switching-on noise in the off-time modulation region. When adjusting the filter constants, check for false detections on the actual apparatus using as many different REF pin voltage V_{REF} settings as possible within the REF voltage range given in the specification. (For details, see Section 5.1.2 [[B] Off-time modulation range] on pages 22 to 23.)

If the filter constants set are too large, the detection delay will grow, along with the change in output current due to the output current setting and the input voltage. Reselect current detection resistors (R1 and R2) or the inductor, if necessary.

3.2.8 Vcc pin smoothing capacitor (C3)

C3 is a capacitor used to stabilize the power supply voltage of the Vcc pin. Check the Vcc pin voltage waveform and select a capacitor with capacitance of 0.1 uF or more. A very large capacitance value will length start times. Check with the actual apparatus.

3.2.9 REF pin capacitor (C5)

C5 is a capacitor used to prevent unintended noise-induced operations. The capacitance of the capacitor should be around 1000 pF. For dimming methods, see Section 5 [Dimming characteristics] on page 20.

3.2.10 Svin pin capacitor (C9)

C9 is a capacitor used to prevent unintended noise-induced operations. The capacitance of the capacitor should be around 1000 pF.

3.2.11 Resonant capacitor (Cr)

In addition to enabling adjustments of the resonant period, Cr will reduce switching-off noise. However, note that it may also increase switching-on noise. If Cr is too large, dimming characteristics and efficiency may be degraded. We recommend against using this capacitor. If you wish to use it, make adjustments with the actual apparatus to minimize capacitance.

3.2.12 Input capacitor (C1) and Output capacitor (C2)

Select input and output capacitors after considering allowable ripple current, life, output holding time, etc. The ripple current of a capacitor is calculated by the following formulas:

Ripple current of input capacitor   Ripple current of output capacitor

$$\text{Iripin} = \text{Ip} \times \sqrt{D \times \left(\frac{1}{3} - \frac{D}{4}\right)}$$

$$\text{Iripout} = \frac{\text{Io}}{\sqrt{3}}$$

Where D represents the switching duty cycle.

D is obtained using the formula, $D = Vo/Vi$, based on the relationship between input and output voltages.

In the case of an input capacitor, ripple currents are added from input circuit devices, such as the full wave rectifier and PFC. Consider these as well when selecting the capacitor.

3.2.13 Svout pin capacitor (C8)

C8 is a capacitor used to adjust the delay shown in Figure 7 and to the on-timing. For a discussion of adjusting on-timing using C8, see [Additional explanation of resonant period in quasi-resonant operation] on page 14.

C8 also prevents unintended noise-induced operations. Adjust the capacitance to around 10 to 100 pF with the actual apparatus.

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Additional explanation of resonant period in quasi-resonant operation
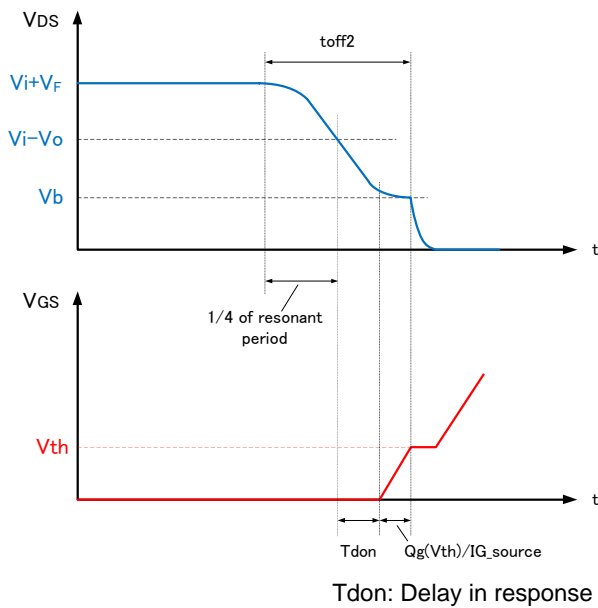
Example of gate charge characteristics
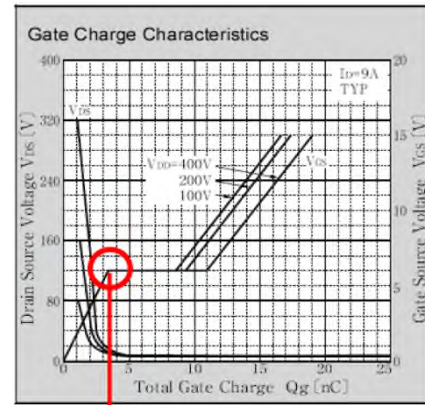
Qg (Vth): Accumulated charge until the voltage reaches the gate threshold

Tdon: Delay in response

Figure 8 Adjusting the delay

Ideally, the MOSFET should be turned on at a valley of resonance as shown in Figure 8. The corresponding condition is expressed by the following formula:

$$\frac{1}{4} \times 2\pi\sqrt{L \times (Cr + Coss + Cj)} = Td_{on} + \frac{Qg(Vth)}{Ig}$$

Coss: Output capacitance of MOSFET
Cr: Capacitance of D-S capacitor
Cj: Junction capacitance of fly-wheel diode

Since Vb = Vi - 2Vo - V$_F$, switching losses are minimized. While the condition above may not be completely fulfilled in actual use, MOSFETs do not need to be switched on precisely at a valley. If the on-timing is far from the valley, it can be adjusted as follows:

(1) The left side is large:
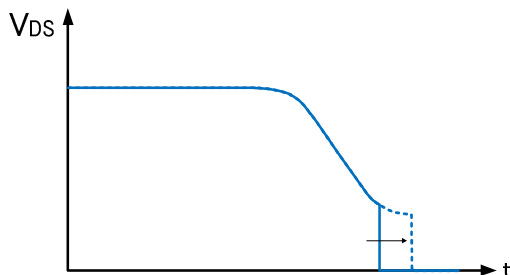
⇒ Delay the on-timing.
• Increase C8 or R4.

(2) The right side is large:
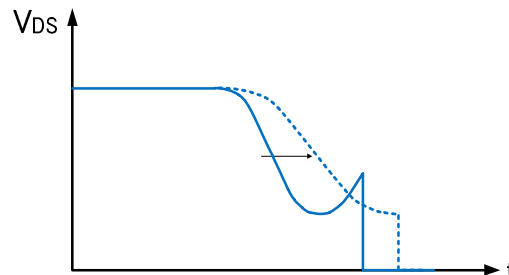
⇒ Lengthen the resonant period.
• Add or increase Cr.

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3.3 Winding voltage supply

3.3.1 Configuration of a winding voltage supply

Using an auxiliary winding shown in Figure 9 protects the MV1011SC against output overvoltages caused (for instance) by LED open circuits and reduces the LED leak current at oscillation stop. Additionally, the operation is ensured even with specifications at which the output voltage Vo does not exceed 10% of the maximum input voltage Vi. (See Section 3.2.6 [Selecting resistors for Svin and Svout pins] on page 12.)

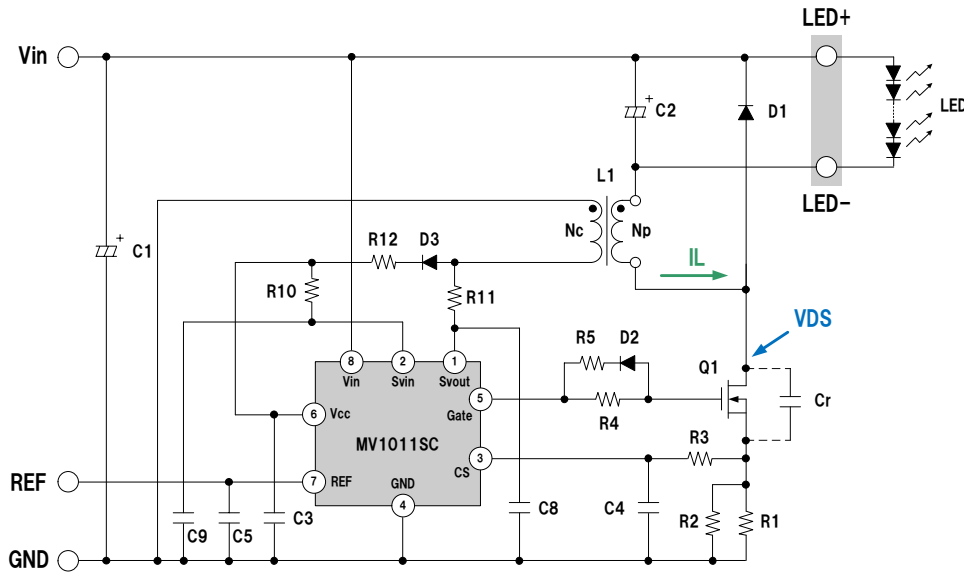When selecting components, select an auxiliary winding and a rectifier diode for the auxiliary winding.

Figure 9 Configuration of a winding voltage supply

3.3.2 Selecting the auxiliary winding (Nc)

If Vc represents the auxiliary winding voltage rectified and applied to the Vcc pin, Vc is obtained by the formula given below. Considering changes in Vo due to dimming and changes in VF of the LED, select the turn ratio at which Vc voltage falls within the range between 10 V and 16 V.

$$\frac{Nc}{Np} \cong \frac{Vc}{Vo}$$

Np: Number of turns of inductor L1 [T]

Nc: Number of turns of auxiliary winding [T]

Depending on the turn ratio or the coupling condition of the winding, a surge voltage is generated in the auxiliary winding, and Vc voltage may exceed the set level. Check with the actual apparatus to determine whether the Vc voltage is between 10 V and 16 V.

3.3.3 Selecting the auxiliary winding rectifier diode (D3)

Vr, a reverse voltage represented by the following formula, is applied to D3. Note the withstand voltage when selecting this component.

$$Vr = Vi \times \frac{Nc}{Np}$$

When the input voltage is at maximum, the reverse voltage applied to D3 is also at maximum. Use a fast recovery diode (FRD) for D3.

(See Table 3 Recommended rectifier diodes.)

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Table 3 Recommended rectifier diodes (as of January 2015)

Product name	Withstand voltage (V)	Io (A)	V_F (V)	Cj (pF)	trr (ns)	Manufacturer	Package
M1FL20U	200	1.1	0.98	-	35	Shindengen	M1F
M1FL40U	400	1.5	1.2	11	25	Shindengen	M1F
D1FK60	600	0.8	1.3	11	75	Shindengen	1F

Placing a resistor R12 in series with D3 may reduce the effects of the surge voltage of the auxiliary winding on the Vcc pin, and reduce Vc voltage increased by the surge voltage.

R10 should be 1 MΩ; R11 should be 220 kΩ.

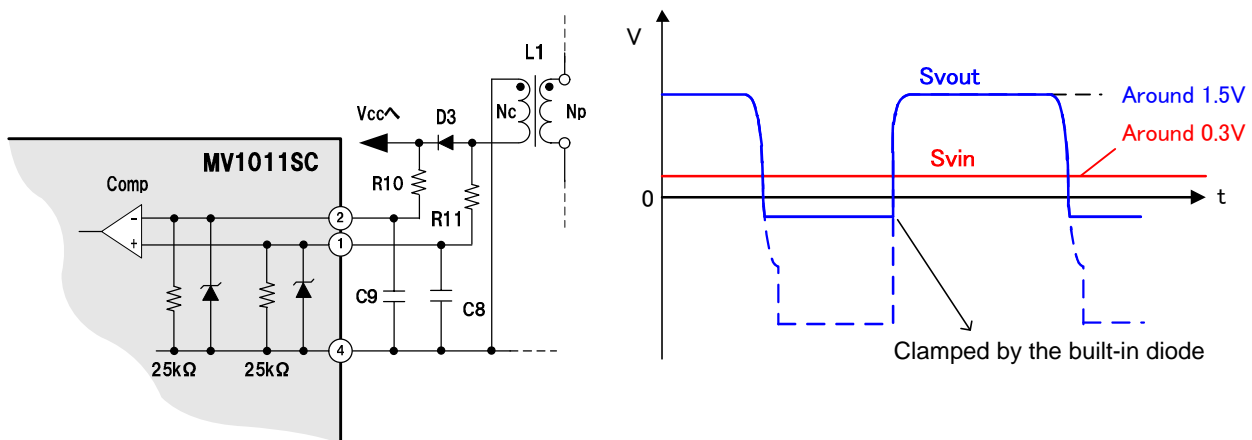The Svin and Svout pin waveforms are as shown in Figure 10 when an auxiliary winding is used.

Figure 10 Waveforms of Svin and Svout pins when an auxiliary winding is used

3.3.4　LED open-circuit protection using auxiliary winding

Using the auxiliary winding of the inductor L1 shown in Figure 9 provides protection against output overvoltages due (for instance) to LED open-circuit. The Vcc pin performs the latch-off function when detecting an overvoltage. It disables the operation when the Vcc pin voltage reaches 20.7 V (typical). If the auxiliary winding is wound with the polarity shown in Figure 9, the auxiliary winding voltage is proportional to output voltage; thus, it is possible to indirectly detect an overvoltage caused by LED open-circuit and to stop the operation.

The following formula gives Vovp, an output voltage at the time of latch-off:

$$\text{Vovp} = \frac{20.7}{\text{Vc}} \times \text{Vo}$$

If the difference between the input voltage Vi and the output voltage Vo is small, the Vcc voltage may not reach 20.7 V. In this case, LED open-circuit protection by the auxiliary winding may fail.

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3.3.5 High-side drive circuit

A winding voltage supply can be configured in a high-side drive configuration, as shown in Figure 11. For component selection, see the description for the winding voltage supply in Sections 3.2.1 to 3.3.3.
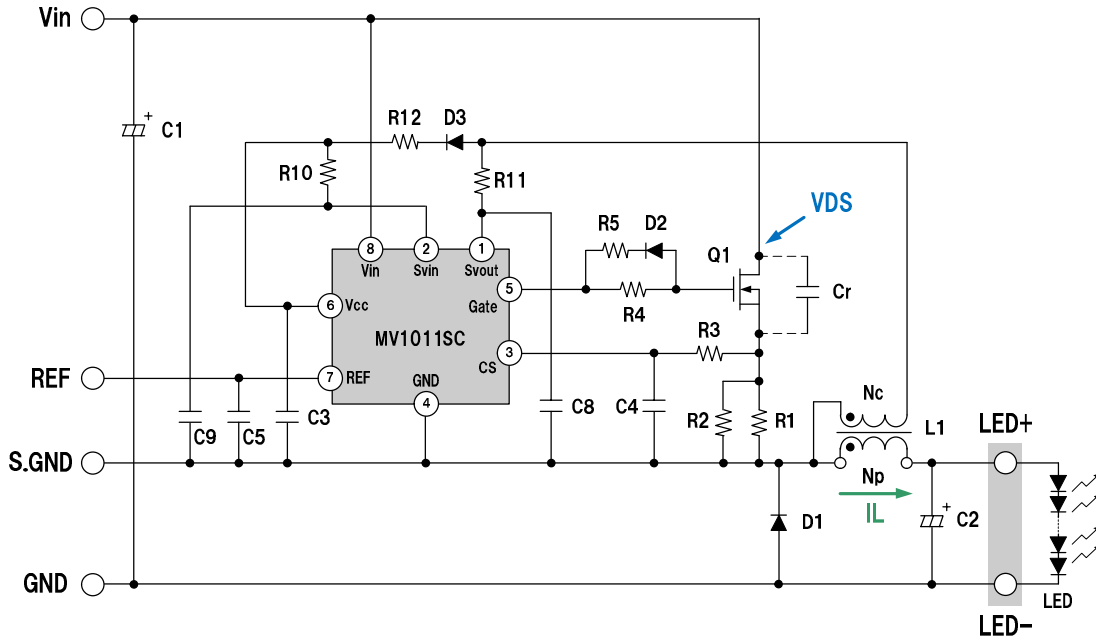

Figure 11 Circuit configuration of High-side drive

4. Cautions on pattern designing

4.1 Cautions

Figure 12 shows the same circuit shown in Figure 4, rewritten after accounting for pattern design. Consider the four items below for pattern design. Due to the potential for false detection, pay special attention to items 1 and 2.

1. The shaded area indicates the main circuit through which the switching current flows. To make this area as small as possible, wire with the shortest possible tracks, prioritizing this aspect over other aspects.

2. The area enclosed with a dotted line indicates the control circuit. Strive to minimize the effects of noise and magnetic flux of the main circuit on the control circuit. The control circuit should have one GND terminal, connected to a stable part of the main circuit, such as a minus terminal of the input capacitor. In particular, make sure that the tracks to input signals to pins such as REF, Svin, Svout, and CS pins are kept at a distance from high-voltage circuits.

3. Magnetic flux is present around the inductor. Use a shield type inductor with a small flux leak. Make sure that the signal tracks are not placed just below the inductor.

4. Wire the tracks for the Svin and Svout pins as close to parallel as possible.
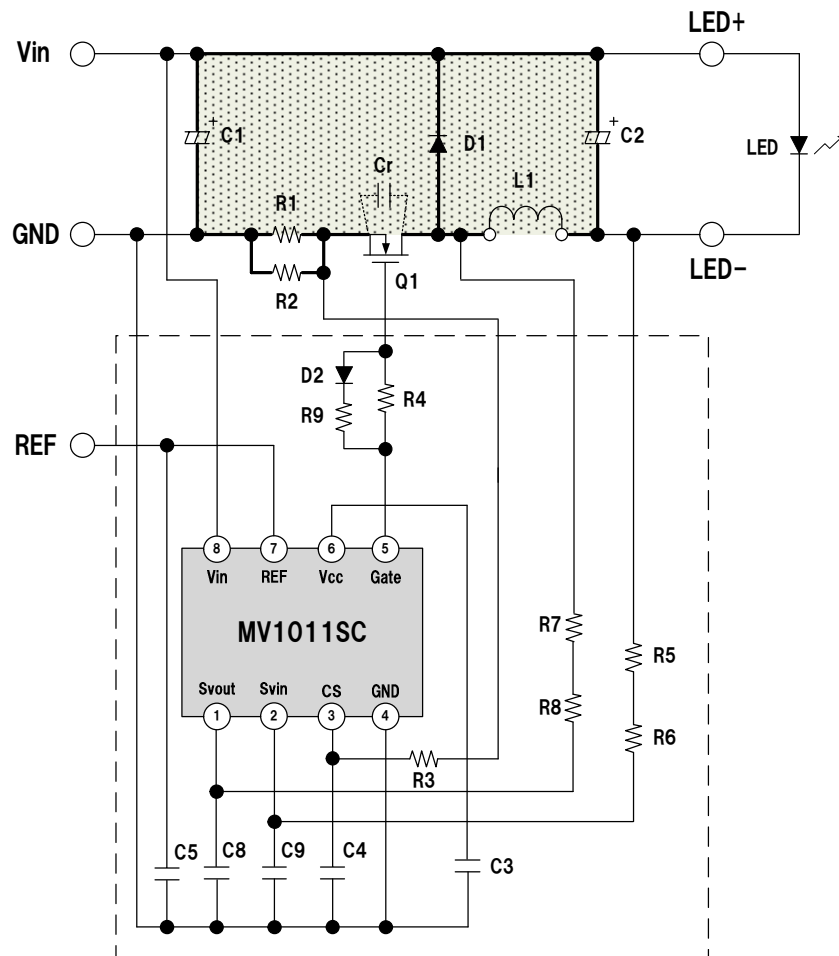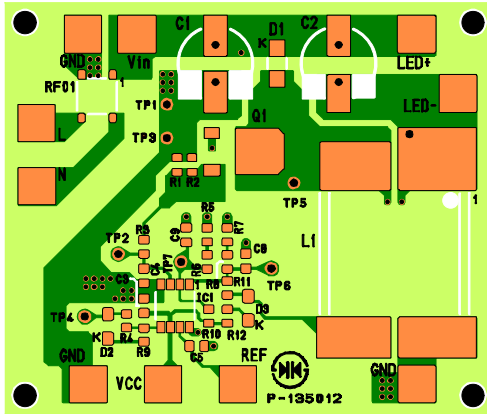
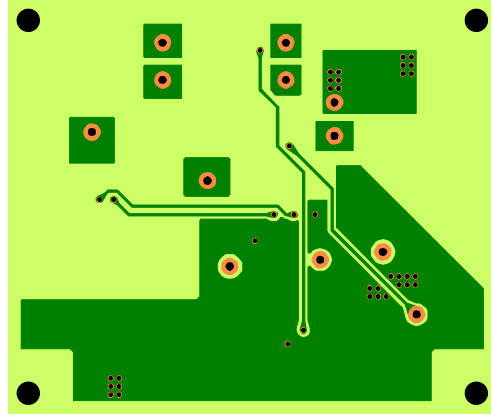Figure 12 Circuit diagram accounting for pattern design

MV1011SC

4.2 PCB pattern example

The diagram below shows an example of a pattern layout using our sample board. The pattern on the sample board lacks an input fuse and input line filter. Be sure to add these components for actual applications.

<Front>

<Back>

[PCB size: 55 mm H x 65 mm W]

The above pattern is an example. It does not guarantee actual operation. Be sure to check actual operation with the actual apparatus.

5. Dimming characteristics

Figure 13 shows typical dimming characteristics for the MV1011SC.

Since the current detection threshold changes with REF pin voltage V_{REF}, the output current can be adjusted using V_{REF}. Apply a DC voltage to the REF pin and adjust the voltage to enable linear dimming control. In addition, sending a PWM signal of 1 kHz or less to the REF pin and controlling the duty cycle enables PWM dimming. Reducing V_{REF} automatically switches operations from critical conduction mode to discontinuous conduction mode, allowing adjustments of the output current to very low levels, even with linear dimming.

[A] frequency modulation region and [B] off-time modulation region shown in Figure 13 are automatically switched over based on a comparison of Toff (CRM) and Toff (DCM) on the IC. Toff (CRM) is the off-time in critical conduction mode (sum of toff1 worked out by the formula in Figure 5 on page 8 and the resonant period toff2). Toff (DCM) is the forced off-time determined on the IC based on V_{REF}. When Toff (CRM) > Toff (DCM), the operating mode switches to the [A] frequency modulation region. When Toff (CRM) < Toff (DCM), the operating mode switches to the [B] off-time modulation region. The REF pin voltage for switchover changes with input/output conditions, choke inductance, and other parameters. Calculate the forced off-time Toff (DCM), using the following approximation formula as a guide.

$$\text{Toff (DCM)} \cong \frac{64.35}{45.9 \times V_{REF} - 9.9} \ [\mu s] \quad (0.24\,V < V_{REF} < 0.7\,V)$$

The lower chart in Figure 13 shows a graph of REF pin voltage and off-time. The red curve represents Toff (CRM). The green curve represents Toff (DCM).

If V_{REF} is equal to or below the oscillation-off REF pin threshold voltage (Vth_REF_sp), the operation will switch to the [C] Oscillation off region.

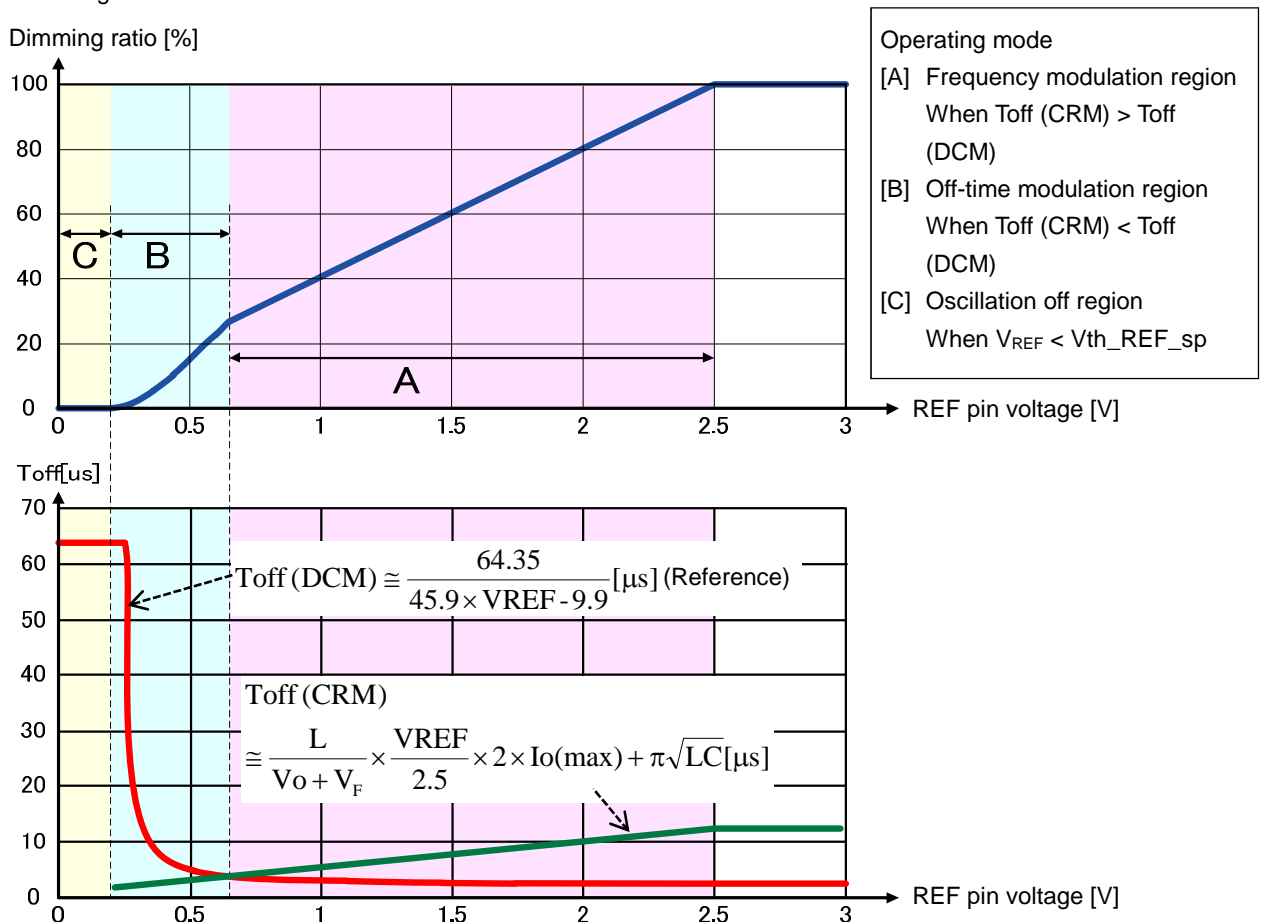Figure 13 Relationship of REF pin voltage V_{REF} to dimming ratio and to off-time

5.1 Operation in each mode

5.1.1 [A] Frequency modulation region

The operation waveforms in the frequency modulation region are those in critical conduction mode shown in Figure 15. Figure 14 shows the internal circuit of the CS pin. Voltage 1/5 of V_{REF} is compared to current detection threshold voltage Vth_CS (0.495V); the lower voltage is used as the CS pin reference voltage. In actual use, both Vth_CS and V_{REF} x1/5 will change slightly. To make sure Vth_CS is used as the reference, set V_{REF} to 2.6 V or greater.

If resonant period Toff2 is significantly less than ton and toff1, IL may be regarded as a triangle wave. Thus, Io = 1/2 x Ip, and output current Io becomes proportional to V_{REF}. However, the oscillation frequency increases as V_{REF} decreases; the ratios of Toff2 and detection delay to the period of a cycle will therefore increase. In this case, the proportional relationship between Io and V_{REF} may change somewhat.
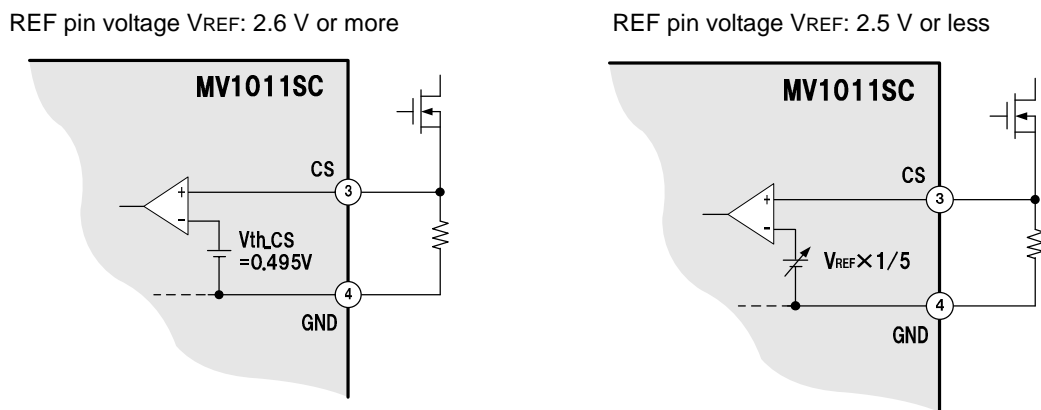
REF pin voltage V_{REF}: 2.6 V or more

REF pin voltage V_{REF}: 2.5 V or less

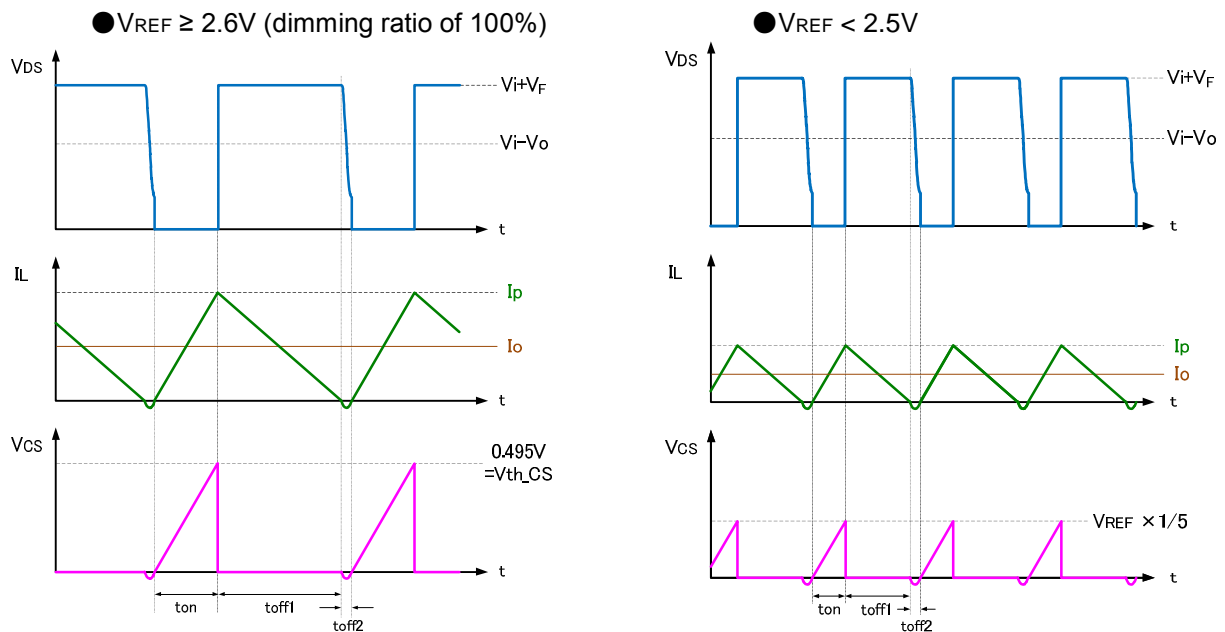Figure 14 CS pin internal circuit diagram

Figure 15 Operation waveforms in [A] frequency modulation region

5.1.2 [B] Off-time modulation region

Operation waveforms in the off-time modulation region are those in discontinuous conduction mode shown in Figure 16. Output current can be controlled to very low levels by increasing the forced off-time Toff (DCM) as V_{REF} falls. The forced off-time includes toff1, the period during which a current flows to D1. As shown by the formula in Figure 5, toff1 depends on Vo. Therefore, if Vo changes, Io in the [B] region will also change.

The reference voltage for the CS pin is 1/5 of V_{REF} in the [B] region as well, and therefore lower than in the [A] region. Thus, the circuit is more likely to be affected by noise in the [B] region. The MOSFET is more likely to switch off at a timing that varies from the time of peak current detection. The switching-on timing does not fall on a valley of the resonant voltage. If the V_{DS} voltage at switching-on exceeds Vb, switching-on noise will increase. In actual use, after the switch is turned on, there will be a leading edge blanking (LEB) period in which noise is rejected. During LEB period, the MOSFET cannot be turned off. (Figure 17(b)) Even during the LEB period, when switching-on noise or noise from an external circuit exceeds the reference voltage, such noise will lead to false detection, and the MOSFET is turned off. (Figure 18(b)) As a result, Io drops below the optimal level. Depending on the timing of the noise, the LED light may flicker.

If Coss of MOSFET, Cr of the resonant capacitor or Cj of the fly-wheel diode is large, the switching-on noise will also be large. If switching-on noise causes false detection, adjust the CS filter (page 12), adjust the gate resistance (page 11), or reselect the components above.

To quickly check whether false detection occurred, use many different V_{REF} settings to check for an apparently short Ton, which is not the peak current detection. Measurements may be incorrect if you measure the Vcs or V_{DS} voltage. We recommend measuring just the gate pin waveform.
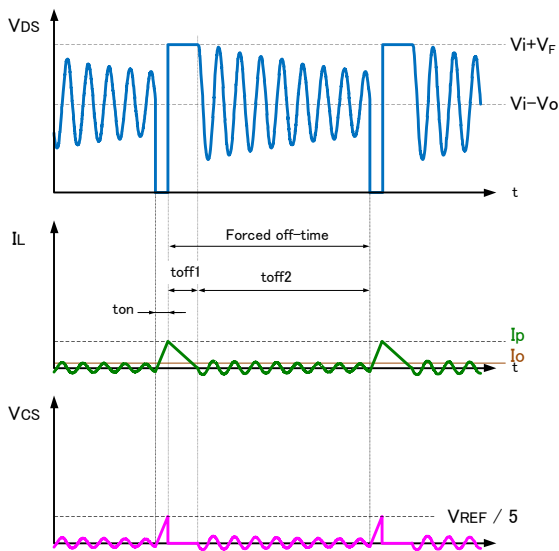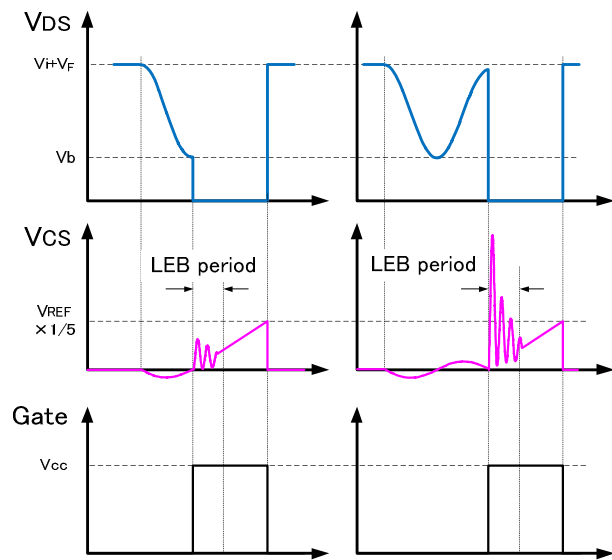

Figure 16 Operation waveform
in the [B] off-time modulation region

(a) Switched on
when $V_{DS} \approx$ Vb

(b) Switched on
when $V_{DS} >$ Vb

Figure 17 Example of switching-on
noise caused by V_{DS}

(a) Noise fades within LEB period
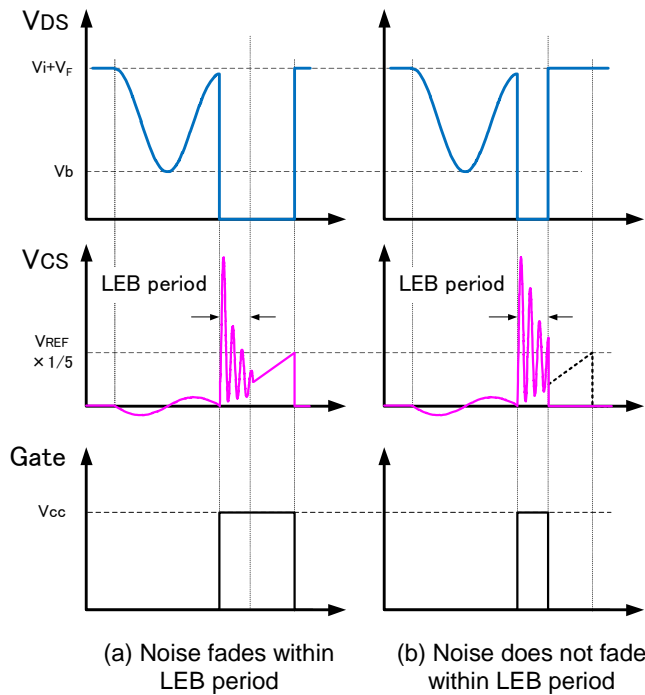
(b) Noise does not fade within LEB period

Figure 18 Example of false detection due to switching-on noise

The resonant current flowing in toff2 period also flows to the current detection resistor Rcs. Vcs oscillates around 0 V during the toff2 period. Even in case of the same V_{REF}, Io accuracy and smoothness of dimming characteristics may be degraded (see V_{REF} ripple: Small in Figure 20) if the on-time changes significantly depending on whether Vcs at on-timing exceeds 0 V, as shown in Figure 19.

The amplitude of Vcs during the toff2 period can be reduced by reducing the Coss of MOSFET and the Cr of the resonant capacitor. Increasing the ripple voltage of V_{REF} averages any changes in the on-time and reduces Vcs-dependent changes in Io at switching-on. (See V_{REF} ripple: Large in Figure 20.)
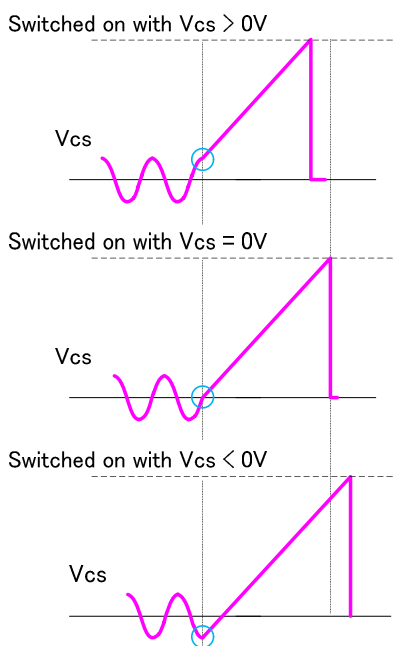

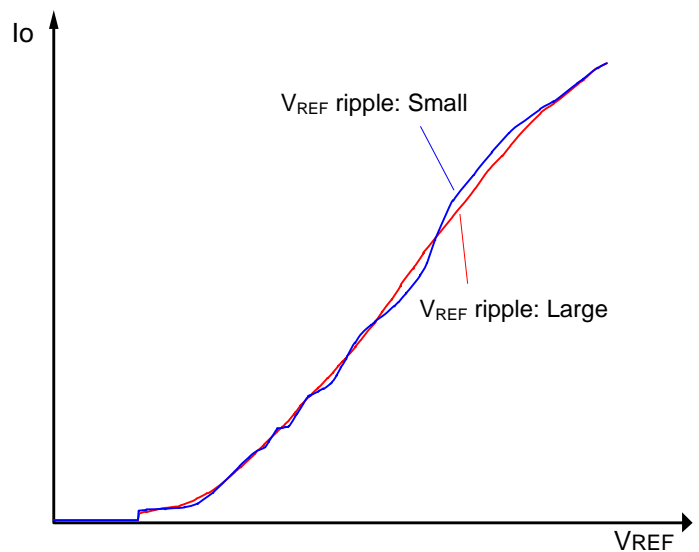Figure 19 Changes in on-time determined by switching-on timing in the [B] region

Figure 20 Example illustrating degraded smoothness of dimming characteristics

5.1.3 [C] Oscillation off region

The MV1012SC can stop gate output by holding the V_{REF} at or below the oscillation-off REF pin threshold voltage (Vth_REF_sp). To turn the MOSFET completely off, Io can be brought closer to zero than in the [B] region.

In the basic circuit configuration shown in Figure 4, a leakage current flows constantly via the internal resistors of the Svin and Svout pins. A leakage current is also present in the [A] and [B] regions. In the [C] region, in which the MOSFET is completely off, Io is just the leakage current. The value of the leakage current is determined by the input/output voltage difference and the values of resistors R5 to R8. To eliminate the leakage current, use the circuit configuration with an auxiliary winding.

The standard values for Vth_REF_sp range from 0.15 V to 0.22 V. Set V_{REF} at or below 0.15 V if using the [C] region.
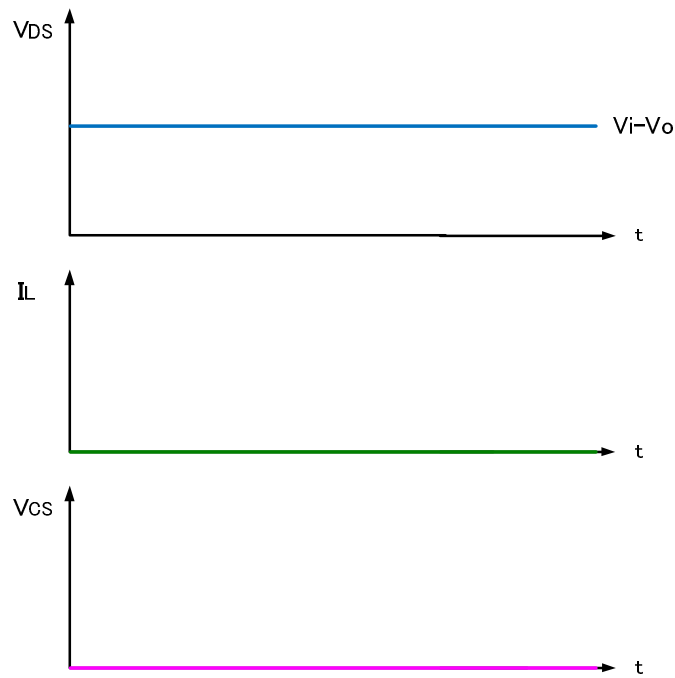

Figure 20 Operation waveform in the [C] Oscillation off region

5.2 PWM dimming

5.2.1 PWM dimming in 100% and oscillation off regions

PWM dimming can be performed by sending a PWM signal to the REF pin with V_{REF} in the 100% dimming ratio as the high level and V_{REF} in the oscillation off region as the low level. Frequency f and on-duty cycle Don of a PWM signal should be 1 kHz or less and 1% or more, respectively.
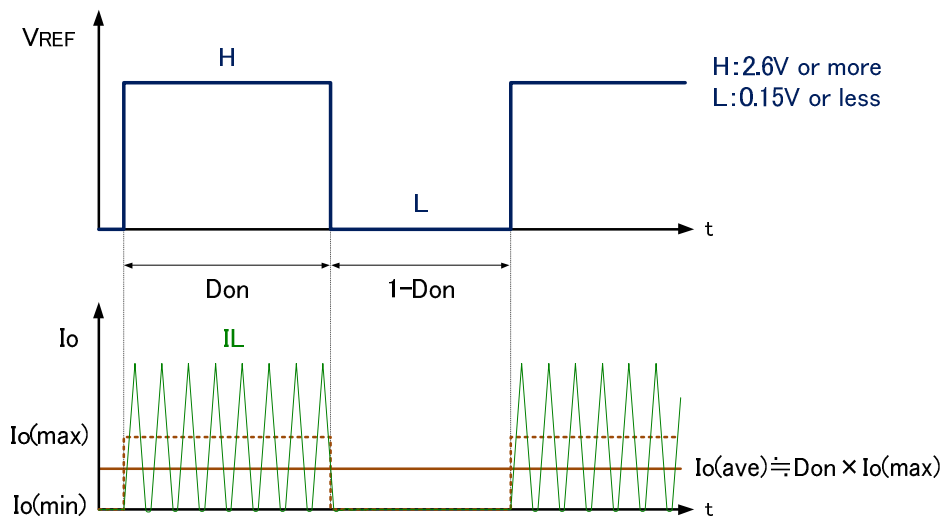

Figure 22 Example of PWM dimming operation

As shown in Figure 22, when a PWM signal with on-duty cycle of Don is applied to the REF pin, Io becomes an average current Io (ave) = Don x Io (max) + (1 – Don) x Io (min). In actual use, Io (min) is very small, and the equation may be rewritten to Io (ave) ≈ Don x Io (max).

In PWM dimming, if the first switching-on timing in the H-level period is irregular, the practical Don will also become irregular and Io will become unstable. The effect is especially significant if Don is small. To avoid this problem, the first switching-on timing in the H-level period of every cycle aligns with each other by detecting a change of VREF from L level to H level and forcibly outputting an on-trigger. This function helps stabilize Io (ave), even if Don is small.

5.2.2 Combination of linear dimming and PWM dimming

Linear dimming and PWM dimming can be combined, as shown in Figure 23, thereby ensuring advantageous output current accuracy throughout the range from 100% rated current to very small currents.

Assume V_{REF_any} represents any given REF voltage in the [A] region and Io' represents Io at that voltage. If Io is Io' or more, linear dimming is used. If Io is Io' or less, PWM dimming is used. The high level of the signal for PWM dimming is V_{REF_any}, and the low level is V_{REF} in the oscillation off region. Combining the dimming methods enables adjustments to smaller currents than PWM dimming alone and achieves control with better output current accuracy than linear dimming alone.
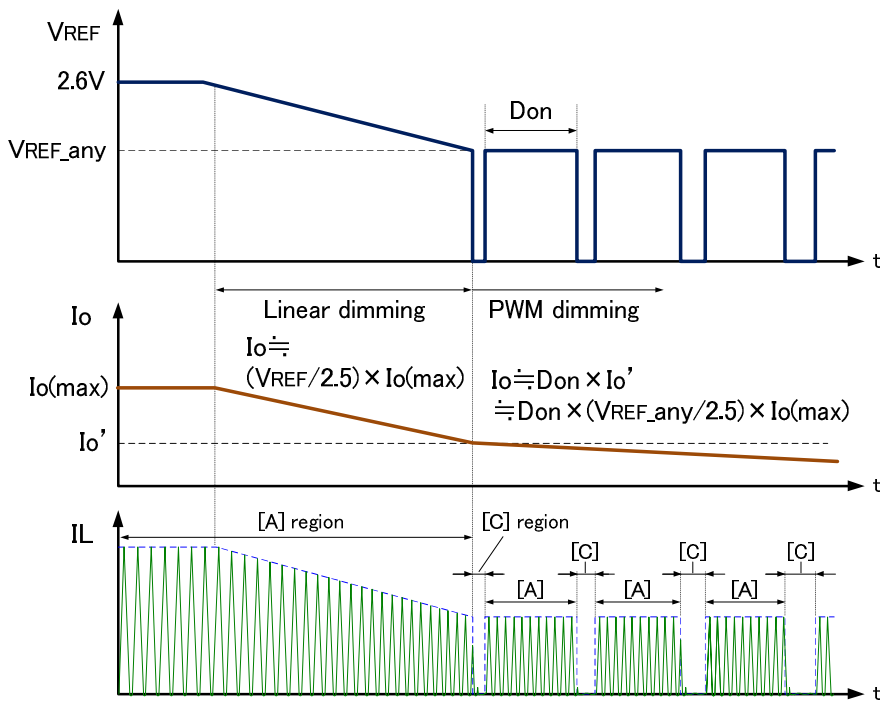

Figure 23 Combination of linear dimming and PWM dimming

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5.3 Dimming circuit

5.3.1 Example of dimming circuit smoothing PWM signal

Figure 24 shows an example of a dimming circuit that smooths a PWM dimming signal and applies it to the REF pin. Assuming that V_{REF}_L represents V_{REF} when the transistor Q101 is turned on and that V_{REF}_H represents V_{REF} when the transistor is turned off in Figure 24, obtain the approximate values of those voltages using the formulas given below.

$$V_{REF}\_H = V_{DD} \times \frac{R102}{(R101 + R102)}$$

$$V_{REF}\_L = I\_ref \times (R103 + R104)$$

Increasing V_{REF}_H narrows the dimming range. Applying the formula above, set the value of resistors R101 + R102 with which the voltage becomes approximately 2.7 V. Make sure V_{DD} applied is stable. A widely changing V_{DD} will affect dimming accuracy.

To ensure that the IC operates in the oscillation off region when Q101 is turned on, set the value of resistors R103 + R104 with which V_{REF}_L, even if varying, does not exceed 0.15 V. I_ref is the REF pin voltage pull-up current and it is 32 µA (typical).

The components R103, R104, C101, and C102 smooth V_{REF}_H and V_{REF}_L, and V_{REF} obtained with the formula below is applied to the REF pin. Adjust the capacitance levels of C101 and C102 to 1 uF or less while checking dimming characteristics.

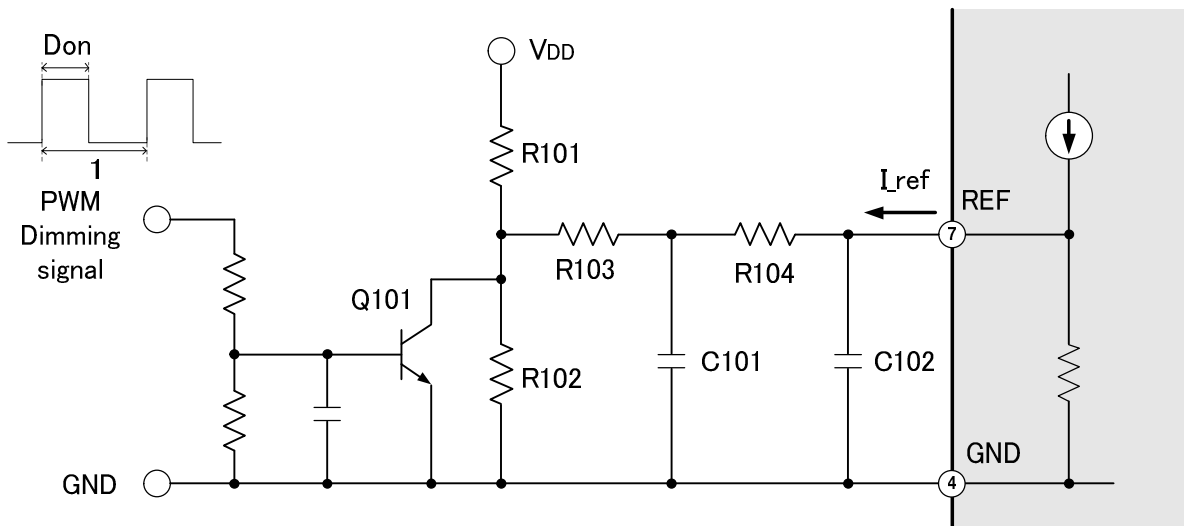$$V_{REF} = (1 - Don) \times V_{REF}\_H + Don \times V_{REF}\_L$$

Figure 24 Example of PWM dimming signal smoothing circuit

5.3.2 Example of dimming circuit in high-side drive configuration

For dimming using a high-side drive configuration, a signal must be applied to the REF pin with the GND of the IC (S.GND) as a reference, distinct from the circuit GND. Figure 25 shows an example of a high-side drive dimming circuit using a photocoupler. Assuming that V_{REF}_H represents V_{REF} when the photocoupler P201 is turned on and that V_{REF}_L represents V_{REF} when the photocoupler is turned off in Figure 25, obtain the approximate values of these voltages using the formulas given below.

$$V_{REF}\_H = V_{DD} \times \frac{R202}{(R201 + R202)}$$

$$V_{REF}\_L = I\_ref \times (R203 + R204)$$

Increasing V_{REF}_H narrows the dimming range. Applying the formula above, set the value of resistors R201 + R202 with which the voltage becomes approximately 2.7 V. Make sure V_{DD} applied is stable with S.GND as a reference. A widely changing V_{DD} will affect dimming accuracy.

To ensure the IC operates in the oscillation off region when Q201 is turned on, set the value of resistors R203 + R204 with which V_{REF}_L, even if varying, does not exceed 0.15 V. I_ref, the REF pin voltage pull-up current, is 32 µA (typical).

The components R203, R204, C201, and C202 smooth V_{REF}_H and V_{REF}_L, and V_{REF} obtained with the formula below is applied to the REF pin. Adjust the capacitance levels of C201 and C202 to 1 uF or less while checking dimming characteristics.

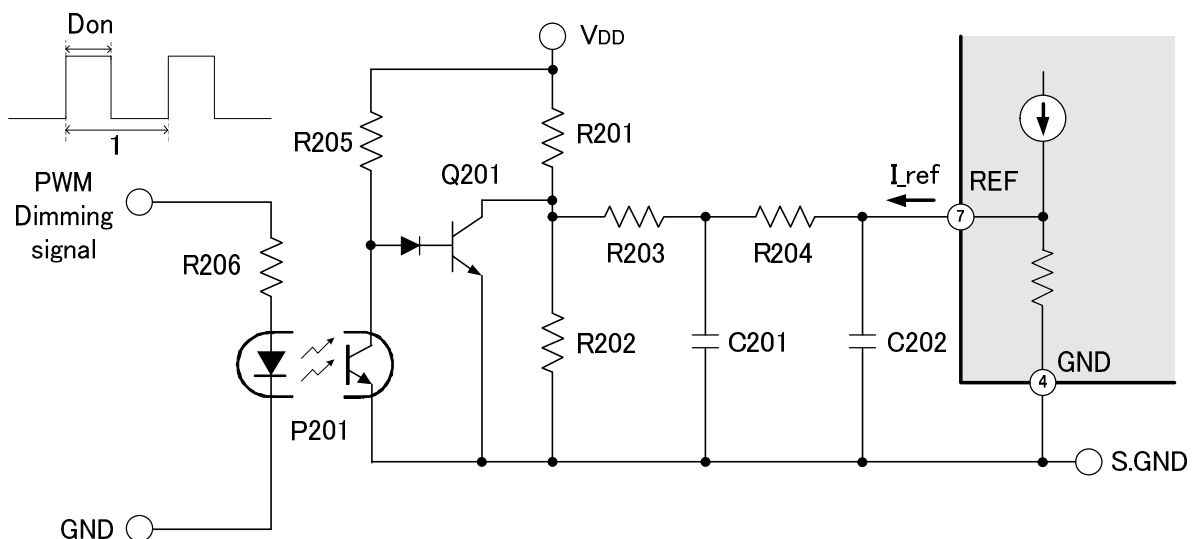$$V_{REF} = Don \times V_{REF}\_H + (1 - Don) \times V_{REF}\_L$$

Figure 25 Example of dimming circuit in high-side drive configuration

6. Operations in abnormal situations

While the MV1011SC incorporates various protection functions, certain problems cannot be averted by the IC functions alone. Provided below are some examples of typical abnormal situations. These are provided as a guide.

Always perform appropriate testing using the actual apparatus, including open-circuit and short-circuit tests, to check operations in abnormal situations.

6.1 LED open-circuit

The MV1011SC has a latch-off function to protect against LED open-circuits using the auxiliary winding voltage and Vcc_OVP function. For details, see [LED open-circuit protection using auxiliary winding] on page 16.

① Auxiliary winding is used:
⇒ The output voltage is detected indirectly using the auxiliary winding voltage, and the latch-off is performed with the Vcc_OVP function.

② Auxiliary winding is not used:
⇒ The IC operates with the maximum on-time, Ton_max. Vo becomes nearly equal to Vi.
The withstand voltage of the output capacitor should be the same as that of the input capacitor.

6.2 LED short-circuit

If Vo becomes 0 V, the operation automatically switches to the restart operation from zero current detection. That makes it possible to limit forcibly the current in the event of an LED short-circuit. After the short-circuit is resolved, the IC is automatically reset and starts to operate with zero current detection.

If the formula below is fulfilled, the IC operates in continuous conduction mode, and a short-circuit current flowing to the MOSFET or the fly-wheel diode is likely to increase. Make sure the actual apparatus is unaffected in such cases.

$$\mathrm{Vi} > \frac{\mathrm{Toff\_max}}{\mathrm{Ton\_min}} \times \mathrm{V_F}$$

V_F is the forward voltage of the fly-wheel diode D1.

Figure 26 shows the ideal waveforms for the Svout and Svin pins in the event of an LED short-circuit. Make sure the Svin voltage always exceeds the Svout voltage in the event of an LED short-circuit. To prevent false switching-on due to noise, we recommend making the value of resistors R5 + R6 about 5% less than R7 + R8. For noise reduction, insert capacitors C8 and C9. (See Sections 3.2.10 and 3.2.13.)
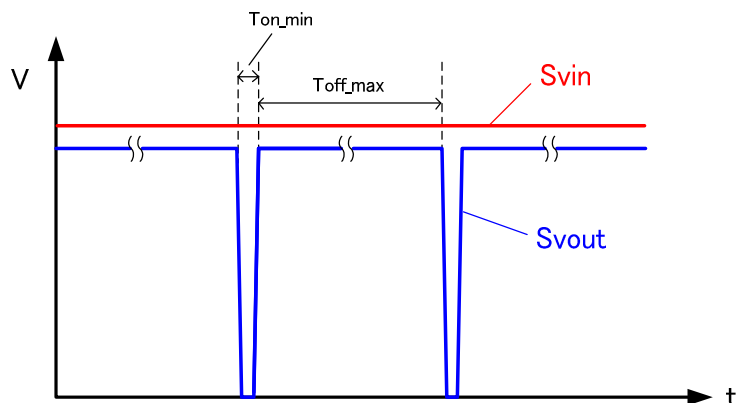

Figure 26 Svin and Svout pin waveforms in the event of an LED short-circuit

6.3 Abnormal heat buildup

The MV1011SC doesn't incorporate thermal shutdown. Install a separate protection circuit, if necessary.

6.4 CS pin open-circuit

If the CS pin open-circuit occurs, Vcs will increase due to the internal pull-up current and remain above the CS pin reference voltage. The IC will therefore operate with the minimum on-time Ton_min, and Io will decrease.

6.5 CS-GND short-circuit

The IC will be unable to perform peak current detection at the CS pin and will operate with the maximum on-time Ton_max. As Io increases, install a separate protection circuit, if necessary.

6.6 Current detection resistor open-circuit

The source of MOSFET will float, and MOSFET operations will become unstable. If the MOSFET switches off, Io will approach zero. However, if the MOSFET is on, overvoltage will be applied to a CS pin, resulting in potential damage to the IC. Install a separate protection circuit, if necessary.

6.7 Current detection resistor short-circuit

Vcs will become nearly equal to GND, and the IC will operate with the maximum on-time Ton_max. As Io increases, install a separate protection circuit, if necessary.
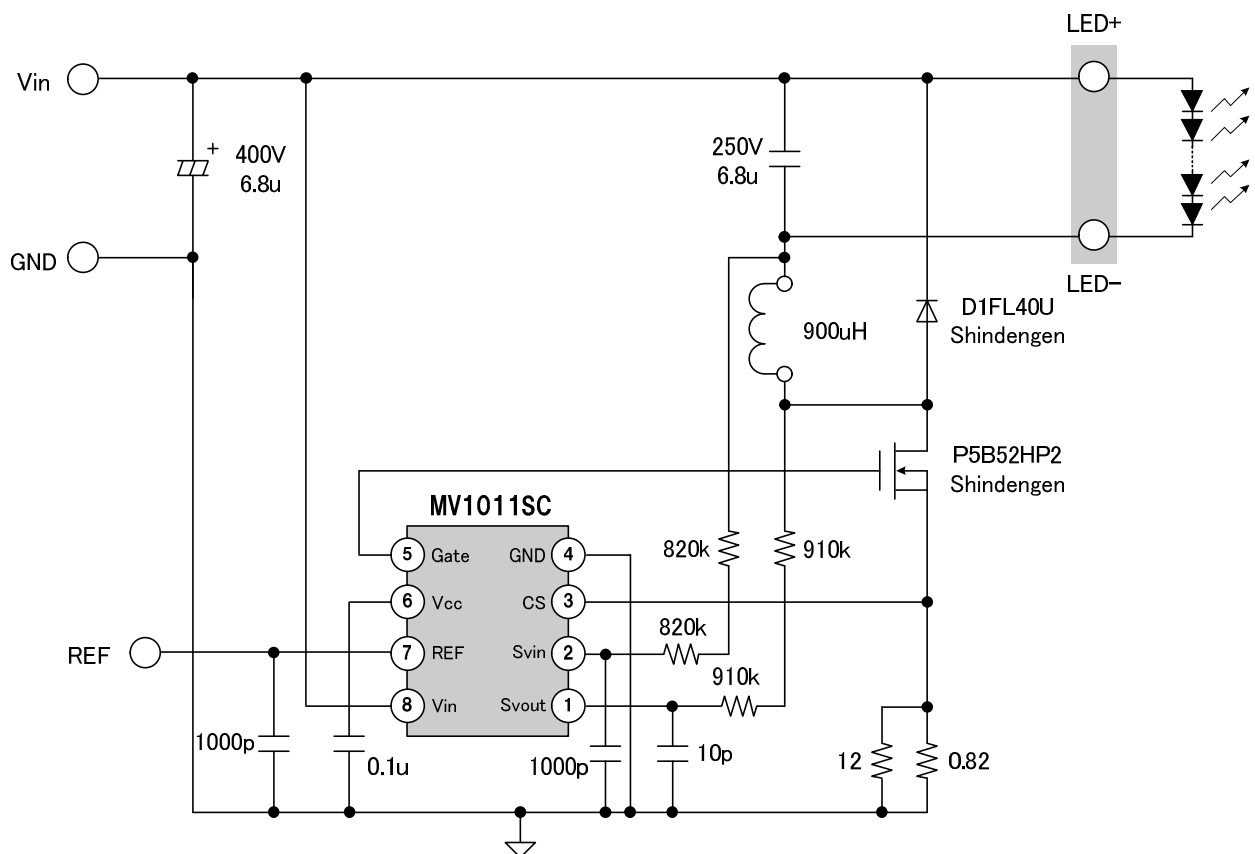
7. Standard circuit example

7.1 Power supply specification and circuit diagram

◆ Power supply specification

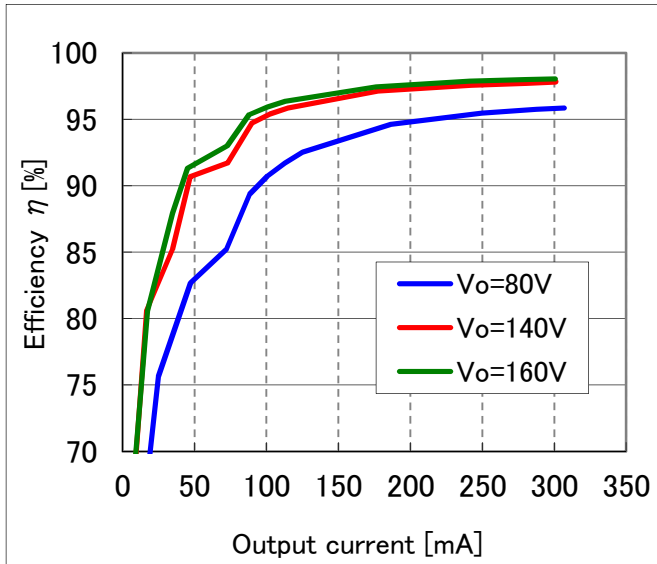|	Min	Typ	Max	Unit
Input voltage (DC)	180		220	V
Output voltage	80	140	160	V
Output current	0.1(*)		300	mA

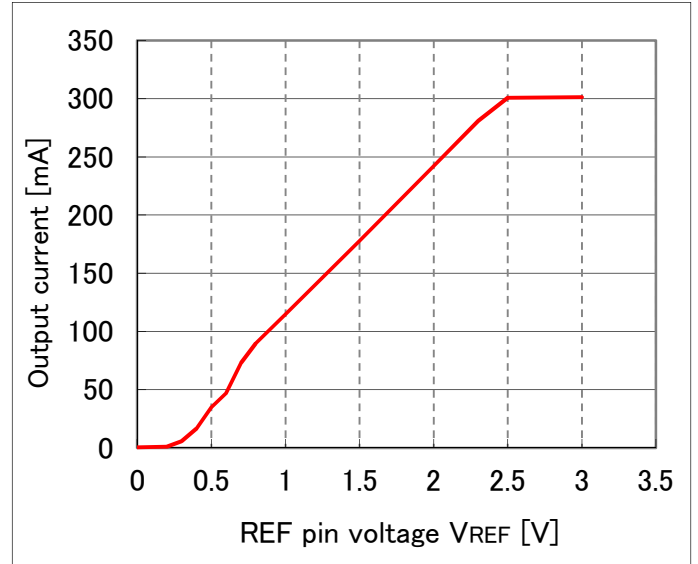(*) When Vin = 200 V DC, Vo = 140 V, V_{REF} = 0 V

◆ Circuit diagram

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7.2 Power supply characteristics

◆ Efficiency characteristics
 (Vin = 200 V DC)
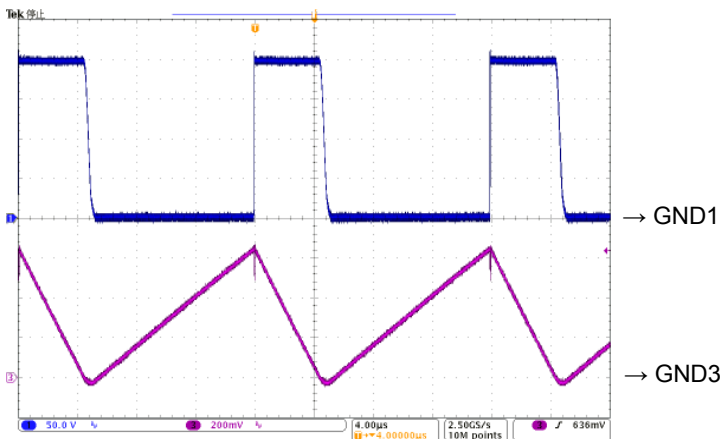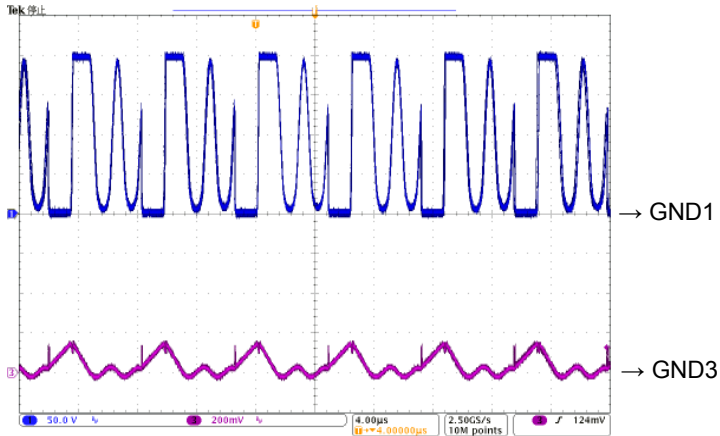

◆ Dimming characteristics
 (Vin = 200 V DC, Vo = 140 V)

7.3 Example of operation waveform

Waveform in the [A] frequency modulation region

→ GND1

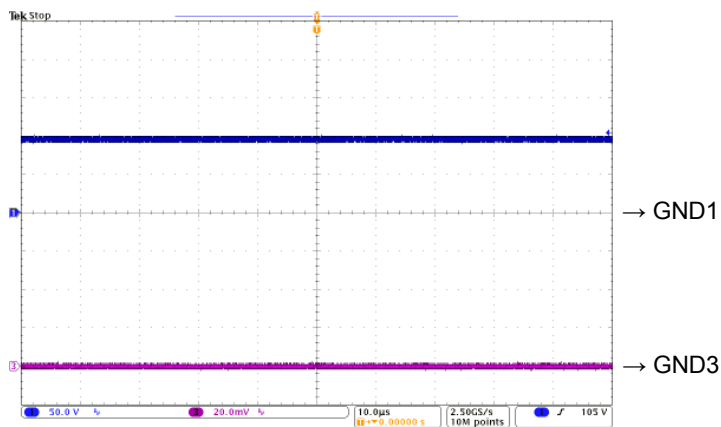→ GND3

CH1	V$_{DS}$	50 V/div
CH3	IL	0.2 A/div
time		4 us/div
Vin		200 V DC
Io		300 mA
Dimming ratio of 100% **Vo = 140 V**		

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Waveform in the [B] off-time modulation region

→ GND1

→ GND3

CH1	V_{DS}	50 V/div
CH3	IL	0.2 A/div
time		4 us/div
Vin		200 V DC
Io		30 mA
Dimming ratio of 10%		
Vo = 140 V		

Waveform in the [C] oscillation off region

→ GND1

→ GND3

CH1	V_{DS}	50 V/div
CH3	IL	0.02 A/div
time		10 us/div
Vin		200 V DC
Io		0.1 mA
oscillation off		
Vo = 140 V		

SHINDENGEN