PR6863/PR6865

High Performance Current Mode PWM Controller

GENERAL DESCRIPTION

PR6863/PR6865 is a highly integrated current mode PWM controller, optimized for high performance, and low standby power. It is suitable for cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to a tight range. In the condition of no load or light load, the IC operates in hiccup mode to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

Low startup current and low operating current contribute to a reliable power on startup and low standby design with PR6863/PR6865.

PR6863/PR6865 offers complete protection coverage with auto-recovery including Cycle-by-cycle current limiting (OCP), over load protection (OLP), and VDD under voltage lockout (UVLO). It also provides the protections with latched shutdown/auto-recovery including over temperature protection (OTP), over voltage (fixed or adjustable) protection (OVP). Excellent EMI performance is achieved with frequency spreading technique.

The tone energy below 20KHz is minimized in the design and audio noise is eliminated during operation.

PR6863/PR6865 is offered in SOT23-6 package.

FEATURES

- Power-on Soft Start Reducing MOSFET Vds Stress
- Frequency spreading to Minimize EMI
- Hiccup Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Comprehensive Protection Coverage
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - Overload Protection (OLP) with auto-recovery
  - Other Protections

	PR6863	PR6865
OTP	L	A
VDD OVP	L	A
Adjustable OUT OVP	L	A

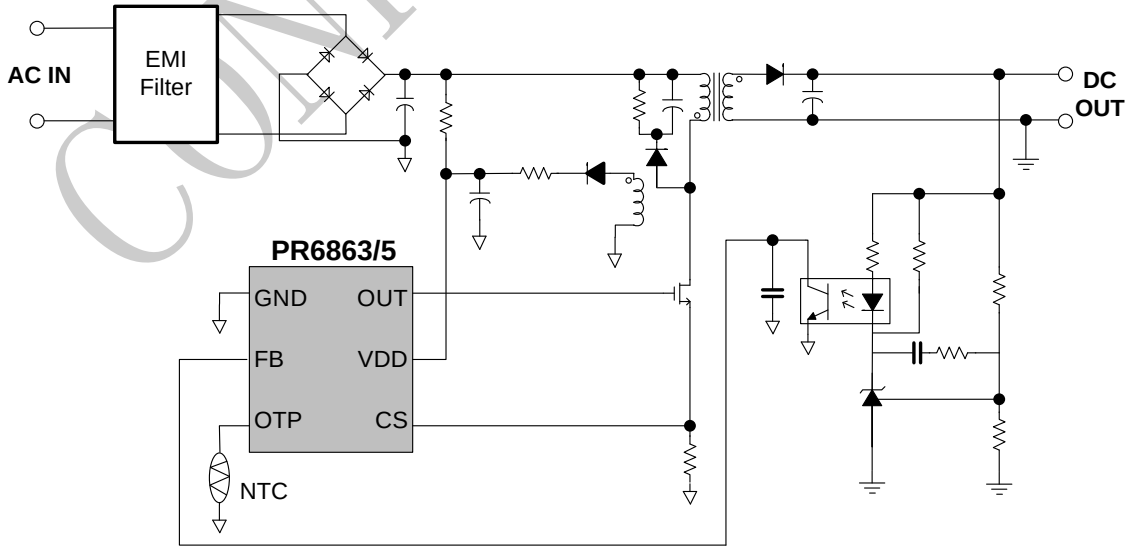
L: Latch shutdown A: Auto-Recovery

APPLICATIONS

Offline AC/DC flyback converter for

- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies
- Open-frame SMPS

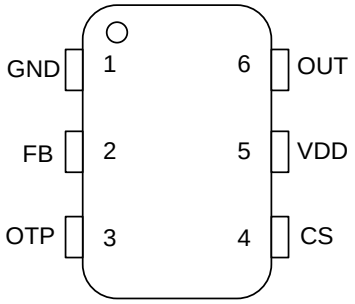
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The PR6863/PR6865 is offered in SOT23-6 package, shown as below.



Order Information

Part Number	Description
PR6863/5	SOT23-6, Pb-free in T&R

Package Dissipation Rating

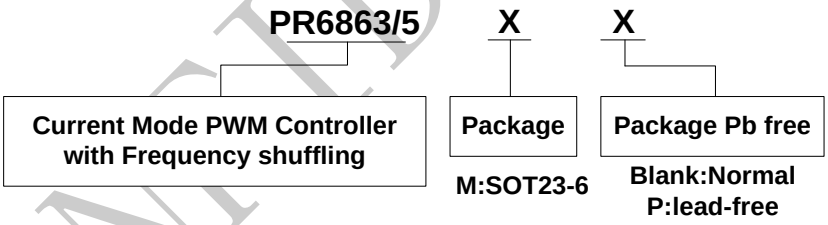
Package	$R_{\theta JA}$(℃/W)
SOT23-6	200

Absolute Maximum Ratings

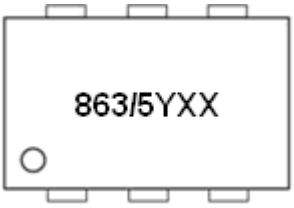
Parameter	Value
VDD DC Supply Voltage	30 V
VDD Zener Clamp VoltageNote	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
Sense Input Voltage	-0.3 to 7V
OTP Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 160 ℃

Note: VDD_Clamp has a nominal value of 30V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device's reliability.



Marking Information



Y: Year Code
XX: Week Code(01-52)

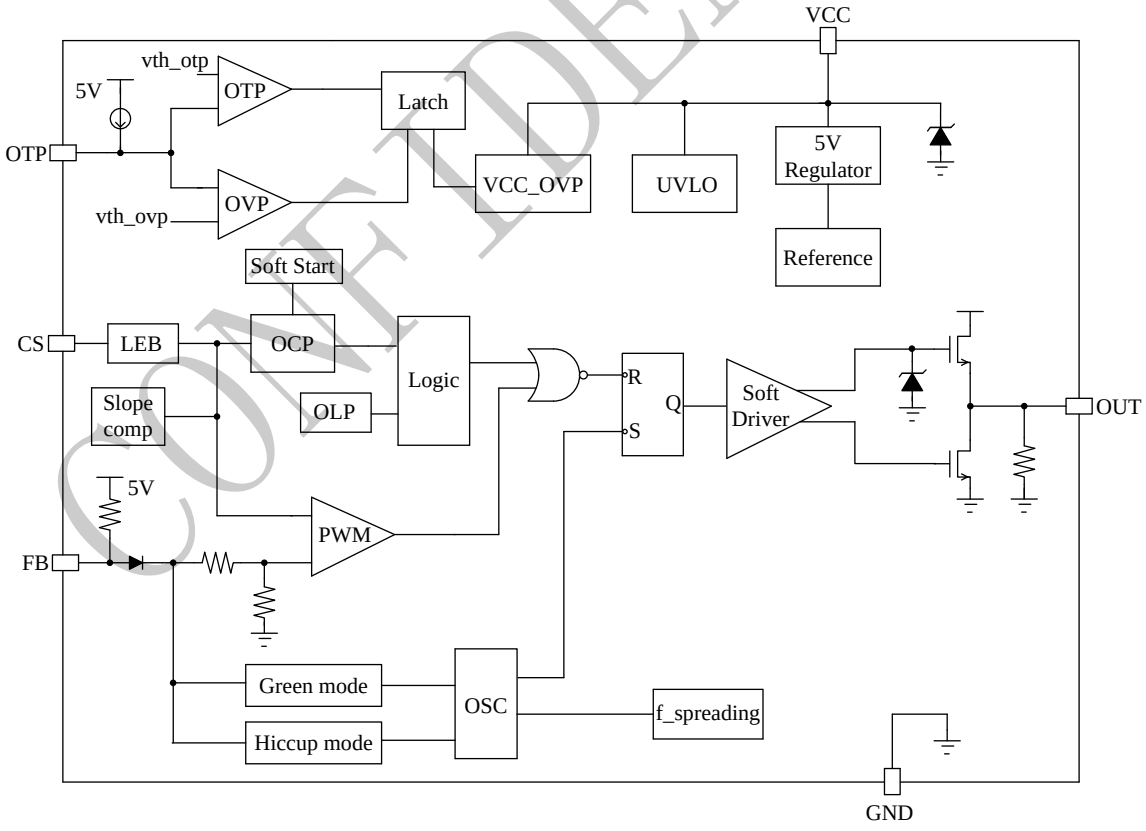
PIN ASSIGNMENTS

Pin #	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level at this pin and the current-sense signal at Pin 4
3	OTP	I	Dual function pin. Either connected through a NTC resistor to ground for over temperature shutdown/latch (OTP) control or connected through Zener to VDD for adjustable over voltage protection (OVP)
4	CS	I	Current sense input, connected through a resistor to GND to set the primary side peak current
5	VDD	P	Power Supply
6	OUT	O	Totem-pole gate driver output for power MOSFET

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	10 to 30	V
OTP	OTP Resistor Value	100	Kohm
TA	Operating Ambient Temperature	-20 to 85	℃

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

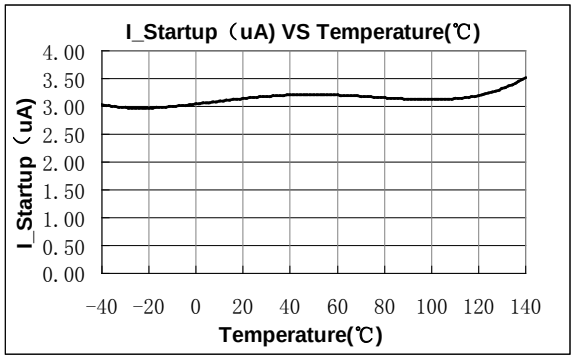
(T_A = 25℃, VDD=16V, unless otherwise noted)

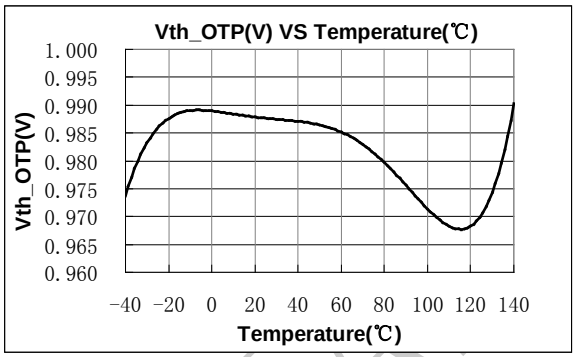
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO_OFF-1V, measure current into VDD		5	20	uA
I_VDD_Operation	Operation Current	VFB=3V		1.5	2.5	mA
UVLO_ON	VDD Under Voltage Lockout ON	6863	6	7	8	V
		6865	7.4	8.4	9.4	
UVLO_OFF	VDD Under Voltage Lockout OFF	6863	12.5	13.5	14.5	V
		6865	13.7	14.7	15.7	
VDD_Clamp		I_{VDD}=10mA	32.5	34	35.5	V
OVP_ON	Over voltage protection voltage	6863	28.5	30.5	32.5	V
		6865	29.8	31.8	33.8	
Vlatch_release	Latch release voltage	6863	4	5		V
Feedback Input Section(FB Pin)						
VFB_Open	VFB Open Loop Voltage		3.8	4.2		V
Avcs	PWM input gain ΔVFB/ΔVCS			1.71		V/V
DC_MAX	Max duty cycle @ VDD=14V,VFB=3V,VCS=0.3V		75	80	85	%
Vref_green	The threshold enter green mode			1.8		V
Vref_Hiccup_H	The threshold exit Hiccup mode			1.3		V
Vref_Hiccup _L	The threshold enter Hiccup mode			1.2		V
IFB_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.4		mA
VTH_PL	Power Limiting FB Threshold Voltage			3.5		V
TD_PL	Power limiting Debounce Time		80	88	96	mSec
ZFB_IN	Input Impedance			16		Kohm
Current Sense Input(CS Pin)						
SST	Soft start time			5		ms
T_blanking	Leading edge blanking time			220		ns
ZSENSE_IN	Input Impedance			40		Kohm
TD_OC	Over Current Detection and Control Delay	From Over Current Occurs till the OUT drive output start to turn off		120		nSec
VTH_OC	Internal Current Limiting Threshold Voltage with zero duty cycle			0.75		V
Vocp_clamping	CS voltage clamper			1		V

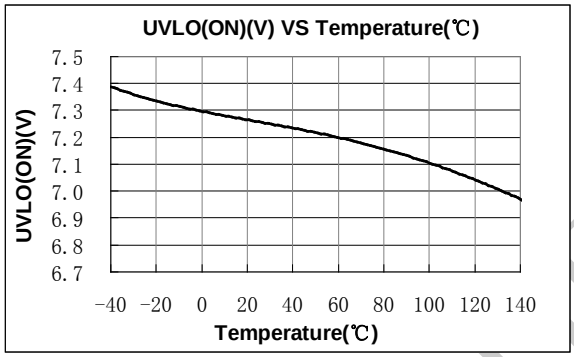
Oscillator						
FOSC	Normal Oscillation Frequency	VDD=14V, FB=3V, CS=0.3V	60	65	70	KHz
△f_OSC	Frequency spreading range			+/-4		%
F_spreading	Spreading frequency			32		Hz
△f_Temp	Frequency Temperature stability			5		%
△f_VDD	Frequency Voltage Stability			1		%
F_Hiccup	Hiccup Mode Switch Frequency			22		KHz
OUT driver						
VOL	Ouput low level @ VDD=14V, Io=5mA			1		V
VOH	Ouput high level @ VDD=14V, Io=20mA		6			V
VO_CLAMP	Output clamp voltage			13		V
T_r	Output rising time 1V ~ 12V@ CL=1000pF			175		nS
T_f	Output falling time 12V ~ 1V@ CL=1000pF			85		nS
Over temperature protection						
IOTP	Output current of OTP pin		95	100	105	uA
VOTP	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time			32		Cycle
VOTP_FL	Float voltage at OTP pin			2.7		V
Vth_OVP	External OVP threshold voltage			4		V

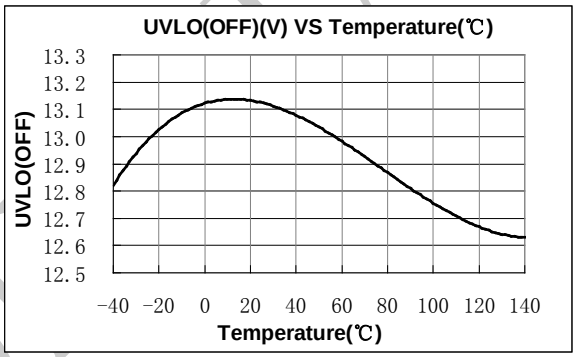
CHARACTERIZATION PLOTS

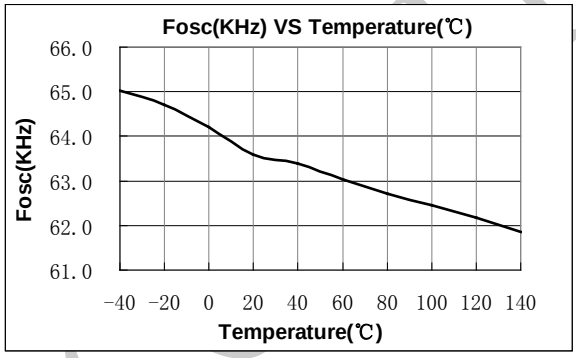
VDD = 16V, TA = 25℃ condition applies if not otherwise noted.











OPERATION DESCRIPTION

PR6863/PR6865 is designed for high performance, low standby power and cost effective offline flyback converter applications. The Hiccup mode control greatly reduces the standby power consumption and helps the system design to meet the international power conservation requirements.

Startup Current and Start up Control
Startup current of PR6863/PR6865 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current
The Operating current of PR6863/PR6865 is low at 1.5mA. Good efficiency is achieved with its low operating current together with the Hiccup mode control features.

Soft Start
PR6863/PR6865 features an internal 5ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO_OFF, the CS peak voltage is gradually increased from 0.15V to the maximum level. Every restart up is followed by a soft start.

Frequency spreading for EMI improvement
The frequency spreading (switching frequency modulation) is implemented in PR6863/PR6865. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Hiccup Mode Operation
At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Hiccup mode threshold level and device enters Hiccup Mode control. The OUT drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the OUT drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation
The switching frequency is internally fixed at 65KHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking
Cycle-by-Cycle current limiting is offered in PR6863/PR6865 current mode PWM control. The switch current is detected by a sense resistor into the cs pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge OUT current of power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation
Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the subharmonic oscillation and thus reduces the output ripple voltage.

Drive
The power MOSFET is driven by a dedicated OUT driver for power switch control. Too weak the OUT drive strength results in higher conduction and switch loss of MOSFET while too strong OUT drive results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole OUT design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Protection Controls
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), and Under Voltage Lockout on VDD (UVLO), and latch shutdown features including over temperature protection (OTP), fixed or adjustable VDD over voltage protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the

converter. It restarts when VDD voltage drops below UVLO limit. For protection with latch shut down mode, control circuit shutdowns (latch) the power MOSFET when an Over Temperature condition or Over Voltage condition is detected until VDD drops below 5V (Latch release voltage), and device enters power on restart-up sequence thereafter.

OTP

A NTC resister connected between pin OTP and GND sets the Over Temperature Protection threshold. A 100uA constant current outflow OTP pin into the NTC resistor. As the rise of temperature, the resistance of the NTC resistor decrease, when the voltage on OTP pin decrease to 1V, OTP becomes active, application circuit goes into latch shutdown mode.

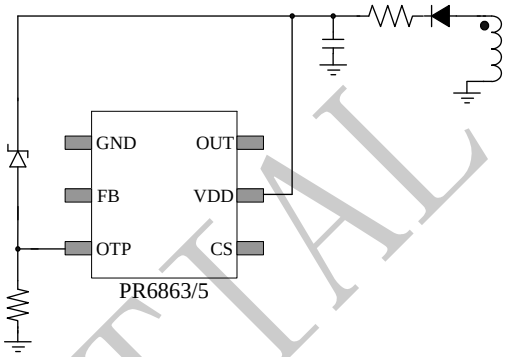
$$100uA \cdot [R_{nom} - K \cdot (T_{OTP} - T_{nom})] = 1V$$

$$T_{OTP} = T_{nom} + \frac{R_{nom} - 10Kohm}{K}$$

While K is the coefficient of the NTC resistor, R_{nom} is the resistance of the NTC resistor at normal temperature.

Output (adjustable) OVP through external Zener

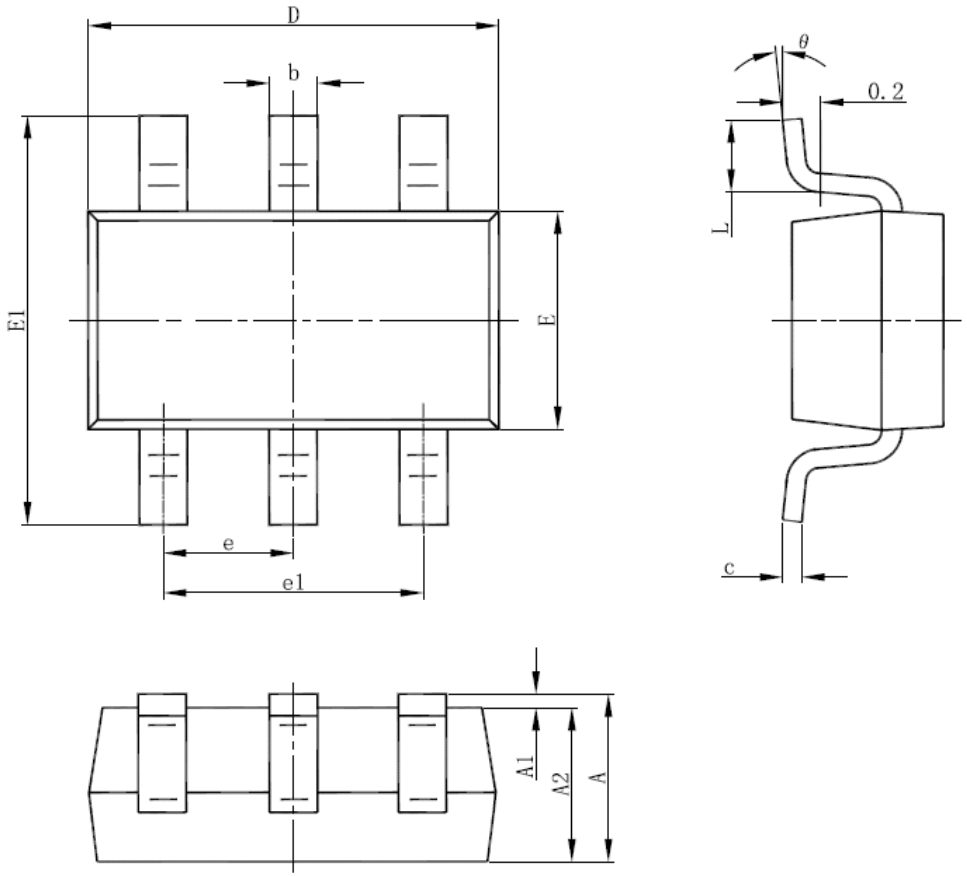
A zener diode connected between pin VDD and OTP sets the output (adjustable) OVP function. When the voltage on OTP pin increase to 4V, output (adjustable) OVP becomes active, application circuit goes into latch shutdown mode.



$$V_{th\_OVP} = V_{zener} + 4V$$

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º