MP5095

Low Iq Dual Channel 2.5A Load Switch

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP5095 integrated a dual load switches to provide load protection covering 0.5V to 5.5V voltage range. Each channel provides up to 2.5A load protection covering 0.5V to 5.5V voltage range with 1.8V Vcc power supply. With the small R_{DSON} in tiny package, MP5095 provide very high efficient and space saving solution in notebook and tablet or other portable devices application.

With the internal soft start function, the MP5095 can avoid inrush current during circuit start up. MP5095 also provides internal current limit, hiccup protection and thermal shutdown features. MP5095 also easily parallel both channels to double current capability.

The MP5095 is available in the small TSOT23-8 package.

FEATURES

- Integrated 20mΩ Low RDSON FETs
- Low Quiescent Current: 30uA
- Wide V_{IN} Range from 0.5V to 5.5V
- <1uA Shutdown Current
- Output Discharge Function
- Continuous Current Capability 2.5A
- Enable Pin
- Short-Circuitry Response Protection
- Easily Parallel Connect Dual Channel
- Support Reverse Block Connection
- Thermal Protection
- Available in a TSOT23-8 Package

APPLICATIONS

- Notebook and Tablet Computers
- Portable Devices
- Solid State Drivers
- Handheld Devices

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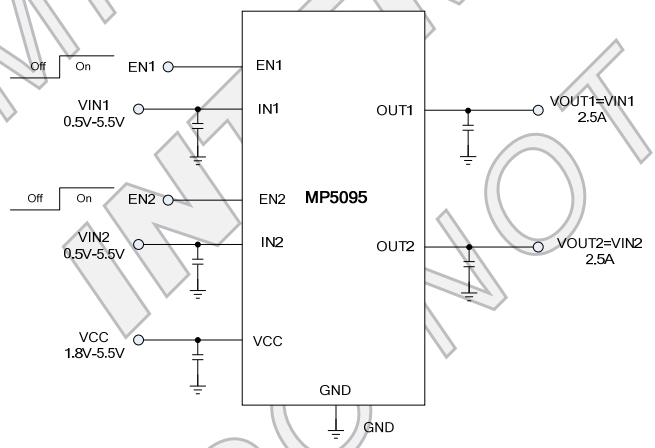
TYPICAL APPLICATION

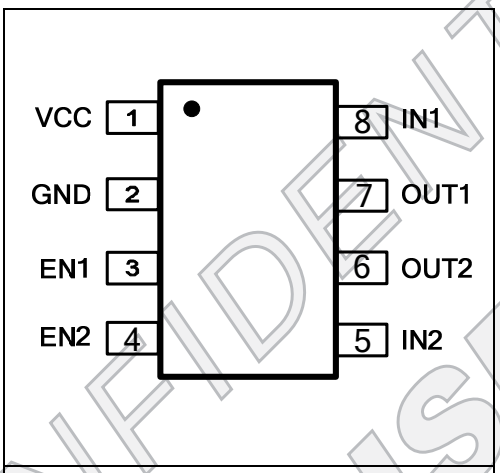


PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

ORDERING INFORMATION

Part Number*	Package	Top Marking

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN1/2}$ .....–0.3V to +6V
$V_{CC1/2}$ .....–0.3V to +6V
$V_{OUT1/2}$ .....–0.3V to +6V
All Other Pins.....–0.3V to Vcc+0.3 V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (2) 1.25W

Recommended Operating Conditions (3)

Supply Voltage $V_{IN1/2}$.....0.5V to 5.5V
Supply Voltage V_{CC}.....1.8V to 5.5V
Output Voltage $V_{OUT1/2}$ .....0.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{CC} = 3.6V, T_J = -40°C to +125°C, Typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input and Supply Voltage Range						
Input Voltage	$V_{IN1/2}$		0.5		5.5	V
Supply Voltage	V_{CC}		1.8		5.5	V
Supply Current (Single Channel)						
Off State Leakage Current	I_{OFF}	V_{IN}=5V, EN=0			1	μA
V_{CC} Standby Current	I_{STBY}	V_{CC}=3.6V, EN=0		0.1	1	μA
		V_{CC}=3.6V, Enable, No load		30		
Power FET						
ON Resistance	$R_{DSON1/2}$	V_{CC}=5.0V, Single Channel		20		mΩ
		V_{CC}=3.3V, Single Channel		24		
Thermal Shutdown and Recovery						
Shutdown Temperature(5)	T_{STD}			155		°C
Hysteresis(5)	T_{HYS}			30		°C
Under Voltage Protection						
V_{CC} Under Voltage Lockout Threshold	V_{CC_UVLO}	UVLO Rising Threshold		1.7	1.8	V
UVLO Hysteresis	$V_{UVLOHYS}$			100		mV
Soft Start						
Vo Rise Time	T_{ss}	Vo=3.6V		50		μs
EN turn on Time	T_{DELAY}			30		μs
Enable						
EN Rising Threshold	V_{ENH}			1	1.2	V
EN Hysteresis	V_{ENHYS}			200		mV
EN pin Resistance		Between EN and GND		1		MΩ
ILIM						
Current Limit(5)	I_{LIM}		2.6		2.9	A
Hiccup On Time	T_{ON}			1.6		ms
Hiccup Off Time	T_{OFF}			100		ms
Discharge Resistance (Single Channel)						
Resistance	R_{DIS}			50		Ω

Notes:

5) Guarantee by characterization -Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{CC} = 3.6V, T_A = 25°C, unless otherwise noted.

TBD

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	Load Switch Supply Voltage to the Control Circuitry.
2	GND	Ground.
3	EN1	Enable Input of Switch 1. Pulling this pin below the specified threshold shuts the chip down.
4	EN2	Enable Input of Switch 2. Pulling this pin below the specified threshold shuts the chip down.
5	IN2	Input Power Supply of Switch 2.
6	OUT2	Output to the Load of Switch 2.
7	OUT1	Output to the Load of Switch 1.
8	IN1	Input Power Supply of Switch 1.

FUNCTIONAL BLOCK DIAGRAM

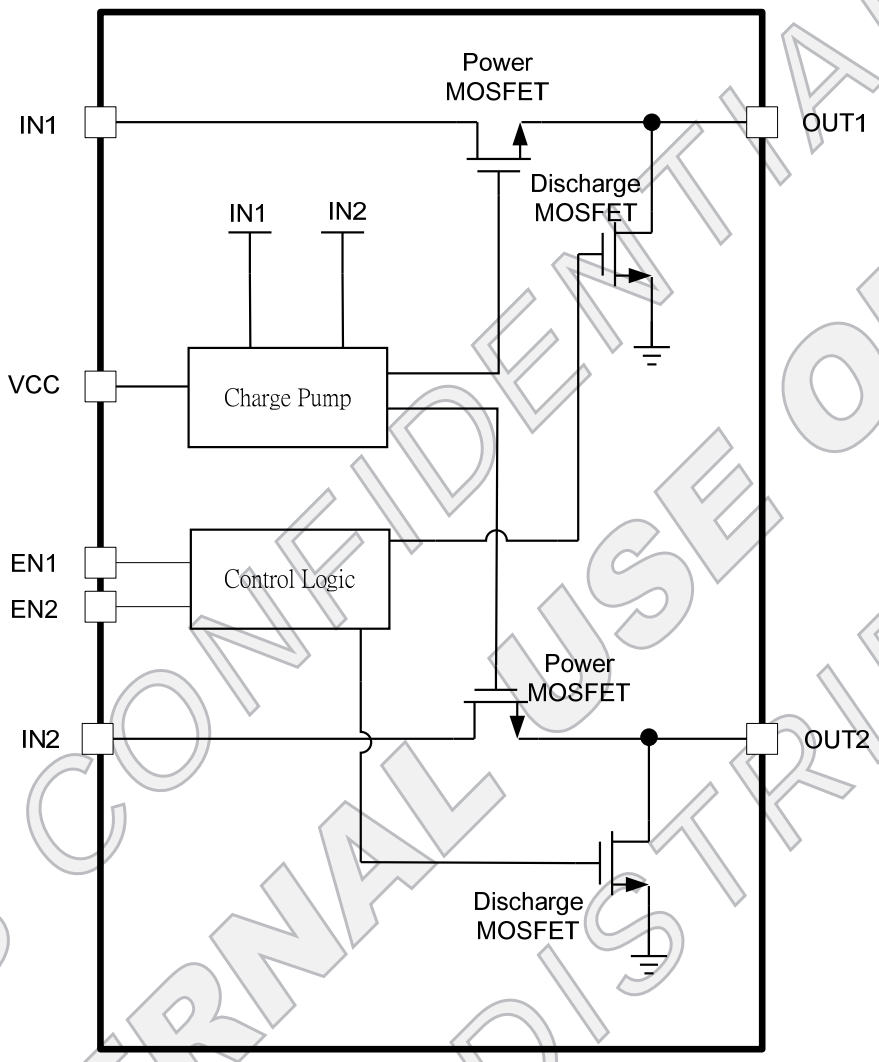


Figure 1: Functional Block Diagram

OPERATION

The MP5095 is designed to limit the in-rush current to the load when a circuit card is inserted into a live backplane power source; thereby limiting the backplane's voltage drop and the slew rate of the voltage to the load. MP5095 integrated dual load switches. Each channel can provide 2.5A load capability. MP5095 also easily parallel both channels connected together to take maximum 5A load.

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 0.5V, and V_{CC} is higher than 1.8V, MP5095 can be enabled by pulling EN pin to higher than 1.2V. Pulling down to ground will disable MP5095.
The recommend start up sequence is power up V_{CC} and V_{IN} first. After they are ready, pull EN voltage to high.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold by a lot before the control loop can respond. If the current reaches an internal secondary current limit level (about 5A), a fast turn-off circuit activates to turn off the power FET. This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. If fast off works, it will keep off the power FET for 80us. After that time period, it will re-turn on power FET.

If the current limit block starts to regulate the output current, the power loss on power MOSFET will cause the IC temperature rise. The hiccup protection will limit current for 2ms then off another 126ms for thermal sink. If the junction temperature rose to high enough in hiccup on time, it will also trigger thermal shutdown. After thermal shutdown happened, it will disable the output until the over temperature fault remove. The over temperature threshold is 155°C and hysteresis is 30°C.

Output Discharge

MP5095 has output discharge function. The output discharge resistor is active when EN or Vcc is low. This function can discharge the Vo by internal pull down resistance when IC disabled and the load is very light.

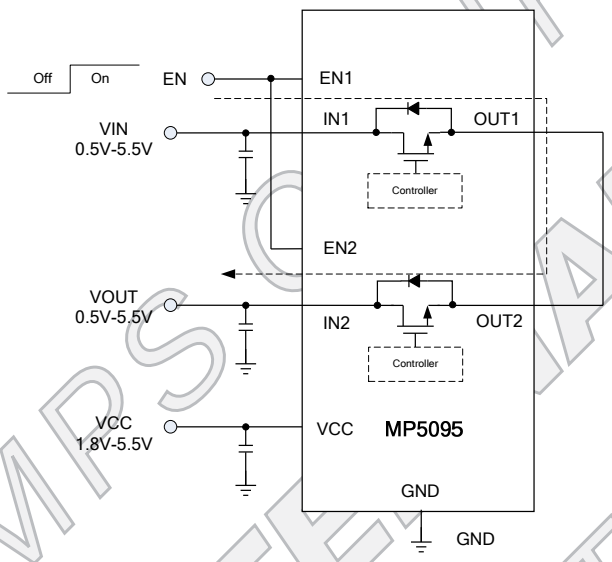
APPLICATION INFORMATION

Selecting the V_{CC} Capacitor

The VCC pin is internal Load Switch Supply Voltage to the Control Circuitry. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 1μF capacitor is sufficient.

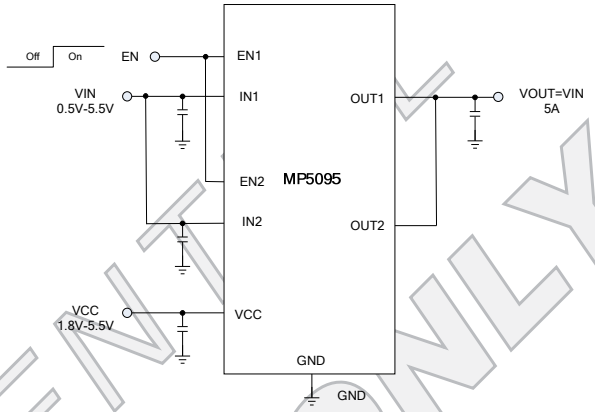
Reverse Current Block Usage

The dual channel load switch can be combined to a single channel load switch with reverse current block function. The circuit is below. The IN1 is input port, and IN2 is output port. When EN1=EN2=high, the internal MOSFET is on. When EN1=EN2=low, the internal MOSFET is off and body diode will block the reverse current.



Parallel Channels Usage

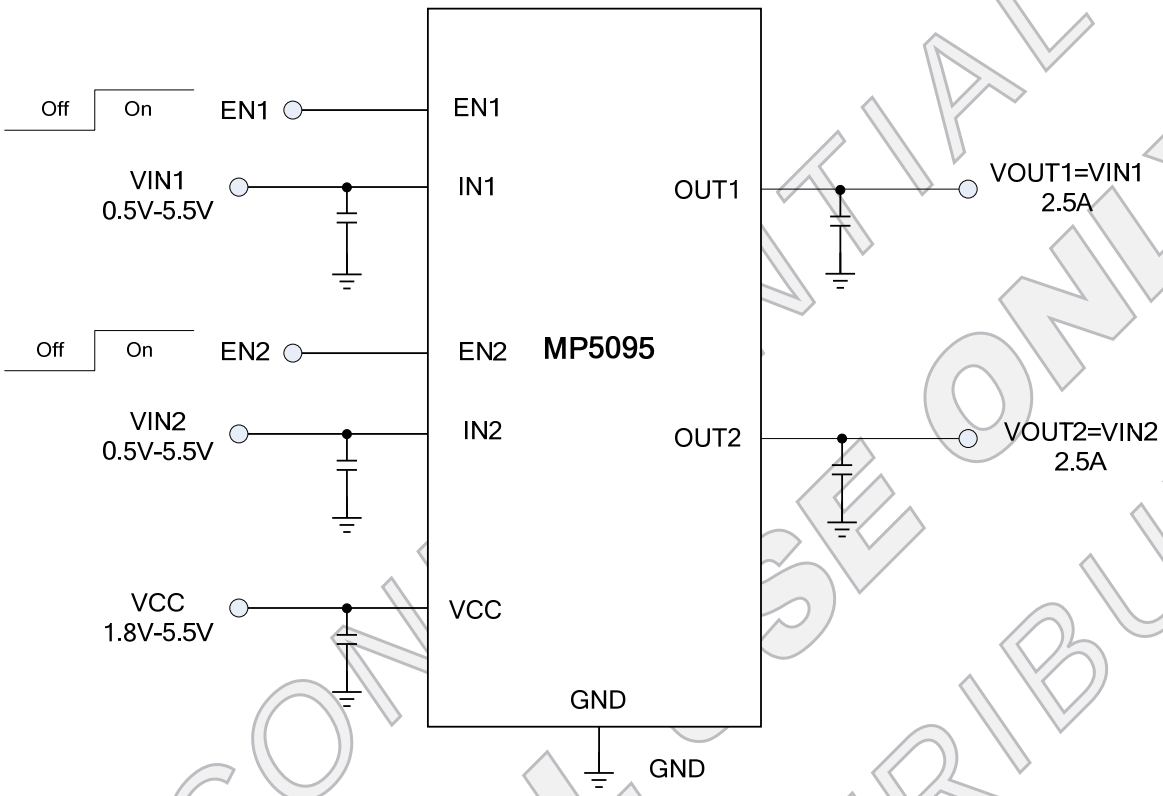
MP5095 can be parallel connected to get a 5A single load switch. The circuit is below. In this parallel connection, the IN1 is connected to IN2 externally, and OUT1 is connected to OUT2 externally too.



Layout Guide

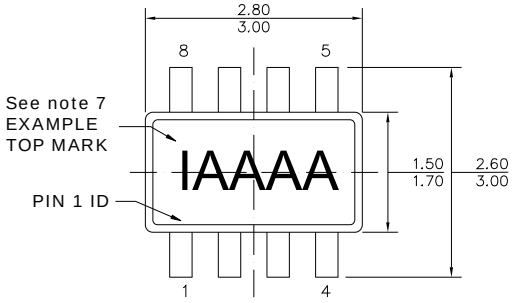
PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference (take schematic in Figure 4 as an example). Place input cap close to V_{CC} pin. Put enough vias around IC to achieve better thermal performance.

TYPICAL APPLICATION CIRCUITS

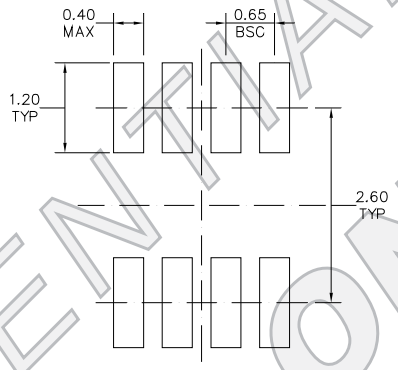


PACKAGE INFORMATION

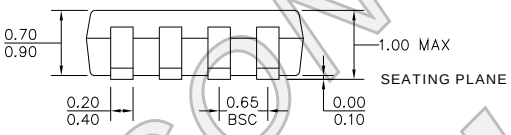
TSOT23-8



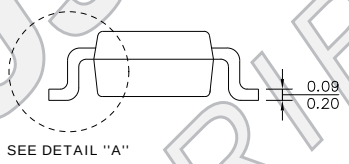
TOP VIEW



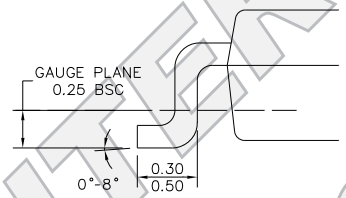
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)