Synchronous Rectification Driver with Green Mode Function

REV. 00

General Description

LD8520 is a secondary side Synchronous Rectification (SR) driver IC. With LD8520 Optimal Dead Time control method, switch power supply not only can achieve high efficiency in dynamic load but also operation safety.

LD8520 is suited for Flyback low side and high side Synchronous Rectification in CCM and DCM. For Forward Freewheeling Rectification application, LD8520 can be applied in CCM and DCM operation.

In light load condition, LD8520 will enter Green Mode to reduce operation current by stopping SR MOSFET driving function.

Load Regulation Improve function is an innovative design in LD8520. With this unique function, switch power supply can achieve better Load Regulation easily.

Features

- Suited for Low Side and High Side Flyback
- Synchronous Rectification in CCM, DCM Suited for Forward Freewheeling Rectification in CCM and DCM.
- Optimal Dead Time Control
- Quickly Response for Dynamic Load
- Enable Function
- 250uA Ultra Low Green Mode Operation Current
- Load Regulation Improve Function

Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

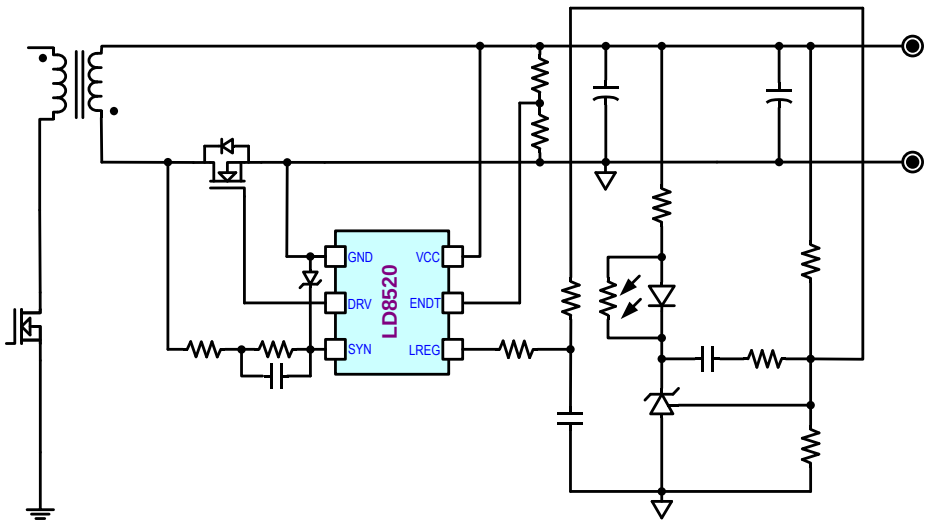


Fig. 1 Flyback Low Side Synchronous Rectification

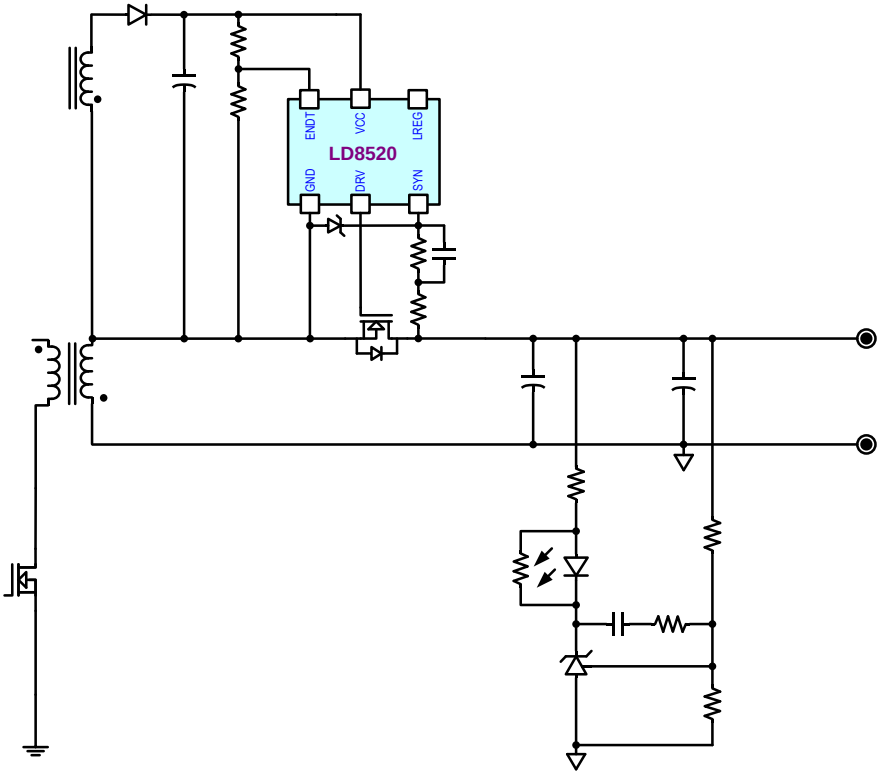


Fig. 2 Flyback High Side Synchronous Rectification

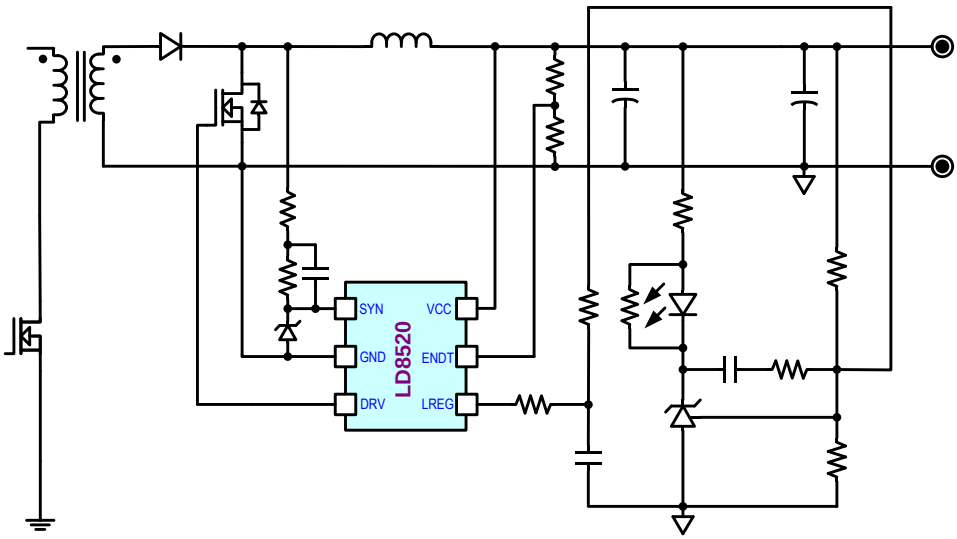
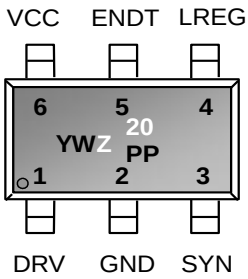


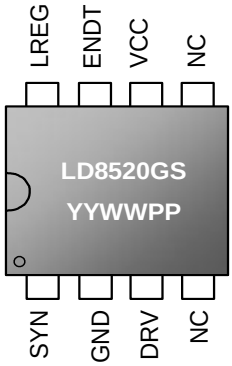
Fig. 3 Forward Freewheeling Rectification

Pin Configuration

SOT-26 (TOP VIEW)



SOP-8 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP, P : Production code
Z20 : LD8520

Ordering Information

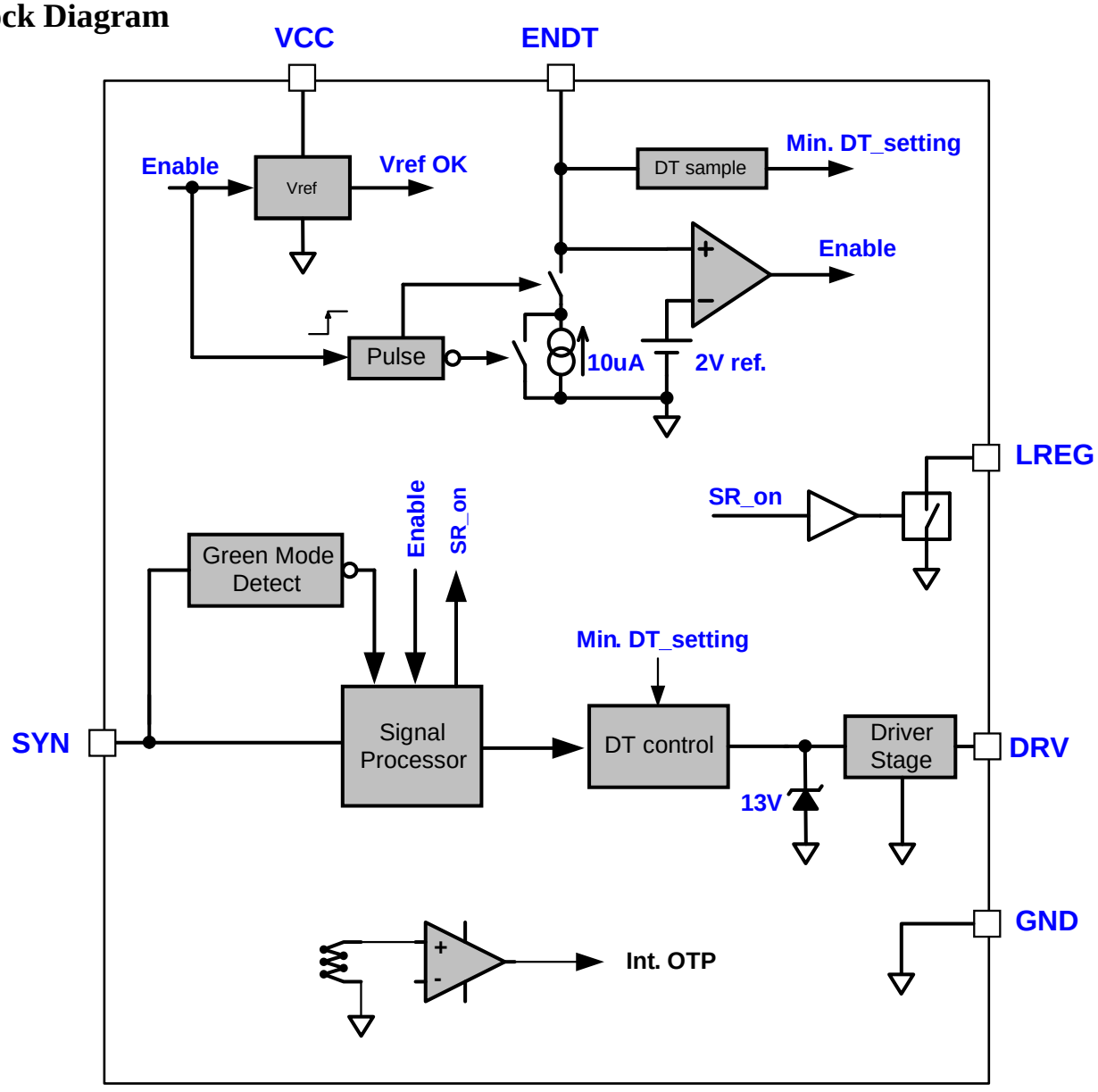
Part number	Package	TOP MARK	Shipping
LD8520GL	SOT-26	YWP/20	3000 /tape & reel
LD8520GS	SOP-8	LD8520	3600 /tube /Carton

The LD8520 is ROHS compliant/Green packaged.

Pin Descriptions

SOT-26	SOP-8	NAME	FUNCTION
1	3	DRV	Driving pin, connector to GATE pin of MOSFET directly or through a resistor
2	2	GND	Ground pin
3	1	SYN	The SYN pin is used to detect V_{DS} of SR MOSFET through a voltage divider.
4	8	LREG	Load regulation compensation pin
5	7	ENDT	Enable & dead time setting pin,
6	6	VCC	Supply voltage pin
—	4	NC	No connect
—	5	NC	No connect

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V ~ 30V
DRV	-0.3V ~ VCC+0.3V
SYN, ENDT, LREG	-0.3V ~ 6V
VCC pin Operating Current	50mA
SYN pin Clamp Current	1mA / -1mA
DRV pin Output Current	1A / -1.5A
LREG pin Sink Current	0.5mA
Operating Junction Temperature	-40°C ~ 125°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage VCC	9	28	V
SYN pin External Resistor	100K	500K	Ω
SYN pin External Capacitor	10	150	pF
ENDT pin	0	4.5	V
LREG pin External Resistor	10K	10M	Ω

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
UVLO(ON)		V_{CC_ON}	7.5	8	8.5	V
UVLO Hysteresis		V_{CC_HYS}	0.35	0.5	0.65	V
Operating Current	VCC=15V, SYN=65kHz, 1nF on DRV pin	I_{VCC_OP}	2	3	4	mA
	Green Mode, SYN pin=4V	I_{VCC_GM}	100	200	250	uA
SYN Reference (SYN Pin)						
SYN High Threshold	Within 80ns at falling edge	V_{SYN_H}	2.3	2.5	2.7	V
SYN Threshold Hysteresis		V_{SYN_HYS}	1.7	2	2.3	V
De-bounce time after SYN pin=Low	*	T_{SYN_DBC}	100	300	500	ns
Clamp Voltage	SYN pin Input Current=1mA	V_{SYN_CLP}	3.5	4	4.5	V
Max Input Current	*	I_{SYN_MAX}			1	mA
					-1	mA
SYN Impedance	*	Z_{SYN}	1			MΩ
Output Driver (DRV Pin)						
Output High Voltage	VCC=12V, Io=10mA	V_{DRV_H}	9			V
Output Low Voltage	VCC=12V, Io=-10mA	V_{DRV_L}			0.5	V
Output Clamp Voltage	VCC=19V	V_{DRV_CLP}	11	13	15	V
Source Capability	*, VCC=12V, Load Capacitor=33nF	I_{DRV_SOC}		1		A
Sink Capability	*, VCC=12V, Load Capacitor=33nF	I_{DRV_SNK}		-1.5		A
Rising Time	VCC=12V, Load Capacitor=1nF GATE=2V~9V	T_r		150		ns
Falling Time	VCC=12V, Load Capacitor=1nF GATE=9V~2V	T_f		30		ns
Propagation Delay Time to GATE High	VCC=12V, T_r：0%~10%	T_d	20	100	200	ns
Max on time		T_{DRV_MAX}	15	25	35	us

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Enable Function (ENDT Pin)						
Enable Voltage		V_{EN}	1.9	2	2.1	V
ENDT pin OVP		V_{EN_OVP}	5	5.5	6	V
ENDT pin OVP de-bounce time	*	T_{EN_OVDBC}	20	50	100	us
Min. Dead Time Setting (ENDT Pin)						
Detecting Current	EN pin= V_{EN}	I_{DT_DET}	9	10	11	uA
Minimum Dead Time Setting	Dead Time A External Resistor < 60kΩ	T_{DT}	0.7	1.0	1.3	us
	Dead Time B External Resistor =100kΩ ~ 130kΩ		1.2	1.5	1.8	us
	Dead Time C External Resistor > 200kΩ		1.7	2.0	2.3	us
Load regulation Compensation (LREG Pin)						
Input Impedance when switch close	*	Z_{LRG_CLS}			50	Ω
Input Impedance when switch open	*	Z_{LRG_OPN}	1			MΩ
On Chip OTP (Over Temperature) Auto-Recovery						
OTP Level	*	T_{OTP}		140		°C
OTP Hysteresis	*	T_{OTP_HYS}		30		°C

*: Guaranteed by designed.

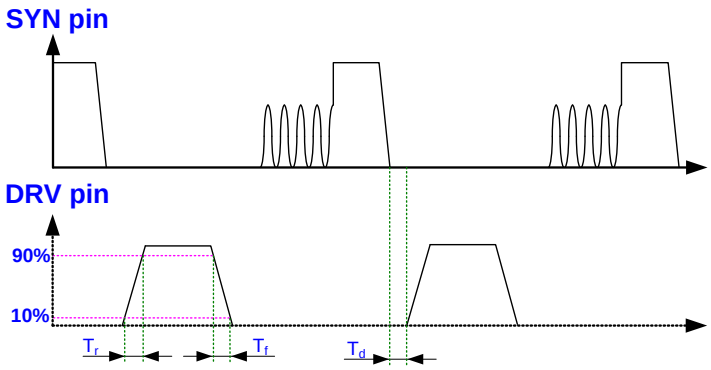


Fig. 4 T_r & T_f & T_d parameters

Typical Performance Characteristics

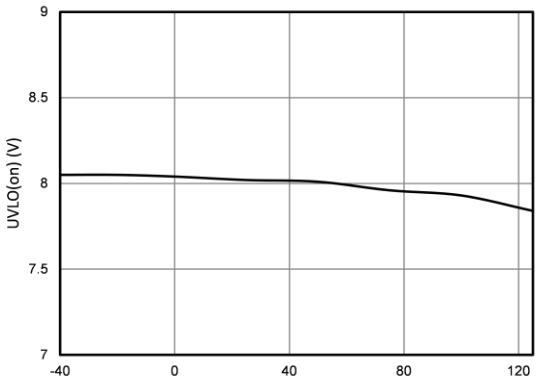


Fig. 5 UVLO(on) vs.Temperature

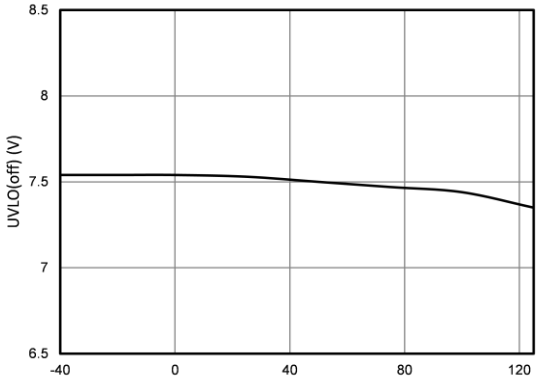


Fig. 6 UVLO(off) vs.Temperature

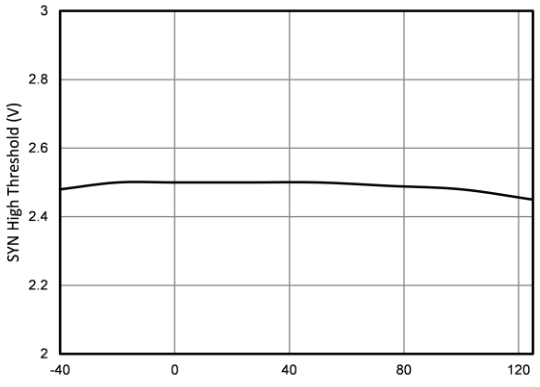


Fig. 7 SYN High Threshold vs.Temperature

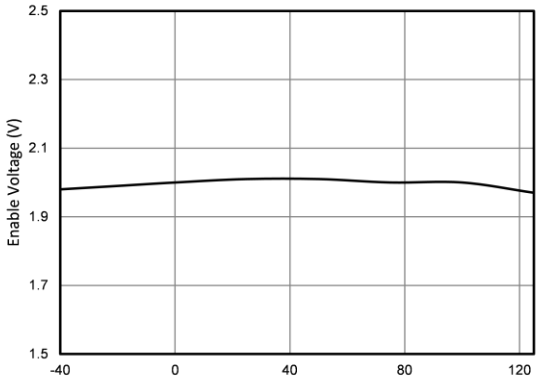


Fig. 8 Enable Voltage vs.Temperature

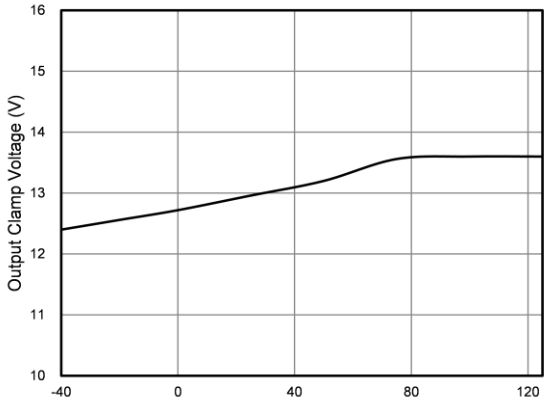


Fig. 9 Output Clamp Voltage vs.Temperature

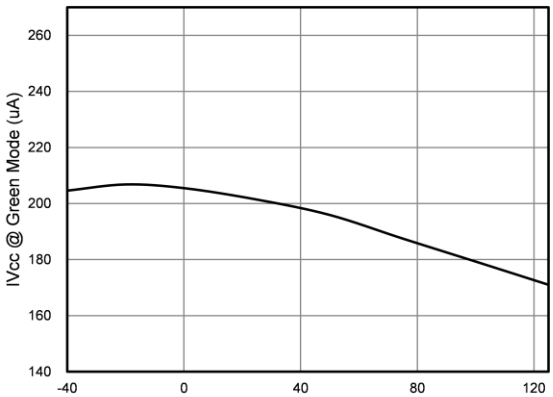


Fig. 10 IVcc@ Green Mode vs.Temperature

Application Information

Operation Overview

LD8520 is a secondary side Synchronous Rectification driver IC for CCM and DCM operation. LD8520 not only has excellent dead time control function for safety in load transient, but also only needs very few operation current in green mode. In addition, LREG pin provides a possibility to improve load regulation; it is useful for power supply with high output current.

Under Voltage Lockout (UVLO) and Enable Function

The UVLO(ON) and UVLO(OFF) are 8.0V and 7.5V, respective. Besides VCC pin > UVLO(ON), ENDT pin > 2V is necessary to achieve DRV pin output signal.

In general design, the recommend sequence shown as Fig. 11

Turn-on sequence:

VCC > UVLO(ON) → ENDT > 2V → DRV enable

Turn-off sequence:

ENDT < 2V → DRV disable → VCC < UVLO(OFF)

With enable function, Synchronous Rectifier always operates in stable condition. Therefore, some unstable transient like turn-on, turn-off, SURGE, ESD…etc. would not make Synchronous Rectifier working unsafe.

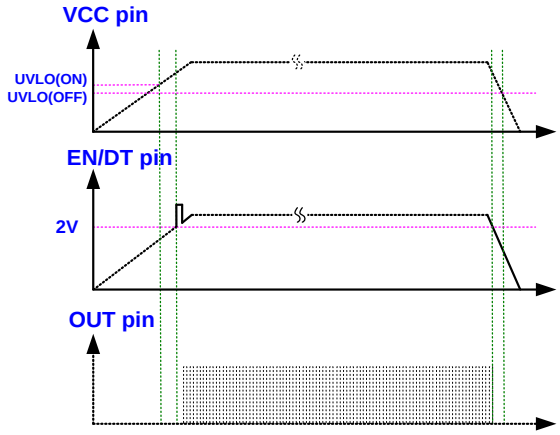


Fig. 11

Dead Time Setting

Besides enables function, ENDT pin has minimum dead time setting function also. When ENDT pin=2V, ENDT pin will source 10uA to detect its external resistance for 50us, as shown in Fig. 12 At that moment, ENDT pin voltage can be described as [10uA * (Ra//Rb)+2V], higher voltage level means longer minimum dead time. The detection function works one time only after VCC pin > UVLO(ON), and the setting would be memorized until VCC < UVLO(OFF).

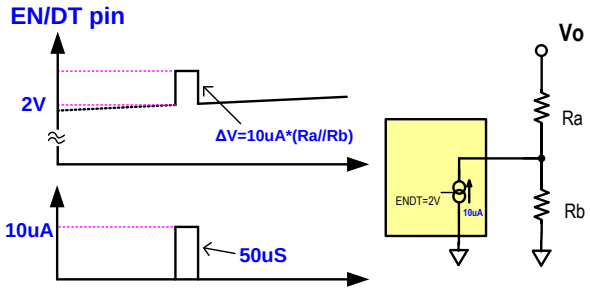


Fig. 12

SYN Pin Behavior

SYN pin detect system behavior, then the internal logic circuit determine when DRV pin turn-on and turn-off , what dynamic dead time is at system in load transient, when LD8520 enter/leave green mode.

As shown in Fig.13, when SYN pin voltage falling fast, that means secondary-side current goes through SR MOSFET and LD8520 will drive DRV pin immediately. Otherwise, falling slow signal on SYN pin would be judged as DCM ring on primary-side, that would not trigger DRV pin high. When system operates in steady condition, the real dead time would close to minimum dead time. In some case of load transient, line voltage change, output short, output over voltage…etc., variable SYN pin signal would causes increasing dynamic dead time to make sure system safety.

When system operates in burst mode, LD8520 works in green mode also. That means LD8520 only needs less than 250uA operation current by its advanced circuitry.

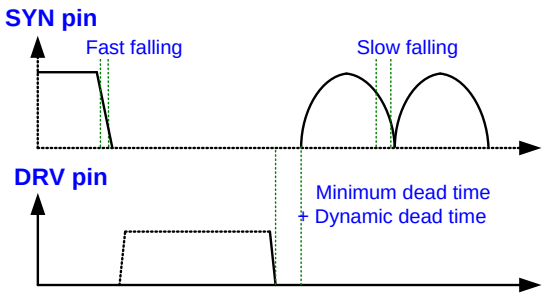


Fig. 13

LREG Pin Behavior

In some higher output current system, series voltage drop on output cable would cause worse load regulation. There is a signal level switch inside LREG pin, the switch turn on by SYN signal. Generally, LREG internal switch has low impedance when secondary-side current existence, as shown in Fig. 14.

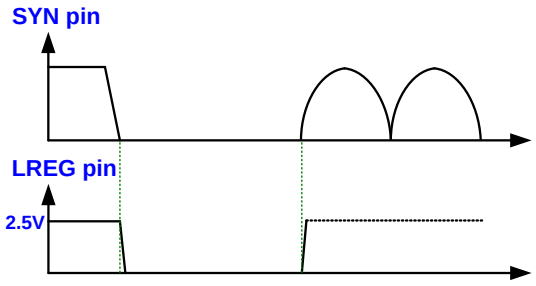


Fig. 14