Title	***Reference Design Report for a 150 W Power Factor Corrected LLC Power Supply Using HiperPFS2™ (PFS7326H) and HiperLCS™ (LCS702HG)***
Specification	90 VAC – 265 VAC Input; 150 W (~43 V at 0 - 3.5A) Output (Constant Current)
Application	LED Streetlight
Author	Applications Engineering Department
Document Number	RD-382
Date	June 24, 2013
Revision	3.0

Summary and Features

- Integrated PFC stage
- Integrated LLC Stage
- Continuous mode PFC using ferrite core
- High Frequency (250 kHz) LLC for extremely small transformer size.
- Tight LLC dead-time control
- >95% full load PFC efficiency at 115 VAC
- >95% full load LLC efficiency
- System efficiency 91% / 93% at 115 VAC / 230 VAC
- Start-up circuit eliminates separate bias supply
- On-board current regulation and analog dimming circuit

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

1 Introduction

This engineering report describes a 43 (nominal) V, 150 W reference design power supply for 90-265 VAC LED street lights. **The power supply is designed with a constant current output in order to directly drive a 150W LED panel with `43-44 V drop.**
The design is based on the PFS7326HG for the PFC front end. An LCS702HG is used in the LLC output stage.

Figure 1 – RD-382 Photograph, Top View.

Figure 2 – RD-382 Photograph, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Power Factor	**PF**	0.97				Full load, 230 VAC
Main Converter Output						
Output Voltage	V_{LG}		43		V	43 VDC (nominal, defined by LED load)
Output Ripple	$V_{RIPPLE(LG)}$			300	mV P-P	20 MHz bandwidth
Output Current	I_{LG}	0.00	3.5		A	Constant Current Supply protected for no-load condition
Total Output Power						
Continuous Output Power	P_{OUT}		150		W	
Peak Output Power	$P_{OUT(PK)}$			N/A	W	
Efficiency						
Total system at Full Load	η_{Main}		91 93		%	Measured at 115 VAC, Full Load Measured at 230 VAC, Full Load
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Surge						1.2/50 μs surge, IEC 1000-4-5,
Differential		2			kV	Differential Mode: 2 Ω
Common Mode		4			kV	Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		60	°C	See thermal section for conditions

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

3 Schematic

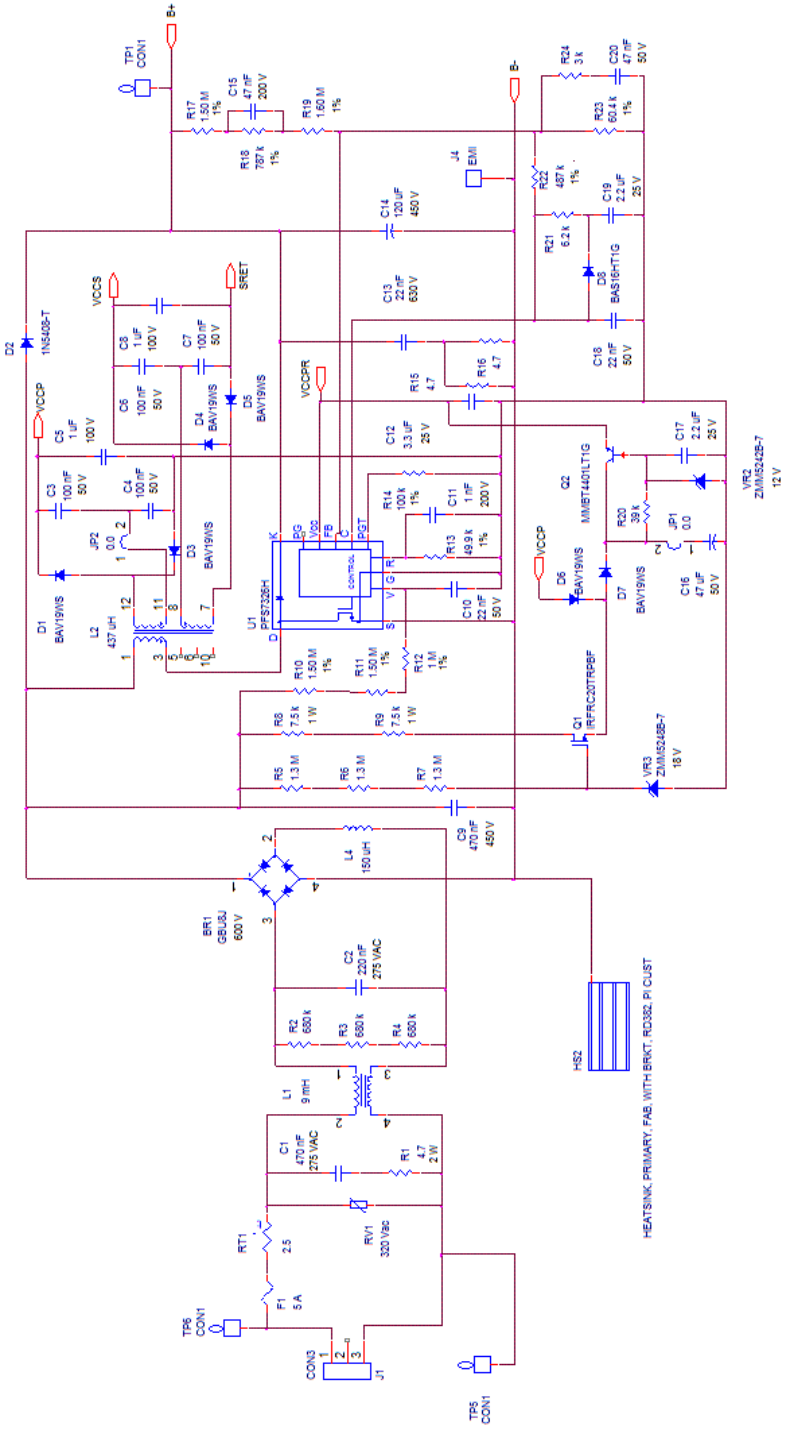


Figure 3 – Schematic RD-382 Street Light Power Supply Application Circuit - Input Filter, PFC Power Stage, and Bias Supplies.

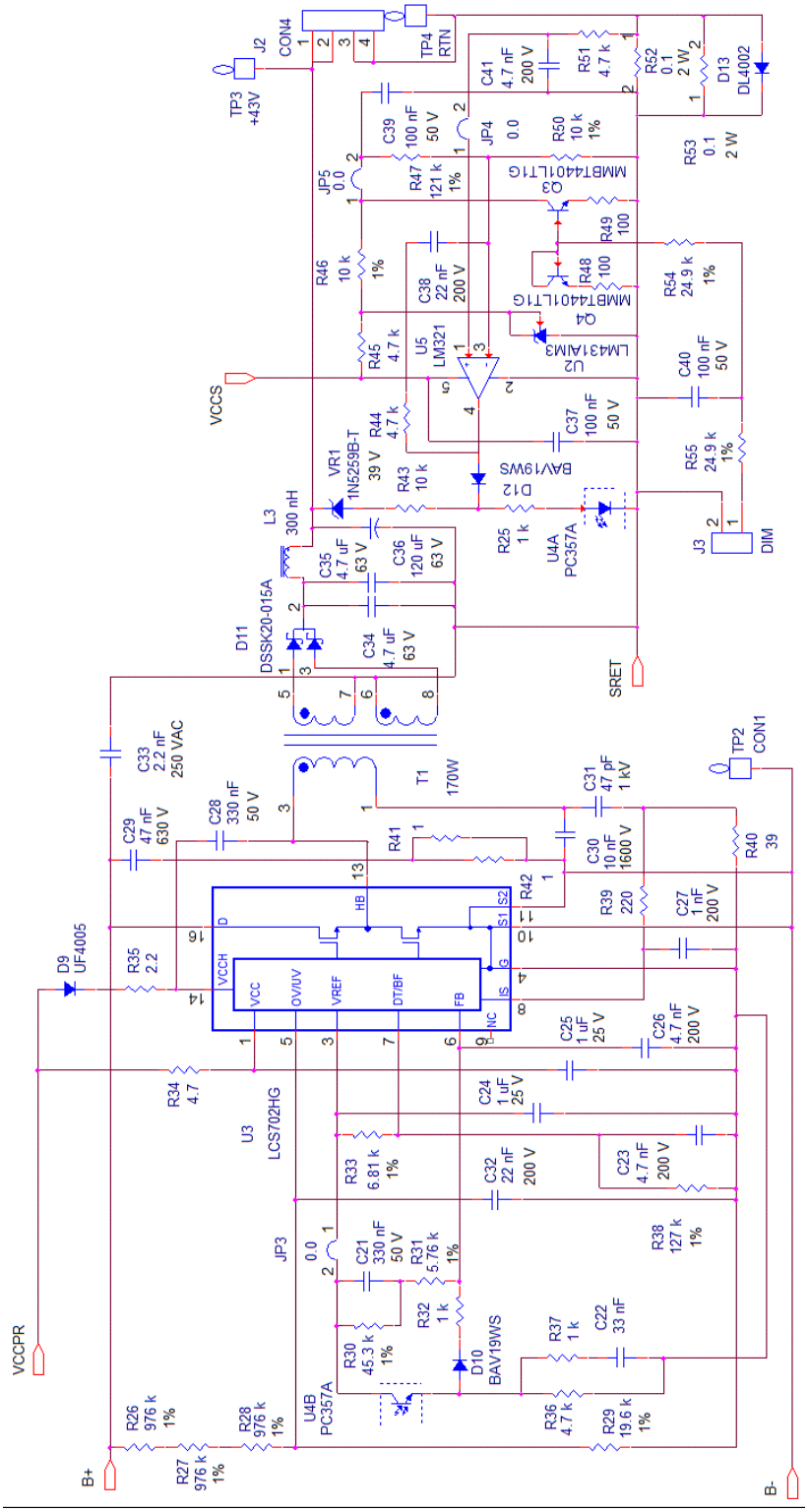


Figure 4 – Schematic of RD-382 Street light Power Supply Application Circuit, LLC Stage.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

4 Circuit Description

The circuit shown in Figures utilizes the PFS7326H and the LCS702H in a ~43V, 150 W power factor corrected constant current LLC power supply intended to power an LED streetlight.

4.1 Input Filter / Boost Converter/Bias Supply

The schematic in Figure 3 shows the input EMI filter, PFC stage, and primary bias supply/startup circuit. The power factor corrector utilizes the PFS7326H. The primary and secondary bias supplies are derived from windings on the PFC inductor (L2).

4.1.1 EMI Filtering/Inrush Limiting

Capacitors C1 and C2 are used to control differential mode noise. Resistor R1 is used for damping to improve power factor and EMI, while resistors R2-4 discharge C1 and C2 when AC power is removed. Inductor L1 controls common mode EMI. The heat sink for U1, U3, and BR1 is connected to primary return to eliminate the heat sink as a source of radiated/capacitively coupled noise. Thermistor RT1 provides inrush limiting. Capacitor C33 (Figure 4) filters common mode EMI. Inductor L4 filters differential mode EMI.

4.1.2 Main PFC Stage

Components R17-19 and R23 provide output voltage feedback, with C15 providing fast dv/dt feedback to the U1 FB pin for undershoot and overshoot response of the PFC circuit. Frequency compensation is provided by C19, C20, and R21, R22, and R24. Resistors R10-12 (filtered by C10) provide input voltage information to U1. Resistor R13 (filtered by C11) programs the U1 current limit for “efficiency” mode. Resistor R14 programs the “power good” threshold for U7.

Capacitor C12 provides local bypassing for U1. Diode D2 charges the PFC output capacitor (C14) when AC is first applied, routing the inrush current around PFC inductor L2 and the internal output diode of U1. Capacitor C13 and R15-16 are used to shrink the high frequency loop around components U1 and C14 to reduce EMI. The resistors in series with C13 damp mid-band EMI peaks. The incoming AC is rectified by BR1 and filtered by C9. Capacitor C9 was selected as a low-loss polypropylene type to provide the high instantaneous current through L2 during U1 on-time. Thermistor RT1 limits inrush current at startup.

4.1.3 Primary Bias Supply/Startup

Components R5-7, R8-R9, Q1, and VR3 provide startup bias for U1. Once U1 starts, components D1, D3, and, C3-5 generate a primary-referred bias supply via a winding on PFC choke L2. This is used to power both the PFC and LLC stages of the power supply. Once the primary bias supply voltage is established, it is used to turn off mosfet Q1 via diode D6, reducing power consumption. Resistors R8-9 protect Q1 from excessive power dissipation if the power supply fails to start.

Components D7, Q2, C16-17 and VR2 regulate the bias supply voltage for U1 and U3. Components D4-5 and C6-8 generate a bias supply for the secondary control circuitry via a triple insulated winding on L2.

4.2 LLC Converter

The schematic in Figures 5 depicts a ~43 V, 150 W LLC DC-DC converter with constant current output implemented using the LCS702HG.

4.3 Primary

Integrated circuit U3 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U3 drives output transformer T1 via a blocking/resonating capacitor (C30). This capacitor was rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T1 was designed for a leakage inductance of 34 μH. This, along with resonating capacitor C30, sets the primary series resonant frequency at ~273 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C30) in Farads.

The transformer turns ratio was set by adjusting the primary turns such that the operating frequency at nominal input voltage and full load is close to, but slightly less than, the previously described resonant frequency.

An operating frequency of 250 kHz was found to be a good compromise between transformer size, output filter capacitance (enabling ceramic/film capacitors), and efficiency.

The number of secondary winding turns was chosen to provide a good compromise between core and copper losses. AWG #44 Litz wire was used for the primary and AWG #42 Litz wire, for the secondary, this combination providing high-efficiency at the operating frequency (~250 kHz). The number of strands within each gauge of Litz wire was chosen as a balance between winding fit and copper losses.

The core material selected was PW4 (from Itacoil). This material yielded acceptable (low loss) performance.

Components D9, R35, and C28 comprise the bootstrap circuit to supply the internal high-side driver of U3.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Components R34 and C25 provide filtering and bypassing of the +12 V input, the V_{CC} supply for U1. *Note: V_{CC} voltage of >15 V may damage U3.*

Voltage divider resistors R26-28 set the high-voltage turn-on, turn-off, and overvoltage thresholds of U3. The voltage divider values are chosen to set the LLC turn-on point at 360 VDC and the turn-off point at 285 VDC, with an input overvoltage turn-off point at 473 VDC. Built-in hysteresis sets the input undervoltage turn-off point at 280 VDC.

Capacitor C29 is a high-frequency bypass capacitor for the +380 V input, connected with short traces between the D and S1/S2 pins of U3. Series resistors R41-42 provide EMI damping.

Capacitor C31 forms a current divider with C30, and is used to sample a portion of the primary current. Resistor R40 senses this current, and the resulting signal is filtered by R39 and C27. Capacitor C31 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used in the RD-382 is a ceramic disc with “SL” temperature characteristic, commonly used in the drivers for CCFL tubes. The values chosen set the 1 cycle (fast) current limit at 5 A, and the 7-cycle (slow) current limit at 2.75 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C31}{C30 + C31}\right) \times R40}$$

I_{CL} is the 7-cycle current limit in Amperes, R40 is the current limit resistor in Ohms, and C30 and C31 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R39 and capacitor C27 filter primary current signal to the IS pin. Resistor R39 is set to 220 Ω, the minimum recommended value. The value of C27 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, the current sense does not require a complicated rectification scheme.

The Thevenin equivalent combination of R33 and R38 sets the dead time at 330 ns and maximum operating frequency for U3 at 847 kHz. The DT/BF input of U3 is filtered by C23. The combination of R33 and R38 also selects burst mode “1” for U3. This sets the lower and upper burst threshold frequencies at 382 kHz and 437 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U3, reducing the output voltage. The series combination of R30 and R31

sets the minimum operating frequency for U3 at ~160 kHz. This value was set to be slightly lower than the frequency required for regulation at full load and minimum bulk capacitor voltage. Resistor R30 is bypassed by C21 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R31 is typically set at the same value as the combination of R33 and R38 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R33 and R38. If the value of R31 is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U4 drives the U3 FEEDBACK pin through R32 which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C26 filters the FEEDBACK pin. Resistor R36 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R32 and R36 also improve large signal step response and burst mode output ripple. Diode D10 isolates R36 from the F_{MAX}/soft start network.

4.4 Output Rectification

The output of transformer T1 is rectified and filtered by D11 and C34-35. These capacitors are polyester dielectric, chosen for output ripple current rating. Output rectifier D11 is a 150 V Schottky rectifier chosen for high efficiency. Intertwining the transformer secondary halves (see transformer construction details in section 8) reduces leakage inductance between the two secondary halves, reducing the worst-case PIV and allowing use of a 150V Schottky diode with consequent higher efficiency. Additional output filtering is provided by L3 and C36. Capacitor C36 also damps the LLC output impedance peak at ~30 kHz caused by the LLC “virtual” output series R-L and output capacitors C35-36.

4.5 Output Current and Voltage Control

Output current is sensed via resistors R52 and R53. These resistors are clamped by diode D13 to avoid damage to the current control circuitry during an output short circuit. Components R45 and U2 provide a voltage reference for current sense amplifier U5. The reference voltage is divided down by R46-47 and R50, and filtered by C39.Voltage from the current sense resistor is filtered by 51 and C41 and applied to the non-inverting input of U5. Opamp U5 drives optocoupler U4 via D12 and R25. Components R25, R44, R51, C38, and C41 are used for frequency compensation of the current loop.
Components VR1 and R43 provide output voltage sensing to protect the power supply in case the output load is removed. These components were selected using a relatively large value for R43 and a relatively low voltage for VR1 to provide a soft voltage limiting characteristic. This helps prevent oscillation at the knee of the V-I curve and improves the startup characteristics of the supply into the specified LED load.

Components J3, Q3-4, R48-49, R54-55, R946, R924, and C40 are used to provide a remote dimming capability. A dimming voltage at J3 is converted to a current by R54 and

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

R55 and applied to R45 via current mirror Q3-Q4. This current pulls down on the reference voltage to current sense amplifier U5 and reduces the programmed output current. A dimming voltage of 0-10 VDC provides an output current range of 100% at 0V to ~20% at 10 VDC input.

5 PCB Layout

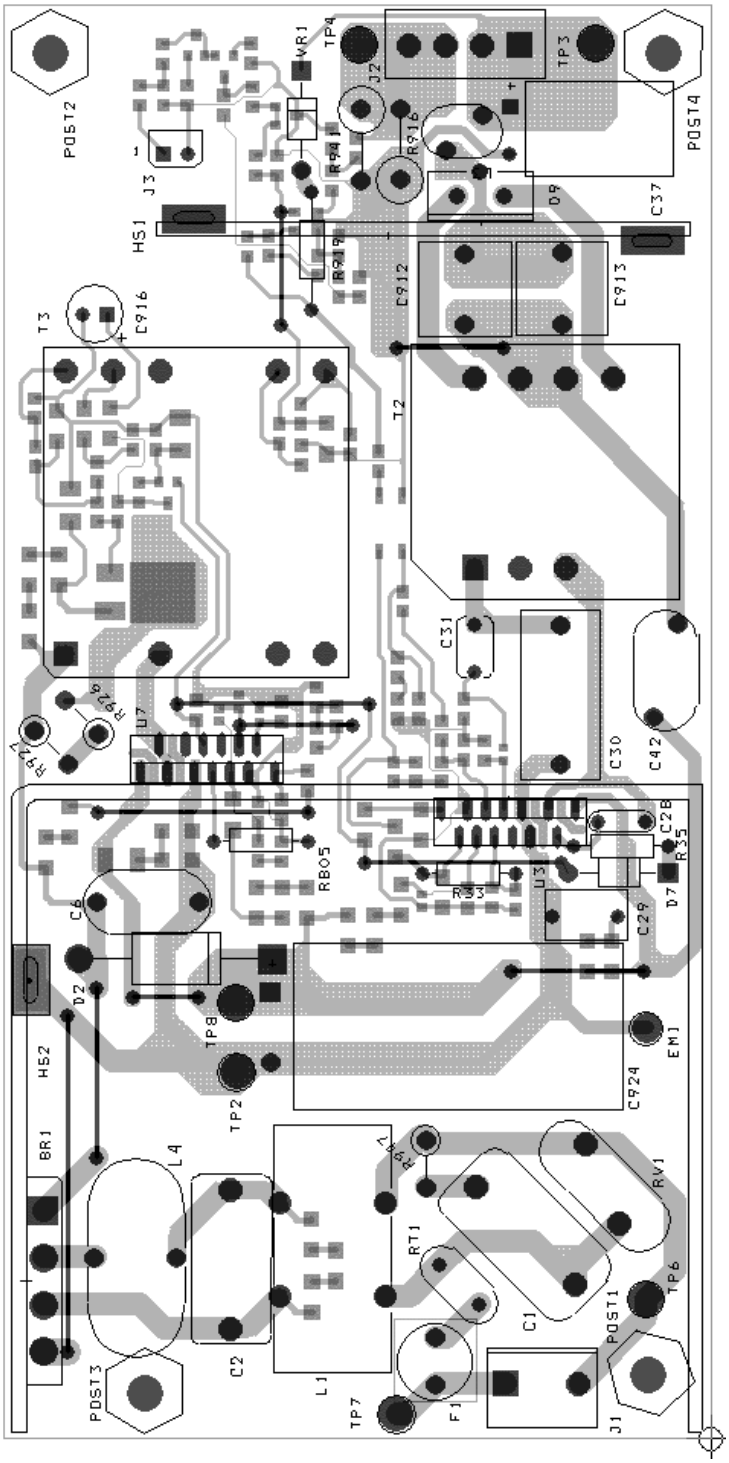


Figure 5 – Printed Circuit Layout, Top Side.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

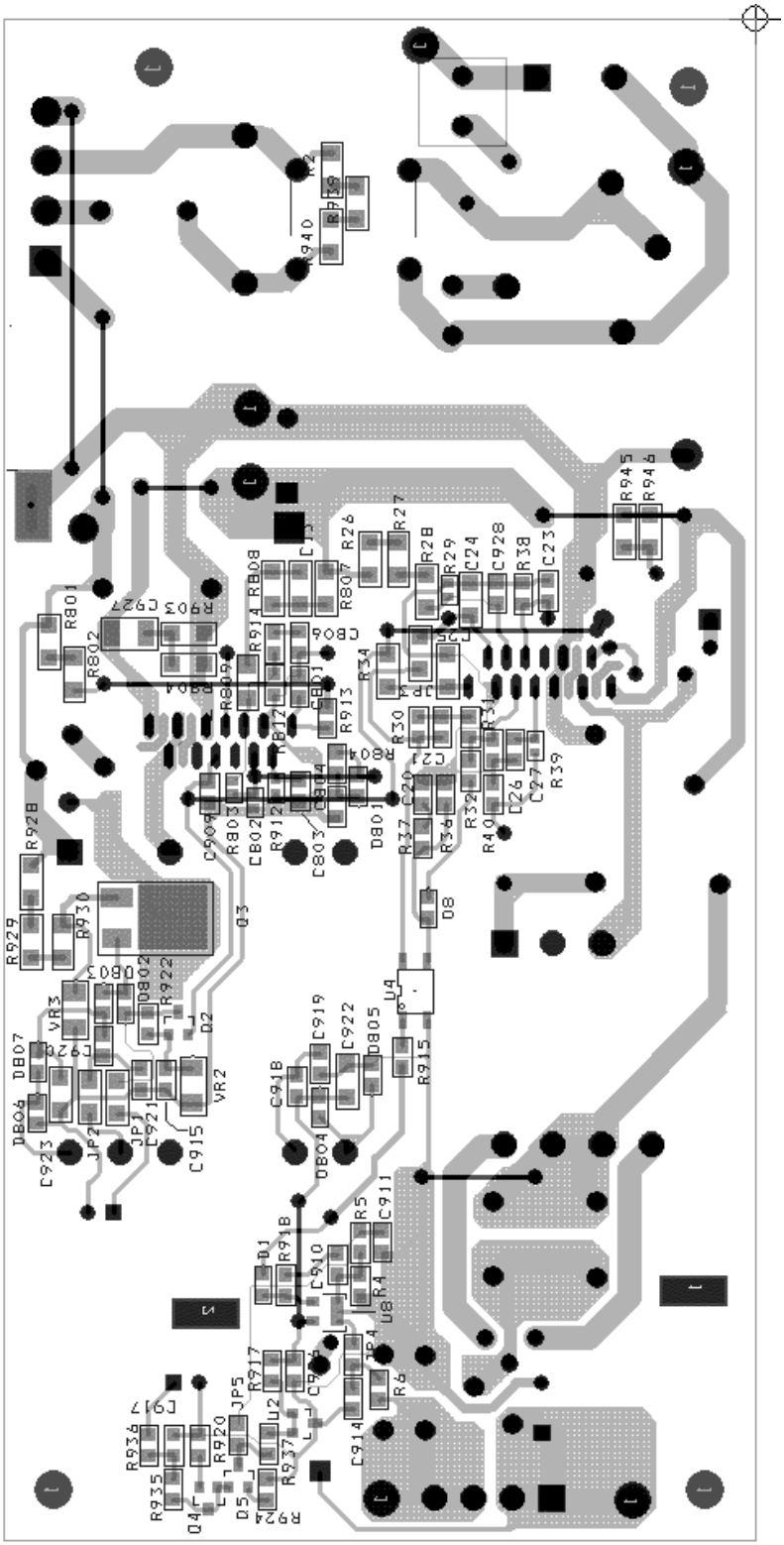


Figure 6 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Part Reference	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial Co.
2	1	C1	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli
3	1	C2	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
4	7	C3 C4 C6 C7 C37 C39 C40	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
5	2	C5 C8	1 uF,100 V, Ceramic, X7R, 1206	HMK316B7105KL-T	Taiyo Yuden
6	1	C9	470 nF, 450 V, METALPOLYPRO	ECW-F2W474JAQ	Panasonic
7	1	C10	22 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H223K	Panasonic
8	1	C11	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
9	1	C12	3.3 uF, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK Corp
10	1	C13	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
11	1	C14	120 uF, 450V, Electrolytic, 20 %, (18 x 37mm)	450BXW120MEFC18X35	Rubycon
12	1	C15	47 nF, 200V, Ceramic, X7R, 1206	12062C473KAT2A	AVX Corp
13	1	C16	47 uF, 50V, Electrolytic, 20 %, (6.3 x 12.5 mm)	50YXM47MEFC6.3X11	Rubycon
14	2	C17 C19	2.2 uF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK Corp
15	1	C18	22 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H223K	TDK Corp
16	1	C20	47 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H473KA01L	Murata
17	1	C21	330 nF, 50 V, Ceramic, X7R, 0805	GRM219R71H334KA88D	Murata
18	1	C22	33 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H333K	Panasonic
19	3	C23 C26 C41	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX Corp
20	2	C24 C25	1 uF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK Corp

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

21	1	C27	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
22	1	C28	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK Corp
23	1	C29	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
24	1	C30	10 nF, 1600 V, Film	B32652A1103J	Epcos
25	1	C31	47 pF, 1 kV, Disc Ceramic	DEA1X3A470JC1B	Murata
26	2	C32 C38	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX Corp
27	1	C33	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
28	2	C34 C35	4.7 uF, 63 V, Polyester Film	B32560J475K	Epcos
29	1	C36	120 uF, 63 V, Electrolytic, Gen. Purpose, (8 x 22)	EEU-FR1J121LB	Panasonic
30	2	CLIP_LCS_PFS1 CLIP_LCS_PFS2	Heatsink Hardware, Clip LCS_II/PFS	EM-285V0	Kang Yang Harware Enterprise Co., Ltd.
31	8	D1 D3 D4 D5 D6 D7 D10 D12	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
32	1	D2	1000 V, 3 A, Recitifier, DO-201AD	1N5408-T	Diodes Inc.
33	1	D8	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semiconductor
34	1	D9	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
35	1	D11	150 V, 20 A, Schottky, TO-220AB	DSSK 20-015A	IXYS
36	1	D13	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002-13-F	Diodes Inc
37	1	F1	5 A, 250V, Slow, TR5	37215000411	Wickman
38	1	HS1	HEATSINK, Custom, Al, 3003, 0.062" Thk		Custom
39	1	HS2	HEATSINK, Custom, Al, 3003, 0.062" Thk		Custom
40	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	B3P-VH	JST
41	1	J2	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex

42	1	J3	2 Position (1 x 2) header, 0.1 pitch, Vertical		Molex
43	3	JP1 JP2 JP3	0 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
44	2	JP4 JP5	0 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
45	1	JP6	Wire Jumper, Insulated, TFE, 18AWG, 1.4 in	C2052A-12-02	Alpha
46	1	JP7	Wire Jumper, Non insulated, 22 AWG, 0.7 in	298	Alpha
47	1	JP8	Wire Jumper, Non insulated, 22 AWG, 0.3 in	298	Alpha
48	1	JP9	Wire Jumper, Insulated, 24 AWG, 0.9 in	C2003A-12-02	Gen Cable
49	1	JP10	Wire Jumper, Non insulated, 22 AWG, 0.6 in	298	Alpha
50	1	JP11	Wire Jumper, Non insulated, 22 AWG, 0.8 in	298	Alpha
51	2	JP12 JP15	Wire Jumper, Non insulated, 22 AWG, 0.5 in	298	Alpha
52	1	JP13	Wire Jumper, Insulated, 24 AWG, 0.8 in	C2003A-12-02	Gen Cable
53	1	JP14	Wire Jumper, Insulated, 24 AWG, 0.5 in	C2003A-12-02	Gen Cable
54	1	L1	9 mH, 5A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine Technologies
55	1	L2	Custom, RD-382 PFC Choke, 437 uH, PQ32/30, Vertical, 9 pins	BQ32/30-1112CPFR	TDK
56	1	L3	Custom, 300nH, +/- 15%, constructed on Micrometals T30-26 toroidal core		Power Integrations
57	1	L4	150uH, 3.4A, Vertical Toroidal	2114-V-RC	Bourns
58	4	POST1 POST2 POST3 POST4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

59	1	Q1	400 V, 2 A, 4.4 Ohm, 600 V, N-Channel, DPAK	IRFRC20TRPBF	Vishay/Siliconix
60	3	Q2 Q3 Q4	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
61	1	R1	4.7 R, 2 W, Flame Proof, Pulse Withstanding, Wire Wound	WHS2-4R7JA25	IT Elect_Welwyn
62	3	R2 R3 R4	680 k, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
63	3	R5 R6 R7	1.3 M, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ135V	Panasonic
64	2	R8 R9	7.5 k, 5%, 1 W, Metal Oxide	RSF100JB-7K5	Yageo
65	3	R10 R11 R17	1.50 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
66	1	R12	1 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1004V	Panasonic
67	1	R13	49.9 k, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4992V	Panasonic
68	1	R14	100 k, 1%, 1/4 W, Metal Film	MFR-25FBF-100K	Yageo
69	3	R15 R16 R34	4.7 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ4R7V	Panasonic
70	1	R18	787 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7873V	Panasonic
71	1	R19	1.60 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1604V	Panasonic
72	1	R20	39 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ393V	Panasonic
73	1	R21	6.2 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ622V	Panasonic

7 LED Panel Characterization

A commercial 150W LED streetlight was used to test the DER-382 power supply. The power supply and driver electronics were stripped out of the streetlight, leaving the LED panels and heat sinks. The LED array consisted of (6) 7 X 4 panels, internally connected as 4 wide, 7 deep. The driver electronics consisted of 3 separate channels, each driving two panels in series. For the purposes of this experiment, the three separate channels were connected in parallel, resulting in an LED array 12 wide, 14 deep. The V-I characteristic of the LED panels connected in this manner is shown below in Figure 7.

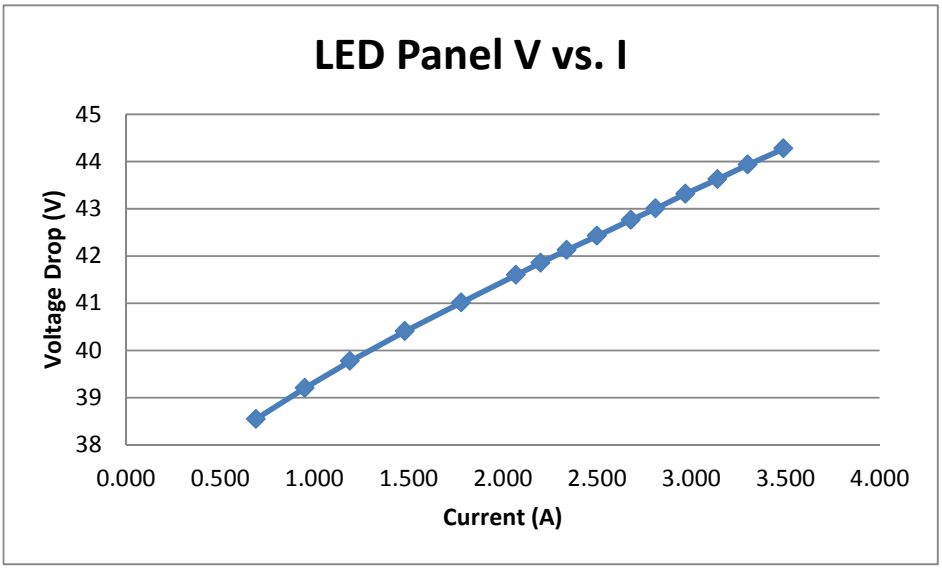


Figure 7 – Streetlight LED Array V-I Characteristic.

7.1 LED Panel Current Sharing

For the purpose of this report, the six LED panels in the street light were partitioned into 3 sections, each section consisting of two LED panels in series. Each panel was internally connected as an array of LEDs 4 wide and 7 deep so that two panels connected in series consisted of an array of LEDS 4 wide by 14 deep. The three sections were connected in parallel, forming a total LED load 12wide and 14 deep. Using a DC current probe, the current in each 4 wide by 14 deep section was measured to determine the current distribution between sections, with results shown below.

Section #	1	2	3
Current (A)	1.113 A	1.159 A	1.126 A

Maximum difference between sections was < 5%.

7.2 Constant Voltage Load

Since this power supply has a constant current output tailored for a relatively fixed constant voltage load, the usual constant current electronic load cannot be used for testing. For bench testing at maximum power, a constant resistance load can be used, set such that the supply output is at maximum current and an output voltage of 43-44V, as indicated by the V-I curve shown in Figure 7. Other testing, including dimming and

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

gain-phase, will require the actual LED load or a constant voltage load that closely mimics its characteristics.

The streetlight LED as a load as a load was both large and heavy, and the light emitted distracting. In order to facilitate EMI and surge testing, a constant voltage load was constructed to emulate the behavior of the LED array in a much smaller package. The circuit is shown in Figure 8. The load consists of paralleled power Darlington transistors Q1-5, each with an emitter resistor (R1-5) to facilitate current sharing. Base resistors R6-10 help prevent oscillation. A string of thirteen 3 mm blue LEDs (D1-13) are used as a voltage reference to mimic the characteristics of the LED panel. Resistor R11 is adjusted to vary the voltage at which the load turns on to match the characteristics of the LED panel. Resistors R12-14 add extra impedance in series with the load to approximate the characteristics of the LED panel. The completed array with heat sink is shown in Figure 9. A small fan was used to cool the heat sink when the load was operated for extended periods at full power. The V-I characteristics of the CV load are shown superimposed on those of the LED array in Figure10. An electronic load with appropriate rating and a constant voltage option (with some series resistance) could also be used for testing, but this load has the advantage that no external AC power is needed.

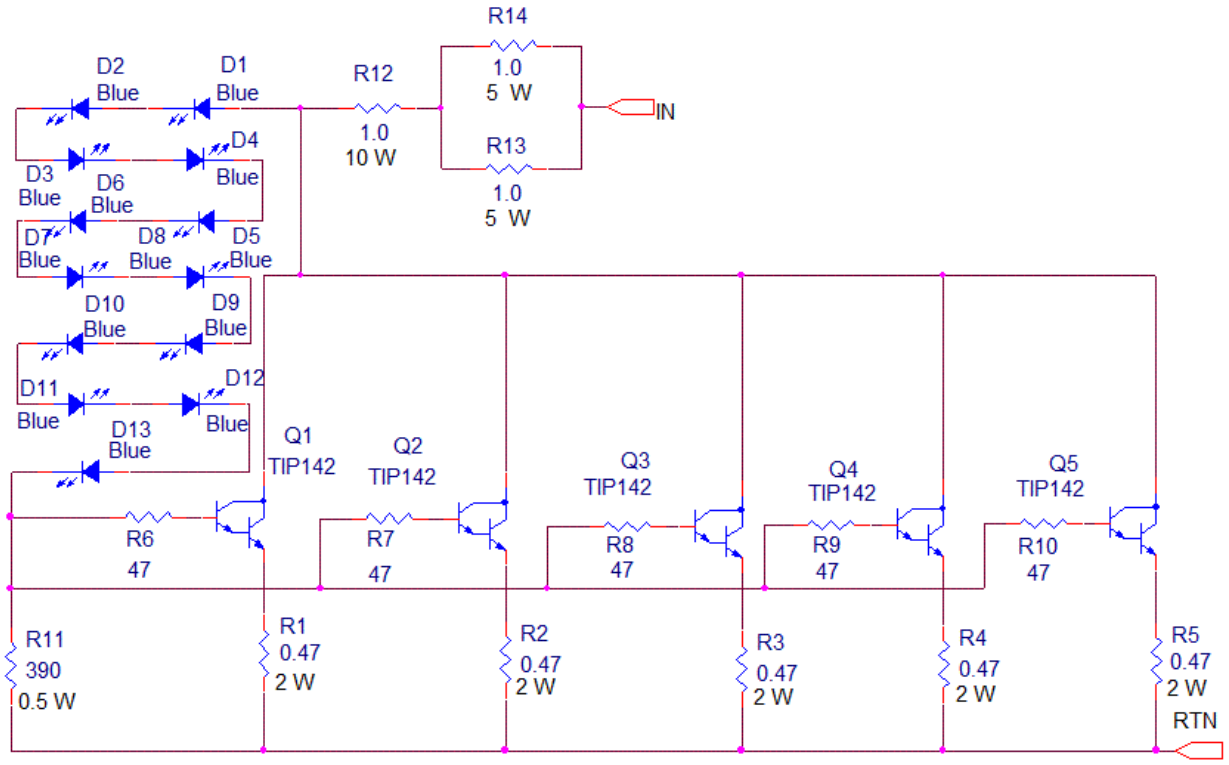


Figure 8 – Constant Voltage Load Schematic.

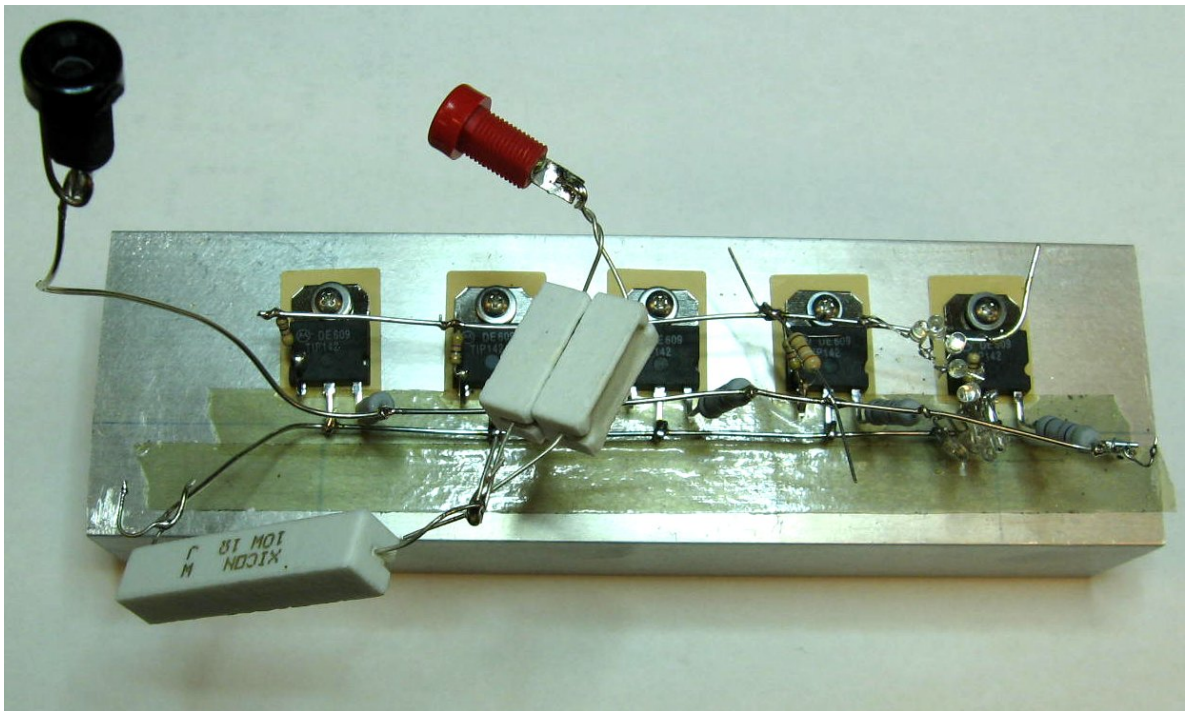


Figure 9 – Constant Voltage Load w./Heat Sink.

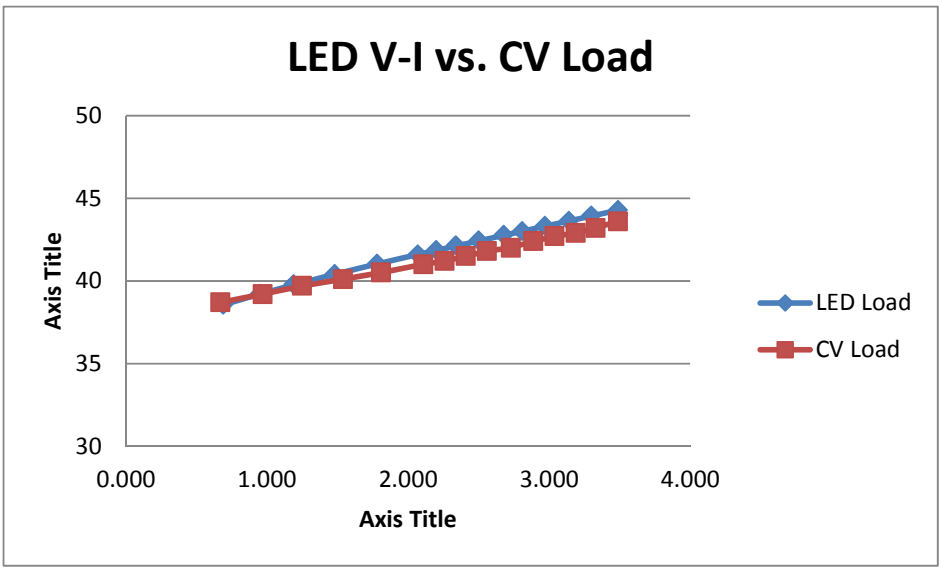


Figure 10 – Comparison of Streetlight LED Array V-I Characteristic with CV Load .

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

8 Magnetics

8.1 PFC Choke (L2) Specification

8.1.1 Electrical Diagram

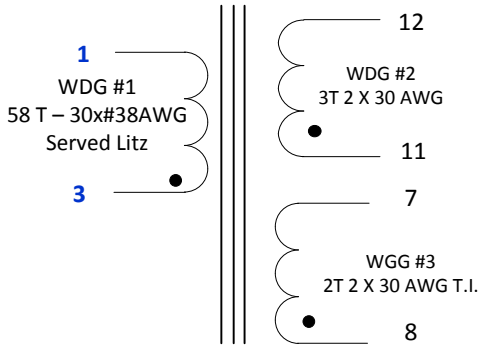


Figure 11 – PFC Choke Electrical Diagram.

8.1.2 Electrical Specifications

Inductance	Pins 1-3 measured at 100kHz, 0.4 RMS.	437 uH +5%
Resonant Frequency	Pins 1-3. N/A	kHz (Min.)

8.1.3 Materials

Item	Description
[1]	Core: TDK Core: PC44PQ32/20Z, gap for A_{LG} of **130** nH/T^2
[2]	Bobbin: BPQ32/20-112CPFR - TDK
[3]	Litz Wire: 30 x #38 AWG Single Coated Solderable, Served
[4]	Tape, Polyester Film: 3M 1350-F1 or equivalent, 9.0 mm wide
[5]	Magnet Wire, 30 AWG, Solderable Double Coated
[6]	Triple Insulated Wire, 30 AWG, Furukawa TEX-E or equivalent.
[7]	Varnish: Dolph BC-359, or equivalent.

8.1.4 PFC Inductor Build Diagram

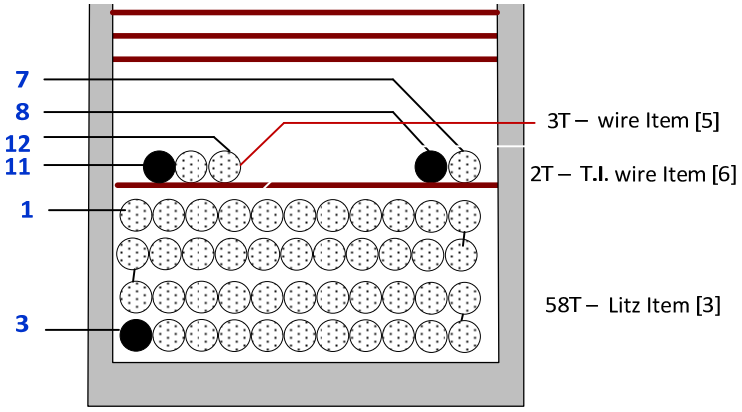


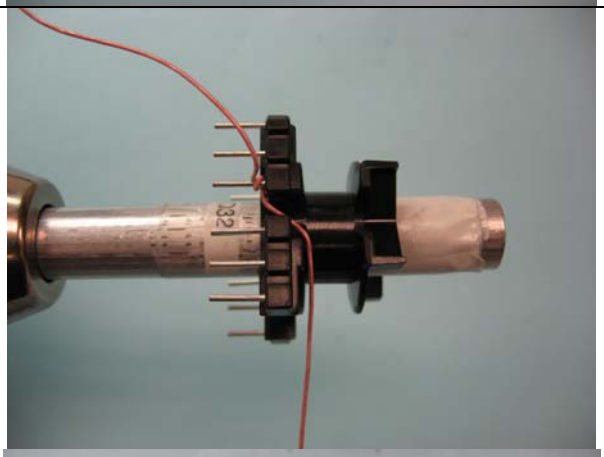
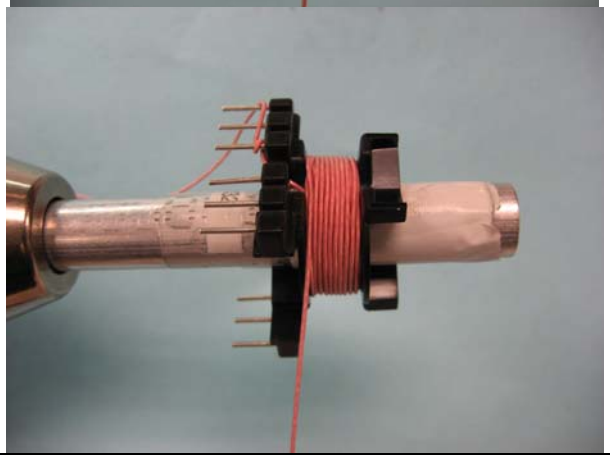
Figure 12 – PFC Inductor Build Diagram

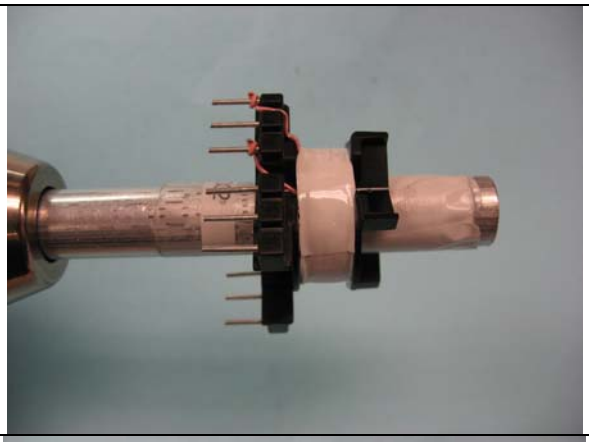
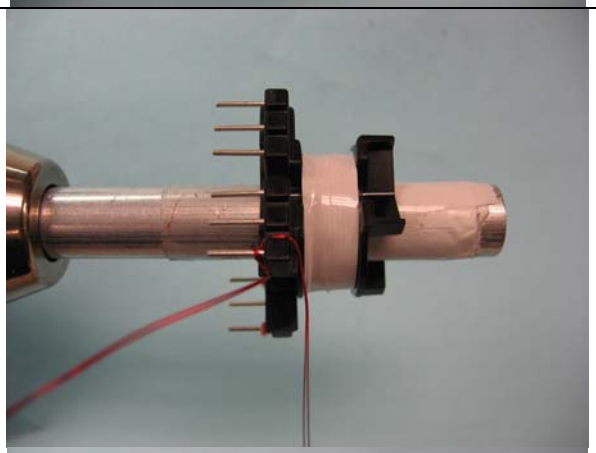
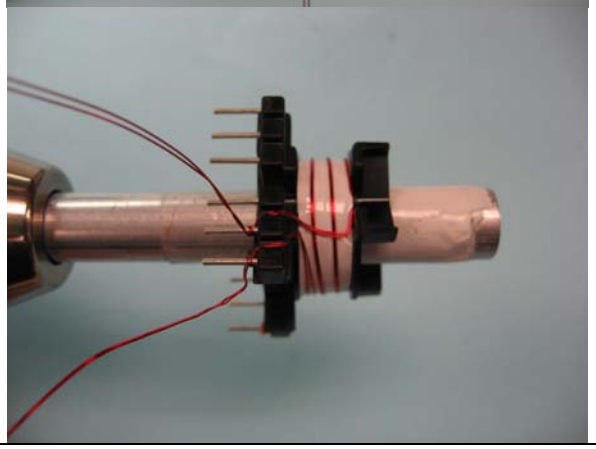
8.1..5 Winding Instructions

Winding preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 3, wind 58 turns of Litz wire item [3], finish at pin 1.
Insulation	Apply one layer of tape item [4]
Winding #2	Starting at Pin 11, wind 3 bifilar turns of wire, item [5]. Spread turns evenly across bobbin window. Finish at Pin 12.
Winding #3	Starting at Pin 8, wind 2 bifilar turns of wire, item [6], directly on top of previous winding. Spread turns evenly across bobbin window. Finish at Pin 7.
Insulation	Apply 3 layers of tape item [4].
Final Assembly	Grind both core to specified inductance. Secure core halves with tape. Remove pins 2,4, and 9. Dip Varnish with item [7].

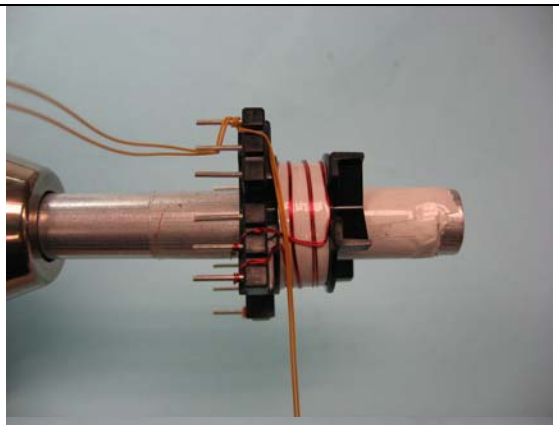
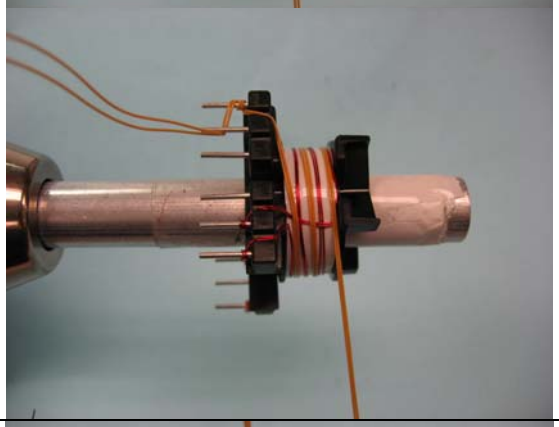
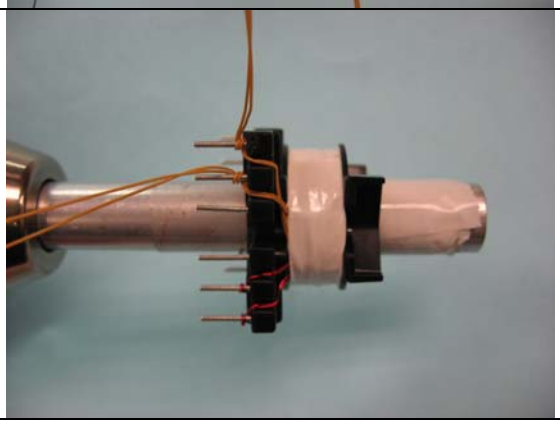
Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

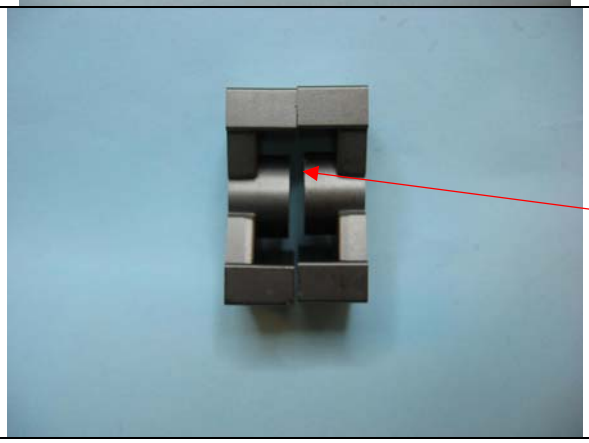
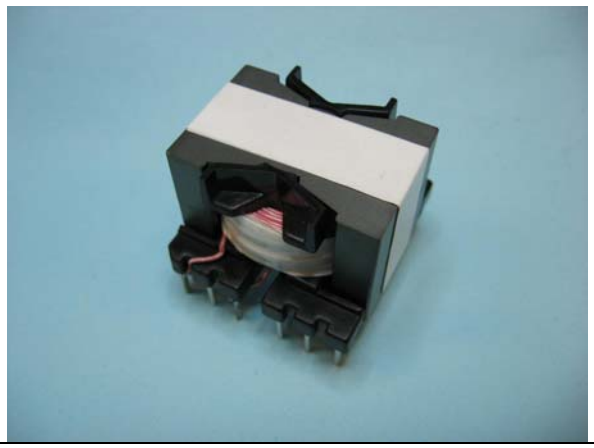
8.1..6 Winding Illustrations

Winding preparation		Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction
Winding 1	 	Starting at pin 3, wind 58 turns with 30x#38 served Litz wire, item [3].

Insulation		Apply 1 layer of insulating tape, item [4]. Terminate wire at pin 1
Winding 2	 	Starting at pin 11, wind 3 bifilar turns with 30AWG double coated wire, item [5]. Terminate wire at pin 12. Do not apply insulating tape to this winding.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Winding 3	 	Starting at pin 8, wind 2 bifilar turns with 30AWG triple insulated wire, item [6].
Insulation		Apply 3 layers of insulating tape, item [4]. Terminate wire at pin 7

Solder Terminations		Solder all wire terminations at pins 1, 3, 7, 8, 11, and 12
Core Grinding		Grind core for specified inductance.
Final Assembly		Secure core halves with tape. Remove pins 2, 4, and 9.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

8.2 LLC Transformer (T2) Specification

8.2.1 Electrical Diagram

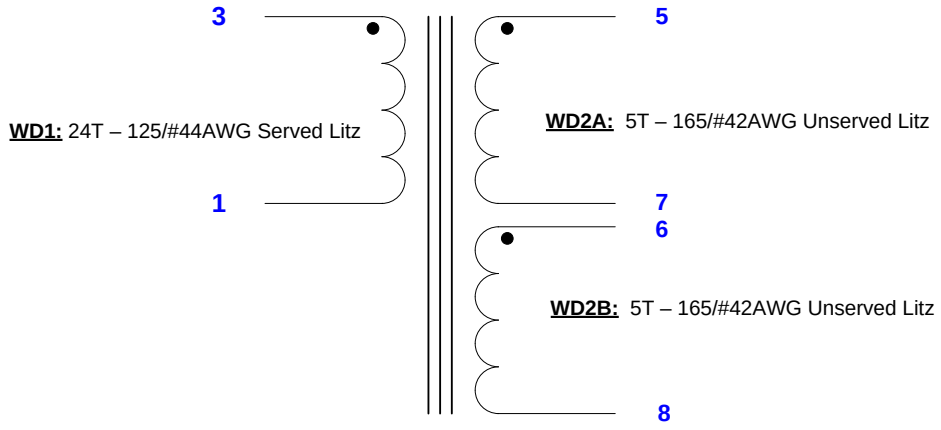


Figure 13 – LLC Transformer Schematic.

8.2.2 Electrical Specification

Electrical Strength	1 second, 60 Hz, from pins 1-6 to FL1, Fl2, FL3, FL4.	3000 VAC
Primary Inductance	Pins 2-5, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	270 µH, ±10%
Resonant Frequency	Pins 2-5, all other windings open	1800 kHz (Min)
Primary Leakage Inductance	Pins 2-5, with FL1, FL2, FL3, FL4 shorted, measured at 100 kHz, 0.4 V_{RMS}	34 µH ±5%

8.2.3 Materials

Item	Description
[1]	Core Pair: Itacoil NFEV25A, PW4 material, gap for A_{LG} of 470 nH/T^2
[2]	Bobbin: Itacoil RCEV25A.
[3]	Bobbin Cover, GSEV25A.
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 6.0mm wide
[5]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 7.0mm wide.
[6]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 12 mm wide.
[7]	Litz wire: 165/#42 Single Coated, Unserved .
[8]	Litz wire: 125/#44 Single Coated, Served.
[9]	Copper Tape, 3M-1181; or equivalent, 10 mm wide.
[10]	Wire, 20 AWG, Black, Stranded , UL 1015 Alpha 3073 BK or equivalent.

8.2.4 Build Diagram

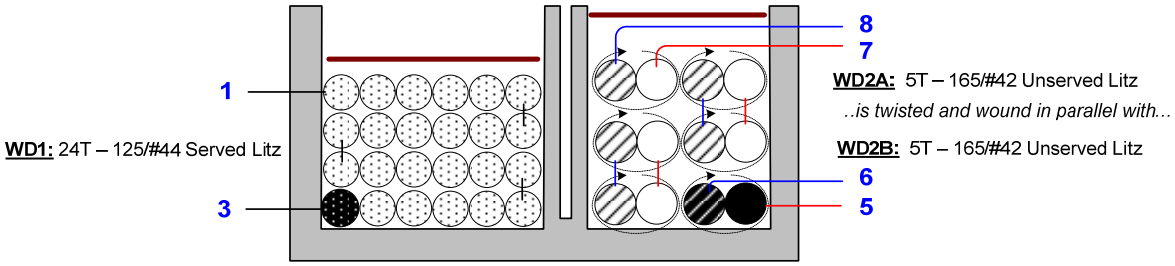


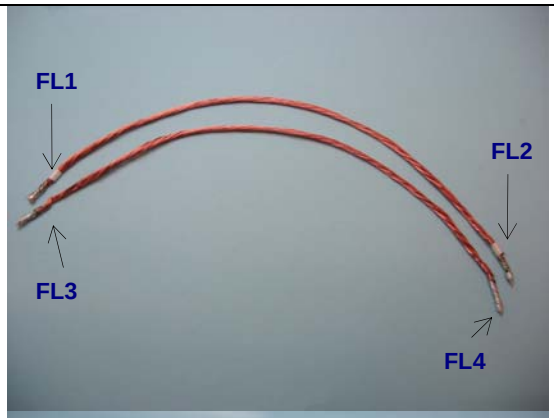
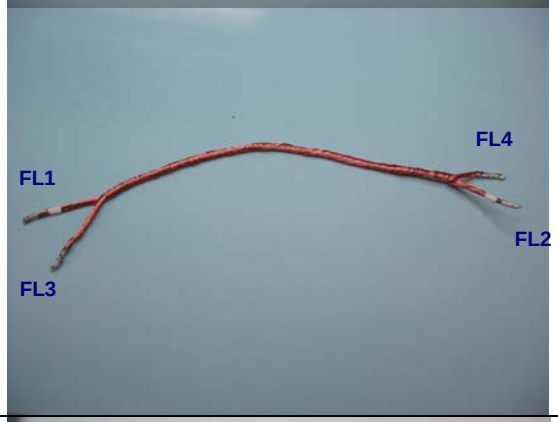
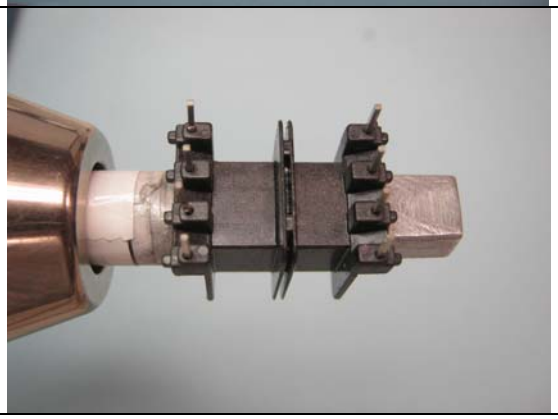
Figure 14 – LLC XFMR Build Diagram.

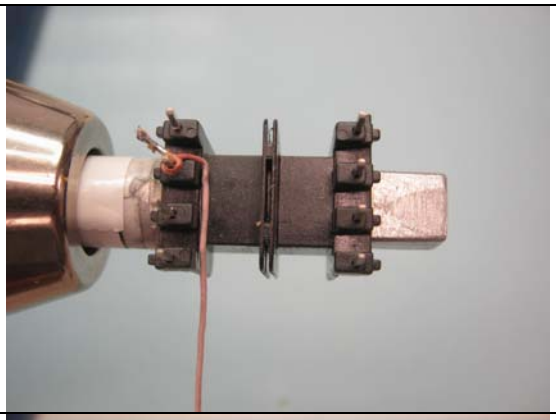
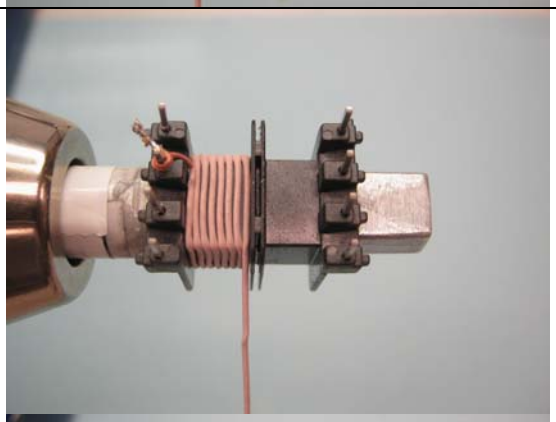
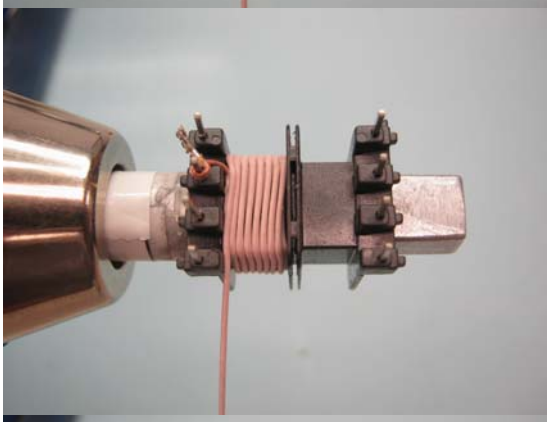
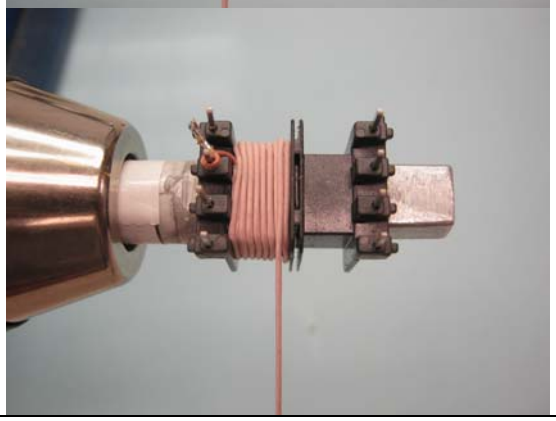
8.2.5 Winding Instructions

Secondary wire preparation	Prepare 2 strands of wire item [7] 10” length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1” free at each end. See pictures below.
WD1 (Primary)	Place the bobbin item [2] on the mandrel with primary chamber on the left side. Note: primary chamber is wider than secondary chamber. Starting on Pin 3, wind 24 turns of served Litz wire [7] in 3 ½ layers, and finish on Pin 1. Secure winding with one turn of tape [5].
WD2A & WD2B (Secondary)	Using unserved Litz assembly prepared in step 1, start with FL1 on Pins 5 and FL3 on Pin 6, tightly wind 5 turns in secondary chamber. Finish with FL2 on Pin 7 and FL4 on Pin 8. Secure winding with one turn of tape [4].
Bobbin Cover	Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish	Grind core halves [1] for specified inductance. Assemble and secure core halves. Remove Pin 4 of bobbin. Apply circumferential turn of copper tape [8] as shown, overlap ends, and solder. Solder 5” termination lead of stranded wire item [10] to core band as shown, secure with two turns of tape item [6].

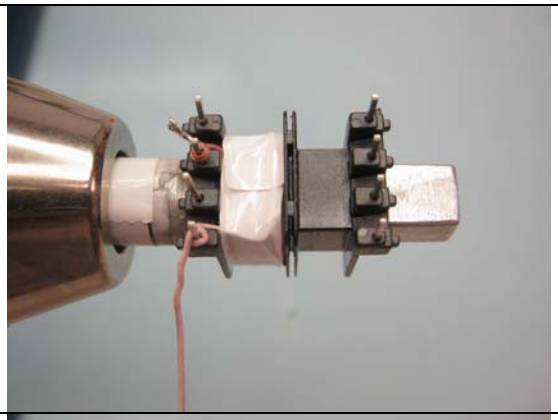
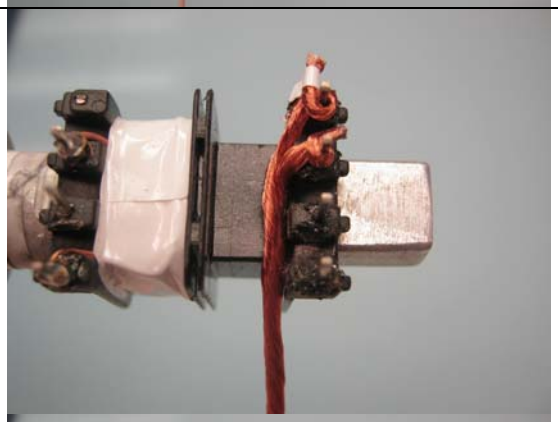
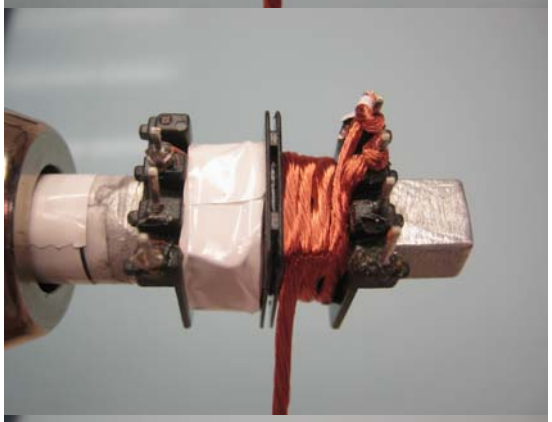
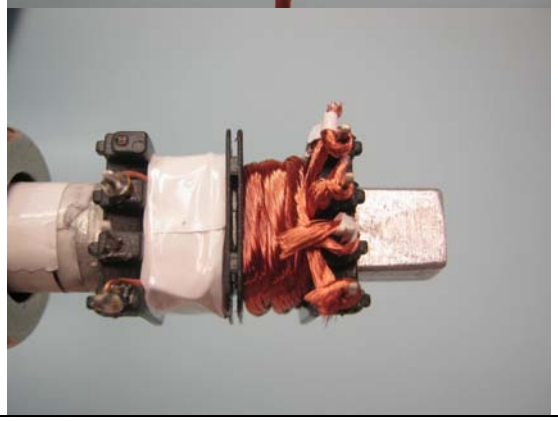
Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

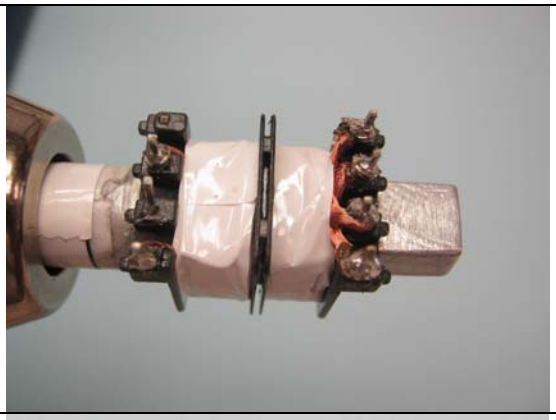
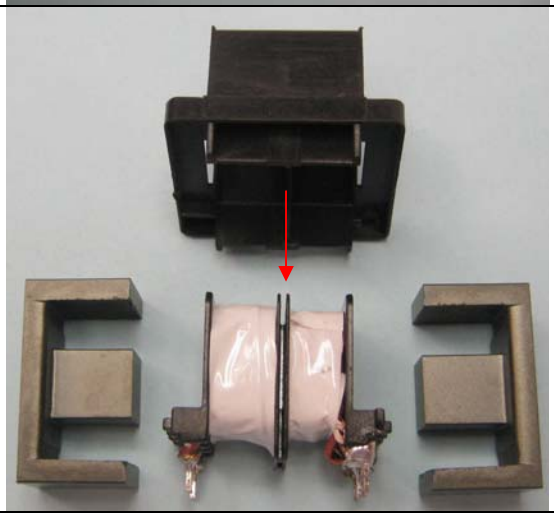
8.2.6 Winding Illustrations

Secondary wire preparation	 	Prepare 2 strands of wire item [7] 10” length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1” free at each end. See pictures below.  Video 1.wmv
WD1 (Primary)		Place the bobbin item [2] on the mandrel with primary chamber on the left side. Note: primary chamber is wider than secondary chamber. **Starting on Pin 3**

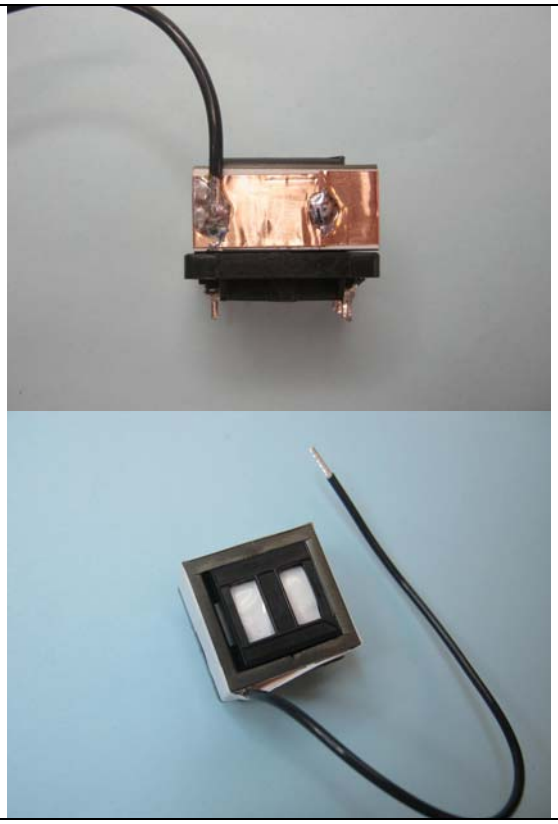
		
WD1 (Primary) (Cont'd)	  	wind 24 turns of served Litz wire [7] in 3 ½ layers, and finish on Pin 1. Secure winding with one turn of tape [5].

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

		
WD2A & WD2B (Secondary)	  	Using unserved Litz assembly prepared in step 1, start with FL1 on Pins 5 and FL3 on Pin 6, tightly wind 5 turns in secondary chamber. Finish with FL2 on Pin 7 and FL4 on Pin 8. Secure winding with one turn of tape [4].

		
Bobbin Cover		Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish)		Grind core halves [1] for specified inductance. Assemble and secure core halves. Remove Pin 4 of bobbin. Apply circumferential turn of copper tape [8] as shown, overlap ends, and solder. Solder 5” termination lead of stranded wire item [10] to core band as shown, secure with two turns of tape item [6].

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com



8.3 Output Inductor

8.3.1 Electrical Diagram

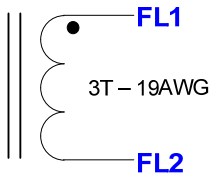


Figure 15 – Inductor Electrical Diagram.

8.3.2 Electrical Specifications

Inductance	Pins FL1 -FL2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	300 nH, ±15%

8.3.3 Material List

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26
[2]	Magnet wire: 19 AWG Solderable Double Coated

8.3..4 Construction Details

Figure 16 – Finished Part, Front View. Tin Leads to within ~ 1/8 “ of Toroid Body

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

9 PFC Design Spreadsheet

Hiper_PFS-II_Boost_042313; Rev.1.0; Copyright Power Integrations 2013	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Hiper_PFS-II_Boost_042313_Rev1-0.xls;**
Enter Applications Variables					**Design Title**
Input Voltage Range			**Universal**		Select Universal or High_Line option
VACMIN			90	V	Minimum AC input voltage
VACMAX			265	V	Maximum AC input voltage
VBROWNIN			76.69		Expected Minimum Brown-in Voltage
VBROWNOUT			68.33	V	Specify brownout voltage.
VO			385.00	V	Nominal Output voltage
PO	160.00		160.00	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	deg C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost c
KP	0.750	*Warning*	0.75		!!!Warning. KP is too high. Reduce KP to be
VO_MIN			365.75	V	Minimum Output voltage
VO_RIPPLE_MAX			20	V	Maximum Output voltage ripple
tHOLDUP	18.00		18	ms	Holdup time
VHOLDUP_MIN			310	V	Minimum Voltage Output can drop to during
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**no**		**no**		Enter "Yes" for Forced air cooling. Otherwis
PFS Parameters					
PFS Part Number	**PFS7326H**		**PFS7326H**		Selected PFS device
MODE	**EFFICIENCY**		**EFFICIENCY**		Mode of operation of PFS. For full mode ent
R_RPIN			49.9	k-ohms	R pin resistor value
C_RPIN			1.00	nF	R pin capacitor value
IOCP min			6.8	A	Minimum Current limit
IOCP typ			7.2	A	Typical current limit
IOCP max			7.5	A	Maximum current limit
RDSON			0.62	ohms	Typical RDSon at 100 'C
RV1			1.50	Mohms	Line sense resistor 1
RV2			1.50	Mohms	Line sense resistor 2
RV3			1.00	Mohms	Line sense resistor 3
C_VCC			3.30	uF	Supply decoupling capacitor
R_VCC			15.00	ohms	VCC resistor
C_V			22.00	nF	V pin decoupling capacitor
C_C			22	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333	V	Power good Vo lower threshold voltage
PGT set resistor			103.79	kohm	Power good threshold setting resistor

FS_PK			60.2	kHz	Estimated frequency of operation a
FS_AVG			50.2	kHz	Estimated average frequency of op
IP			3.97	A	MOSFET peak current
PFS_IRMS			1.67	A	PFS MOSFET RMS current
PCOND_LOSS_PFS			1.73	W	Estimated PFS conduction losses
PSW_LOSS_PFS			0.78	W	Estimated PFS switching losses
PFS_TOTAL			2.51	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction tem
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junc
HEATSINK Theta-CA			15.30	degC/W	Maximum thermal resistance of he
Basic Inductor Calculation					
LPFC			437	uH	Value of PFC inductor at peak of V
LPFC (0 Bias)			437	uH	Value of PFC inductor at No load. T
LP_TOL	5.00		5	%	Tolerance of PFC Inductor Value
LPFC_RMS			1.97	A	Inductor RMS current (calculated a
Inductor Construction Parameters					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Fer
Core Material	**Auto**		**PC44**		Select from 60u, 75u, 90u or 125 u material for Pow Iron cores.
Core Geometry	**Auto**		**PQ**		Select from Toroid or EE for Sendu
Core	**PQ32/20**		**PQ32/20**		Core part number
AE			170	mm^2	Core cross sectional area
LE			55.5	mm	Core mean path length
AL			6530	nH/t^2	Core AL value
VE			9.44	cm^3	Core volume
HT			5.12	mm	Core height/Height of window
MLT			67.1	cm	Mean length per turn
BW			8.98	mm	Bobbin width
NL			58		Inductor turns
LG			2.06	mm	Gap length (Ferrite cores only)
ILRMS			1.97	A	Inductor RMS current
Wire type	**LITZ**		**LITZ**		Select between "Litz" or "Regular"
AWG	40		40	AWG	Inductor wire gauge
Filar	50		50		Inductor wire number of parallel str
OD			0.079	mm	Outer diameter of single strand of v
AC Resistance Ratio			1.00		Ratio of AC resistance to the DC re

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

J		*Warning*	8.11	A/mm^2	!!! Warning Current density is too high and n
BP_TARGET			3500	Gauss	Target flux density at VACMIN (Ferrite cores
BM			1757	Gauss	Maximum operating flux density
BP			3487	Gauss	Peak Flux density (Estimated at VBROWNO
LPFC_CORE_LOSS			0.09	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			1.79	W	Estimated Inductor copper losses
LPFC_TOTAL LOSS			2	W	Total estimated Inductor Losses
FIT			79.81%	%	Estimated FIT factor for inductor
Layers			5.1		Estimated layers in winding
Critical Parameters					
IRMS			1.91	A	AC input RMS current
IO_AVG			0.42	A	Output average current
Output Diode (DO)					
Part Number	**Auto**		**INTERNAL**		PFC Diode Part Number
Type			SPECIAL		Diode Type - Special - Diodes specially cate recovery type
Manufacturer			PI		Diode Manufacturer
VRRM			600	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
TRR			31	ns	Diode Reverse recovery time
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			0.61	W	Estimated Diode conduction losses
PSW_DIODE			0.16	W	Estimated Diode switching losses
P_DIODE			0.77	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperatu
Rth-JS			3.85	degC/W	Maximum thermal resistance (Junction to he
HEATSINK Theta-CA			15.30	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
CO	**120**		**120.00**	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			11.9	V	Expected ripple voltage on Output with sele
T_HOLDUP_EXPECTED			19.5	ms	Expected holdup time with selected Output
ESR_LF			1.38	ohms	Low Frequency Capacitor ESR
ESR_HF			0.55	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.29	A	Low Frequency Capacitor RMS current
IC_RMS_HF			0.85	A	High Frequency Capacitor RMS current

CO_LF_LOSS			0.12	W	Estimated Low Frequency ESR los
CO_HF_LOSS			0.39	W	Estimated High frequency ESR los
Total CO LOSS			0.51	W	Total estimated losses in Output C
Input Bridge (BR1) and Fuse (F1)					
I^2t Rating			8.43	A^2s	Minimum I^2t rating for fuse
Fuse Current rating			3.00	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode d
IAVG			1.86	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridg
PCOND_LOSS_BRIDGE			3.10	W	Estimated Bridge Diode conduction
CIN			0.47	uF	Input capacitor. Use metallized pol
RT			9.37	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
Feedback Components					
R1			1.5	Mohms	Feedback network, first high voltag
R3			1.6	Mohms	Feedback network, third high volta
R2			787	kohms	Feedback network, second high vo
C1			47	nF	Feedback network, loop speedup c
R4			60.4	kohms	Feedback network, lower divider re
R6			487	kohms	Feedback network - pole setting re
R7			6.34	kohms	Feedback network - zero setting re
C2			47	nF	Feedback component- noise suppr
R5			3.00	kohms	Damping resistor in serise with C3
C3			2.2	uF	Feedback network - compensation
D1			BAV116		Feedback network - capacitor failu
Loss Budget (Estimated at VACMIN)					
PFS Losses			2.51	W	Total estimated losses in PFS
Boost diode Losses			0.77	W	Total estimated losses in Output D
Input Bridge losses			3.10	W	Total estimated losses in input brid
Inductor losses			1.88	W	Total estimated losses in PFC chok
Output Capacitor Loss			0.51	W	Total estimated losses in Output ca
Total losses			8.77	W	Overall loss estimate
Efficiency			0.95		Estimated efficiency at VACMIN. V

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

10 LLC Transformer Design Spreadsheet

HiperLCS_040312; Rev.1.3; Copyright Power Integrations 2012	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_040312_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					**Design Title**
Vbulk_nom			380	V	Nominal LLC input voltage
Vbrownout	287		287	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			362	V	Startup threshold on bulk capacitor
VOV_shut			476	V	OV protection on bulk voltage
VOV_restart			459	V	Restart voltage after OV protection.
CBULK	120.00		120	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			23.8	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	43.00		43.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	3.50		3.5	A	Main output maximum current
VD1	0.70		0.70	V	Forward voltage of diode in Main output
PO1			151	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			151	W	Specified LLC output power
LCS Device Selection					
Device	**LCS702**		**LCS702**		LCS Device
RDS-ON (MAX)			1.39	ohms	RDS-ON (max) of selected device
Coss			250	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.6	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			104	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature

Theta HS-A		26	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)				
Vres_target	380	380	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po		153	W	LLC output power including diode loss
Vo		43.70	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target		250	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar		236	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	270.00	270	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom
Lres	34.00	34.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio		6.9		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	10.00	10.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec		11.719	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m		50	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq		4.49		Turns ratio of LLC equivalent circuit ideal transformer
Npri	24.0	24.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	5.0	5.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted		242	kHz	Expected frequency at nominal input voltage

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

			and full load; Heavily influenced by n_eq and primary turns
f_res	273	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout	160	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par	97	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion	131	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion	230	V	LLC full load gain inversion point input voltage
Vres_expected Warning	392	V	
RMS Currents and Voltages			
IRMS_LLC_Primary	1.06	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current	2.7	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current	1.6	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current	0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current	0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms	70	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)			
New primary turns	24.0		Trial transformer primary turns; default value is from resonant section
New secondary turns	5.0		Trial transformer secondary turns; default value is from resonant section
New Lpri	270	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres	10.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above
New estimated Lres	34.0	uH	Trial transformer estimated Lres
New estimated Lpar	236	uH	Estimated value of Lpar for trial transformer
New estimated Lsec	11.719	uH	Estimated value of secondary leakage inductance
New Kratio	6.9		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio	4.49		Estimated effective transformer turns ratio
V powertrain inversion new	230	V	Input voltage at LLC full load gain inversion point

f_res_trial		273	kHz	New Series resonant frequency
f_predicted_trial		242	kHz	New nominal operating frequency
IRMS_LLC_Primary		1.06	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current		2.7	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current		1.6	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current		2.7	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current		0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial	Warning	392	V	!!! Warning. Vres_expected_trial is more than 3% away from target value. Adjust New Primary turns or New Lpri to fix this problem

Transformer Core Calculations (Calculates From Resonant Parameter Section)

Transformer Core	**Auto**	**EEL25**		**Transformer Core**
Ae	0.76	0.76	cm^2	Enter transformer core cross-sectional area
Ve	5.35	5.35	cm^3	Enter the volume of core
Aw		107.9	mm^2	Area of window
Bw	15.50	15.5	mm	Total Width of Bobbin
Loss density		200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT	5.20	5.2	cm	Mean length per turn
Nchambers	2	2		Number of Bobbin chambers
Wsep	1.60	1.6	mm	Winding separator distance (will result in loss of winding area)
Ploss		1.1	W	Estimated core loss
Bpkfmin		180	mT	First Quadrant peak flux density at minimum frequency.
BAC		238	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding				
Npri		24.0		Number of primary turns; determined in LLC resonant section
Primary gauge	44	44	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge		0.050	mm	Equivalent diameter of wire in metric units
Primary litz strands	125	125		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor		50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P		48	mm^2	Winding window area for primary
Fill Factor		20%	%	% Fill factor for primary winding (typical max

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

				fill is 60%)
Resistivity_25 C_Primary		75.42	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C		94.12	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C		126.13	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current		1.06	A	Measured RMS current through the primary winding
ACR_Trf_Primary		195.24	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss		0.22	W	Total primary winding copper loss at 85 C
Primary Layers		2.50		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)				**Note - Power loss calculations are for each winding half of secondary**
Output Voltage		43.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns		5.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)		2.7	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)		1.75	A	DC component of winding current
Winding current (AC RMS component)		2.08	A	AC component of winding current
Sec 1 Wire gauge		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge		0.060	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	165	165		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1		35.93	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1		9.34	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1		12.52	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1		0.31	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1		12.70	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1		0.11	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses		0.42	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current		1.6	A	Output capacitor RMS current
Co1		1.7	uF	Secondary 1 output capacitor
Capacitor ripple voltage		3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current		2.7	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current

Secondary 1 Layers	1.00		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)			**Note - Power loss calculations are for each winding half of secondary**
Output Voltage	0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns	0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)	2.7	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)	0.0	A	DC component of winding current
Winding current (AC RMS component)	0.0	A	AC component of winding current
Sec 2 Wire gauge	42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge	0.060	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2	59292.53	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT	5.20	cm	Mean length per turn
DCR_25C_Sec2	0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2	0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1	0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2	0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2	0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses	0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current	0.0	A	Output capacitor RMS current
Co2	N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage	N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current	0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers	1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations			**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)	0.22	W	Total primary winding copper loss at 85 C
Secondary copper Loss	0.42	W	Total copper loss in secondary winding
Transformer total copper loss	0.64	W	Total copper loss in transformer (primary + secondary)
AW_S	48.38	mm^2	Area of window for secondary winding
Secondary Fill Factor	16%	%	% Fill factor for secondary windings; typical

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

				max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values				
f_min		160	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time		320	ns	Dead time
Burst Mode	**1**	**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max		847	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start		382	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop		437	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor		6.79	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor		129	k-ohms	Resistor from DT/BF pin to G pin
Rstart		5.79	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay		0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin		44.3	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart		0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto		1.2	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	19.60	19.6	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor		2.93	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit				
Slow current limit		2.49	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit		4.49	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor		47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor		42.9	ohms	LLC current sense resistor, senses current in sense capacitor

IS pin current limit resistor	220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor	1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency	724	kHz	This pole attenuates IS pin signal
Loss Budget			
LCS device Conduction loss	1.6	W	Conduction loss at nominal line and full load
Output diode Loss	2.5	W	Estimated diode losses
Transformer estimated total copper loss	0.64	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss	1.1	W	Estimated core loss
Total transformer losses	1.7	W	Total transformer losses
Total estimated losses	5.7	W	Total losses in LLC stage
Estimated Efficiency	96%	%	Estimated efficiency
PIN	156	W	LLC input power

11 Heat Sinks

11.1 Primary Heat Sink

11.1.1 Primary Heat Sink Sheet Metal

11.1.2 Primary Heat Sink w/Fasteners

11.1.3 Primary Heat Sink Assembly

11.2 Secondary heat Sink

11.2.1 Secondary heat Sink Sheet Metal

11.2.2 Secondary Heat Sink w/ Fasteners

11.2.3 Secondary Heat Sink Assembly

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

12 RD-292 Performance Data

All measurements were taken at room temperature and 60 Hz input frequency unless otherwise specified. Output voltage measurements were taken at the output connectors.

12.1 LLC Stage Efficiency

To make this measurement, the LLC stage was supplied by connecting an external 380 VDC source across bulk capacitor C924, with a 2-channel bench supply to source the primary and secondary bias voltages. The output of the supply was used to power the LED streetlight described in Section 7, and the dimming input of the supply was used to program the current delivered to this load in order to vary the output power.

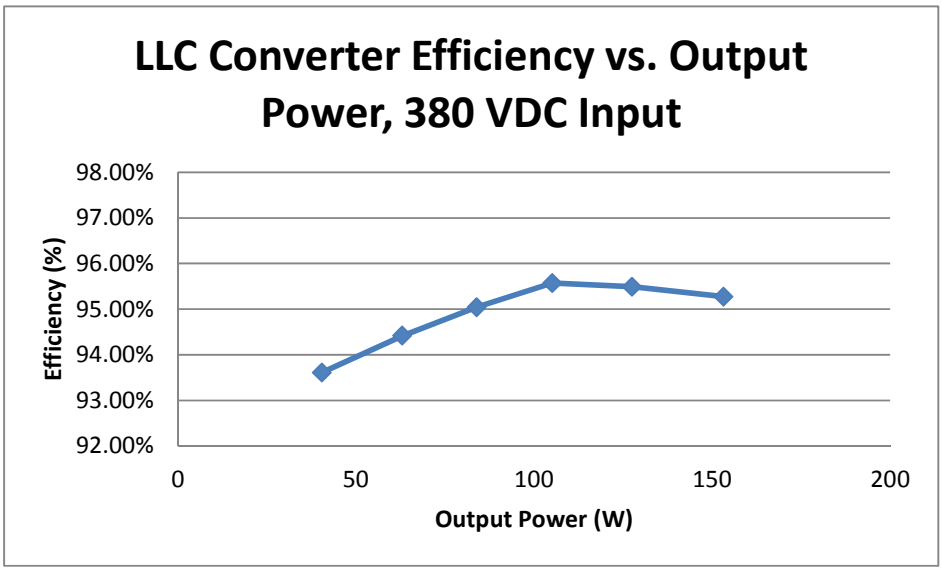


Figure 17 – LLC Stage Efficiency vs. Load, 380 VDC Input

12.2 Total Efficiency

Figures below show the total supply efficiency (PFC and LLC stages). AC input was supplied using a sine wave source. The output was loaded with an electronic load set for constant resistance, with the load adjusted for maximum output current and 43V output voltage.

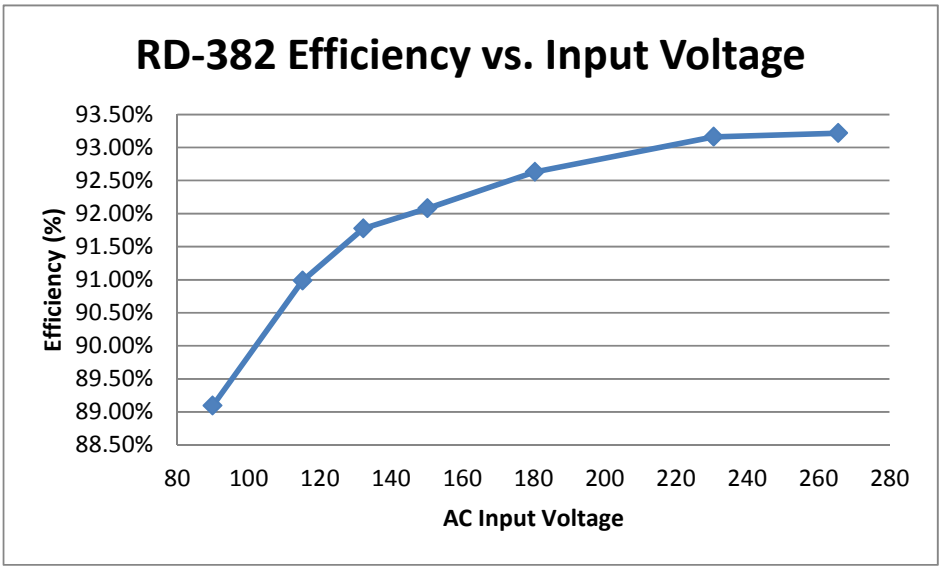


Figure 18 – Total Efficiency vs. Input Voltage, 100% Load.

12.3 Power Factor

Power factor measurements were made using a sine wave AC source and a constant resistance electronic load as described in section 10.2.

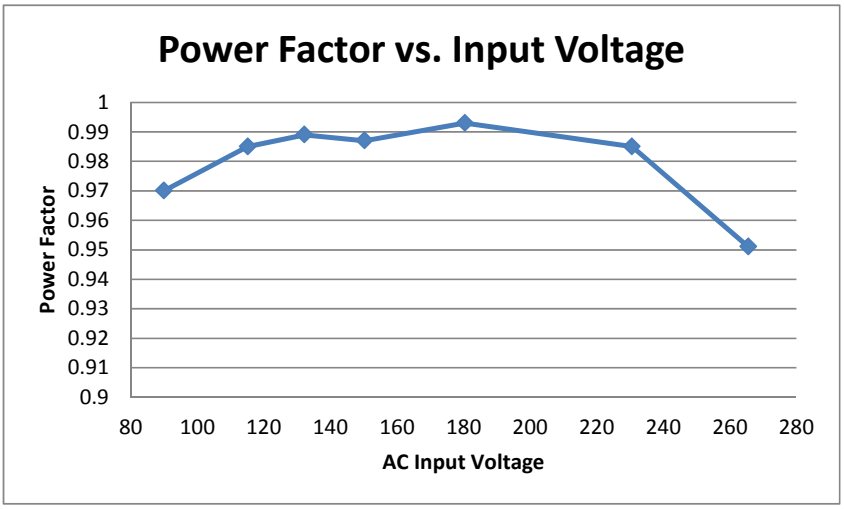


Figure 19 – Power Factor vs. Input Voltage,100% Load

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

12.4 Harmonic Distribution

Input current harmonic distribution was measured using a sine wave source and an LED load (Section 7).

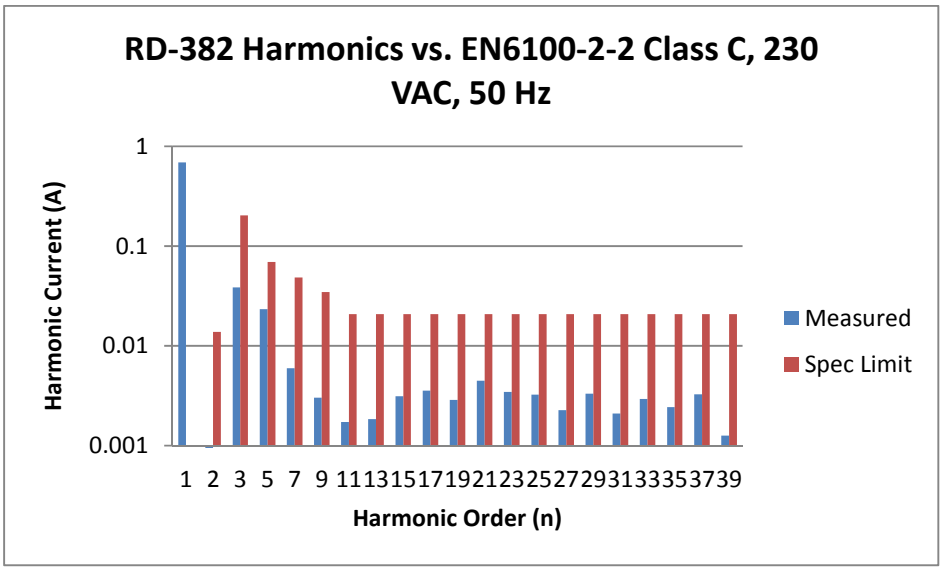


Figure 20 - Input Current Harmonic Distribution, 230 VAC/50 Hz Input, 100% Load.

12.5 THD, 100% Load

Vin	Frequency	THD (%)
115 VAC	60 Hz	8.30%
230 VAC	50 Hz	7.38 %

12.6 Output Current vs. Dimming Input Voltage

Output dimming characteristics were measured using a sine wave AC source and the streetlight LED array described in Section 7. Dimming voltage was provided using a bench supply.

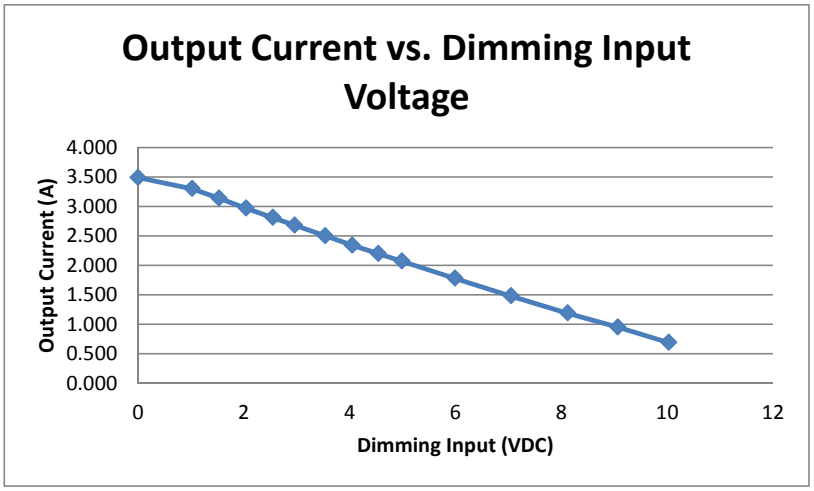


Figure 21 – DER-382 Output Current vs. Dimming Voltage.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

13 Waveforms

13.1 Input Current, 100% Load

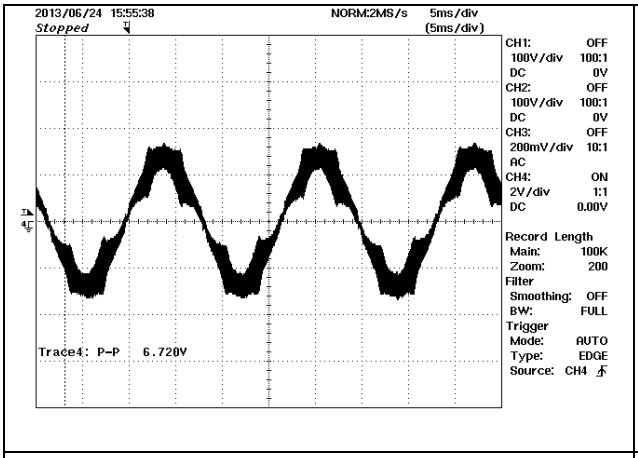


Figure 22 – 90 VAC, 150 W Load.
Upper – Input Current, 2 A/div.
Lower – Input Voltage, 100 V, 5 ms/div

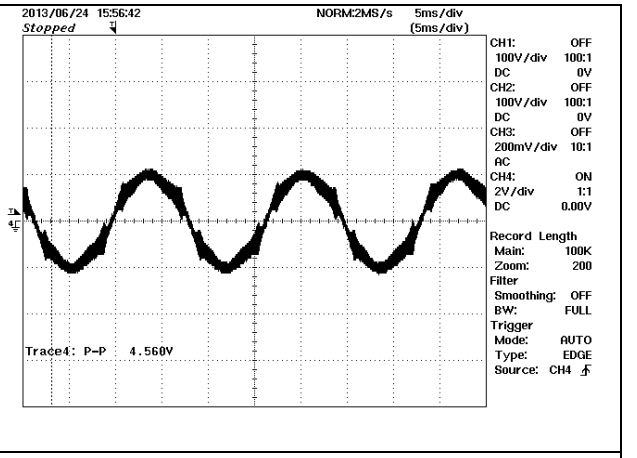


Figure 23 – 115 VAC, 150 W Load.
Upper – Input Current, 2 A/div.
Lower – Input Voltage, 100 V, 5 ms/div

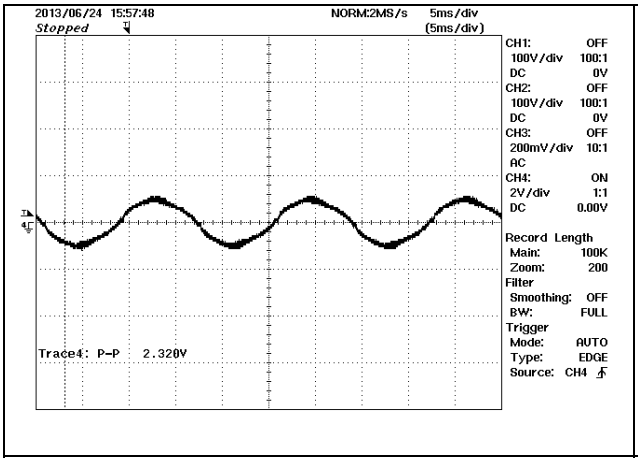


Figure 24 – 230 VAC, 150 W Load.
Upper – Input Current, 2 A/div.
Lower – Input Voltage, 100 V, 5 ms/div

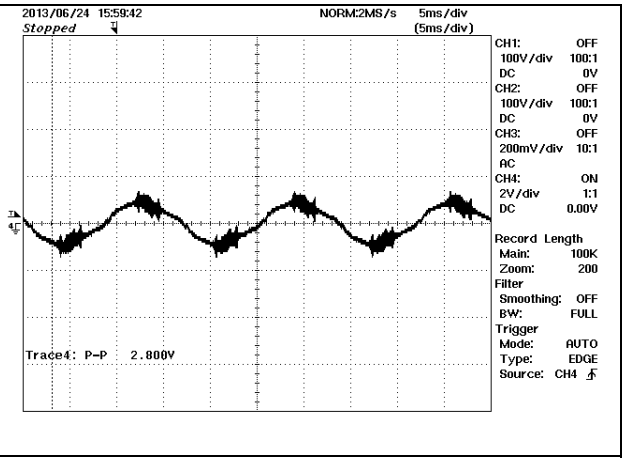


Figure 25 – 265 VAC, 150 W Load.
Upper – Input Current, 2 A/div.
Lower – Input Voltage, 100 V, 5 ms/div

13.2 LLC Primary Voltage and Current

The LLC stage current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C30 that measures the LLC transformer (T2) primary current. The output was loaded with an electronic load set for constant resistance, with the load adjusted for maximum output current and 43V output voltage.

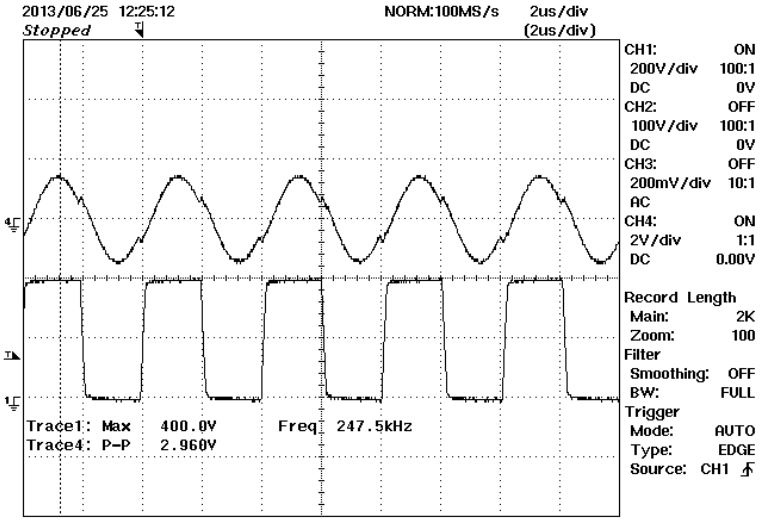


Figure 26 – LLC Stage Primary Voltage and Current., 100% Load
Upper – Current, 2 A/div.
Lower – Voltage, 200 V, 2 μs/div.

13.3 Output Rectifier PRV

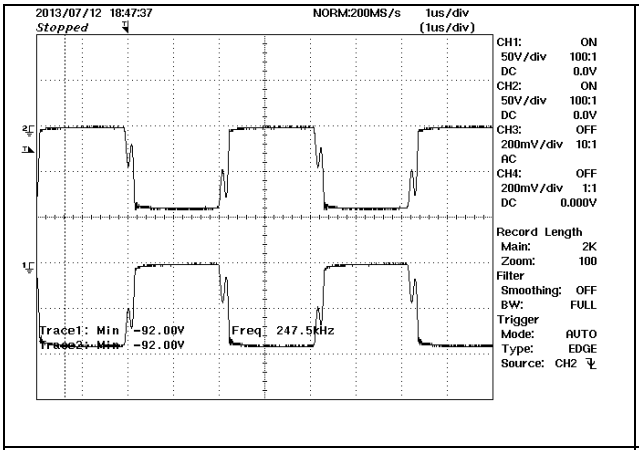


Figure 27 – Output Rectifier (D11) Reverse Voltage, 100% Load. Top and Bottom Traces Show Voltages on Each Half of D11.

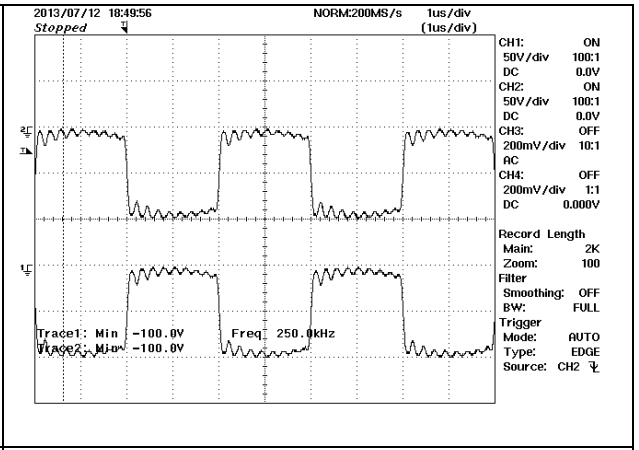


Figure 28 – Output Rectifier (D11) Reverse Voltage, Zero Load. Top and Bottom Traces Show Voltages on Each Half of D11.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

PFC Inductor/Switch Voltage and Current, 100% Load

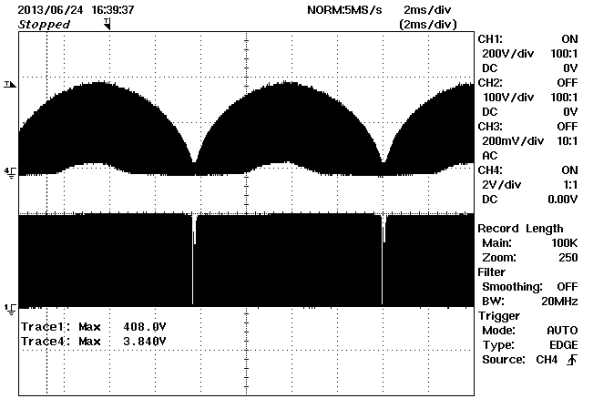


Figure 29 – PFC Stage Drain Voltage and Current, Full Load, 115 VAC
Upper – Drain/Inductor Current, 1 A/div.
Lower – Drain Voltage, 200 V, 2 ms/div.

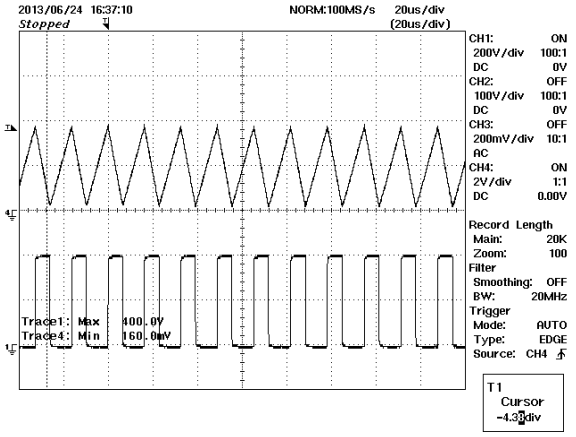


Figure 30 – PFC Stage Drain Voltage and Current, Full Load, 115 VAC.
Upper – Drain/Inductor Current, 1 A/div.
Lower – Drain Voltage, 200 V, 10 µs/div.

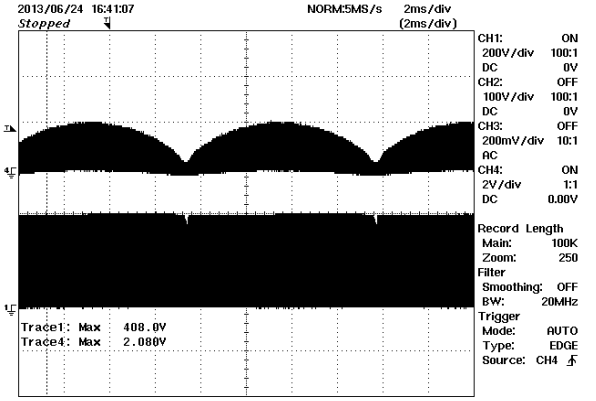


Figure 31 – PFC Stage Drain Voltage and Current, Full Load, 230 VAC.
Upper – Drain/Inductor Current, 1 A/div.
Lower – Drain Voltage, 200 V, 2 ms/div.

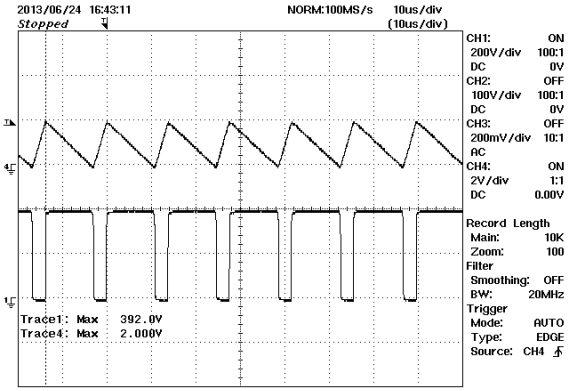


Figure 32 – PFC Stage Drain Voltage and Current, Full Load, 230 VAC.
Upper – Drain/Inductor Current, 1 A/div.
Lower – Drain Voltage, 200 V, 10 µs/div.

13.4 AC Input Current and PFC Output Voltage during Start-up

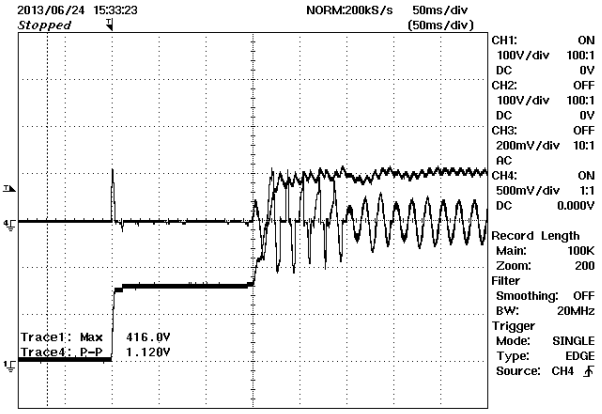


Figure 33 – AC Input Current vs. PFC Output Voltage at Startup, Full Load, 115 VAC.
Top Trace - AC Input Current, 2 A/div.
Bottom Trace – PFC Voltage, 200 V, 20 ms/div

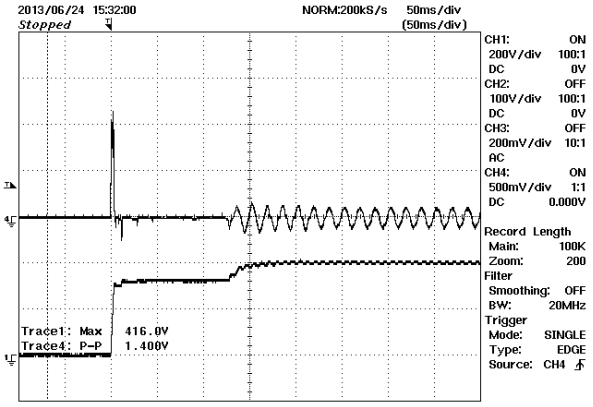


Figure 34 – AC Input Current vs. PFC Output Voltage at Startup, Full Load, 230 VAC.
Top Trace, AC Input Current, 2A/div.
Bottom Trace – PFC Voltage, 200 V, 20 ms/div.

13.5 LLC Start-up Into LED Load

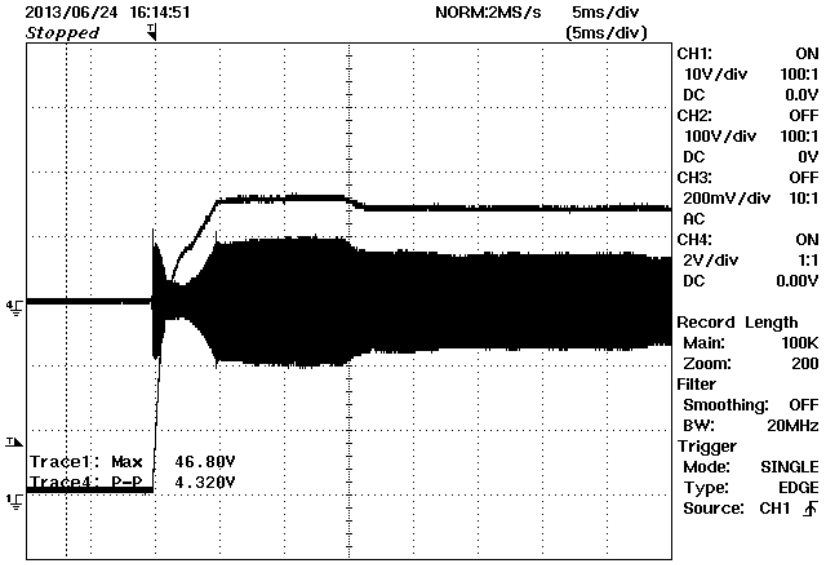


Figure 35 – LLC Startup. 115 VAC, 100% Load
Upper – LLC Primary Current, 2 A/div.
Lower – LLC Output Voltage, 10V, 5 ms/div.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

13.6 Output Voltage/Current Startup into LED Load

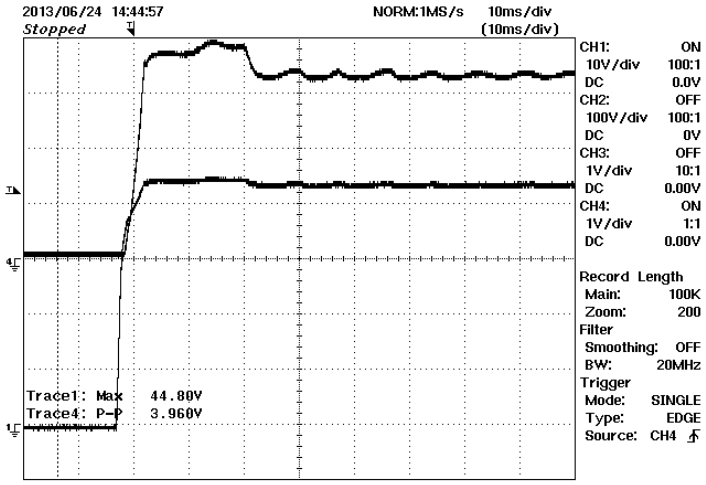


Figure 36 – LLC Startup. 115 VAC, 100% Load, LED Load. Upper Trace – LLC Output Current, 1 A/div. Lower Trace – LLC Output Voltage, 10V, 10 ms/div.

10.7 LLC Output Short-Circuit

The figure below shows the effect of an output short circuit on the LLC primary current and on the output current. A mercury displacement relay was used to short the output to get a fast, bounce-free connection.

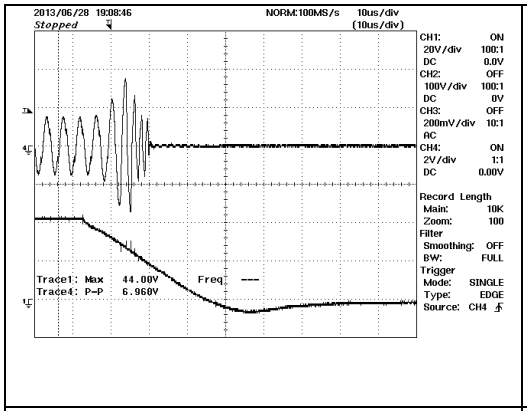


Figure 37 – Output Short Circuit Test Upper – LLC Primary Current, 2 A/div. Lower – LLC Output, 20V, 10 µs/div.

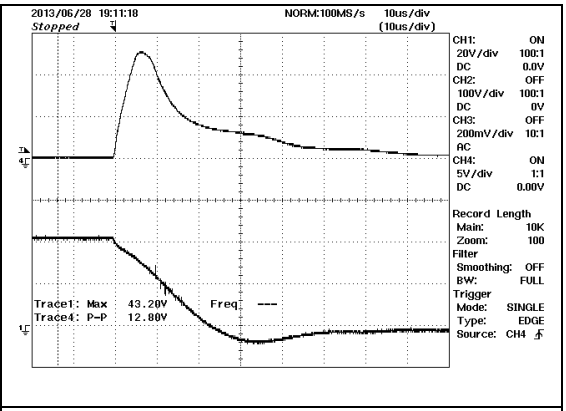


Figure 38 – Output Short Circuit Test Upper – LLC Output Current, 50 A/div. Lower – LLC Output, 20V, 10 µs/div.

13.7 Output Ripple Measurements

10.7.1 Ripple Measurement Technique

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

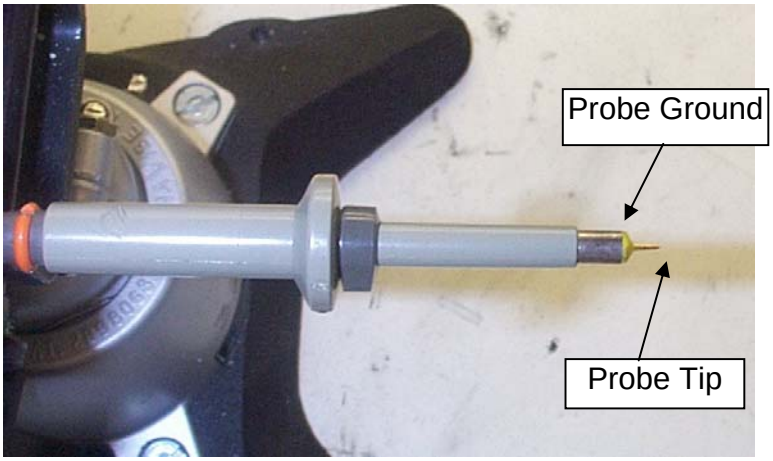


Figure 39 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

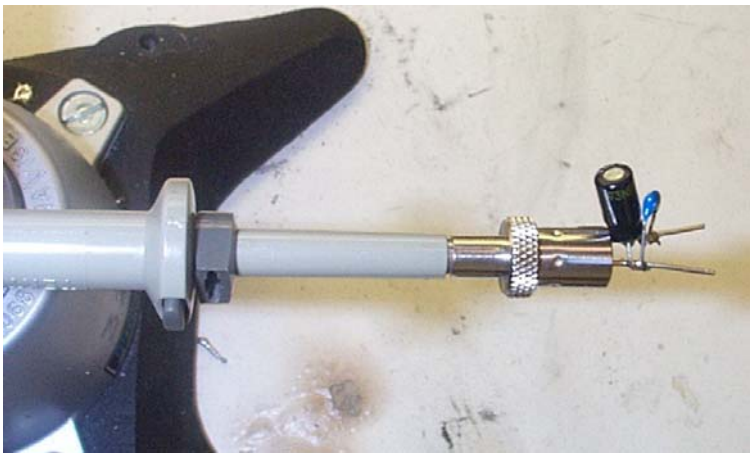


Figure 40 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

10.7.2 Ripple Measurements

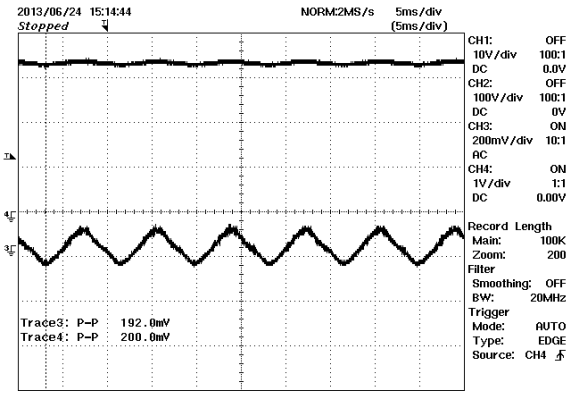


Figure 41 – 48 V Output Ripple, Full Load, 115 VAC. Upper Trace – Output Current, 1A/div. Lower Trace – Output Voltage Ripple, 200 mV, 5 ms/div

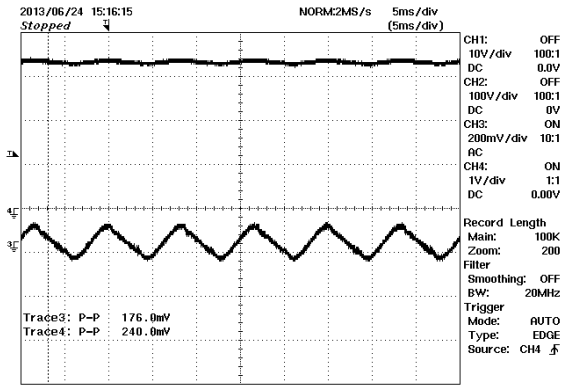


Figure 42 – 48 V Output Ripple, Full Load, 115 VAC. Upper Trace – Output Current, 1A/div. Lower Trace – Output Voltage Ripple, 200 mV, 5 ms/div

14 Temperature Profiles

The board was operated at room temperature, with output set at maximum using a constant resistance load. For each test condition the unit was allowed to thermally stabilize (~1 hr) before measurements were made.

14.1 90 VAC, 60 Hz, 150 W Output

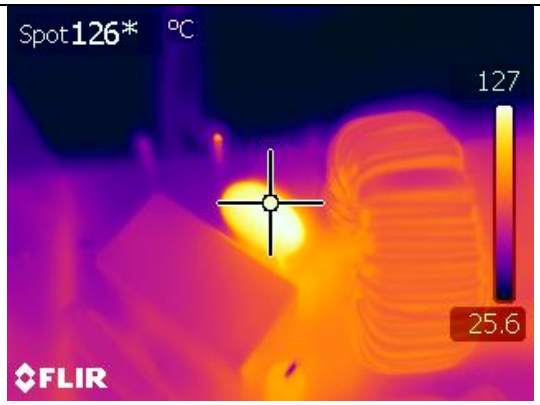


Figure 43 – Inrush Limiting Thermistor (RT1), 90VAC Input, 100% Load, Room Temperature.

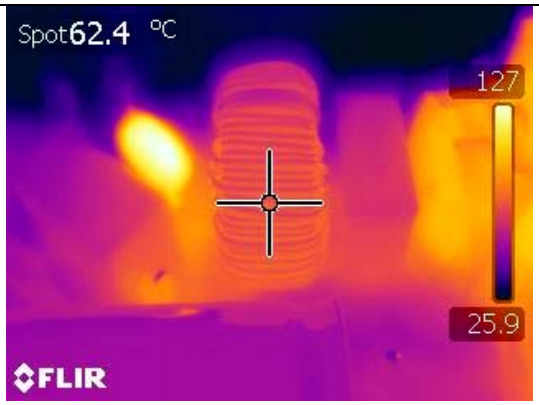


Figure 44 – Common Mode Choke (L1), 90 VAC Input, 100% Load, Room Temperature.

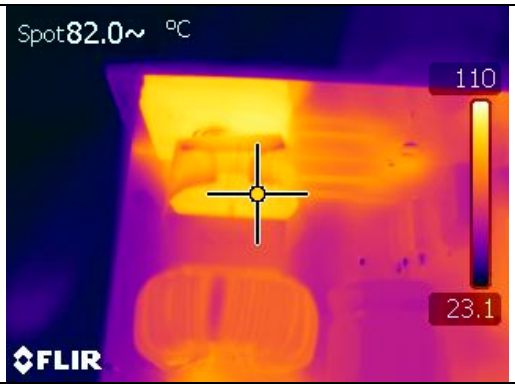


Figure 45 – Differential Mode Choke (L4), 90 VAC Input, 100% Load, Room Temperature.

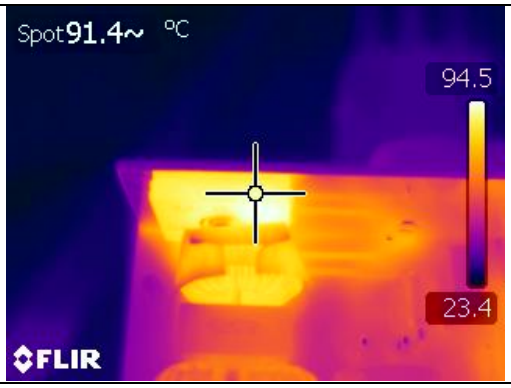


Figure 46 – Input Rectifier Bridge (BR1), 90 VAC Input, 100% Load, Room Temperature.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

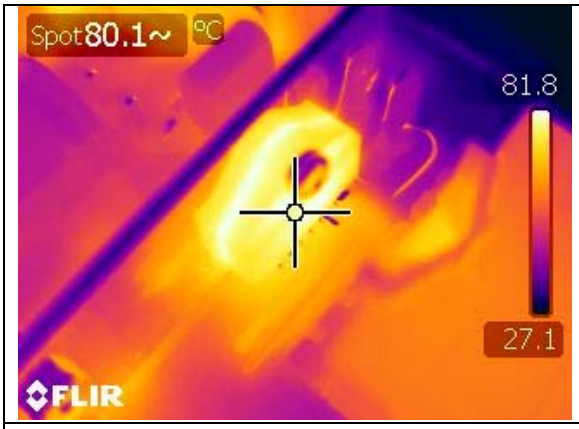


Figure 47 – PFC IC (U7), 90 VAC Input, 100% Load, Room Temperature.

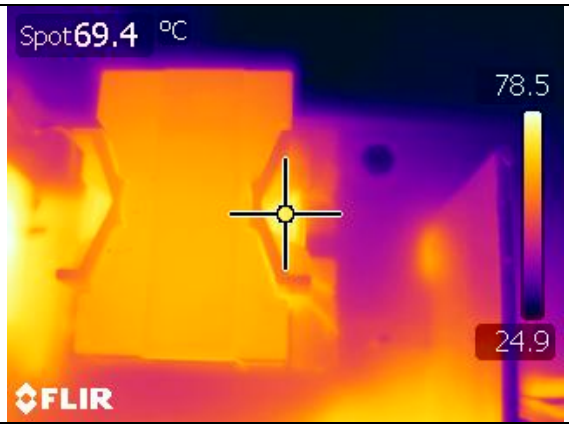


Figure 48 - PFC Inductor (T3), 90 VAC Input, 100% Load, Room Temperature.

Figure 49 – LLC IC (U3), 90 VAC Input, 100% Load, Room Temperature.

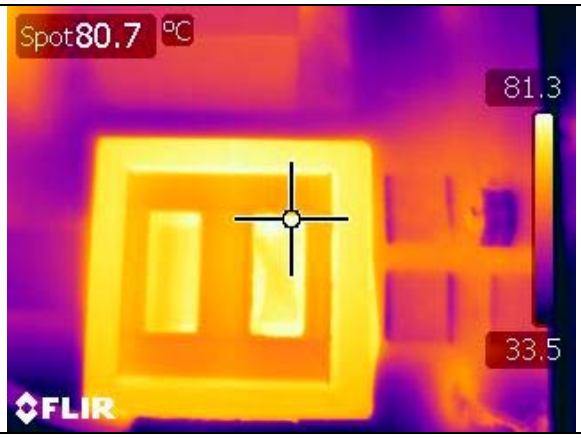


Figure 50 – LLC Transformer (T2), 90 VAC Input, 100% Load, Room Temperature.

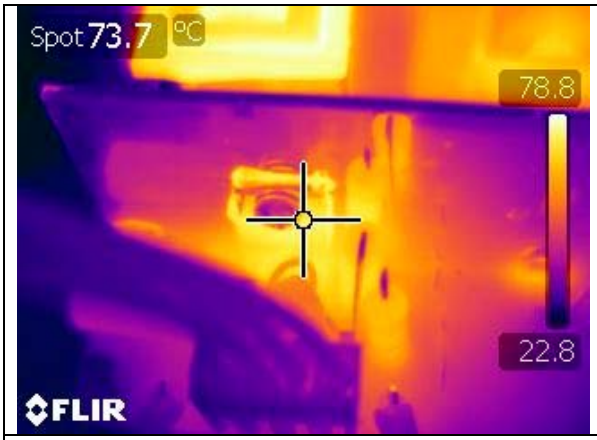


Figure 51 – Output Rectifier (D9), 90 VAC Input, 100% Load, Room Temperature.

Figure 52 – Current Sense Resistor (R916), 90 VAC Input, 100% Load, Room Temperature.

14.2 115 VAC, 60 Hz, 150 W Output

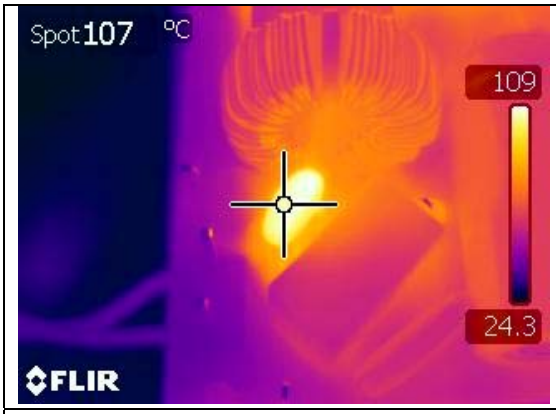


Figure 53 - Inrush Limiting Thermistor (RT1), 115 VAC Input, 100% Load, Room Temperature.

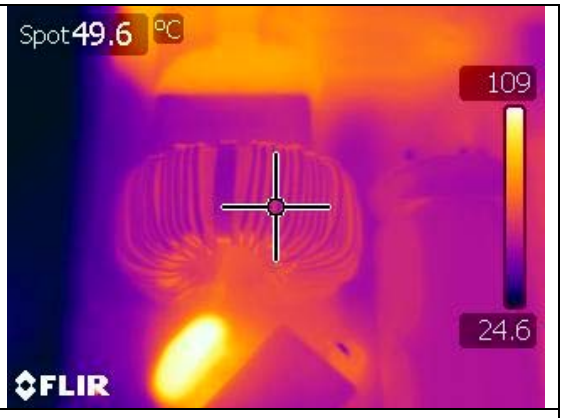


Figure 54 - Common Mode Choke (L1), 115 VAC Input, 100% Load, Room Temperature.

Figure 55 - Differential Mode Choke (L4), 115 VAC Input, 100% Load, Room Temperature.

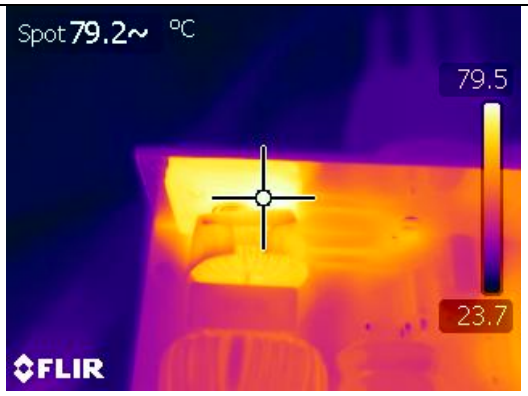


Figure 56 - Input Rectifier Bridge (BR1), 115 VAC Input, 100% Load, Room Temperature.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Figure 57 – PFC IC (U7), 115 VAC Input, 100% Load, Room Temperature.

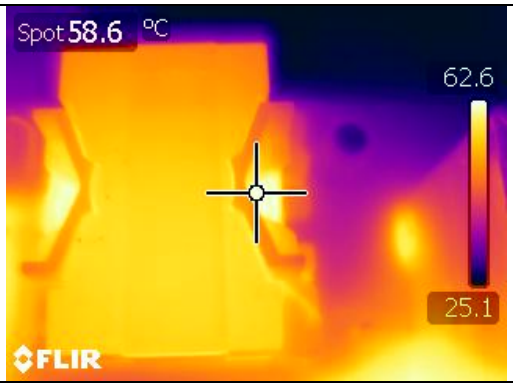


Figure 58 - PFC Inductor (T3), 115 VAC Input, 100% Load, Room Temperature

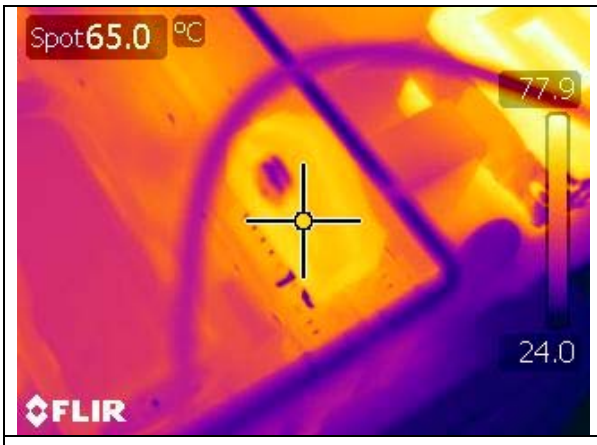


Figure 59 – LLC IC (U3), 115 VAC Input, 100% Load, Room Temperature.

Figure 60 – LLC Transformer (T2), 115 VAC Input, 100% Load, Room Temperature.

Figure 61 – Output Rectifier (D9), 115 VAC Input, 100% Load, Room Temperature.

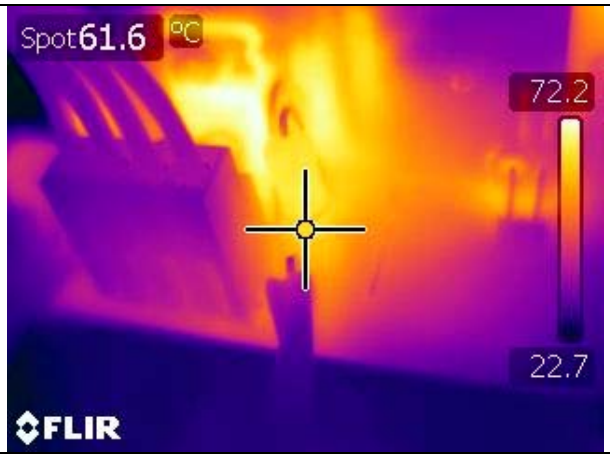


Figure 62 – Current Sense Resistor (R916), 115 VAC Input, 100% Load, Room Temperature.

14.3 230 VAC, 150 W, Room Temperature

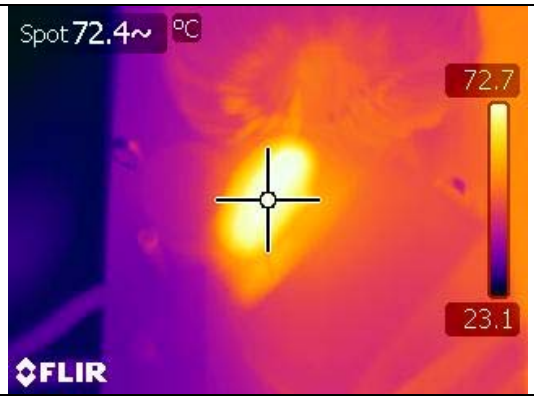


Figure 63 - Inrush Limiting Thermistor (RT1), 230 VAC Input, 100% Load, Room Temperature.

Figure 64 - Common Mode Choke (L1), 230 VAC Input, 100% Load, Room Temperature.

Figure 65 - Differential Mode Choke (L4), 230 VAC Input, 100% Load, Room Temperature.

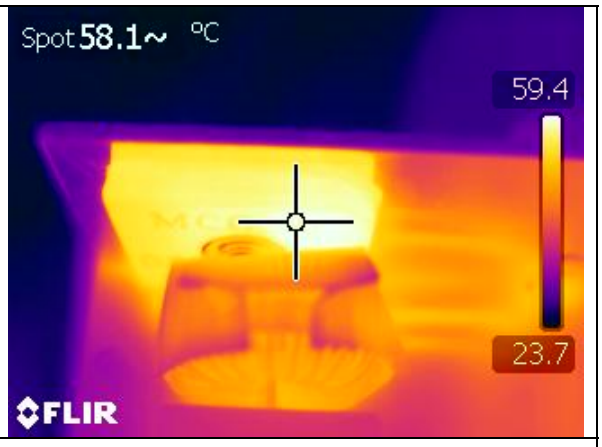


Figure 66 - Input Rectifier Bridge (BR1), 230 VAC Input, 100% Load, Room Temperature.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Figure 67 – PFC IC (U7), 230 VAC Input, 100% Load, Room Temperature.

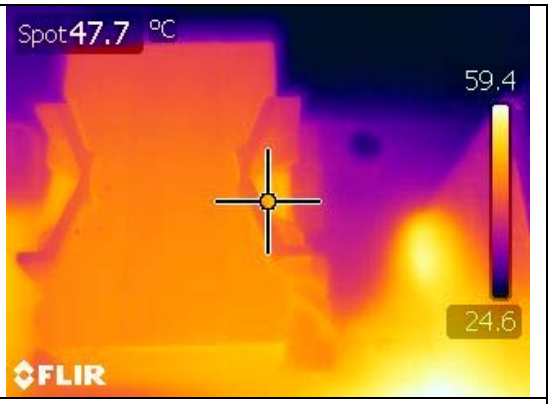


Figure 68 - PFC Inductor (T3), 230 VAC Input, 100% Load, Room Temperature

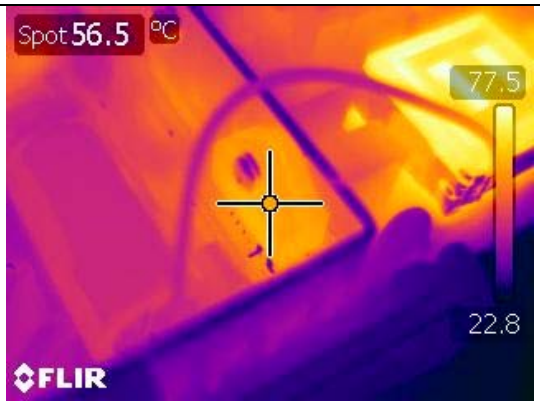


Figure 69 – LLC IC (U3), 230 VAC Input, 100% Load, Room Temperature.

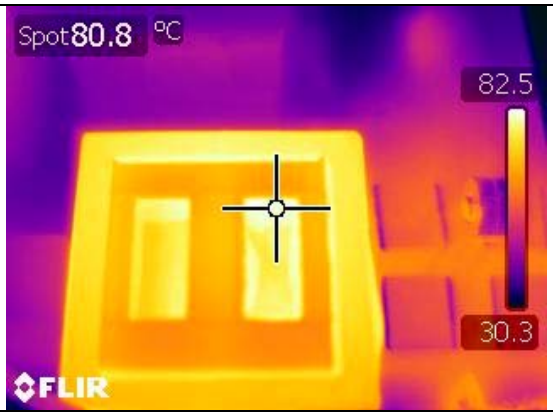


Figure 70 – LLC Transformer (T2), 230 VAC Input, 100% Load, Room Temperature.

Figure 71 – Output Rectifier (D9), 230 VAC Input, 100% Load, Room Temperature.

Figure 72 – Current Sense Resistor (R916), 230 VAC Input, 100% Load, Room Temperature.

15 Output Gain-Phase

Gain-phase was tested a maximum load using the constant voltage load described in section 7.1. It is important to use the actual LED load or a load with similar characteristics during gain-phase testing, as a load with different output characteristic will yield inaccurate results.

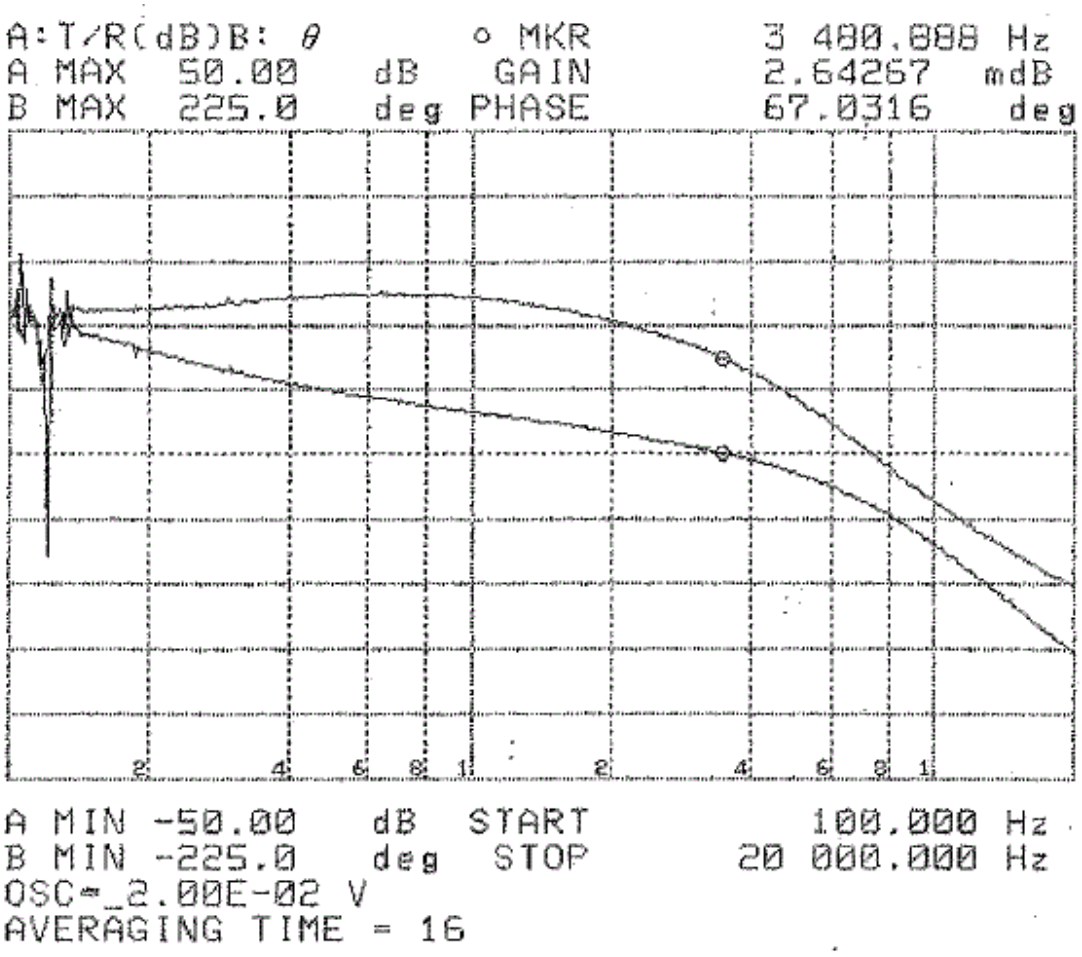


Figure 73 – LLC Converter Gain-Phase, 100% Load Crossover Frequency – 3.48 kHz, Phase Margin - 67°.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

16 Conducted EMI

Conducted EMI tests were performed using the constant voltage load described in section 7.1. The output return was connected to the LISN artificial hand to simulate the capacitance of a typical set of LED panels to chassis ground.

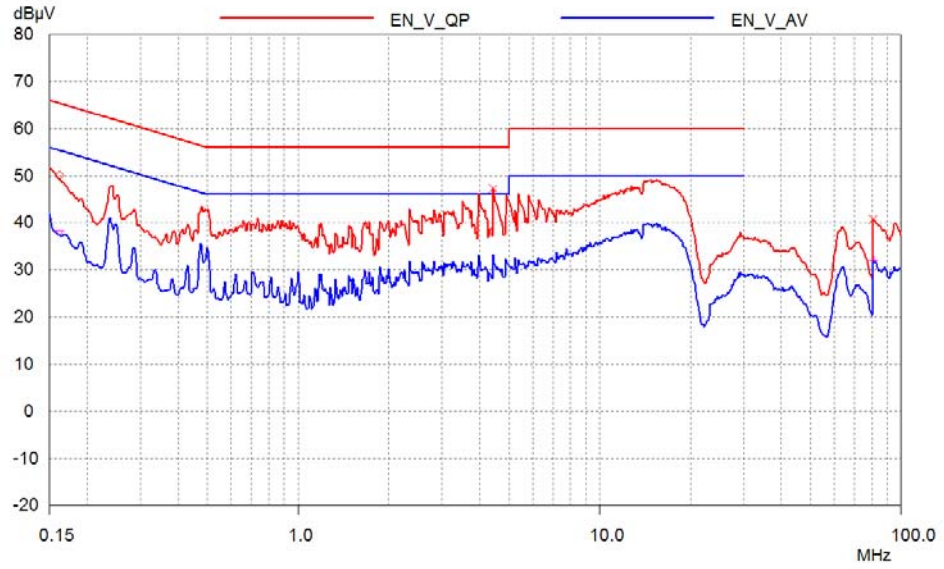


Figure 74 – Conducted EMI, 115 VAC

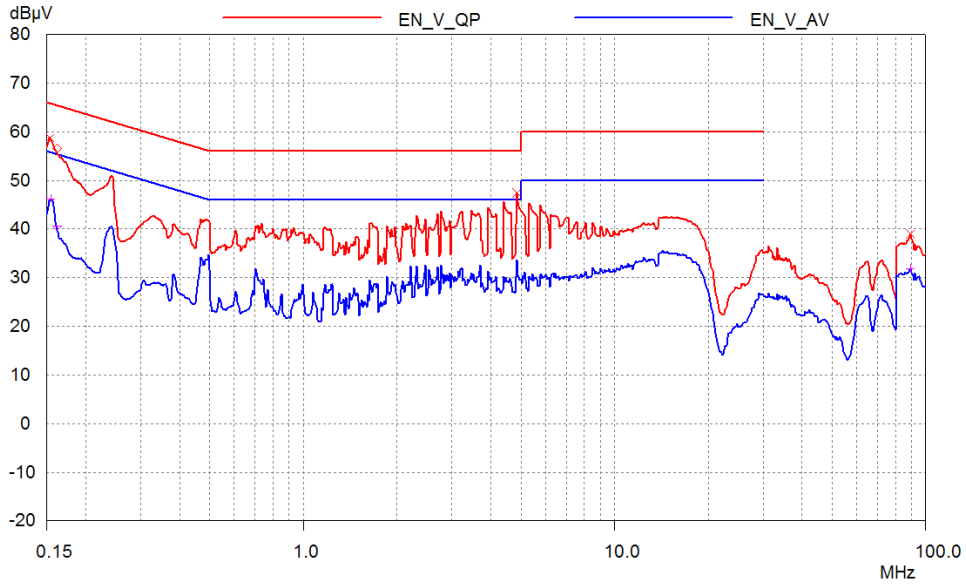


Figure 75 – Conducted EMI, 230 VAC

17 Line Surge Testing

17.1 Line Surge Test Setup

The picture below shows the power supply set-up for surge testing. The supply is placed on a ground plane approximately the size of the power supply. A piece of single-sided copper clad printed circuit material was used in this case, but a piece of aluminum sheet with appropriate insulation would also work. An IEC AC connector was wired to the power supply AC input, with the safety ground connected to the ground plane. The CV output load (described in section 7) was placed on top of the ground plane so that it would capacitively couple to the safety ground. A 48V fan was located inside the plastic shroud shown in the figure, and used to cool the CV load during testing. An indicator consisting of a GaP yellow-green led in series with a 39V zener diode and a 100 ohm resistor was placed across the output of the supply and used as a sensitive output dropout detector during line surge testing.

The UUT was tested using a Teseq NSG 3060 surge tester. Results of common mode and differential mode surge testing are shown below. A test failure was defined as a non-recoverable output interruption requiring supply repair or recycling AC input voltage.

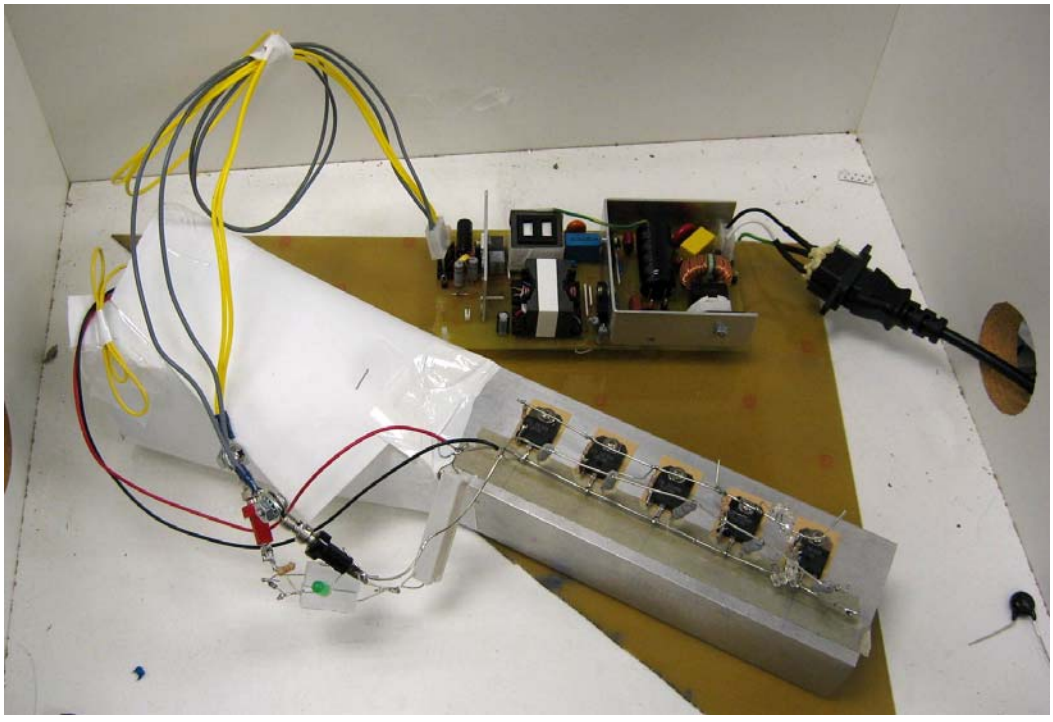


Figure 76 – Line Surge Physical Setup

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

17.2 Differential Mode Surge, 1.2/50 µsec

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+2	90	2	10	PASS
115	-2	90	2	10	PASS
115	+2	270	2	10	PASS
115	-2	270	2	10	PASS
115	+2	0	2	10	PASS
115	-2	0	2	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	90	2	10	PASS
230	-2	90	2	10	PASS
230	+2	270	2	10	PASS
230	-2	270	2	10	PASS
230	+2	0	2	10	PASS
230	-2	0	2	10	PASS

17.3 Common Mode Surge, 1.2/50 µsec

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+4	90	12	10	PASS
115	-4	90	12	10	PASS
115	+4	270	12	10	PASS
115	-4	270	12	10	PASS
115	+4	0	12	10	PASS
115	-4	0	12	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4	90	12	10	PASS
230	-4	90	12	10	PASS
230	+4	270	12	10	PASS
230	-4	270	12	10	PASS
230	+4	0	12	10	PASS
230	-4	0	12	10	PASS

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

18 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-May-13	RH	1.0	Initial Draft	
24-Jun-13	RH	3.0	Additional Figures	

For the latest updates, visit our website: *www.powerint.com*

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3911
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

JAPAN
Kosei Dai-3 Bldg.,
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail:
japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail:
chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-41138020
Fax: +91-80-41138023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail:
koreasales@powerint.com

UNITED KINGDOM
1st Floor, St. James's House
East Street, Farnham
Surrey, GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail:
eurosales@powerint.com

CHINA (SHENZHEN)
Rm A, B & C 4th Floor, Block C,
Electronics Science and
Technology Building, 2070
Shennan Zhong Rd,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail:
chinasales@powerint.com

ITALY
Via De Amicis 2
20091 Bresso MI – Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760