MP4033

TRIAC Dimmable, Primary Side Control Offline LED Controller with Active PFC

The Future of Analog IC Technology

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

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DESCRIPTION

The MP4033 is a TRIAC-dimmable and 0-10V dimmable, primary-side–control, offline LED lighting controller with active PFC. It can output an accurate LED current for an isolated lighting application with a single-stage converter. The proprietary real-current–control method can accurately control the LED current using primary-side information. It can significantly simplify LED lighting system design by eliminating secondary-side feedback components and the opto-coupler.

The MP4033 implements power-factor correction and works in boundary-conduction mode to reduce MOSFET switching losses.

The MP4033 has an integrated charging circuit at the supply pin for fast start-up without a perceptible delay.

The proprietary dimming control expands the TRIAC-based dimming range.

The MP4033 has multiple protections that greatly enhance system reliability and safety, and include output over-voltage protection, output short-circuit protection, winding short circuit protection, programmable primary-side over-current protection, programmable thermal fold-back (MSOP10), ZCD pin short circuit protection, supply-pin under-voltage lockout, and over-temperature protection.

All fault protections feature auto-restart.

The MP4033 is available in SOIC8/MSOP10/SOIC14 packages.

FEATURES

- Primary-Side-Control without Requiring a Secondary-Side Feedback Circuit
- Flicker-Free, Phase-Controlled Dimming (TRIAC dimmer/Trailing edge dimmer) with Deep Dimming Range.
- PWM/Analog dimming for 0-10V dimming
- Fast Start-Up without Perceptible Delay
- Programmable Current Fold-back to Prolong the LED lifetime
- Accurate Line & Load Regulation
- High Power Factor
- Operates in Boundary Conduction Mode
- Cycle-by-Cycle Current Limit
- Winding Short Circuit Protection
- Output Over-Voltage Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Available in SOIC8/MSOP10/SOIC14 Packages

APPLICATIONS

- Solid-State Lighting, including:
- Industrial and Commercial Lighting
- Residential Lighting

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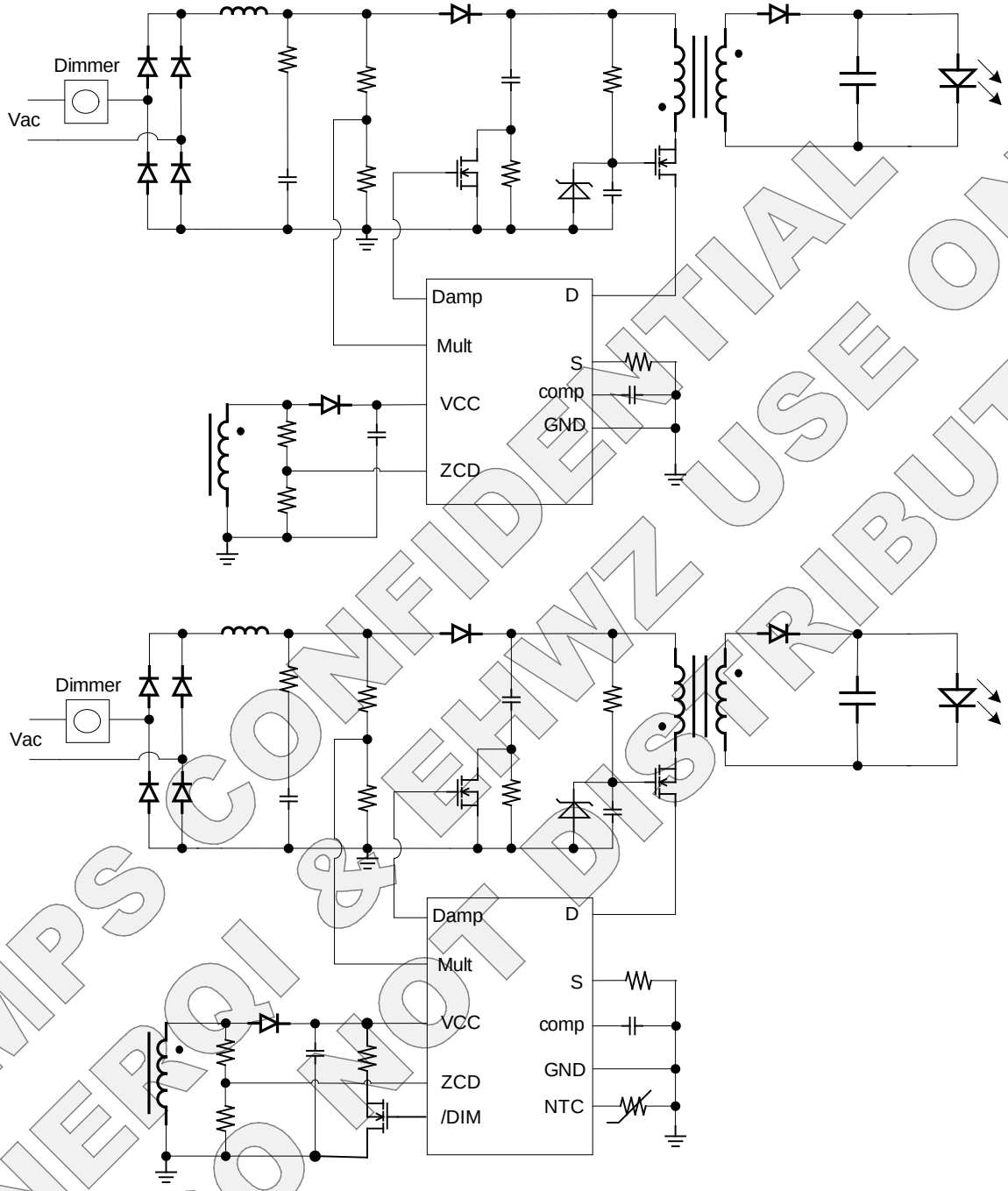
TYPICAL APPLICATION CIRCUIT



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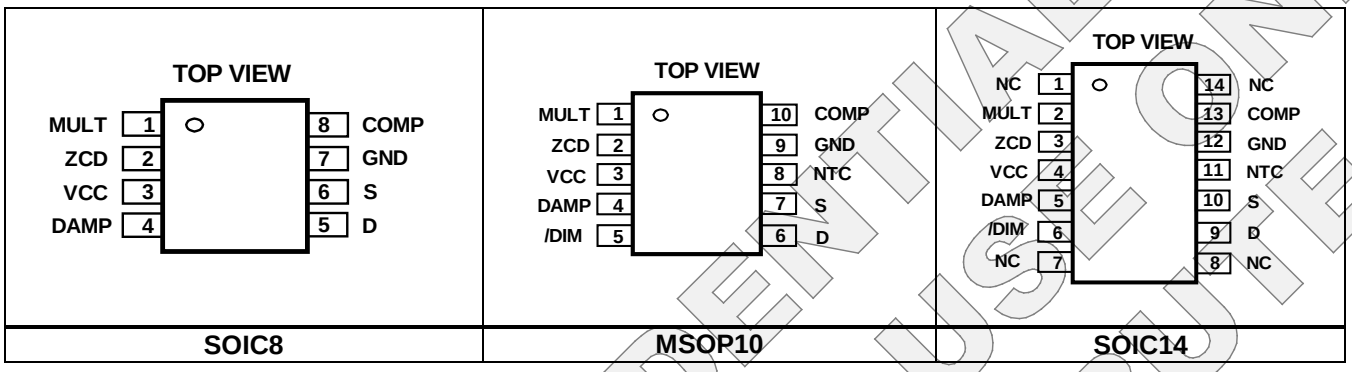
ORDERING INFORMATION

Part Number*	Package	Top Marking

PACKAGE REFERENCE



SOIC8	MSOP10	SOIC14

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage VCC ..... -0.3V to +30V
Low-Side MOSFET Drain Voltage -0.7V to +30V
Damp Pin Voltage ..... -0.3V to +15V
ZCD Pin Voltage ..... -7V to +7V
Other Analog Inputs and Outputs..... -0.3V to 7V
ZCD Pin Current ..... -5mA to +5mA
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8..... 1.3W
SOIC14..... 1.45W
MSOP10..... 0.83W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage VCC ..... 11V to 27V
Operating Junction Temp (T_J). . -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8 ……	96....	45.. °C/W
MSOP10 ……	150....	65.. °C/W
SOIC14 ……	86....	38.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	V_{CC}	After turn on	11		27	V
VCC Upper Level: Internal Charging Circuit Stops and IC Turns On	V_{CCH}		9.5	10	10.5	V
VCC Lower Level: Internal Charging Circuit Triggers	V_{CCL}		8.55	9	9.45	V
Vcc Re-charge and IC turns off Level in Fault Condition	V_{CCEN}	Fault condition	6.55	7	7.45	V
Supply Current						
VCC Charging Current from D	$I_{D\ charge}$	VD=16V, VCC=5V	20	25	30	mA
Pull Down Current at VCC_UVLO	$I_{VCC\_PULL\_DOWN}$	VCC<9V	0.8	1	1.2	mA
Quiescent Current	I_Q	No switching, VCC=15V		800	1000	µA
Quiescent Current at Fault	I_{Q_FAULT}	Fault condition, IC latch,VCC=15V	300	350	400	µA
Operating Current	I_{CC}	f_s =70kHz, VCC=15V		1	2	mA
Multiplier						
Linear Operation Range	V_{MULT}	V_{COMP} from 1.9V to 4.9V	0		3	V
Gain	$K^{(5)}$	V_{COMP}=2V, V_{MULT}=0.5V	0.84	1.06	1.26	1/V
		V_{COMP}=2V, V_{MULT}=1.5V	0.9	1.08	1.23	1/V
		V_{COMP}=2V, V_{MULT}=3V	0.93	1.1	1.25	1/V
TRIAC Dimming Phase Off Detection Threshold	V_{MULT_OFF}		0.08	0.1	0.12	V
TRIAC Dimming Phase On Detection Threshold	V_{MULT_ON}		0.26	0.28	0.30	V
TRIAC Dimming Off Line-Cycle Blanking Ratio	D_{OFF_LEB}		29.8%	30%	30.2%	
Dimming Pull-Down MOSFET Turn on Threshold	$V_{MULT\_DP\_ON\_TL}$	Trailing edge dimmer	0.48	0.5	0.52	V
	$V_{MULT\_DP\_ON\_LD}$	Leading edge dimmer	0.22	0.25	0.28	V
Dimming Pull-Down MOSFET Turn off Threshold	$V_{MULT\_DP\_OFF\_TL}$	Trailing edge dimmer	0.32	0.35	0.38	V
	$V_{MULT\_DP\_OFF\_LD}$	Leading edge dimmer	0.32	0.35	0.38	V
Leading Edge Dimming Detection Low Threshold	$V_{MULT\_LD\_LOW}$		0.08	0.1	0.12	V
Leading Edge Dimming Detection High Threshold	$V_{MULT\_LD\_HIGH}$		0.26	0.28	0.30	V

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Trailing Edge Dimming Detection High Threshold	$V_{MULT\_TL\_HIGH}$	Rising, V_{MULT_PK}≥0.61V Falling, V_{MULT_PK}≥0.54V	0.48	0.5	0.52	V
		Rising, V_{MULT_PK}≥0.56V Falling, V_{MULT_PK}≥0.49V	0.43	0.45	0.47	V
		Rising, V_{MULT_PK}≥0.51V Falling, V_{MULT_PK}≥0.44V	0.38	0.4	0.42	V
Trailing Edge Dimming Detection High Threshold	$V_{MULT\_TL\_HIGH}$	Rising, V_{MULT_PK}≥0.46V Falling, V_{MULT_PK}≥0.39V	0.33	0.35	0.37	V
		Rising, V_{MULT_PK}≥0.41V Falling, V_{MULT_PK}≥0.34V	0.28	0.3	0.32	V
		Rising, V_{MULT_PK}<0.41V Falling, V_{MULT_PK}<0.34V	0.23	0.25	0.27	V
Trailing Edge Dimming Detection High Threshold Hysteresis	$V_{MULT\_TL\_H\_HYS}$			50		mV
Trailing Edge Dimming Detection Low Threshold	$V_{MULT\_TL\_LOW}$		0.08	0.1	0.12	V
Leading Edge dimmer detection Time threshold	$t_{LEADING}$	Ta=-40~125°C, Rising	90	100	110	µs
Trailing Edge dimmer detection Time threshold	$t_{TRAILING}$	Ta=-40~125°C, Falling	405	450	495	µs
Error Amplifier						
Reference Voltage	V_{REF}		0.408	0.414	0.424	V
Transconductance	G_{EA}	Guaranteed by design		250		µA/V
COMP Lower Clamp Voltage	V_{COMPL_LD}	Leading edge dimmer	1.85	1.9	1.95	V
	V_{COMPL_TL}	Trailing edge dimmer	1.55	1.6	1.65	V
	V_{COMPL_N}	No dimmer	1.55	1.6	1.65	V
	$V_{COMPL\_NTC≤1.0V}$	NTC≤1.0V	1.45	1.5	1.55	V
Max. Source Current	I_{COMP+}			57		µA
Max. Sink Current without Dimmer	I_{COMP-}			-300		µA
Sink Current at TRIAC Dimming Off	$I_{SINK\_DIM\_LD}$	Leading Edge Dimmer		85.5		µA
	$I_{SINK\_DIM\_TL}$	Trailing Edge Dimmer		133		µA
Current Sense Comparator						
Leading-Edge-Blanking Time	t_{LEB}		400	500	600	ns
Over-Current-Protection Leading-Edge-Blanking Time	t_{LEB_OCP}			0.7		T_{LEB}
Over-Current-Protection Threshold	V_{OCP}		2.6	2. 7	2.8	V

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense Upper Clamp Voltage	$V_{S\ CLAMP\ H}$		2.0	2. 1	2.2	V
Current Sense Lower Clamp Voltage	$V_{S\ CLAMP\ L}$		0.01	0.03	0.05	V
Zero-Current Detector						
Zero-Current–Detect Threshold	V_{ZCD_T}	Falling Edge	0.27	0.30	0.33	V
Zero-Current–Detect Hysteresis	$V_{ZCD\ HYS}$		570	600	630	mV
ZCD Pin Short Circuit Threshold	V_{ZCD_SC}		80	100	120	mV
ZCD Pin Short Circuit Blanking time	$t_{ZCD\_SC\_LEB}$	Only dimming on time is counted		33.28		ms
Zero-Current–Detect LEB	t_{ZCD_LEB}	Starts at Gate Turn Off when $V_{MULT\ O}$ ⩾0.25V	1.99	2.2	2.58	µs
		Starts at Gate Turn Off when $V_{MULT\ 0}$ <0.25V	0.85	1.1	1.35	µs
Over-Voltage Threshold	$V_{ZCD\ OVP}$		5.1	5.36	5.7	V
OVP Detect LEB	t_{OVP_LEB}	Starts at Gate Turn Off when $V_{MULT\ O}$⩾0.25V	1.99	2.2	2.58	µs
		Starts at Gate Turn Off when $V_{MULT\ O}$ <0.25V	0.85	1.1	1.35	µs
Minimum Off Time	t_{OFF_MIN}	Normal	4.62	5.1	5.92	µs
		NTC≤1.0V		10.2		µs
Weak/Strong DP Mode detector current (for leading edge dimmer)	$I_{DP\_DET\_LD}$	Ta=-40~125°C	160	200	240	µA
Strong DP Mode Enable Threshold (for leading edge dimmer)	$V_{EN\_DP\_STR\_LD}$		0.579	0.600	0.621	V
Weak/Strong DP Mode Detection Time (for leading edge dimmer)	$t_{DP\_DET\_LD}$		150	200	250	µs
Starter						
Start Timer Period	t_{start}		100	130	160	µs
Internal Main MOSFET						
Breakdown Voltage	BV_{DSS_MAIN}	$V_{GS=0}$	30			V
Drain-Source On-Resistor	$R_{DS(ON)\_MAIN}$	I_D=100mA, Ta=25 °C	200	250	300	mΩ
		I_D=100mA, Ta=25 °C, VCC= V_{CCEN} +50mV		250		mΩ

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal OVP Pull Up MOSFET						
Breakdown Voltage	$BV_{DSS\_D\_VCC}$	$V_{GS=0}$	30			V
Drain-Source On-Resistor	$R_{DS(on)\_D\_VCC}$	I_D=50mA		100		Ω
Internal Dimming Pull Down Current Source						
Breakdown Voltage	BV_{DSS_DP}	$V_{GS=0}$	30			V
Strong Dimming Pull Down Current for leading edge dimmer	$I_{DP\_STRONG\_LD}$		32	40	48	mA
Weak Dimming Pull Down Current for leading edge dimmer	$I_{DP\_WEAK\_LD}$		8	10	12	mA
Pull Down Current for Trailing edge dimmer	I_{DP_TL}		135	150	165	mA
Min Clamp Ratio of Pull Down Current for Trailing edge dimmer (I_Min/I_Normal)			13%	13.3%	14%	
NTC						
High Threshold Voltage	V_{H_NTC}		1.14	1.2	1.26	V
Low Threshold Voltage	V_{L_NTC}		0.76	0.8	0.84	V
Shutdown Threshold	V_{SD_NTC}		0.38	0.4	0.42	V
Shutdown Voltage Hysteresis	$V_{SD\_NTC\_HSY}$		90	100	110	mV
Pull Up Current Source	$I_{PULL\_UP\_NTC}$		57	60	63	μA
Leakage Current	$I_{LEAKAGE\_NTC}$				1	μA
PWM Dimming Blanking Time	t_{PWM_LEB}			20		ms
DAMP						
Turn Off Threshold	$V_{MULT\_DAMP\_OFF}$		0.22	0.25	0.28	V
Turn On Threshold	$V_{MULT\_DAMP\_ON}$		0.32	0.35	0.38	V
Pull Down Current	$I_{DAMP\_PULL\_DOWN}$	V_{DAMP}=5V	320	400	480	μA
Pull Up Current	$I_{DAMP\_PULL\_UP}$	V_{DAMP}=0.3V	80	100	120	μA
Upper Clamp Voltage	$V_{DAMP\_CLAMP\_UP}$			13.5	15	V
Min Pull Up Voltage	V_{DAMP_MIN}	VCC= V_{CCEN} +50mV	6			V
DIM						
Source Current	I_{DIM_SOURCE}		1	2		mA
Sink Current	I_{DIM_SINK}		2	4		mA
High Level	V_{DIM_HIGH}		5.0		5.5	V
Low Level	V_{DIM_LOW}				0.3	V

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown						
Thermal Shutdown Threshold(6)	T_{SD}			150		˚C
Thermal Shutdown Recovery Hysteresis(6	T_{HYS}			25		˚C

Notes:
5) The multiplier output is given by: Vs=K•VMULT• (VCOMP-1.5)
6) Guaranteed by characterization.

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PIN FUNCTIONS

Pin #			Name	Description
SOIC 8	SOIC 14	MSOP10		
1	2	1	MULT	One of the Internal Multiplier Input. Connect to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal to this pin provides a reference signal for the internal current control loop. The MULT pin also detects the TRIAC dimming phase.
2	3	2	ZCD	Zero-Current Detection. A negative going edge triggers the internal MOSFET's turn-on signal. Connect to the tap of a resistor divider from the auxiliary winding to GND. The ZCD pin can also detect over-voltage and over-current conditions. Over-voltage occurs if V_{ZCD} exceeds the over-voltage-protection (OVP) threshold after a 2μs blanking time when the internal MOSFET turns off.
3	4	3	VCC	Supply Voltage. Supplies power for both the control signal and the internal MOSFET's gate driver. Connect to an external bulk capacitor—typically 22μF with a 100pF ceramic capacitor to reduce noise.
4	5	4	DAMP	Gate Control pin of the external Damping MOSFET.
NA	6	5	/DIM	This is the Dim signal from the internal control logic, can be used to drive an external dummy Load to program the dimming curve.
5	9	6	D	Internal Low-Side main MOSFET Drain. This pin also internally connects to VCC via a diode and a JFET to form an internal charging circuit for VCC. Connect to the source of the high-side MOSFET. There is an internal MOS through a diode to pull up the D to VCC at fault condition to turn off the main switch reliable. There is an intelligent Weak/Strong Dimming Pull down Current Source on this pin.
6	10	7	S	Internal Low-Side main MOSFET Source. Connect a resistor from this pin to GND to sense the internal MOSFET current. An internal comparator compares the resulting voltage to the internal sinusoid shaped current reference signal to determine when the MOSFET turns off. If the voltage exceeds the current-limit threshold of 2.3V after the leading edge blanking time during the turn-on interval, the gate signal turns off. Over-current occurs if V_s exceeds 2.7V during the gate-on interval after the leading edge blanking time
NA	11	8	NTC	LED temperature protection input. Connect a NTC resistor from this pin to GND can reduce the output current to protect the LED. Apply an external PWM signal on this pin through a resistor can dim the LED with PWM mode. 1kΩ is recommended.
7	12	9	GND	Ground. Current return of the control signal and the gate drive signal.
8	13	10	COMP	Loop Compensation. Connects to a compensation network to stabilize the LED driver and accurately control the LED driver current.
	1, 7, 8, 14		NC	

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OPERATION

The MP4033 is a TRIAC-dimmable and 0-10V dimmable, primary-side–control, offline LED controller designed for high-performance LED lighting. The MP4033 can accurately control the LED current using the real-current–control method based on primary-side information. It can also achieve a high power factor to eliminate noise pollution on the AC line. The integrated VCC charging circuit can achieve fast start-up without any perceptible delay. The Programmable thermal current fold back function can prolong the life time of the LED. The MP4033 is suitable for TRIAC-based dimming and 0-10V dimming with deep dimming range.

Boundary-Conduction Mode

During the external MOSFET ON time (T_{ON}), the rectified input voltage applied across the primary-side inductor (Lm) increases the primary current increases linearly from zero to the peak value (I_{pk}). When the external MOSFET turns off, the energy stored in the inductor forces the secondary side diode to turn on, and the inductor current decreases linearly from the peak value to zero. When the current decreases to zero, the parasitic resonance caused by the inductor and the combined parasitic capacitances decreases the MOSFET drain-source voltage that is also reflected on the auxiliary winding (see Figure 1). The zero-current detector generates the external MOSFET turn-on signal when the ZCD voltage falls below 0.35V after a blanking time and ensures the MOSFET turns on at a relatively low voltage (see Figure 2).

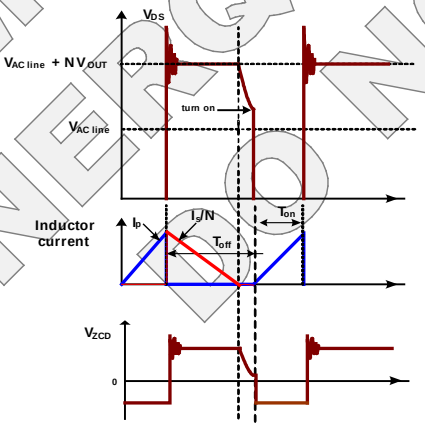

Figure 1: Boundary-Conduction Mode

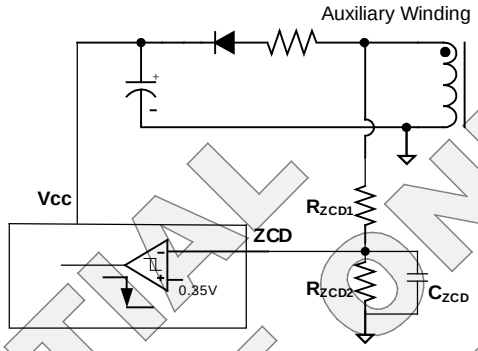

Figure 2: Zero-Current Detector

As a result, there are virtually small primary switch turn-on losses and no secondary-diode reverse-recovery losses. This ensures high efficiency and low EMI noise.

Real-Current Control

The proprietary real-current–control method allows the MP4033 to control the secondary-side LED current based on primary-side information. The output LED mean current can be calculated approximately as:

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

Where:

- N is the turn ratio of the primary side to the secondary side,
- V_{FB} is the feedback reference voltage (typically 0.4), and
- R_s is the sense resistor between the MOSFET source and GND.

Power-Factor Correction

The MULT pin connects to the tap of a resistor divider from the rectified instantaneous line voltage. The multiplier output also has a sinusoidal shape. This signal provides the reference for the current comparator against the primary-side–inductor current, which shapes the primary-peak current into a sinusoid with the same phase as the input line voltage. This achieves a high power factor.

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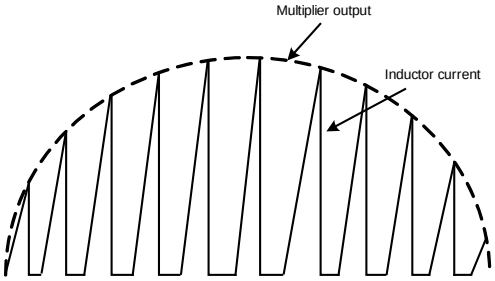

Figure 3: Power-Factor Correction

The multiplier's maximum output voltage to the current comparator is clamped to 2.3V to limit the cycle-by-cycle current. The multiplier's minimum output voltage is clamped to 0.15V to ensure a turn-on signal during the TRIAC dimming OFF interval, which pulls down the rectifier input voltage and accurately detects the dimming phase.

VCC Timing Sequence

Initially, VCC charges through the internal charging circuit from the AC line. When VCC reaches 10V, the internal charging circuit stops charging, the control logic initializes and the internal main MOSFET begins to switch. Then the auxiliary winding takes over the power supply. However, the initial auxiliary-winding positive voltage may not be large enough to charge VCC, causing VCC to drop. Instead, if the VCC voltage drops below the 9V threshold, the internal charging circuit triggers and charges VCC to 10V again. This cycle repeats until the auxiliary winding voltage is high enough to power VCC.

If any fault occurs during this time, the switching and the internal charging circuit will stop and latch, and VCC drops. When VCC decreases to 7V, the internal charging circuit re-charges for auto-restart.

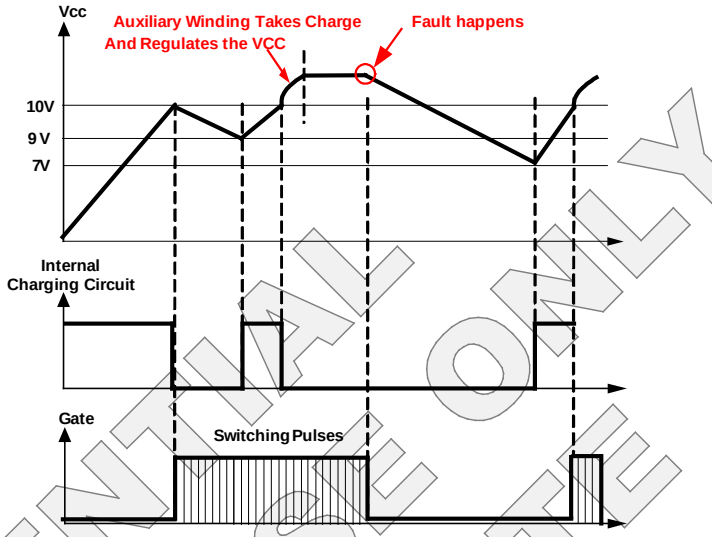

Figure 4: VCC Timing Sequence

Auto Start

The MP4033 includes an auto starter that starts timing when the MOSFET turns off. If ZCD fails to send a turn-on signal after 130μs, the starter will automatically sends a turn-on signal to avoid unnecessary Ic shutdowns if ZCD fails.

Minimum OFF Time

The MP4033 operates with a variable switching frequency; the frequency changes with the instantaneous input-line voltage. To limit the maximum frequency and get good EMI performance, the MP4033 employs an internal minimum OFF-time limiter.

Leading-Edge Blanking

In order to avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on, an internal leading-edge blanking (LEB) unit between the S pin and the current-comparator input blocks the path from the S pin to the current comparator input during the blanking time. Figure 5 shows the leading-edge blanking.

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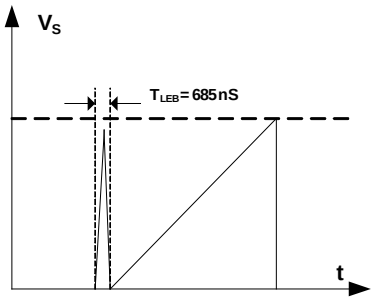

Figure 5: Leading-Edge Blanking

Output Over-Voltage Protection (OVP)

Output over-voltage protection (OVP) prevents component damage from over-voltage conditions. The auxiliary winding voltage's positive plateau is proportional to the output voltage, and the OVP monitors this auxiliary winding voltage instead of directly monitoring the output voltage as shown in Figure 6. Once the ZCD pin voltage exceeds 5.5V, the OVP signal triggers and latches, the gate driver turns off, the IC works in quiescent mode. When the VCC voltage drops below the UVLO threshold, the IC shuts down and the system restarts. The output OVP set point can be calculated as:

$$V_{out\_ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1}+R_{ZCD2}} = 5.5$$

Where:

$V_{out-ovp}$ is the output OVP threshold,

N_{aux} is the number of auxiliary winding turns, and

N_{sec} is the number of secondary winding turns

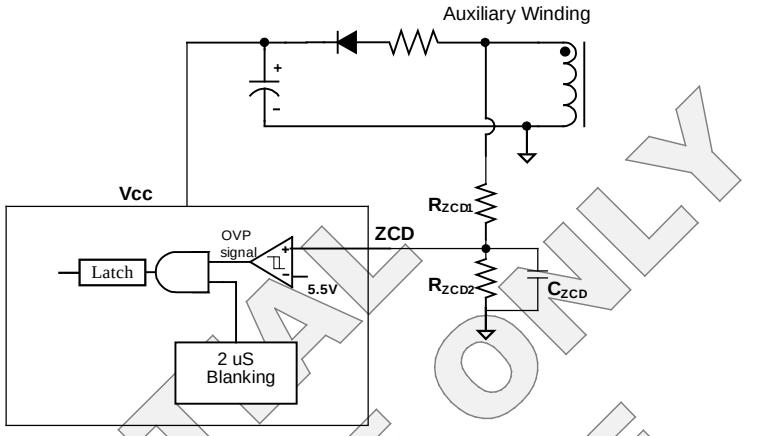

Figure 6: OVP Sampling Circuit

To avoid switch-on spikes mis-triggering OVP, OVP sampling has a T_{OVPS} blanking period of around 2μs, as shown in Figure 7.

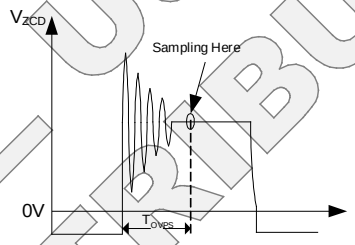

Figure 7: ZCD Voltage and OVP Sampling

Cycle by cycle Current Limit

There is cycle by cycle current limit on the S pin, when the voltage of S pin reach to 2.2V after a Blanking time, the switching MOS will be turn off to limit the peak current value.

Primary Over-Current Protection (OCP)

The S pin has an internally-integrated comparator for primary OCP. When the gate is on, the comparator is enabled. Over-current occurs when V_S exceeds 2.7V after a blanking time. Then the IC shuts down and restarts until VCC dropping below UVLO. Figure 8 shows OCP.

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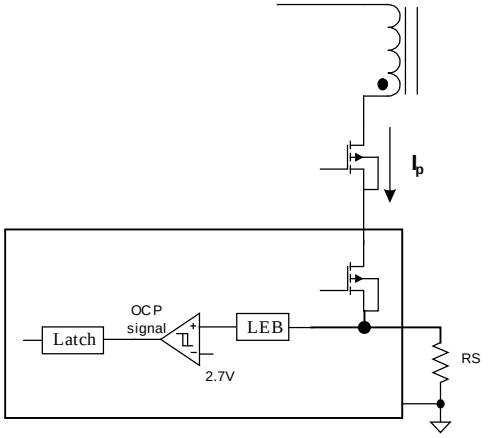

Figure 8: Over-Current Protection Circuit

LED Short Circuit Protection (SCP)

When the LED Short Circuit occurs, IC can automatically reduce the switching frequency to 7kHz to limit the short circuit power to safely protect all the components at this condition.

Thermal Shutdown

To prevent internal temperatures from exceeding 150°C and causing lethal thermal damage, the MP4033 shuts down the switching cycle and latched until VCC dropping below UVLO and restarts again.

Phase-Cut-Based Dimming Control

The MP4033 can implement Phase-cut-based dimming (including leading edge dimmer and trailing edge dimmer). For the leading edge dimmer, most of them are TRIAC-base, so it off called TRIAC dimmer. The TRIAC dimmer usually consists of a bi-directional SCR with an adjustable turn-on phase. Figure 99 shows the leading-edge TRIAC dimmer waveforms.

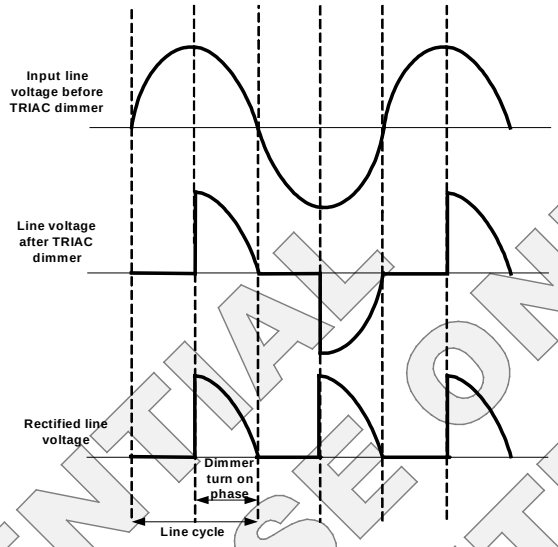

Figure 9: TRIAC Dimmer Waveforms

For the Trailing edge dimmer, the waveforms show at Figure 10.

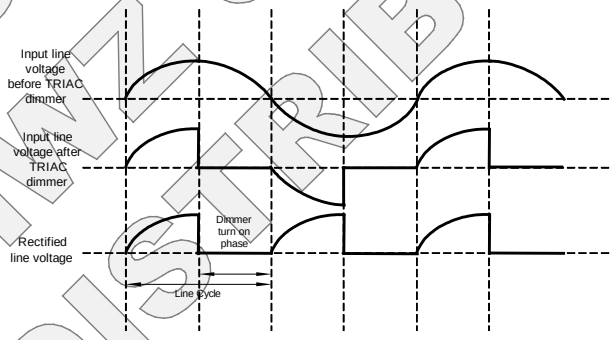

Figure 10: TRIAC Dimmer Waveforms

The MP4033 detects the dimming turn-on cycle through the MULT pin, which is fed into the control loop to adjust the internal reference voltage. When the MULT voltage exceeds 0.35V, the device treats this signal as a dimmer turn-on signal. When the MULT voltage falls below 0.15V, the system treats this as a dimmer turn-off signal. The MP4033 has a 30% line-cycle–detection blanking time with each line cycle, The real phase detector output adds this time, as shown in Figure. That means if the turn-on cycle exceeds 70% of the line cycle, the output remains at the same maximum current. It improves the line regulation during the maximum turn-on cycle or without a dimmer.

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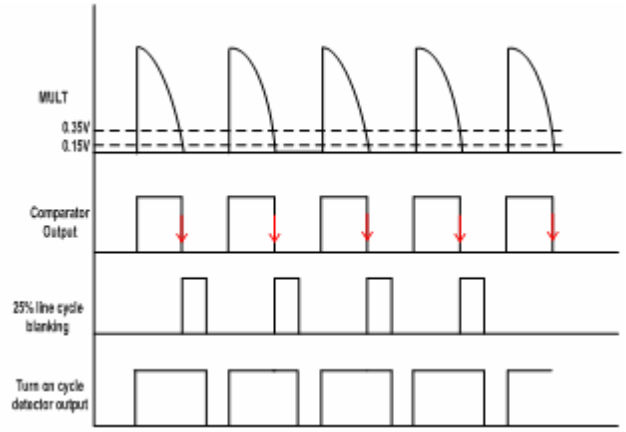

Figure11: Dimming Turn-On Cycle Detector

If the turn-on cycle decreases to less than 70% of the line cycle, the internal reference voltage decreases as the dimming turn-on phase decreasing, and the output current decreases accordingly to implement dimming. As the dimming turn-on cycle decreases, the COMP voltage also decreases. Once the COMP voltage reaches to 1.9V, it is clamped so that the output current decreases slowly to maintain the TRIAC holding current and avoid random flicker. Figure12 shows the relationship between the dimming turn-on phase and output current.

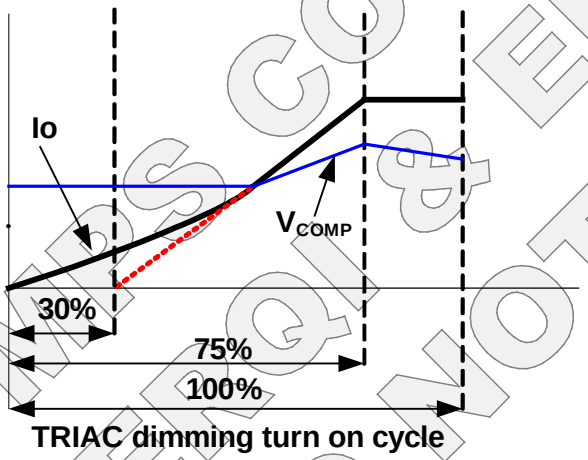

Figure 12: Dimming Curve

Dimming Pull-Down current source

If the leading edge dimmer is detected, The dimming pull-down current source turns on when the MULT decreases to 0.25V. if None Leading dimmer is detected, the dimming pull-down current source turns on when the MULT decrease at 0.5V, and pull down the rectified line voltage to zero quickly to avoid any mis-detection on the MULT pin.

There are weak/strong dimming pull down current source inside the chip, it can be selected through different resistance on the ZCD pin. Figure 13 shows the selected logic:

If Istrong_DP*(R1+R2//R3)≥Vstrong_DP

Strong dimming pull-down current source is selected, otherwise, weak dimming pull down current source is selected.

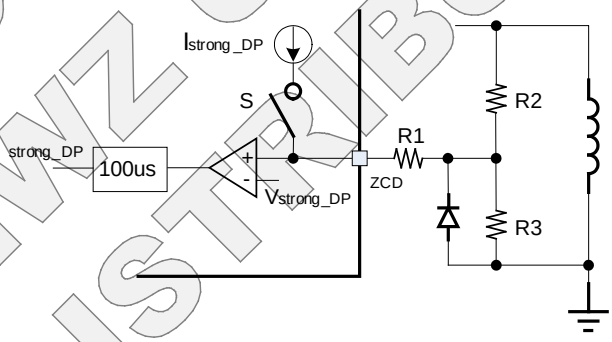

Figure 13: dimming pull down current source selection

Damp Circuit Control

If the leading edge dimmer is detected, the damping circuit is enabled, otherwise it is disabled by pulling up the damp pin voltage. The damp pin voltage begins to be pull up if Vmult>0.35V and begins to be pull down when Vmult<0.25V. the max pull up current source is 100μA while the max pull down current source is 300μA.

Thermal Protection

The NTC pin can be used as the LED thermal protection. An NTC resistor to monitor the LED temperature can be connected to this pin directly. The internal pull up resistor will generate corresponding voltage on the external NTC resistor, and the LED current changes as the Figure 14;

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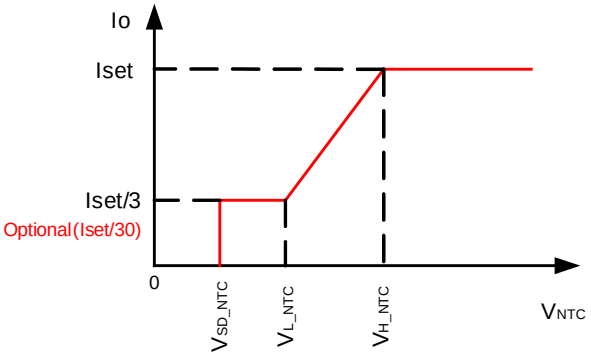


Figure 14: NTC Curve

If the voltage on the NTC pin is lower than the VSD_NTC, the LED current can be zero, so the LED lamp can be shutdown by pulling down NTC pin.

As additional, to prevent from any lethal thermal damage, when the inner temperature exceeds OTP threshold, the MP4033 shuts down switching cycle and latched until VCC drop below UVLO and restart again.

PWM dimming

Apply a PWM signal to the NTC pin can dim the LED brightness, this feature can dramatically reduce the BOM cost for the PWM dimming system.

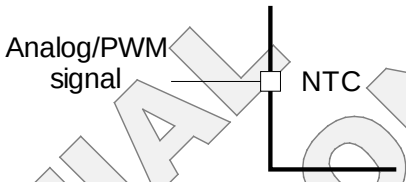
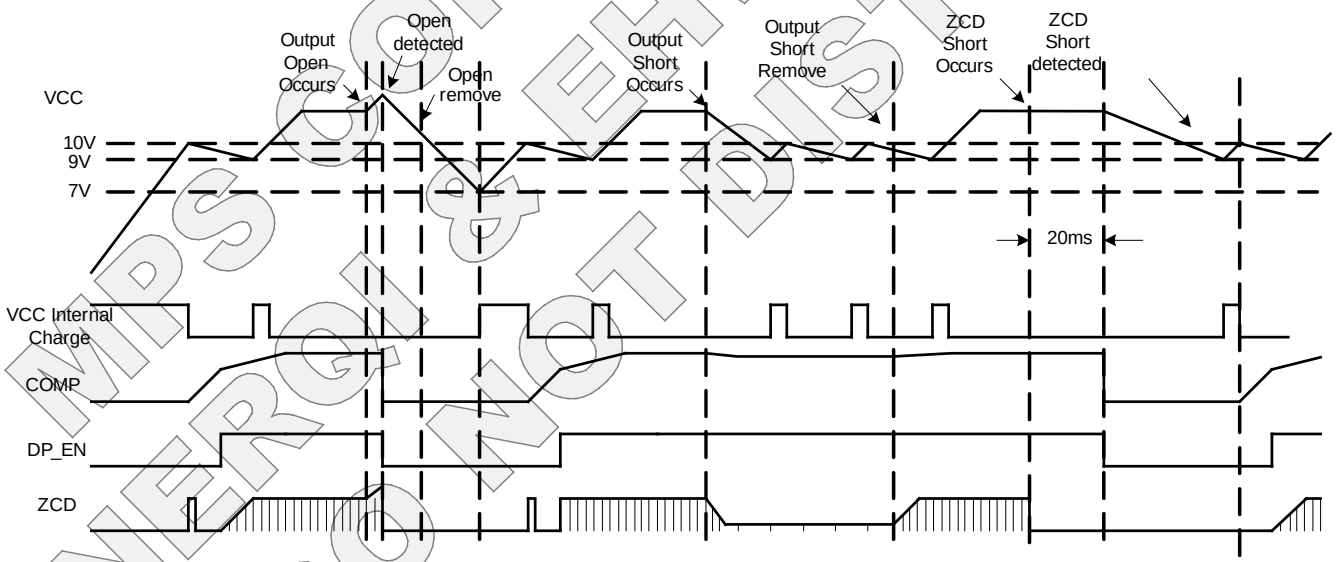


Figure 15: Analog/PWM Dimming interface

ZCD Short Circuit Protection

If the ZCD voltage is lower than the Short Circuit Protection for 20ms (only counting the Dimming On time for both phase-cut dimming and PWM dimming), the ZCD Short Circuit Protection is recognized, and the gate will keeping off until the VCC recycle.

Time Sequence



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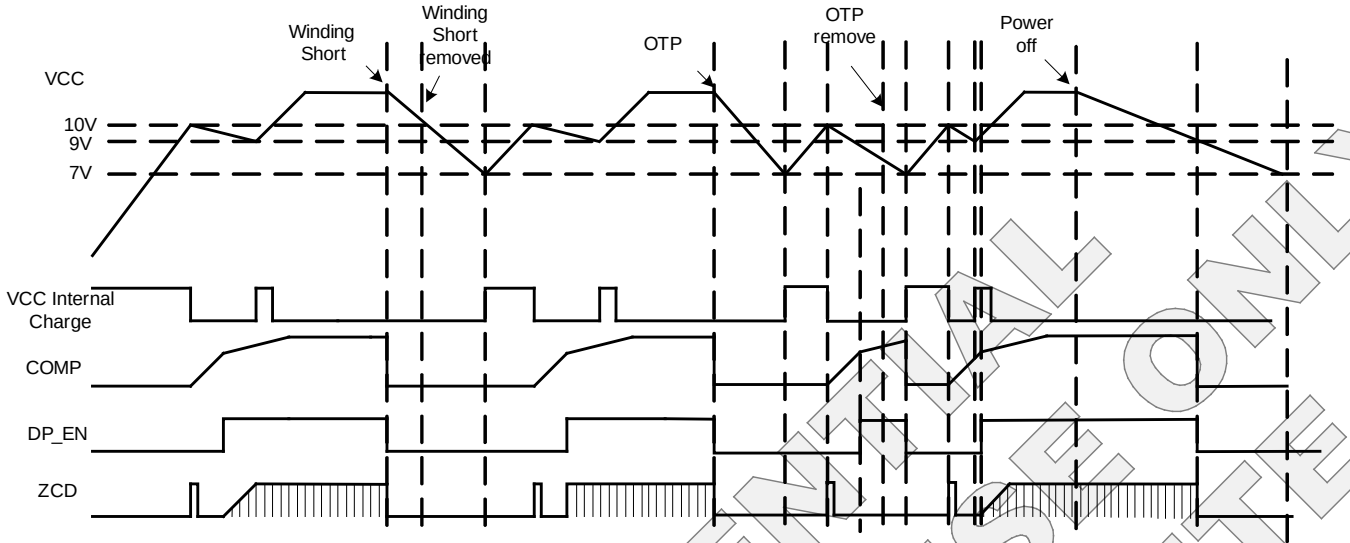

Figure 16:Time Sequence

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TYPICAL APPLICATION CIRCUITS

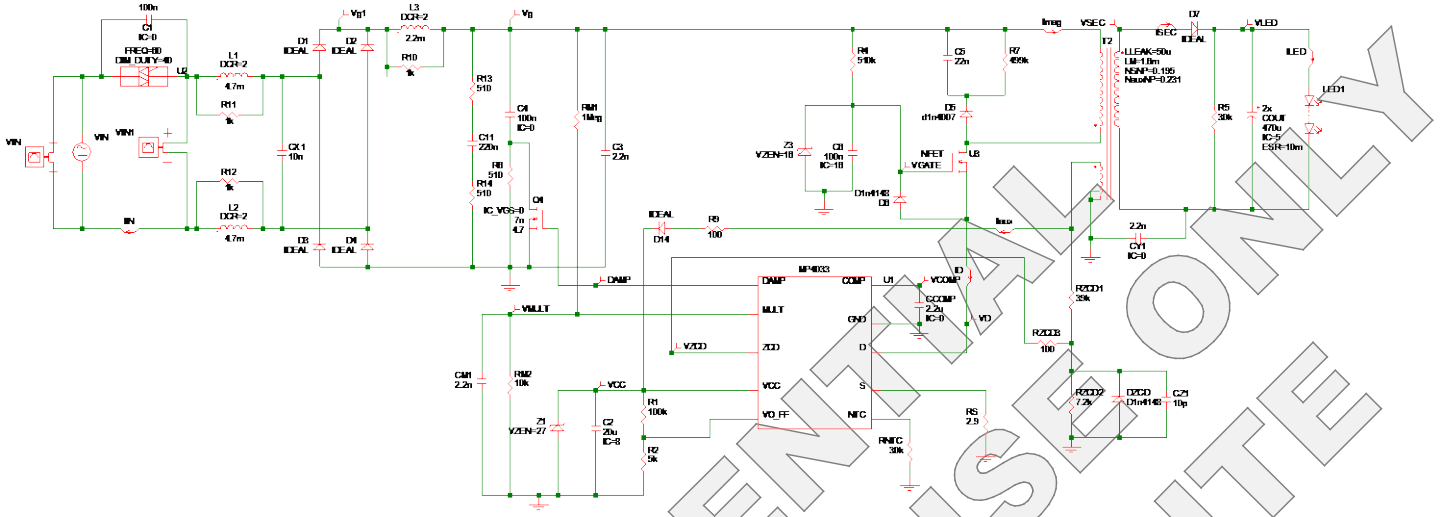

Figure 17: Application Circuit

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PACKAGE INFORMATION

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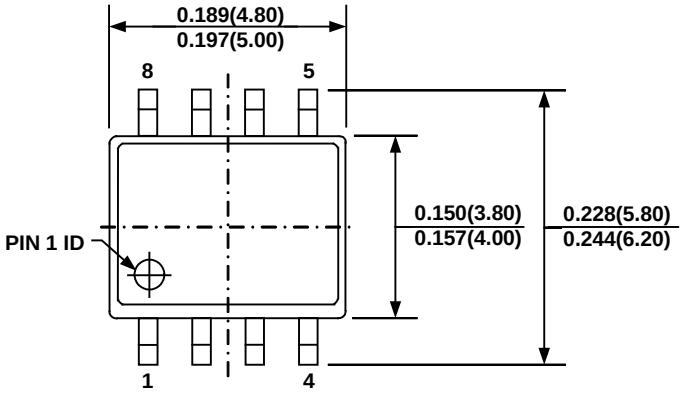
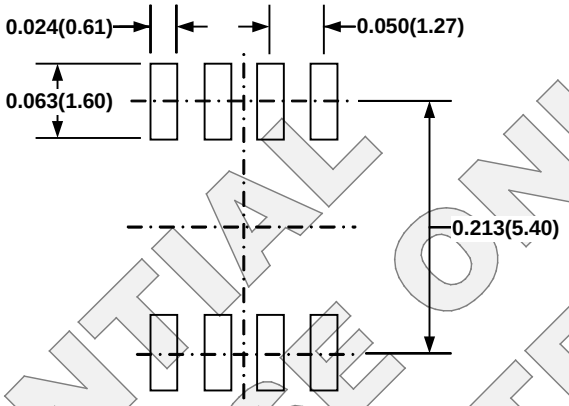


TOP VIEW



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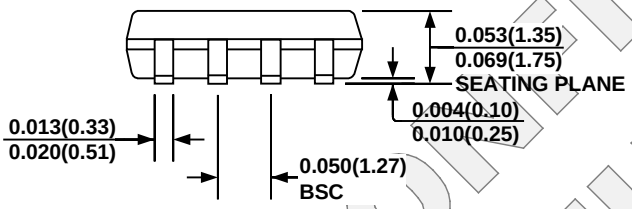
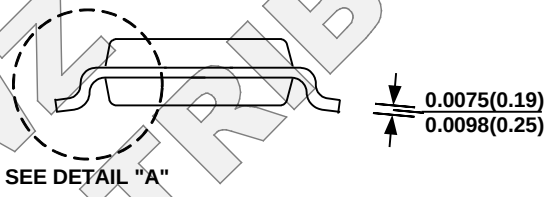
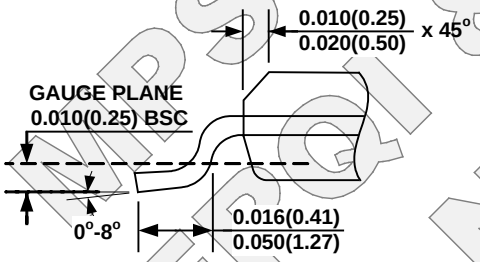


FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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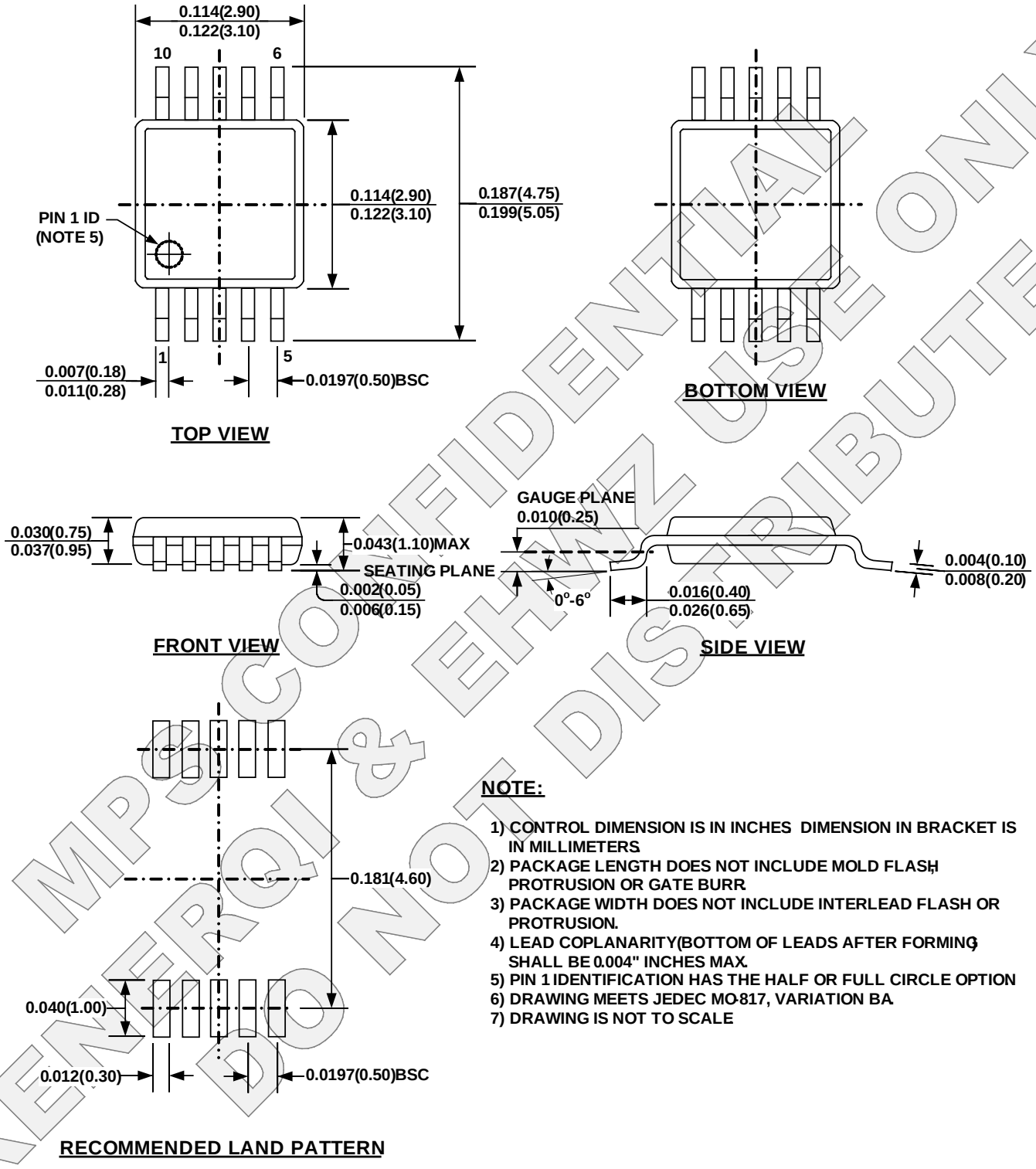

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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
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