DIGITAL IC

1.0 General Description

The PN8162 is a high performance AC/DC power supply control device which uses digital control technology to build peak current mode PWM flyback power supplies. This device includes an internal power BJT and operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design, and lowering the total bill of material cost. The PN8162 removes the need for secondary feedback circuit while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability in all operating conditions. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.
GlobalSemi's innovative proprietary technology ensures that power supplies built with the PN8162 can achieve the highest average efficiency, lowest standby power consumption, and fast smooth startup with a wide range of output voltage, that are ideal for LED lighting applications.

Features

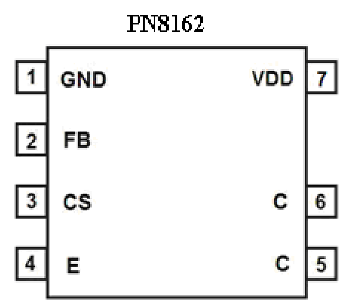
- ◆ No-load power consumption < 30mW at 230VAC with typical application circuit
- ◆ Supports universal input voltage range (90VAC to 277VAC)
- ◆ Isolated design without opto-coupler
- ◆ Internal 800V power bipolar junction transistor (BJT)
- ◆ Very tight LED current regulation (±5%) across line and load, and within primary inductance tolerance (±20%)
- ◆ Supports wide range of capacitive loads (from 33μF to 2000μF or higher)
- ◆ Intrinsically low common mode noise
- ◆ Adaptively controlled soft start-up enables fast and smooth LED current start-up
- ◆ Optimized 72kHz maximum PWM switching frequency achieves best size and efficiency
- ◆ Quasi-resonant operation for highest overall efficiency
- ◆ Dynamic base current control to drive internal BJT
- ◆ No external compensation components required
- ◆ Built-in short circuit protection and output overvoltage protection
- ◆ No audible noise over entire operating range
- ◆ No external compensation components required

Applications

- Cell Phone Charger
- Solid-state LED lighting
- LED lighting ballast

2.0 Products Information

2.1 Pin configuration



Pin Configuration: PN8162 Series (SOIC-7)

Pin Name	I/O	Description
GND	P	Ground.
FB	I	Analog Input Auxiliary voltage sense (used for primary regulation).
CS	I	Analog Input Primary current sense. Used for cycle-by-cycle peak current control and limit.
E	Emitter	Emitter of internal BJT（pin3 and pin4 must be shorted externally on the PCB）.
C	Collector	Collector of internal bipolar junction transistor（BJT）.
VDD	P	Power supply for control logic.

2.2 Marking Information

Part Number	Marking Information
PN8162	PNXXX

2.3 Series description

Part Number	Description
PN8162-10	Cable Comp = 0mV
PN8162-11	Cable Comp = 150mV
PN8162-13	Cable Comp = 300mV

2.4 Block diagram

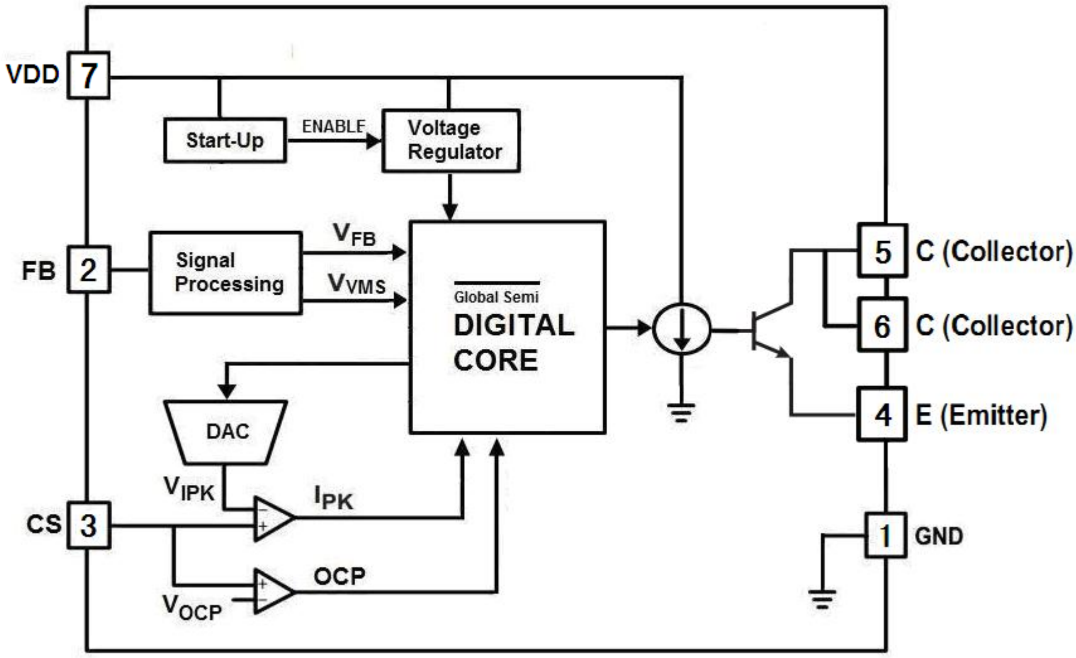


Figure2.1 PN8162 Functional Block Diagram

3.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
DC supply voltage range (pin 7, I_{DD} = 20mA max)	V_{DD}	-0.3 to 18.0	V
Continuous DC supply current at V_{DD} pin (V_{DD} = 15 V)	I_{DD}	20	mA
FB input (Pin 2, $I_{FB} \leq$ 10mA)		-0.7 to 4.0	V
CS input (Pin 3)		-0.3 to 4.0	V
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-up test per JEDEC 78		±100	mA
Collector-Emitter breakdown voltage (Emitter and base shorted together; IC = 1mA, REB = 0Ω)	VCES	800	V
Collector current1	IC	1.5	A
Collector peak current1 (tp < 1ms)	ICM	3	A
Maximum junction temperature	$T_{J\ MAX}$	150	℃
Storage temperature	T_{STG}	–55 to 150	℃
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	℃

Parameter	Symbol	Value	Units
Thermal Resistance Junction-to-Ambient	θ_{JA}	132	℃/W
Thermal Resistance Junction-to-GND pin (pin 5)2	Ψ_{JB}	71	℃/W
Thermal Resistance Junction-to-Collector pin	Ψ_{J-B}	49	℃/W

Notes:

1. θ_{JA} is measured in a one-cubic-foot natural convection chamber.

2. ψ_{JB} [Psi Junction to Board] provides an estimation of the die junction temperature relative to the PCB [Board] surface temperature. ψ_{J-BJT} [Psi Junction to Collector pin] provides an estimation of the die junction temperature relative to the collector pin [internal BJT Collector] surface temperature. ψ_{JB} is measured at the ground pin (pin 1) without using any thermal adhesives.

4.0 Typical Application

The PN8162 contains a controller for a flyback circuit.

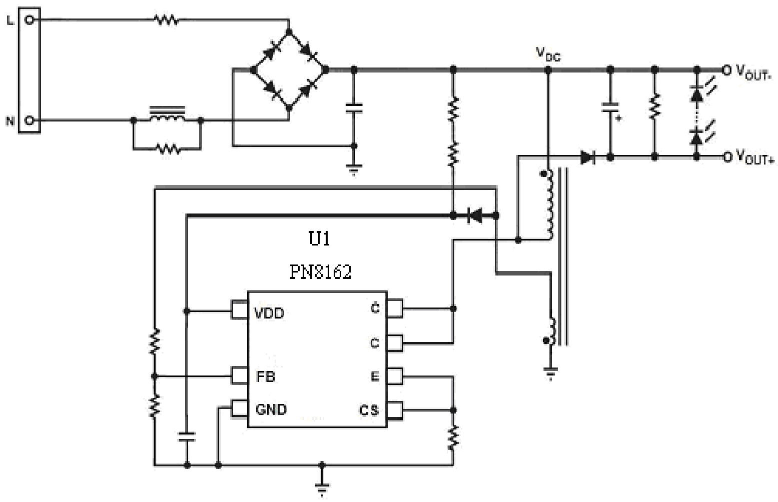


Figure4.1 PN8162 Typical Application Circuit (Non-Isolated Application)

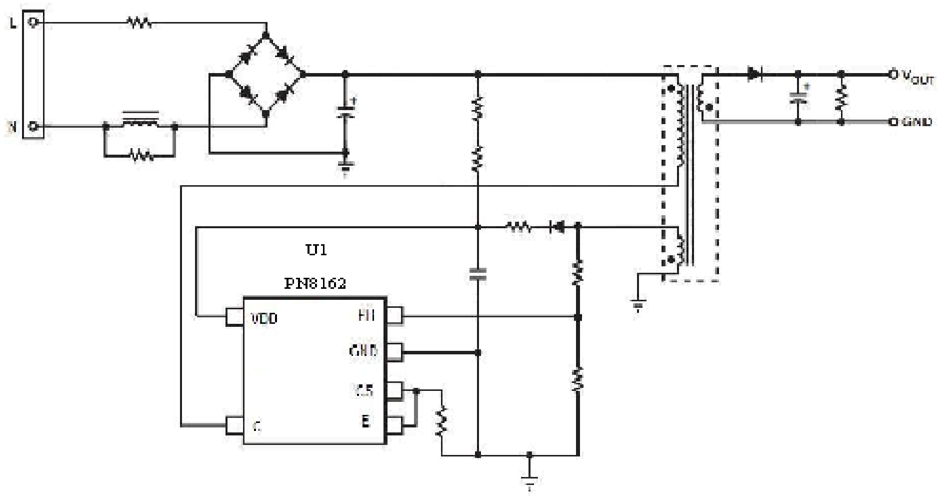


Figure4.2 Typical Application Circuit (Isolated Application)

5.0 Electrical Characteristics

(TA=25℃, V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (Pin8)						
$V_{DD(MAX)}$	Maximum operating voltage (Note 1)				16	V
$V_{DD(ST)}$	Start-up threshold	V_{DD} rising	10.0	11.0	12.0	V
$V_{DD(UVL)}$	Under voltage lockout threshold	V_{DD} falling	3.8	4.0	4.2	V
$I_{IN(ST)}$	Start-up current	V_{DD} = 10V	1.0	1.7	3.0	uA
I_{DDQ}	Quiescent current	No I_B current		2.7	4.0	mA
V_{ZB}	Zener breakdown voltage	Zener current=5mA	18.5	19.5	20.5	V
Feedback (Pin2)						
I_{BVS}	Input leakage current	V_{FB}=2V			1	uA
$V_{FB(NOM)}$	Nominal voltage threshold	TA=25°C, negative edge	1.518	1.533	1.548	V
VFB(MAX)	Output OVP threshold	TA=25°C, negative edge		1.834		V
CS Section (Pin3)						
V_{OCP}	Over current threshold		1.11	1.15	1.19	V
$V_{IPK(HIGH)}$	I_{CS} regulation upper limit (Note 1)			1.0		V
$V_{IPK(LOW)}$	I_{CS} regulation lower limit (Note 1)			0.23		V
I_{LK}	Input leakage current	V_{CS}=1.0V			1	uA
BJT Section (Pin4，Pin5，and Pin6)						
ICBO	Collector cutoff current	VCB = 800V, IE = 0A			0.01	mA
ICES	Collector-Emitter cutoff current	VCE = 800V, REB = 0Ω TA = 25°C			0.01	mA
		VCE = 800V, REB = 0Ω TA = 100°C			0.02	
		VCE = 450V, REB = 0Ω TA = 25°C			0.005	
hFE	DC Current Gain	VCE = 5V, IC = 0.2A	15		40	
		VCE = 5V, IC = 0.3A	10		30	
		VCE = 5V, IC = 1mA	10			
VCBO	Collector-Base breakdown voltage	IC = 0.1mA	800			V
VCES	Collector-Emitter breakdown voltage (Emitter and base shorted together)	IC = 1mA, REB = 0Ω	800			V

VCEO(SUS)	Collector-Emitter sustain voltage	IC = 1mA, LM = 25mH	450			V
VCE(SAT)	Collector-Emitter saturation voltage2	IC = 0.1A, IB = 0.02A		0.1	0.3	V
F_{SW}	Switching frequency (Note 2)	> 50% load		72		kHz

Notes:

1.These parameters are not 100% tested and guaranteed by design and characterization.

2. Impulse tP ≤ 300μs, duty cycle ≤ 2%.

3. Operating frequency varies based on the load conditions, see Section 7.6 for more details.

6.0 Typical Performance Characteristics

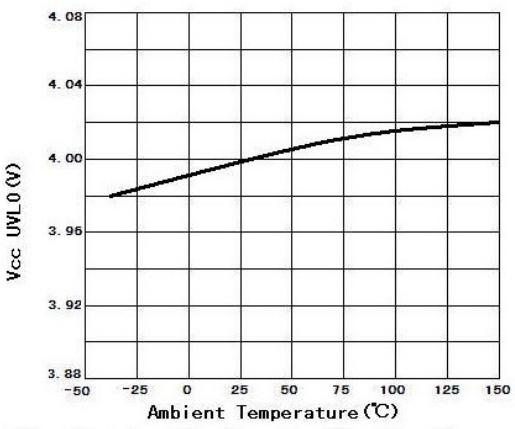


Figure 6.1 VCC UVLO vs. Temperature

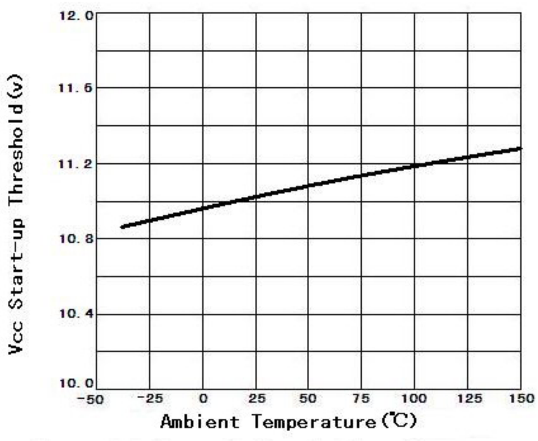


Figure 6.2 Start-Up Threshold vs. Temperature

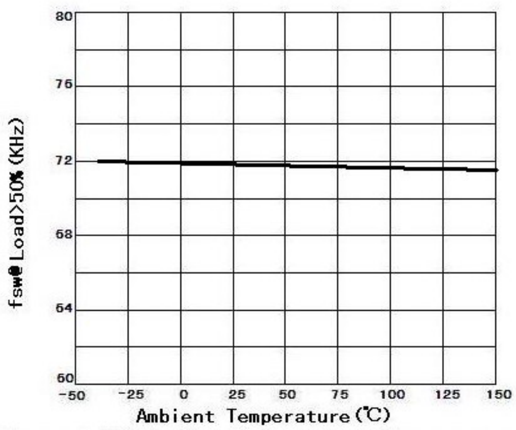


Figure 6.3 Switching Frequency vs. Temperature

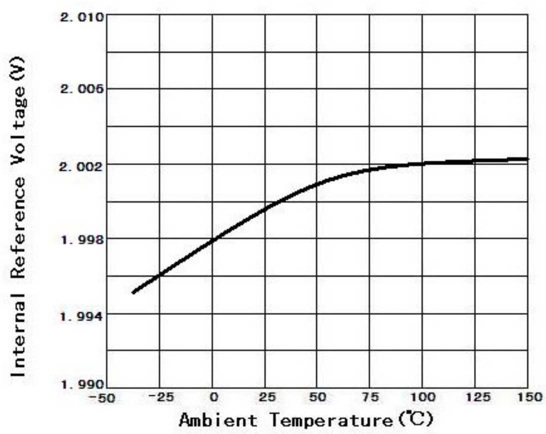


Figure 6.4 Internal Reference vs. Temperature

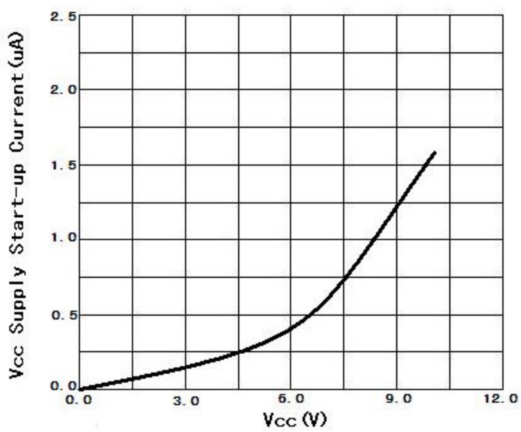


Figure 6.5 VCC vs. VCC Supply Start-up Current

Notes:

Note 1. Operating frequency varies based on the load conditions, see Section 7.6 for more details.

7.0 Theory of Operation

The PN8162 is a digital controller integrated with a power BJT. It uses a proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power LED driver. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, GlobalSemi's digital control technology enables tight output regulation, low no-load power consumption, and full-featured circuit protection with primary-side control.

The block diagram in Figure 2.1 shows the digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides instructions to dynamically control the internal BJT base current. The CS is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the VIPK sets the threshold for the CS to compare with, and it varies in the range of 0.23V (typical) and 1.00V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The PN8162 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The PN8162 uses adaptive multi-mode PWM/PFM control to dynamically change the BJT switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique BJT quasi-resonant switching to further improve efficiency and reduce EMI. The built-in single-point fault protection features include over-voltage protection (OVP), output-short-circuit protection (SCP), over-current protection (OCP), and CS fault detection. GlobalSemi's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new requirements for green mode operation with more practical design considerations such as the lowest possible cost, smallest size and high performance output control.

7.1 Pin Detail

Pin 1 – GND
Ground.

Pin 2 – FB
Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 3 – CS
Primary current sense. It is used for cycle-by-cycle peak current control and limit

Pin 4 – E
Emitter pin of the internal power BJT. This pin must be shorted to pin 7 (the CS pin).

Pin 5 and Pin 6 - C
Collector pin of the internal power BJT.

Pin 7 – VDD
Power supply for the controller during normal operation. The controller will start up when VDD reaches 11.0V (typical) and will shut-down when the VDD voltage is 4.0V (typical). A decoupling capacitor should be connected between the VDD pin and GND.

7.2 Active Start-up and Soft-start

The PN8162 features a proprietary soft-start scheme to achieve fast build-up of output voltage and smooth ramp-up of LED current for a variety of output conditions including output voltage up to 100V or above and output capacitor ranging from 33μF to 2000μF or higher. Prior to the start-up, the VDD pin is charged through startup resistors. When VDD bypass capacitor is fully charged to a voltage higher than the start-up threshold VDD(ST), the ENABLE signal becomes active to enable the control logic, and the PN8162 commences the soft-start function. During the soft-start process, the primary-side peak current is limited cycle by cycle by the IPEAK comparator. The whole soft-start process can break down into several stages based on the output voltage levels, which is indirectly sensed by FB signal at the primary side. At different stages, the PN8162 adaptively controls the switching frequency and primary-side peak current such that the output voltage can always build up very fast at the early stages before LEDs light up, and smoothly transition to the desired regulation current level, regardless of any capacitive loads that the applications may incur.

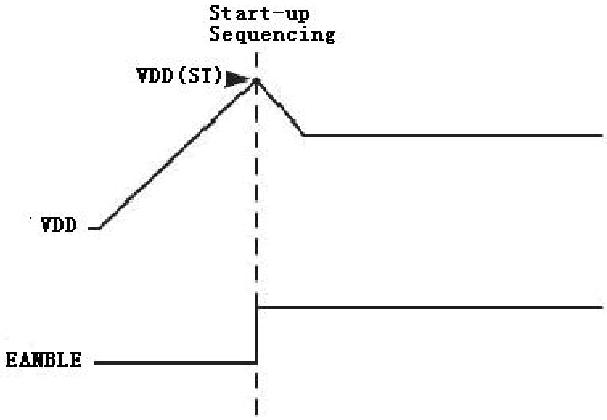


Figure 7.1: Start-up Sequencing Diagram

7.3 Understanding Primary Feedback

Figure 7.2 illustrates a simplified flyback converter. When the switch Q1 conducts during tON(t), the current ig(t) is directly drawn from the rectified sinusoid vg(t). The energy EG(t) is stored in the magnetizing inductance LM. The rectifying diode D1 is reverse biased and the load current IO is supplied by the secondary capacitor CO. When Q1 turns off, D1 conducts and the stored energy Eg(t) is delivered to the output.

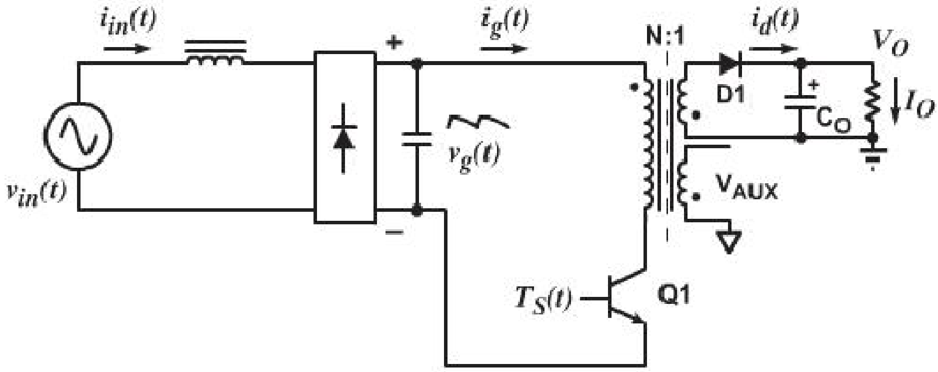


Figure 7.2: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (7.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (7.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (7.3)$$

When Q1 turns off at t_o, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_o, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (7.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

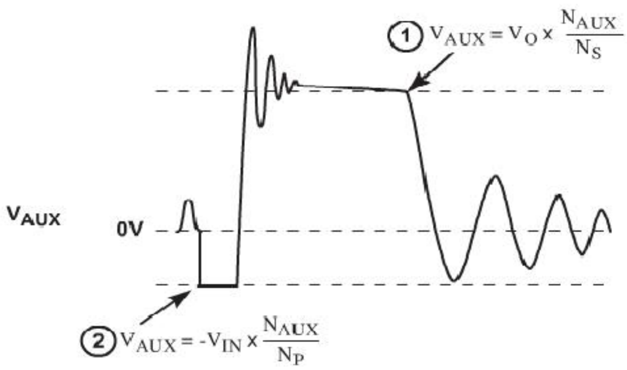


Figure 7.3: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (7.5)$$

and reflects the output voltage as shown in Figure 7.3.The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV will also be small. With the PN8162 ΔV can be ignored.

The real-time waveform analyzer in the PN8162 reads this information cycle by cycle. The part then generates a feedback voltage VFB. The VFB signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

7.4 Constant Current Operation

The PN8162 employs a patented primary-side-only technology to regulate output current. It senses the load current indirectly through the primary current. The primary current is detected by the CS pin through a resistor from the BJT emitter to ground.

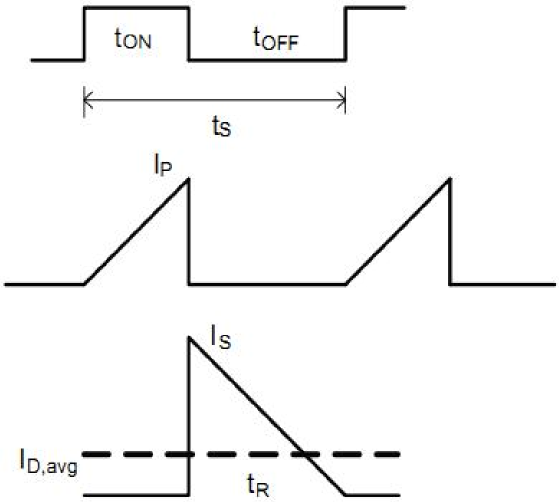


Figure 7.4: Constant Current Operation

The cycle-by-cycle averaged current of the secondary diode current is determined by:

$$I_{D,avg} = \frac{1}{2} \times N_{PS} \times \frac{V_{IPK}}{R_{CS}} \times \frac{t_R}{t_S} \qquad (7.6)$$

where the NPS is the transformer turns-ratio (primary over secondary), and RCS is the current sense resistor connected from the CS pin to GND.

In the PN8162, the current ID, avg is controlled in order to achieve good current regulation, while avoiding continuous conduction mode operation During constant current (CC) operation, the output voltage regulation is not guaranteed. The point 1 in Figure 7.3, which reflects output voltage is not regulated to FB(NOM) (i.e. 1.533V). For LED applications, where current regulation is critical, design needs to ensure the point 1 is well below FB(NOM) with some margin.

7.5 Constant Voltage Operation

The PN8162 also incorporates constant voltage (CV) operation, where output voltage maintains constant by regulating the point 1 indicated in Figure 7.3 to FB(NOM) (1.533V typically). During constant voltage operation, the PN8162 may operate in pulse-width-modulation (PWM) mode or pulse-frequency-modulation (PFM) mode, depending on load conditions. In particular, the PN8162 allows the switching frequency to drop as low as 1.8kHz at PFM mode, which helps system stay regulated at very light load condition, thus achieving <30mW no-load power consumption and meanwhile improving active operating efficiency by using large pre-load resistor.

Figure 7.5 shows power envelope for the PN8162 After soft-start is completed, t.he digital. control block measures the output conditions. It determines output power levels and adjusts the control system to operate either in CV mode or CC mode.

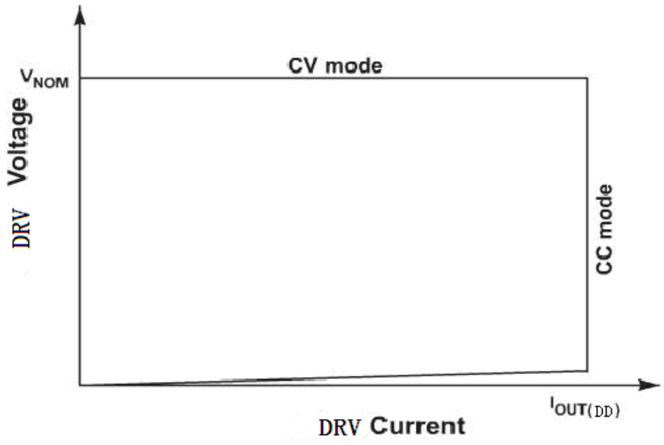


Figure 7.5: Power Envelope

If no voltage is detected on FB, it is assumed that the auxiliary winding of the transformer is either open or shorted and the PN8162 shuts down.

7.6 Variable Frequency Operation Mode

During each of the switching cycles, the falling edge of FB is checked. If the falling edge of FB is not detected, the off-time is extended until the falling edge of FB is detected. This results in the variable switching frequency operation. In particular, the PN8162 may work in constant-current PWM (CC-PWM) mode at high load and costant-current PFM (CC-PFM) mode at ligh load. With CC-PWM mode, the switching frequency is at 72kHz, while during CC-PFM mode, the VIPK is fixed at 0.76V, and the switching frequency varies for different output loads.

In the PN8162, the maximum transformer reset time allowed is 125μs. When the transformer reset time reaches 125μs, the PN8162 shuts off.

7.7 Internal Loop Compensation

The PN8162 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

7.8 Voltage Protection Features

The secondary maximum output DC voltage is limited by the PN8162. When the FB signal exceeds the output OVP threshold at point 1 (as shown in Figure 7.3), the PN8162 shuts down.

The PN8162 protects against input line under-voltage by setting a maximum TON time. Since output power is proportional to the squared VINTON product, for a given output power, the TON increases as the VIN decreases. Thus by knowing when the maximum TON time occurs, the PN8162 detectsthat the minimum VIN is reached, and then it shuts down. The maximum TON limit is set to 15.6μs. Also, the PN8162 monitors the voltage on the VCC pin and when the voltage on this pin is below UVLO threshold the IC shuts down immediately.

When any of these faults is met the IC remains biased to discharge the VCC supply. Once VCC drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

7.9 LED Open and Short Protections

The constant voltage operation in the PN8162 provides protection against LED open fault. During normal operation, the PN8162 operates in CC mode with the output voltage below the nominal voltage set by FB(NOM). After LED is open, the output voltage will be pushed higher momentarily. Depending on the output capacitor and LED operating current, system may gradually settle down and stay regulated at constant voltage operation at no-load condition. Or, if the output voltage overshoot exceeds the output OVP threshold set by FB(OVP) in Section 5.0, the PN8162 shuts down.

LED short fault is detected via FB pin. When the point 1 in Figure 7.3 is below 115mV for several consecutive cycles, the PN8162 shuts down.

When any of these faults are met the IC remains biased to discharge the VCC supply. Once VCC drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

7.10 PCL, OCP and SRS Protection

The peak-current limit (PCL), over-current protection (OCP) and sense-resistor short protection (SRSP) are built-in features in the PN8162. With the CS pin the PN8162 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the CS resistor is greater than

1.15V, over-current protection (OCP) is detected and the IC immediately turns off the base driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the PN8162 shuts down.

If the CS resistor is shorted, there is a potential danger that the over-current condition is not detected. Thus, the IC is designed to detect this sense-resistor-short fault after start-up and immediate shutdown. The VCC is discharged since the IC remains biased.

Once the VCC drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

7.11 Dynamic Base Current Control

An important feature of the PN8162 is that it directly drives an internal BJT switching device with dynamic base current control to optimize performance. The BJT base current ranges from 10mA to 31mA, and is dynamically controlled according to the power supply load change. The higher the output power, the higher the base current. Specifically, the base current is related to VIPK, as shown in Figure 7.6.

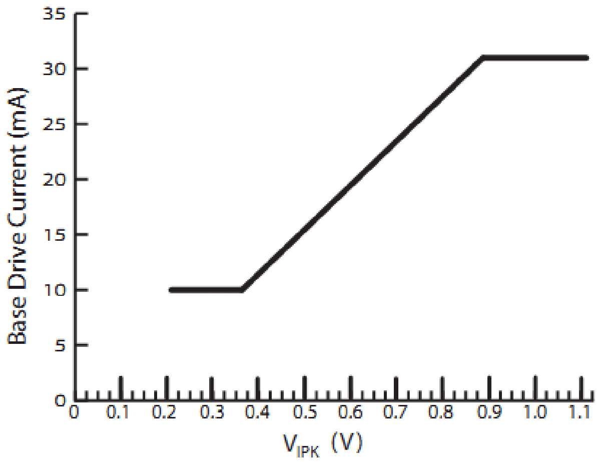
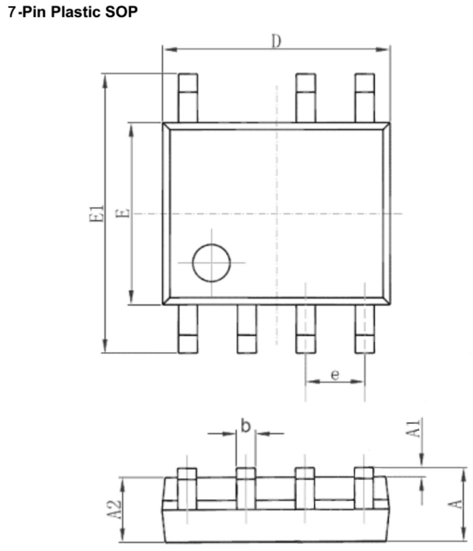


Figure 7.6: Base Drive Current vs. V_{IPK}

8.0 Package Information

SOIC-7



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial Level and Lead-Free.
Qualification Standards can be found on GS's Web site.