AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



1.0 Features

- Isolated AC/DC off-line LED driver
- Power factor > 0.95 for wide input voltage range 100 - 277V_{AC}
- Total harmonic distortion (THD) < 10%
- Under 5% 100Hz/120Hz output current ripple
- Resonant control to achieve high efficiency
- LED current foldback with external NTC
- Small size design
 - » Small size input bulk capacitor
 - » Small size output capacitor
 - » Small transformer
- Primary-side sensing eliminates the need for opto-isolator feedback and simplifies design
- Tight LED current regulation ± 5%
- Under 0.5 second start-up time
- Hot-plug LED module support
- Multiple protection features:
 - » LED open circuit protection
 - » Single-fault protection
 - » Over-current protection
 - » LED short-circuit protection
 - » Current sense-resistor-short-circuit protection
 - » Input over-voltage and brown-out protection

2.0 Description

The iW3623 is a high-performance AC/DC off-line power supply controller for LED luminaires. The iW3623 combines power factor correction and LED current regulation into one controller. It achieves PF > 0.95 and THD < 10% for 100–277 V_{AC} input voltage range.

The iW3623 operates in quasi-resonant mode to provide high efficiency. The device uses iWatt's advanced primary-side sensing technology to achieve excellent line and load regulation without secondary-feedback circuit. In addition, the iW3623's pulse-by-pulse waveform analysis technology allows accurate LED current regulation. The iW3623 maintains stability over all operating conditions without the need for loop compensation components.

3.0 Applications

- Non-dimmable LED lamps and luminaires
- · Optimized for up to 40W output power



AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



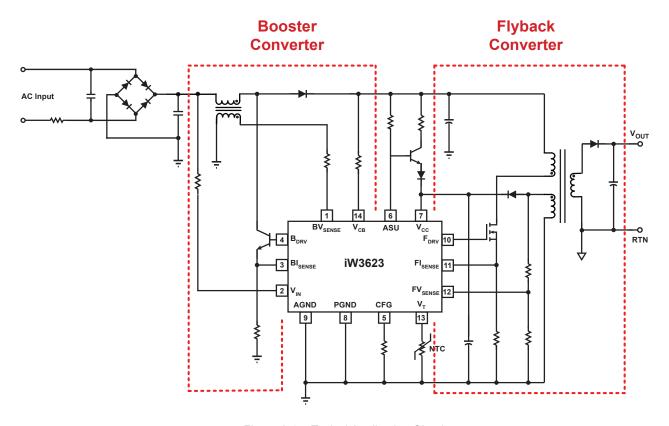


Figure 3.1: Typical Application Circuit

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



4.0 Pinout Description

iW3623							
1	BV _{SENSE}	V _{CB}	14				
2	V _{IN}	V_{T}	13				
3	BISENSE	FV _{SENSE}	12				
4	B _{DRV}	FISENSE	11				
5	CFG	F_{DRV}	10				
6	ASU	AGND	9				
7	v _{cc}	PGND	8				

Pin#	Name	Туре	Pin Description
1	BV _{SENSE}	Analog Input	Boost inductor voltage feedback
2	V _{IN}	Analog Input	Rectified AC line voltage feedback
3	BI _{SENSE}	Analog Input	Boost current sense (used for cycle-by-cycle peak current limit)
4	B_{DRV}	Output	Base drive for Boost BJT
5	CFG	Analog In/Out	Chooses input start-up voltage and brown-out shutdown voltage
6	ASU	Output	Active start-up control
7	V_{cc}	Power	Power supply for control logic and voltage sense for power-on reset circuitry
8	PGND	Ground	Power ground
9	AGND	Ground	Signal ground
10	F_{DRV}	Output	Gate drive for Flyback MOSFET
11	FI _{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit)
12	FV _{SENSE}	Analog Input	Auxiliary voltage sense (used for primary-side regulation and ZVS)
13	V_{T}	Analog Input	Output power limit and shutdown control
14	V_{CB}	Analog Input	Boost output voltage feedback

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 7, I _{CC} = 20mA max)	V _{CC}	-0.3 to 18	V
DC supply current at V _{CC} pin	I _{cc}	20	mA
F _{DRV} output (pin 10)		-0.3 to 18	V
B _{DRV} output (pin 4)		-0.3 to 4.0	V
CFG input (pin 5)		-0.3 to 4.0	V
CFG output (pin 5)		-0.3 to 18	V
FV _{SENSE} input (pin 12, I ≤ 10mA)		-0.7 to 4.0	V
BV _{SENSE} input (pin 1, I ≤ 3mA)		-0.7 to 4.0	V
V _{IN} input (pin 2)		-0.3 to 18	V
V _{CB} input (pin 14)		-0.3 to 18	V
FI _{SENSE} input (pin 11)		-0.3 to 4.0	V
BI _{SENSE} input (pin 3)		-0.3 to 4.0	V
ASU output (pin 6)		-0.3 to 18	V
V _T input (pin 13)		-0.3 to 4.0	V
Power dissipation at T _A ≤ 25°C		900	mW
Maximum junction temperature	T _{J MAX}	150	°C
Storage temperature	T _{STG}	-65 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T _{LEAD}	260	°C
Thermal Resistance Junction-to-PCB Board Surface Temperature	Ψ _{JB} (Note 1)	45	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-up test per JEDEC 78		±100	mA

Notes:

Note 1. ψ_{JB} [Psi Junction to Board] provides an estimation of the die junction temperature relative to the PCB surface temperature. This data is measured at the ground pins (pin 8 and pin 9) without using any thermal adhesives.

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



6.0 Electrical Characteristics

 V_{CC} = 12 V, -40°C \leq T_A \leq 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
V _{IN} SECTION						
Object was confidence that a let (Night O)	V	$T_A = 25^{\circ}C$, CFG resistor = $20k\Omega$		0.283		V
Start-up voltage threshold (Note 2)	V_{IN_ST}	$T_A = 25^{\circ}\text{C}$, CFG resistor = 4.7k Ω		0.212		V
Drawn out throughold (Note 2)	V	$T_A = 25^{\circ}\text{C}$, CFG resistor = $20\text{k}\Omega$		0.283		V
Brown-out threshold (Note 3)	V_{BR_TH}	$T_A = 25^{\circ}C$, CFG resistor = $4.7k\Omega$		0.212		V
Over-voltage shutdown threshold	V_{IN_OVP}	T _A = 25°C, positive edge	1.512	1.68	1.848	V
Input impedance	Z _{IN}	After start-up		5		kΩ
V _{IN} range	V _{IN}		0		1.8	V
V _{CB} SECTION						
Over-voltage shutdown threshold	$V_{\text{CB_OVP}}$	T _A = 25°C, positive edge	1.62	1.8	1.98	V
Input impedance	Z _{CB}	After start-up		15		kΩ
V _{CB} range	V _{CB}		0		1.8	V
FV _{SENSE} SECTION						
Input leakage current	 BVS(FVSENSE)	V _{SENSE} = 2V			1	μΑ
Normal voltage threshold	$V_{\text{SENSE(NOM)}}$	T _A = 25°C, negative edge	1.521	1.536	1.551	V
Output OVP threshold (default)	$V_{\text{SENSE(MAX)}}$	T _A = 25°C, negative edge	1.683	1.7	1.717	V
BV _{SENSE} SECTION						
Input leakage current	I _{BVS(BVSENSE)}	V _{SENSE} = 0.1V			1	μΑ
F _{DRV} SECTION						
Output low level ON-resistance	R _{DS_ON_LO(FDRV)}	I _{SINK} = 5mA		16		Ω
Output high level ON-resistance 1	R _{DS_ON_HI(FDRV)}	I _{SOURCE} = 5mA		25		Ω
Maximum switching frequency (Note 4)	f_SW_FDRV(MAX)			200		kHz
B _{DRV} SECTION						
Output low level ON-resistance	$R_{DS_ON_LO(BDRV)}$	I _{SINK} = 5mA		1		Ω
Maximum switching frequency	f _{SW_BDRV(MAX)}	if V _{IN_A} < 130mV		200		kHz
(Note 4)	2M RDKA(WYX)	if V _{IN_A} > 130mV		90		kHz
Output source current	I _B				90	mA

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



6.0 Electrical Characteristics (cont.)

 V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
ASU SECTION						
Maximum operating voltage	V _{ASU(MAX)}				18	V
Resistance between V _{cc} and ASU	R _{VCC_ASU}			830		kΩ
V _{cc} SECTION						
Maximum operating voltage	$V_{CC(MAX)}$				17	V
Start-up threshold	$V_{CC(ST)}$		11.5	12.5	13.5	V
Under-voltage lockout threshold	$V_{CC(UVL)}$		6.0	6.5	7.0	V
Operating current	I _{CCQ}			6.5		mA
ASU turn-off threshold	V _{CC_ASU_OFF}			16.25		V
FI _{SENSE} SECTION						
CC regulation threshold limit	V _{REG_TH(FLYBACK)}			1.4		V
I _{SENSE} short protection reference	V _{RSENS(EFLYBACK)}			0.16		V
Over-current limit threshold	V _{OCP(FLYBACK)}			1.5		V
BI _{SENSE} SECTION						
I _{SENSE} short protection reference	V _{RSENSE(BOOST)}			0.15		V
Over-current limit threshold	V _{OCP(BOOST)}			1.9		V
V _T SECTION						
Power limit high threshold (Note 5)	V _{P_LIM(HI)}			0.56		V
Power limit low threshold (Note 5)	V _{P_LIM(LO)}			0.44		V
Shutdown threshold (Note 5)	V _{SH_TH}			0.22		V
Input leakage current	I _{BVS(VT)}	V _{VT} = 1.0V			1	μA

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



6.0 Electrical Characteristics (cont.)

 V_{CC} = 12 V, -40°C \leq T_{Δ} \leq 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Pull-up current source	l _{vt}		90	100	110	μA
CFG SECTION						
Pull-up current source	I _{CFG}		90	100	110	μA

Notes:

- Note 1. Adjust $V_{\rm cc}$ above the start-up threshold before setting at 12V.
- Note 2. V_{IN} pin voltage is greater than $V_{IN ST}$ for more than three miliseconds.
- Note 3. Once $V_{_{\mbox{\scriptsize IN}}}$ pin maximum voltage is less than $V_{_{\mbox{\scriptsize BR}}}$ TH, IC will shut down immediately.
- Note 4. Operating frequency varies based on the line and load conditions. See the Theory of Operation section for more details.
- Note 5. These parameters refer to digital preset values. They are not 100% tested.

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



7.0 Typical Performance Characteristics

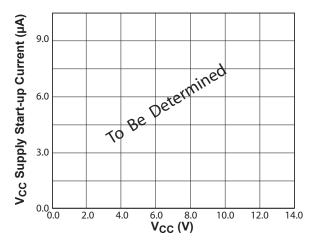


Figure 7.1 : V_{cc} vs. V_{cc} Supply Start-up Current

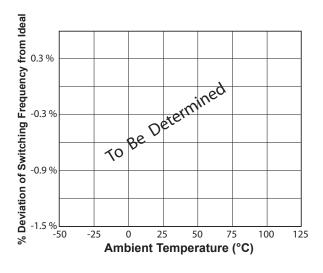


Figure 7.3 : % Deviation of Switching Frequency to Ideal Switching Frequency vs. Temperature

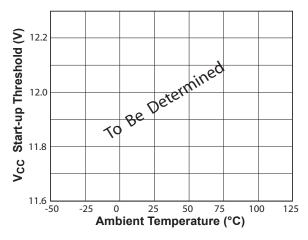


Figure 7.2: Start-Up Threshold vs. Temperature

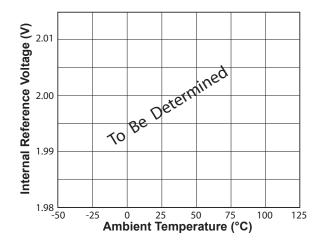


Figure 7.4: Internal Reference vs. Temperature

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



8.0 Functional Block Diagram

The iW3623 uses iWatt's proprietary digital control technology, which consists of: 1) Boost control circuit. 2) Primary-side controlled flyback converter control circuit. It uses iWatt's proprietary BJT boost switch control technique, which achieves high power factor and low THD within wide input voltage range at high efficiency. The flyback controller operates with valley mode switching to achieve high efficiency and minimum EMI. It incorporates iWatt's proprietary primary-feedback constant current control technology to achieve tight LED current regulation.

Figure 8.1 shows the functional block diagram. The advanced digital control mechanism reduces system design time and improves reliability. The start-up algorithm makes sure the $V_{\rm CC}$ supply voltage is ready before powering up the IC.

The iW3623 provides multiple protection features for current limit, over-voltage protection, and over-temperature protection.

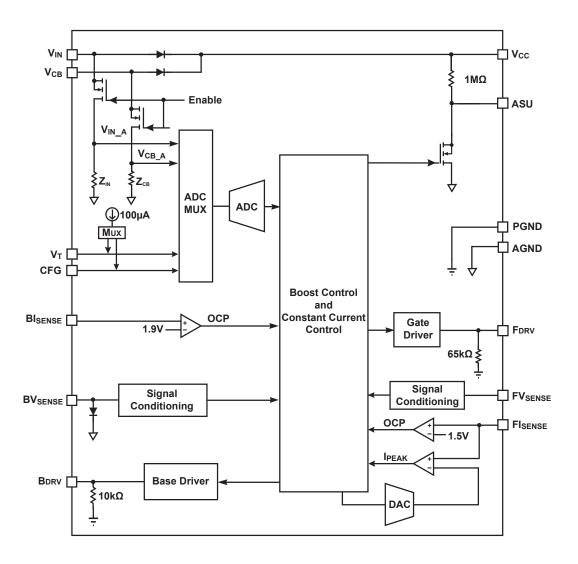


Figure 8.1: iW3623 Functional Block Diagram

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



9.0 Theory of Operation

The iW3623 is a high performance AC/DC off-line power supply controller for non-dimmable LED luminaires.

The iW3623 actively shapes the input current to match the phase of the input voltage to increase power factor (PF) and reduce total harmonic distortion (THD). The LED luminaires can easily conform to the IEC harmonic current limit specifications.

The iW3623 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3623 includes a number of key built-in protection features. Using iWatt's state-of-the-art primary-feedback technology, the iW3623 removes the need for secondary-feedback circuitry while achieving excellent line and load regulation. The iW3623 also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for accurate LED current regulation. The two-stage design can achieve almost zero 2X line frequency output current ripple.

9.1 Pin Detail

Pin 1 - BV_{SENSE}

Sense signal input from boost inductor winding, which provides the boost switching timing feedback used for valley mode switching.

Pin 2 - V_{IN}

Sense signal input from the rectified line voltage. The input line voltage is scaled down using a resistor network. It is used for input over-voltage protection, brown-out protection, and start-up voltage setting.

Pin 3 - BI_{SENSE}

Boost switch current sense. Used for cycle-by-cycle peak current limit.

Pin 4 – B_{DRV}

Base drive for the boost switching circuit BJT switch.

Pin 5 - CFG

Configure the start-up voltage and brown-out voltage through an external resistor during initial start-up.

Pin 6 - ASU

Control the external high voltage start-up switch.

Pin 7 - V_{cc}

Power supply for the controller during normal operation. The controller starts up when $V_{\rm CC}$ reaches 12.5V (typical). The controller shuts down when the $V_{\rm CC}$ voltage is below 6.5V (typical).

High-frequency transients and ripples can be easily generated on the V_{CC} pin due to power supply switching transitions, and line and load disturbances. Excess ripples and noises on V_{CC} may lower the controller function performance. A decoupling capacitor should be connected between the V_{CC} pin and AGND/PGND. It is suggested that a ceramic capacitor of minimum 0.1 μF is connected to the V_{CC} pin as closely as possible.

Pin 8 - PGND

Power ground. This pin should be connected to the negative terminal of the bulk capacitor.

Pin 9 - AGND

Analog ground. This pin should be connected to the PGND.

Pin 10 - F_{DRV}

Gate drive for the flyback circuit MOSFET switch.

Pin 11 - FI_{SENSE}

Primary current sense. Used for cycle-by-cycle peak current control.

Pin 12 – FV_{SENSE}

Sense signal input from auxiliary winding, which provides the secondary voltage feedback used for output regulation.

Pin 13 - V₋

External power limit and shutdown control. If the shutdown control is not used, this pin should be connected to GND via a $20k\Omega$ resistor.

Pin 14 - V_{CR}

Sense signal input from the boost output voltage. $V_{\rm CB}$ is used for boost output voltage regulation. It is also used for boost output over-voltage protection.

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



9.2 IC Start-up

Prior to start-up, the $V_{\rm CC}$ capacitor is charged up through active start-up circuit controlled by the ASU pin, and through the $V_{\rm IN}$ and $V_{\rm CB}$ to $V_{\rm CC}$ internal diodes. When $V_{\rm CC}$ is fully charged to a voltage higher than the start-up threshold $V_{\rm CC(ST)}$, the "Enable" signal becomes active and enables the control logic, as shown in Figure 9.1. The iW3623 detects the input voltage at $V_{\rm IN}$ pin. If the input voltage reaches the start-up threshold, then constant output current mode is enabled and the output-voltage starts to ramp up. When the output-voltage rises above the forward-voltage of LED, the controller operates in constant current mode. The ASU is disabled after the flyback operates for about 50 miliseconds.

The iW3623 implements an output current soft-start. The output current starts at 5% and move quickly to 100% level. This feature helps to eliminate output current overshoot during the start-up.

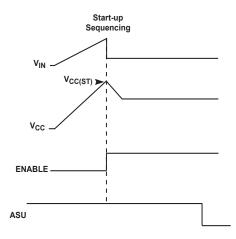


Figure 9.1: Start-up Sequencing Diagram

9.3 **Boost Operation**

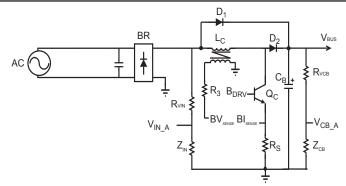


Figure 9.2 : Boost Schematic

The PFC control block provides an on-time (T_{ON}) controlled, valley mode switching power factor correction controller.

The T_{on} is determined by the V_{IN_A} and V_{CB_A} voltage. V_{CB_A} is scaled down from the bus voltage. V_{IN_A} is scaled down from the rectified input voltage.

After power up, V_{IN_A} voltage is monitored. If V_{IN_A} voltage is higher than V_{IN_ST} , IC will send out driver signal to the boost and flyback switch.

The frequency of boost circuit is limited to below 90kHz when $V_{_{\rm IN_A}}$ is greater than 0.13V. It is limited to below 200kHz when $V_{_{\rm IN_A}}$ is less than 0.13V.

The BJT emitter resistor provides over-current protection for boost circuit:

$$I_{OC(MAX)} = V_{OCP \text{ (boost)}} / R_s$$
 (9.1)

To minimize BJT turn-on loss and reduce EMI, the BJT is turned on at valley point of collector pin voltage. This valley signal is sensed by the ${\rm BV}_{\rm SENSE}$ pin connected to a secondary winding on boost choke.

The DC bus voltage is typically 30V above the peak of line voltage. The minimum value is clamped to 200V (see Section 9.5 for bus voltage calculation).

9.4 BJT Drive

One important feature of the iW3623 is that it directly drives a BJT switching device in boost circuit.

In the switching operation mode, the iW3623 drives the BJT with dynamic base current control to optimize performance. The BJT base current ranges from 10mA to 90mA, and it is dynamically controlled according to the BJT peak conducting current. The higher the BJT current, the higher the base current.

9.5 V_{IN} and V_{CB} Resistors

The $V_{\rm IN}$ and $V_{\rm CB}$ pin resistors are chosen primarily to scale down the AC line voltage and input bulk capacitor voltage of the flyback circuit. The typical scale factor $K_{\rm CB}$ and $K_{\rm IN}$ is:

- K_{CB} and K_{IN} = 0.004 for 230V V_{AC} (rms)
- K_{CR} and $K_{IN} = 0.033$ for 277V V_{AC} (rms)

The scale factor can be adjusted to optimize efficiency and power factor. The R_{VIN} and R_{VCB} resistance can be equated by

$$R_{VIN} = Z_{IN} / K_{IN} - Z_{IN}$$
 and $R_{VCB} = Z_{CB} / K_{CB} - Z_{CB}$

The internal impedance Z $_{\rm IN}$ is 5k Ω ± 5%, Z $_{\rm CB}$ is 15k Ω ± 5%. For example, with V $_{\rm IN}$ (rms) = 230V, the V $_{\rm IN}$ and V $_{\rm CB}$ pin resistors should add up to

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



$$R_{VIN} = 5k\Omega / 0.004 - 5k\Omega = 1245k\Omega$$

$$R_{VCB} = 15k\Omega / 0.004 - 15k\Omega = 3735k\Omega$$

The relationship between V_{IN} and V_{CB} pin voltage for boost output voltage regulation is:

$$V_{CB A} = V_{IN A(MAX)} + 0.12V$$

The DC bus voltage is determined by:

$$V_{BUS} = V_{CBA}/K_{CB}$$

 V_{CB_A} regulation range is from 0.8V to 1.48V (for example, when K_{CB} = 0.004, V_{BUS} will be clamped to minimum 0.8/0.004 = 200V).

9.6 Primary Feedback

Figure 9.3 illustrates a simplified flyback converter. When the switch Q_1 conducts during $T_{ON}(t)$, the current $i_g(t)$ is directly drawn from the rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M . The rectifying diode D_1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O . When Q_1 turns off, D_1 conducts and the stored energy $E_g(t)$ is delivered to the output.

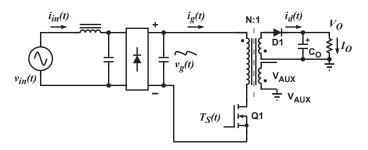


Figure 9.3: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance ($L_{\rm M}$). During the $Q_{\rm 1}$ on-time, the load current is supplied from the output filter capacitor $C_{\rm O}$. The voltage across $L_{\rm M}$ is $v_{\rm g}(t)$, assuming the voltage dropped across $Q_{\rm 1}$ is zero. The current in $Q_{\rm 1}$ ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \tag{9.2}$$

At the end of on-time, the current has ramped up to:

$$i_{g_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_{VV}} \tag{9.3}$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g_peak}(t)^2 \tag{9.4}$$

When Q_1 turns off, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g_peak}(t) \tag{9.5}$$

Assuming the secondary winding is master and the auxiliary winding is slave.

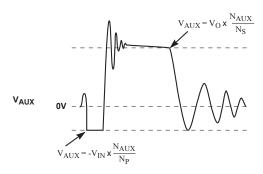


Figure 9.4: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{Ns} (V_O + \Delta V) \tag{9.6}$$

and reflects the output voltage as shown in Figure 9.4.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV . Furthermore, if the voltage can be read when the secondary current is small, for example, at the knee of the auxiliary waveform (see Figure 9.4), then ΔV is also small. With the iW3623, ΔV can be ignored.

The real-time waveform analyzer in the iW3623 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage $V_{\it FB}$. The $V_{\it FB}$ signal precisely represents the output voltage and is used to regulate the output voltage.

PAGE 12

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



9.7 Valley Mode Switching

In order to reduce switching losses in the MOSFET, BJT, and to lower EMI, the iW3623 employs valley mode switching during constant output current operation for both MOSFET and BJT. In valley mode switching, the MOSFET and BJT switches are turned on at the point where the resonant voltage across the drain and source of the MOSFET (or across the collector and emitter of BJT) is at its lowest point (see Figure 9.5). By switching at the lowest $\rm V_{\rm DS}$, the switching loss is minimized.

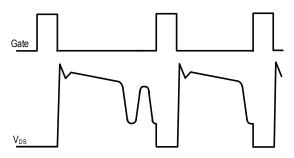


Figure 9.5: Valley Mode Switching

Turning on at the lowest V_{DS} generates the lowest dV/dt, thus valley mode switching can also reduce EMI.

At each of the switching cycles, the falling edge of FV_{SENSE} is checked. If the falling edge of FV_{SENSE} is not detected, the off-time is extended until the falling edge of FV_{SENSE} is detected.

9.8 LED Current Regulation

After soft-start has been completed, the digital block measures the output conditions. When the FV_{SENSE} pin voltage is less than 1.538V, the control system works in constant current (CC) mode. The device regulates the output current I_{OUT} to its nominal value. The iW3623 incorporates a patented primary-side only constant current regulation technology. The iW3623 regulates the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode. To achieve this regulation, the iW3623 senses the load current indirectly through the primary current. The primary current is detected by the FI_{SENSE} pin through a resistor from the MOSFET source to ground.

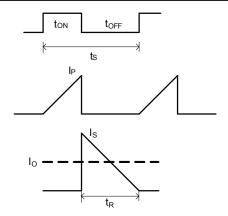


Figure 9.6: Constant LED Current Regulation

The FI_{SENSE} resistor determines the maximum current output of the power supply. The output current of the power supply is determined by:

$$I_{OUT} = \frac{1}{2} \times N_{PS} \times \frac{V_{REG_TH}}{R_{SENSE}} \times \frac{t_R}{t_S}$$
 (9.7)

where $\rm N_{PS}$ is the turns ratio of the primary and secondary windings and $\rm R_{SENSE}$ is the $\rm FI_{SENSE}$ resistor. IC will set $\rm V_{REG_TH}$ to:

$$V_{REG_TH} = K_{CC} \times \frac{t_S}{t_R} \tag{9.8}$$

where $K_{\rm CC}$ is equal to 0.7V. From equation 9.7 and 9.8 we get:

$$I_{OUT} = \frac{1}{2} \times N_{PS} \times \frac{K_{CC}}{R_{SENSE}}$$
 (9.9)

From equation 9.9, $\rm R_{\rm SENSE}$ can be calculated based on $\rm I_{\rm OUT}$ and $\rm N_{\rm PS}.$

9.9 Constant Voltage Mode

If FV_{SENSE} pin voltage is higher than 1.538V, the control system will change T_{ON} and T_{OFF} to regulate the FV_{SENSE} voltage to 1.538V. The device operates in constant voltage (CV) mode. The output current I_{OUT} will be lower than nominal.

If less than 0.2V is detected on $FV_{SENSE,}$ it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW3623 shuts down.

The iW3623 normally operates in a fixed frequency PWM or critical discontinuous conduction mode when $I_{\rm OUT}$ is greater than approximately 10% of the specified maximum load current. As the output load $I_{\rm OUT}$ is reduced, the

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



on-time T_{ON} is decreased. During this mode the PWM switching frequency is between 30kHz and 130 kHz, depending on the line and load conditions. At the moment that the load current drops below 10% of nominal, the controller transitions to Pulse Frequency Modulation (PFM) mode. Thereafter, the on-time is modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.

9.10 CFG Pin

The CFG pin is used to set up start-up and brown-out voltage. The CFG pin outputs 100 μ A current source after V_{cc} reaches the start-up threshold. The start-up voltage is configured based on the information in Table 9.1.

CFG Option	CFG Pin	Resistor			
Number	Value	Tolerance	V _{IN_ST}	V _{BR_TH}	
1	20kΩ	≤ 5%	0.283V	0.283V	
2	4.7k Ω	≤ 5%	0.212V	0.212V	

Table 9.1 CFG Pin Resistor

IC will start sending out drive signal for PFC and flyback circuit after $V_{\rm IN}$ is greater than $V_{\rm IN_ST}$ for three miliseconds.

9.11 PCL, OCP and SRSP Protection

Peak-current limit (PCL), over-current protection (OCP), and sense-resistor short protection (SRSP) are features built into the iW3623.

With the $\mathrm{Fl}_{\mathrm{SENSE}}$ pin the iW3623 is able to monitor the primary-peak current of the flyback circuit. This allows for cycle-by-cycle peak current control and limit. When the primary-peak current multiplied by the $\mathrm{Fl}_{\mathrm{SENSE}}$ sense resistor is greater than 1.5V, over-current is detected and the IC immediately turnes off the gate drive until the next cycle. The output driver sends out switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is still reached. The $\mathrm{Bl}_{\mathrm{SENSE}}$ pin provides the same protection mechanism for the boost circuit. The $\mathrm{Bl}_{\mathrm{SENSE}}$ OCP threshold is 1.9V.

If the ${\rm FI}_{\rm SENSE}$ sense resistor is shorted, there is a potential danger of the over-current condition not being detected. Thus the IC is designed to detect this sense-resistor short fault after the start-up, and shut down immediately. The V $_{\rm CC}$ is discharged since the IC remains biased. In order to avoid

overcharging the output voltage, the iW3623 employs an extended discharge time before restart.

If the BI_{SENSE} resistor is shorted, the iW3623 cannot determine the base drive current of the boost BJT, which can ultimately result in the boost BJT exceeding its safe operating area. Thus the IC is designed to detect this boost sense-resistor short fault during the CONFIGURATION state. When the iW3623 detects a boost-sense-resistor-short fault for two consecutive detection cycles, then the IC shuts down immediately. The $V_{\rm CC}$ is discharged since the IC remains biased. To prevent over-stress on the boost circuit components, the iW3623 employs an extended discharge time before restart. Initially if $V_{\rm CC}$ drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle.

9.12 Output Over-Voltage/LED Open Protection

The iW3623 includes a function that protects against an output over-voltage (OVP).

The output voltage is monitored by the FV $_{\rm SENSE}$ pin. If the voltage at this pin exceeds its over-voltage threshold the iW3623 shuts down immediately. However, the IC remains biased which discharges the V $_{\rm CC}$ supply. In order to avoid overcharging the output voltage, the iW3623 employs an extended discharge time before restart. Initially if V $_{\rm CC}$ drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle.

Under the output over-voltage fault condition, the controller tries to start up for three consecutive times. If all three start-up attempts fail, the controller enters the inactive mode, during which the controller does not respond to $V_{\rm CC}$ power-on requests. The controller is activated again after it sees 29 start-up attempts. The controller can also be reset to the initial condition if $V_{\rm CC}$ is discharged. Typically, this extended discharge time is around three to five seconds.

This extended discharge time allows the iW3623 to support hot-plug LED modules without causing dangerously high output voltages while maintaining a quick recovery.

In additional to the output over-voltage protection, the iW3623 also employs the constant output voltage regulation operation mode. This allows the output voltage sustains at the reference level if the LED module is disconnected from the driver and the output voltage does not overshoot above the over-voltage protection threshold.

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



9.13 Input and Bulk Over-Voltage

The iW3623 supports the over-voltage protection from AC input and boost output. If the input voltage sense the $\rm V_{IN}$ pin voltage is higher than 1.68V for continuous 2ms within every 16ms period, and this condition lasts for eight consecutive times, the iW3623 shuts down both the boost and flyback driving signals. When $\rm V_{CC}$ drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle.

If the boost voltage sense V_{CB} pin voltage is higher than 1.8V for continuous 128ms, the iW3623 shuts down both the boost and flyback driving signals. When V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle.

Under both the input and boost over-voltage fault conditions, the controller tries to start up for three consecutive times. If all three start-up attempts fail, the controller enters the inactive mode, during which the controller does not respond to $V_{\rm cc}$ power-on requests. The controller is activated again after it sees 29 start-up attempts. The controller can also be reset to the initial condition if $V_{\rm cc}$ is discharged. Typically, this extended discharge time is around three to five seconds.

9.14 Input Brown-Out Protection

After start-up, if $V_{\rm IN}$ pin maximum voltage is below $V_{\rm BR_TH}$, IC will shut down the PFC and flyback circuit. IC will enter an inactive mode, during which the controller does not respond to the $V_{\rm CC}$ power-on requests. The controller is activated again after it sees 29 start-up attempts.

9.15 Output Short Protection

The iW3623 includes a function that protects against an output short-circuit fault.

If the voltage at the FV_{SENSE} pin is below 0.228V, the iW3623 shuts down immediately. After the shutdown, the iW3623 remains powered, which discharges the V $_{\rm CC}$. In order to avoid excessive power stress due to auto-restart, the iW3623 employs an extended discharge time.

To support applications with high output capacitance, output short protection is not activated in the initial LED current soft start period. This allows the voltage to build up in the output capacitor without mis-triggering the protection.

9.16 Over-Temperature Protection

If an NTC thermistor is connected between the $V_{\scriptscriptstyle T}$ pin and GND, the iW3623 is able to detect and protect against an over-temperature event.

The iW3623 provides an I_{VT} to the V_T pin and detects the voltage on the pin. Based on this voltage, the iW3623 can monitor the resistance of the NTC thermistor, which is related to the temperature of the thermistor. As the V_T pin voltage reduces, the iW3623 reduces the power in boost and flyback converter.

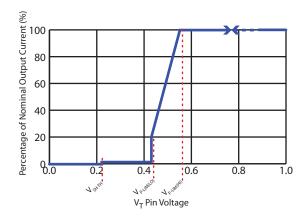


Figure 9.7 : V_T Pin Voltage vs. % of Nominal Output Current

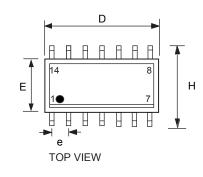
When the $V_{\scriptscriptstyle T}$ pin voltage reaches $V_{\scriptscriptstyle P\text{-}LIM(HI)}$ the output current begins to reduce linearly from 100% to 20% as shown in Figure 9.7. At $V_{\scriptscriptstyle P\text{-}LIM(LO)}$ the output current will be clamped to 1%. If the $V_{\scriptscriptstyle T}$ pin further decreases to below $V_{\scriptscriptstyle SH_TH,}$ the iW3623 will shut down.

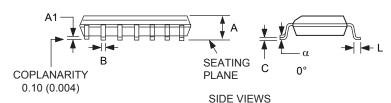
AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



10.0 Physical Dimensions

14-Lead SOIC Package





Symbol Inches Millimeters MIN MAX MIN MAX Α 0.053 1.35 0.069 1.75 Α1 0.004 0.010 0.10 0.25 В 0.013 0.020 0.33 0.51 С 0.007 0.010 0.19 0.25 D 0.337 0.344 8.55 8.75 Ε 0.150 0.157 3.80 4.00 0.050 BSC 1.27 BSC Н 0.228 0.244 5.80 6.20 Ν 2.18 0.086 0.094 2.39 М 0.126 3.00 3.20 0.118 0.016 0.050 0.40 1.27 8°

Figure 10.1: Physical dimensions, 8-lead SOIC package

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:

- [a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
- [b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270°C</p>

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E are determined at the outermost extremes of the plastic bocy exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

11.0 Ordering Information

Part Number	Options	Package	Description
iW3623-00		SOIC-14	Tape & Reel ¹

Note 1: Tape & Reel packing quantity is 2,500/reel.

AC/DC Digital Power Controller for High Power Factor Off-Line LED Drivers



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Contact Information

Web: https://www.iwatt.com
E-mail: info@iwatt.com
Phone: +1 (408) 374-4200
Fax: +1 (408) 341-0455

iWatt Inc.

675 Campbell Technology Parkway, Suite 150

Campbell, CA 95008

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